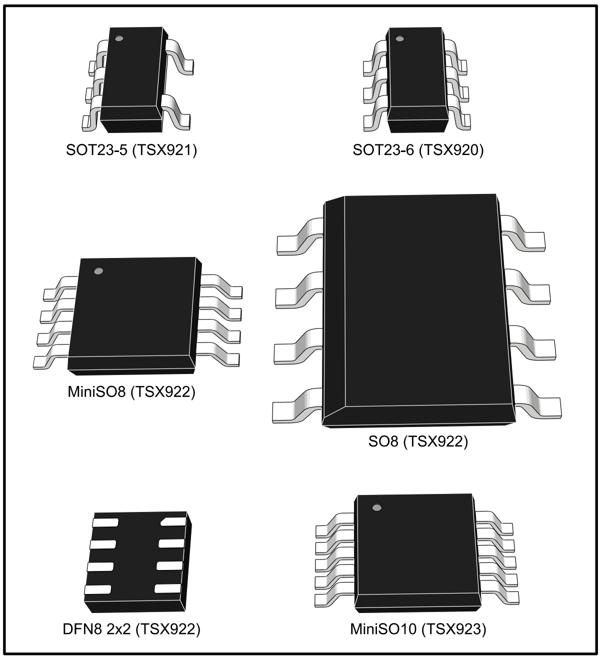
TSX920, TSX921, TSX922, TSX923

10 MHz rail-to-rail CMOS 16 V operational amplifiers

Datasheet - production data



Features

- Rail-to-rail input and output
- Wide supply voltage: 4 V - 16 V
- Gain bandwidth product: 10 MHz typ at 16 V
- Low power consumption: 2.8 mA typ per amplifier at 16 V
- Unity gain stable
- Low input bias current: 10 pA typ
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

Related products

- See the TSX5 series for low-power features
- See the TSX6 series for micro-power features
- See the TSX929 series for higher speeds
- See the TSV9 series for lower voltages

Applications

- Communications
- Process control
- Test equipment

Description

The TSX92x single and dual operational amplifiers (op amps) offer excellent AC characteristics such as 10 MHz gain bandwidth, 17 V/ms slew rate, and 0.0003 % THD+N. These features make the TSX92x family particularly well-adapted for communications, I/V amplifiers for ADCs, and active filtering applications.

Their rail-to-rail input and output capability, while operating on a wide supply voltage range of 4 V to 16 V, allows these devices to be used in a wide range of applications. Automotive qualification is available as these devices can be used in this market segment.

Shutdown mode is available on the single (TSX920) and dual (TSX923) versions enabling an important current consumption reduction while this function is active.

The TSX92x family is available in SMD packages featuring a high level of integration. The DFN8 package, used in the TSX922, with a typical size of 2x2 mm and a maximum height of 0.8 mm offers even greater package size reduction.

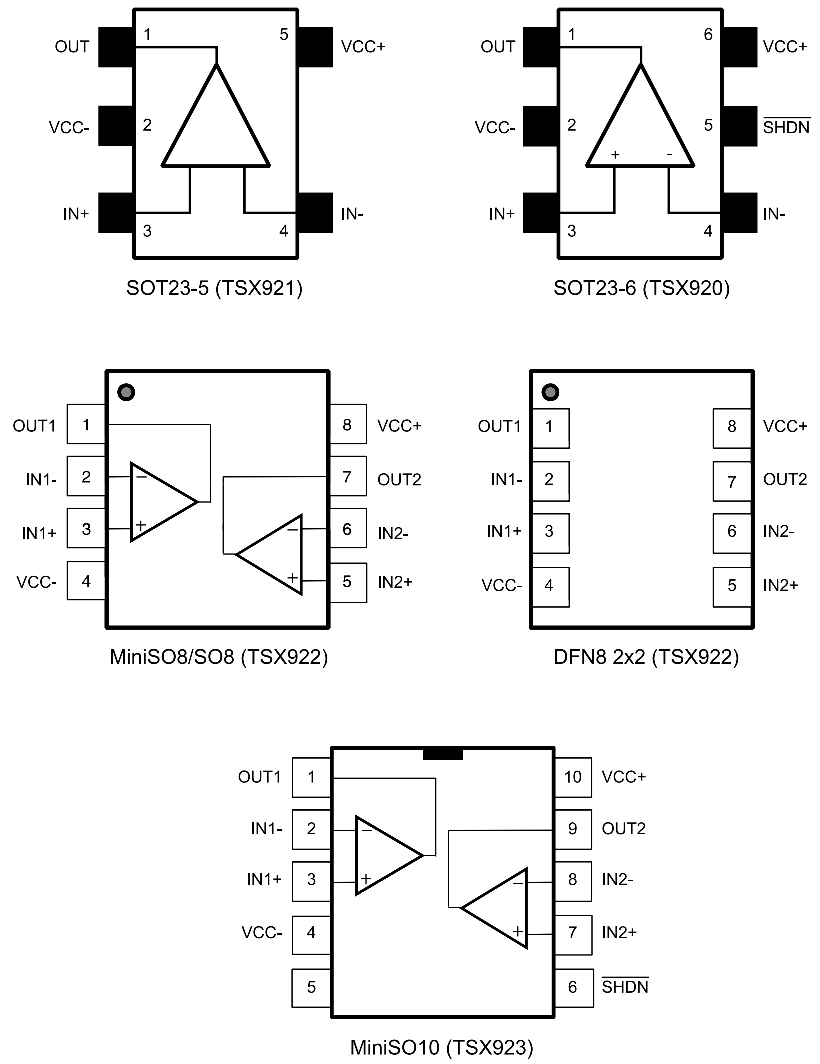
Table 1: Device summary

Op-amp version	With shutdown mode	Without shutdown mode
Single	TSX920	TSX921
Dual	TSX923	TSX922

Contents

1 Package pin connections

Figure 1: Pin connections (top view)



2 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage [1]		18	V
V_{id}	Differential input voltage [2]		$\pm V_{CC}$	mV
V_{in}	Input voltage		(V_{CC-})- 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current [3]		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	°C
R_{thja}	Thermal resistance junction to ambient [4][5]	SOT23-5	250	°C/W
		SOT23-6	240	
		MiniSO8	190	
		SO8	125	
		DFN8 2x2	57	
		MiniSO10	113	
ESD	HBM: human body model [6]		4000	V
	MM: machine model [7]		100	
	CDM: charged device model [8]		1500	
	Latch-up immunity		200	mA

Notes:

(1) All voltage values, except the differential voltage are with respect to network ground terminal.

(2) The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.

(3) Input current must be limited by a resistor in series with the inputs.

(4) R_{th} are typical values.

(5) Short-circuits can cause excessive heating and destructive dissipation.

(6) According to JEDEC standard JESD22-A114F

(7) According to JEDEC standard JESD22-A115A

(8) According to ANSI/ESD STM5.3.1

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4 to 16	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	V
T_{oper}	Operating free air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4: Electrical characteristics at VCC+ = 4.5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{icm} = 2 V (all order codes except TSX922IYST and TSX922IYDT)			4	mV
		$T_{min} < T_{op} < T_{max}$			5	
		V_{icm} = 2 V (TSX922IYST, TSX922IYDT order codes only)			5	
		$T_{min} < T_{op} < T_{max}$			6.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	All order codes except TSX922IYST and TSX922IYDT		2	10	μV/°C
		TSX922IYST and TSX922IYDT order codes only		2	15	
ΔV_{io}	Long-term input offset voltage drift (1)(2)	TSX920/TSX921		6		nV/√month
		TSX922/TSX923		9		
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		10	100	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		10	100	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 2 V, $V_{OUT} = V_{CC}/2$	61	82		dB
		$T_{min} < T_{op} < T_{max}$	59			
		V_{icm} = -0.1 V to 4.6 V, $V_{OUT} = V_{CC}/2$	59	72		
		$T_{min} < T_{op} < T_{max}$	57			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 V to 4.2 V	100	108		
		$T_{min} < T_{op} < T_{max}$	90			
		R_L= 10 kΩ, V_{out} = 0.2 V to 4.3 V	100	112		
		$T_{min} < T_{op} < T_{max}$	90			
V_{OH}	High level output voltage	R_L= 2 kΩ to $V_{CC}/2$		50	80	mV from V_{CC}+
		$T_{min} < T_{op} < T_{max}$			100	
		R_L= 10 kΩ to $V_{CC}/2$		10	16	
		$T_{min} < T_{op} < T_{max}$			20	
V_{OL}	Low level output voltage	R_L= 2 kΩ to $V_{CC}/2$		42	80	mV
		$T_{min} < T_{op} < T_{max}$			100	
		R_L= 10 kΩ to $V_{CC}/2$		9	16	
		$T_{min} < T_{op} < T_{max}$			20	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out}	I_{sink}	V_{out} = 4.5 V	16	21		mA
		$T_{min} < T_{op} < T_{max}$	13			
	I_{source}	V_{out} = 0 V	16	21		
		$T_{min} < T_{op} < T_{max}$	13			
I_{CC}	Supply current (per amplifier)	No load, $V_{out} = V_{CC}/2$		2.9	3.4	
		$T_{min} < T_{op} < T_{max}$			3.5	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		9		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		9.3		
ϕm	Phase margin			60		Degrees
G_m	Gain margin			6.7		dB
SR+	Positive slew rate	Av = 1, V_{out} = 0.5 to 4.0 V, measured between 10 % to 90 %		14.7		V/μs
SR-	Negative slew rate	Av = 1, V_{out} = 4.0 to 0.5 V, measured between 90 % to 10 %		17.2		
e_n	Equivalent input noise voltage	f = 10 kHz		17.9		nV√Hz
		f = 100 kHz		12.9		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.1		μV_{pp}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, $V_{out} = 2\ V_{rms}$		0.002		%
Shutdown characteristics (TSX920 and TSX923 only)						
I_{CC_shdn}	Supply current in shutdown mode (per amplifier)	$\overline{SHDN} = V_{CC-}$		7	15	μA
		$T_{min} < T_{op} < T_{max}$			20	
t_{on}	Amplifier turn-on time			9		μs
t_{off}	Amplifier turn-off time			0.7		

Notes:

(1)Typical value is based on the Vio drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 5.5: "Long term input offset voltage drift"*).

(2)When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16 V and $V_{icm} > V_{CC}/2$, Vio can experience a permanent drift of a few mV drift. This phenomenon is notably worse at low temperatures.

Table 5: Electrical characteristics at VCC+ = 10 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{icm} = 2 V (all order codes except TSX922IYST and TSX922IYDT)			4	mV
		$T_{min} < T_{op} < T_{max}$			5	
		V_{icm} = 2 V (TSX922IYST and TSX922IYDT order codes only)			5	
		$T_{min} < T_{op} < T_{max}$			6.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	All order codes except TSX922IYST and TSX922IYDT		2	10	μV/°C
		TSX922IYST and TSX922IYDT order codes only		2	15	
ΔV_{io}	Long-term input offset voltage drift (1)(2)	TSX920/TSX921		92		nV/√month
		TSX922/TSX923		128		
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		10	100	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		10	100	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 7 V, $V_{OUT} = V_{CC}/2$	72	85		dB
		$T_{min} < T_{op} < T_{max}$	70			
		V_{icm} = -0.1 V to 10.1 V, $V_{OUT} = V_{CC}/2$	64	75		
		$T_{min} < T_{op} < T_{max}$	62			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 V to 9.7 V	100	107		
		$T_{min} < T_{op} < T_{max}$	90			
		R_L= 10 kΩ, V_{out} = 0.2 V to 9.8 V	100	117		
		$T_{min} < T_{op} < T_{max}$	90			
V_{OH}	High-level output voltage	R_L= 2 kΩ to $V_{CC}/2$		94	110	mV from $V_{CC}+$
		$T_{min} < T_{op} < T_{max}$			130	
		R_L= 10 kΩ to $V_{CC}/2$		31	40	
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low-level output voltage	R_L= 2 kΩ to $V_{CC}/2$		80	110	mV
		$T_{min} < T_{op} < T_{max}$			130	
		R_L= 10 kΩ to $V_{CC}/2$		14	40	
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_{out} = 10 V	50	55		mA
		$T_{min} < T_{op} < T_{max}$	42			
	I_{source}	V_{out} = 0 V	75	82		
		$T_{min} < T_{op} < T_{max}$	70			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (per amplifier)	No load, $V_{out} = V_{CC}/2$		3.1	3.6	mA
		$T_{min} < T_{op} < T_{max}$			3.6	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		10		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		11.2		
ϕm	Phase margin			56		Degrees
G_m	Gain margin			6		dB
SR+	Positive slew rate	Av = 1, V_{out} = 0.5 to 9.5 V, measured between 10 % to 90 %		17.7		V/μs
SR-	Negative slew rate	Av = 1, V_{out} = 9.5 to 0.5 V, measured between 90 % to 10 %		19.6		
e_n	Equivalent input noise voltage	f = 10 kHz		16.8		nV√Hz
		f = 100 kHz		12		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.64		μV_{pp}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, $V_{out} = 2\ V_{rms}$		0.0006		%
Shutdown characteristics (TSX920 and TSX923 only)						
I_{CC_shdn}	Supply current in shutdown mode (per amplifier)	$\overline{SHDN} = V_{CC-}$		7	15	μA
		$T_{min} < T_{op} < T_{max}$			20	
t_{on}	Amplifier turn-on time			2.4		μs
t_{off}	Amplifier turn-off time			0.35		

Notes:

(1)Typical value is based on the Vio drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 5.5: "Long term input offset voltage drift"*).

(2)When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16 V and $V_{icm}>V_{CC}/2$, Vio can experience a permanent drift of a few mV drift. This phenomenon is notably worse at low temperatures.

Table 6: Electrical characteristics at VCC+ = 16 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{icm} = 2 V (all order codes except TSX922IYST and TSX922IYDT)			4	mV
		$T_{min} < T_{op} < T_{max}$			5	
		V_{icm} = 2 V (TSX922IYST and TSX922IYDT order codes only)			5	
		$T_{min} < T_{op} < T_{max}$			6.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	All order codes except TSX922IYST and TSX922IYDT		2	10	μV/°C
		TSX922IYST and TSX922IYDT order codes only		2	15	
ΔV_{io}	Long-term input offset voltage drift (1)(2)	TSX920/TSX921		1.73		nV/√month
		TSX922/TSX923		2.26		
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		10	100	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		10	100	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 13 V, $V_{OUT} = V_{CC}/2$	73	85		dB
		$T_{min} < T_{op} < T_{max}$	71			
		V_{icm} = -0.1 V to 16.1 V, $V_{OUT} = V_{CC}/2$	67	76		
		$T_{min} < T_{op} < T_{max}$	65			
SVRR	Supply voltage rejection ratio	V_{CC} = 4.5 V to 16 V	73	85		
		$T_{min} < T_{op} < T_{max}$	71			
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 V to 15.7 V	100	105		
		$T_{min} < T_{op} < T_{max}$	90			
		R_L= 10 kΩ, V_{out} = 0.2 V to 15.8 V	100	113		
		$T_{min} < T_{op} < T_{max}$	90			
V_{OH}	High-level output voltage	R_L= 2 kΩ to $V_{CC}/2$		150	200	mV from V_{CC}+
		$T_{min} < T_{op} < T_{max}$			230	
		R_L= 10 kΩ to $V_{CC}/2$		43	50	
		$T_{min} < T_{op} < T_{max}$			70	
V_{OL}	Low-level output voltage	R_L= 2 kΩ to $V_{CC}/2$		140	200	mV
		$T_{min} < T_{op} < T_{max}$			230	
		R_L= 10 kΩ to $V_{CC}/2$		30	50	
		$T_{min} < T_{op} < T_{max}$			70	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out}	I_{sink}	V_{out} = 16 V	45	50		mA
		$T_{min} < T_{op} < T_{max}$	40			
	I_{source}	V_{out} = 0 V	65	74		
		$T_{min} < T_{op} < T_{max}$	60			
I_{CC}	Supply current (per amplifier)	No load, $V_{out} = V_{CC}/2$		2.8	3.4	
		$T_{min} < T_{op} < T_{max}$			3.4	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		10		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		12		
ϕm	Phase margin			55		Degrees
G_m	Gain margin			5.9		dB
SR+	Positive slew rate	Av = 1, V_{out} = 0.5 to 15.5 V, measured between 10 % to 90 %		16.2		V/μs
SR-	Negative slew rate	Av = 1, V_{out} = 15.5 to 0.5 V, measured between 90 % to 10 %		17.2		
e_n	Equivalent input noise voltage	f = 10 kHz		16.5		nV√Hz
		f = 100 kHz		11.8		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.58		μV_{pp}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, $V_{out} = 4\ V_{rms}$		0.0003		%
t_S	Setting time	Gain = 1, 100 mV input voltage, 0.1 % of final value		245		ns
		Gain = 1, 100 mV input voltage, 1 % of final value		178		
Shutdown characteristics (TSX920 and TSX923 only)						
I_{CC_shdn}	Supply current in shutdown mode (per amplifier)	$\overline{SHDN} = V_{CC-}$		7	15	μA
		$T_{min} < T_{op} < T_{max}$			20	
t_{on}	Amplifier turn-on time			1.5		μs
t_{off}	Amplifier turn-off time			0.2		

Notes:

(1) Typical value is based on the Vio drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see *Section 5.5: "Long term input offset voltage drift"*).

(2) When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16 V and $V_{icm} > V_{CC}/2$, Vio can experience a permanent drift of a few mV drift. This phenomenon is notably worse at low temperatures.

4 Electrical characteristic curves

Figure 2: Supply current vs.supply voltage

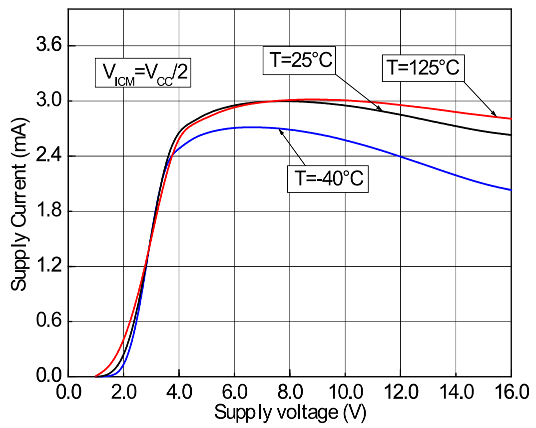


Figure 3: Distribution of input offset voltage at VCC = 4.5 V

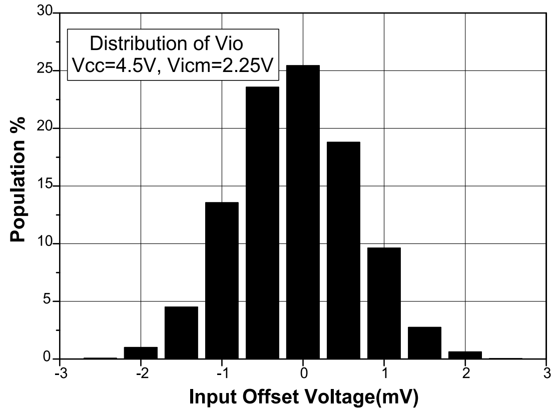


Figure 4: Distribution of input offset voltage at VCC = 10 V

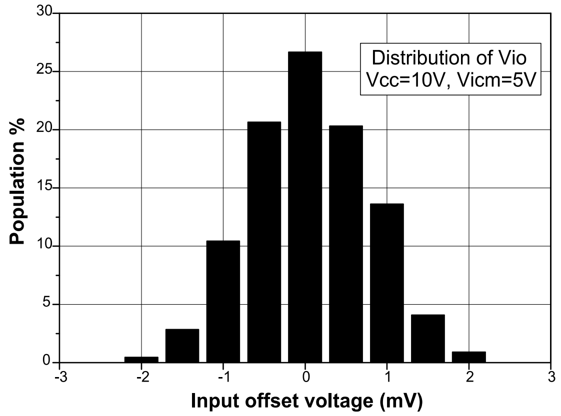


Figure 5: Distribution of input offset voltage at VCC = 16 V

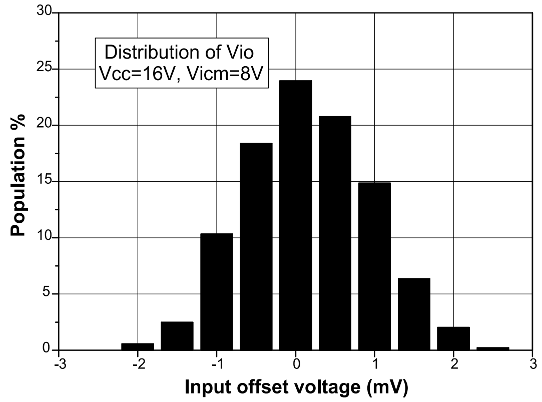


Figure 6: Input offset voltage vs. temperature at VCC = 16 V

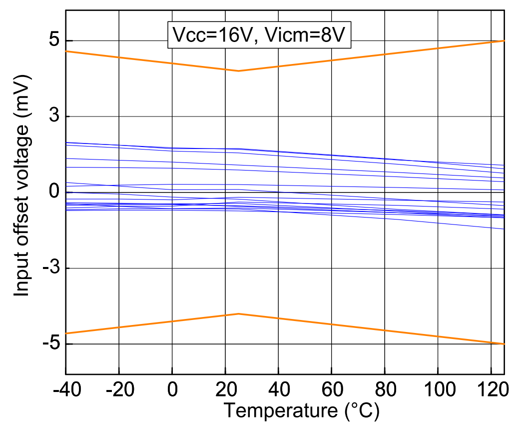


Figure 7: Distribution of input offset voltage drift over temperature

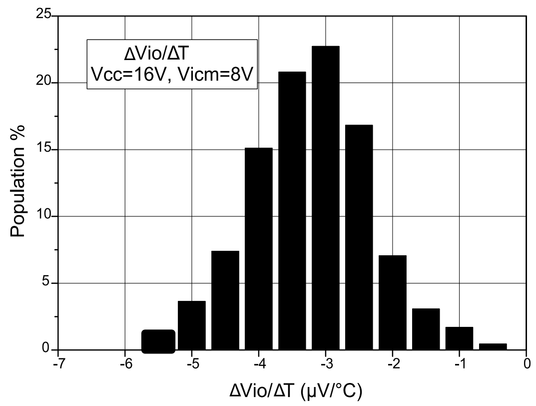


Figure 8: Input offset voltage vs. common-mode voltage at VCC = 4 V

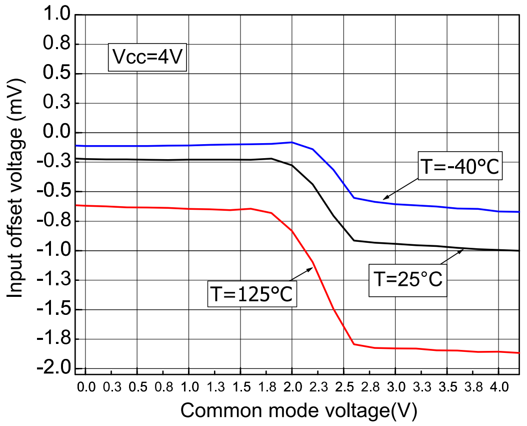


Figure 9: Input offset voltage vs. common-mode voltage at VCC = 16 V

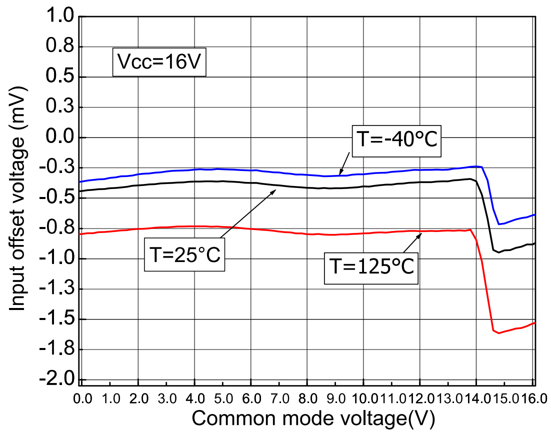


Figure 10: Output current vs. output voltage at VCC = 4 V

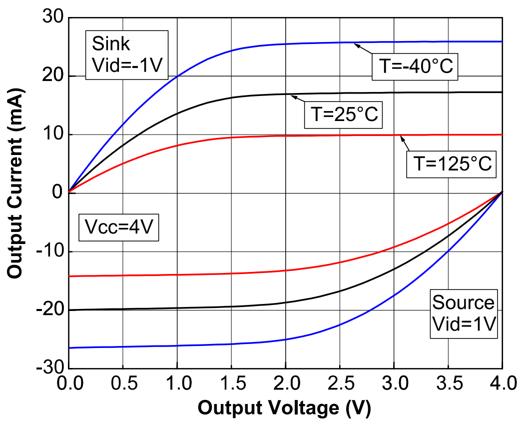


Figure 11: Output current vs. output voltage at VCC = 10 V

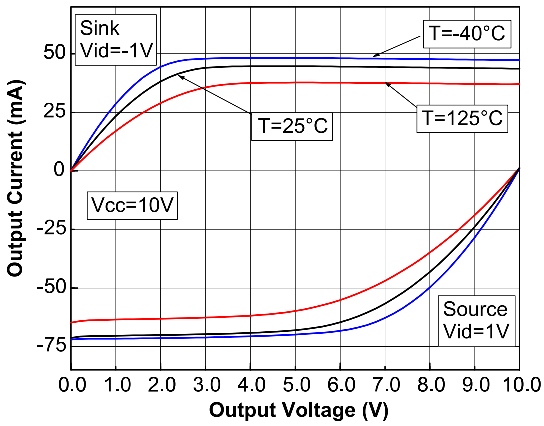


Figure 12: Output current vs. output voltage at VCC = 16 V

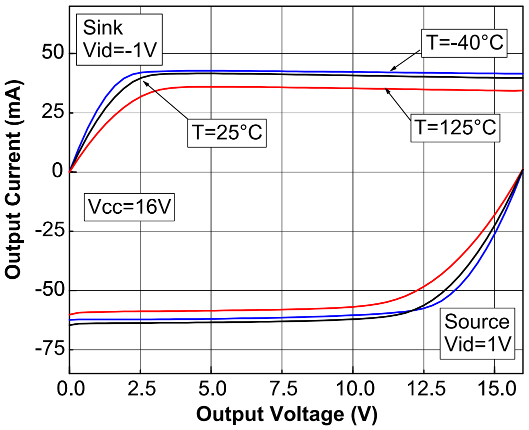


Figure 13: Output rail linearity

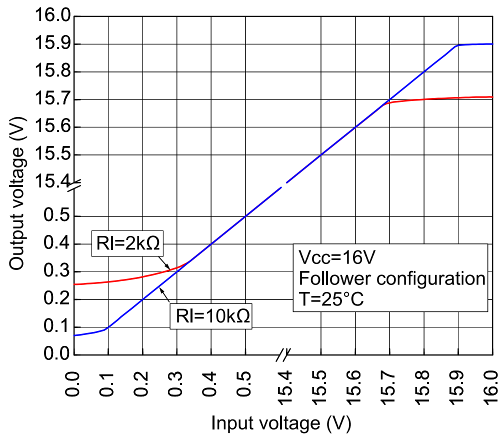


Figure 14: Open loop gain vs. frequency

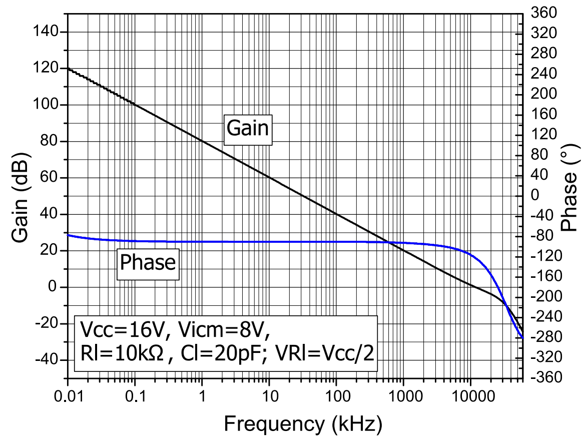


Figure 15: Bode diagram vs. temperature for VCC = 4 V

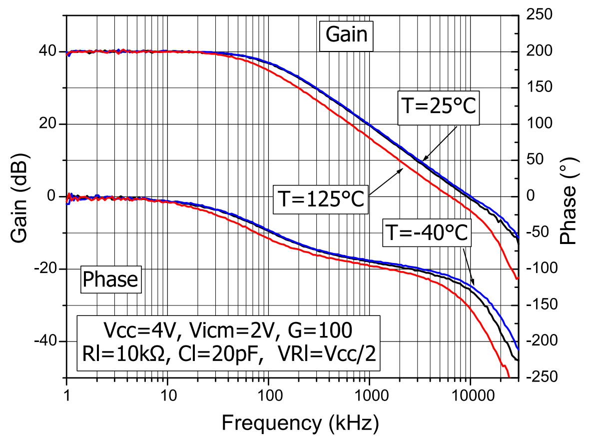


Figure 16: Bode diagram vs. temperature for VCC = 10 V

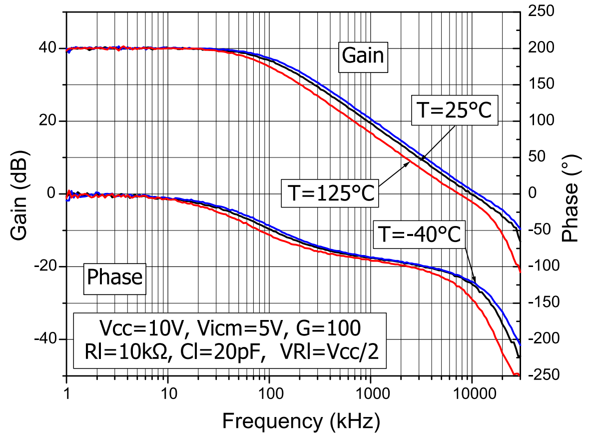


Figure 17: Bode diagram vs. temperature for VCC = 16 V

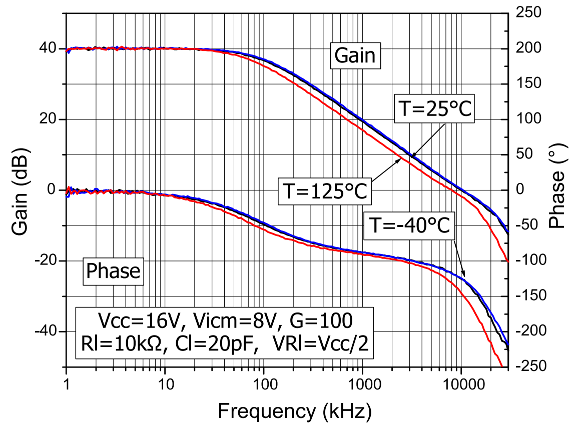


Figure 18: Bode diagram at VCC = 16 V with low common-mode voltage

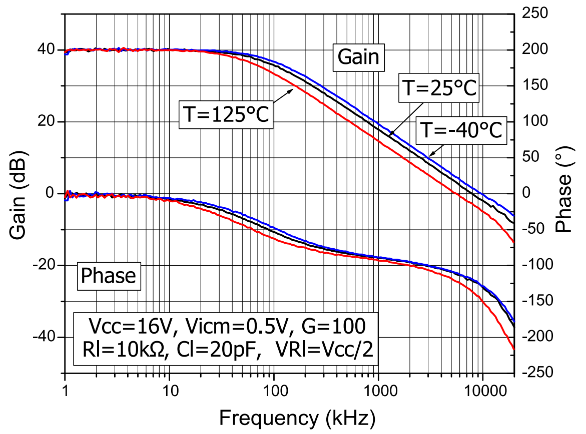


Figure 19: Bode diagram at VCC = 16 V with high common-mode voltage

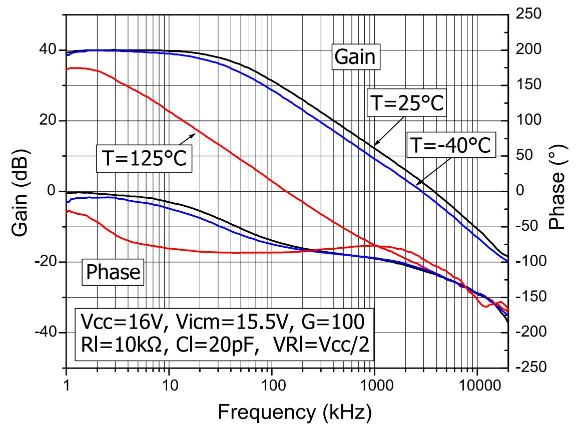


Figure 20: Bode diagram at VCC = 16 V and RL = 10 kΩ, CL = 47 pF

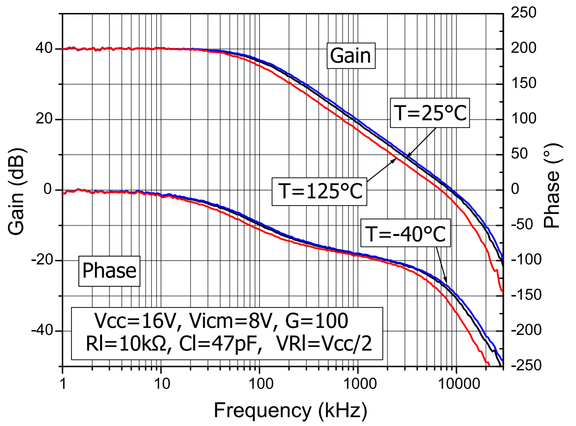


Figure 21: Bode diagram at VCC = 16 V and RL = 10 kΩ, CL = 120 pF

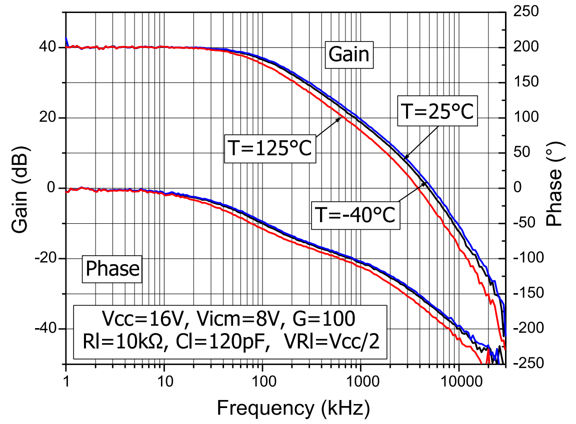


Figure 22: Bode diagram at VCC = 16 V and RL = 2.2 kΩ, CL = 20 pF

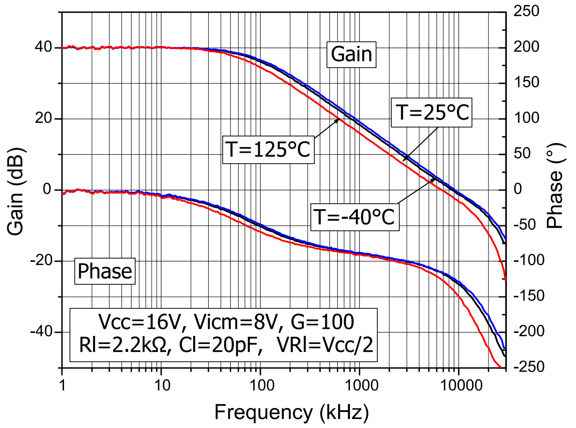


Figure 23: Slew rate vs. supply voltage and temperature

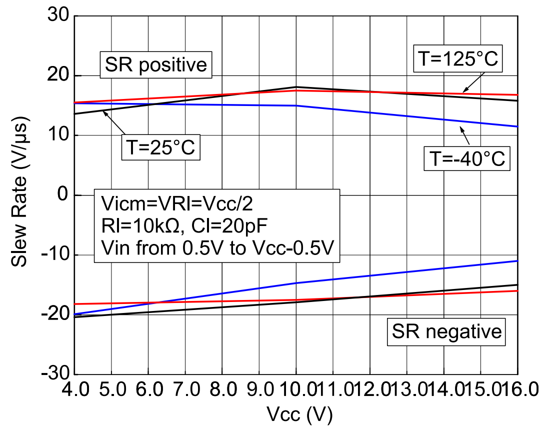


Figure 24: Overshoot vs. capacitive load without feedback capacitor

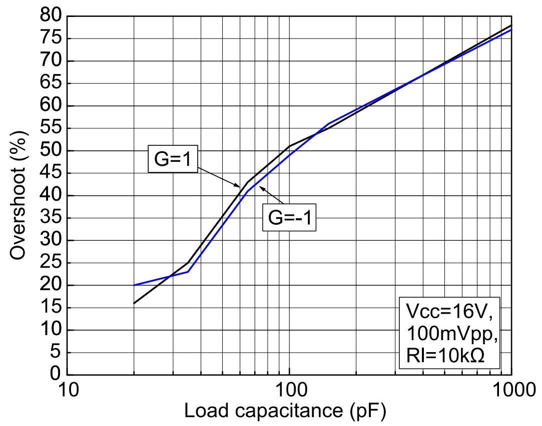


Figure 25: Closed loop gain vs. frequency with different gain resistors

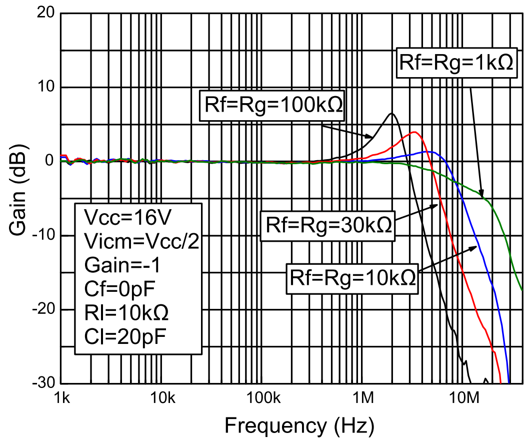


Figure 26: Large step response

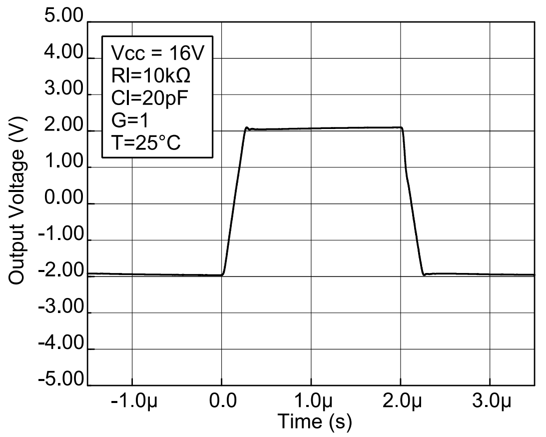


Figure 27: Small step response

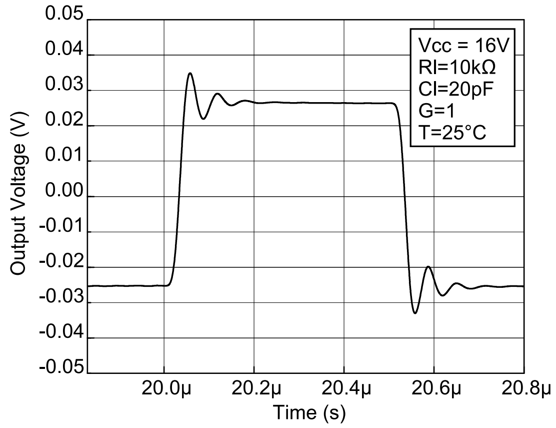


Figure 28: Small step response with feedback capacitor CF

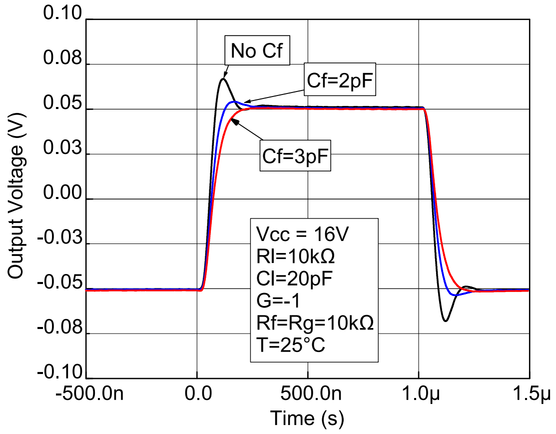


Figure 29: Output impedance vs. frequency in closed loop configuration

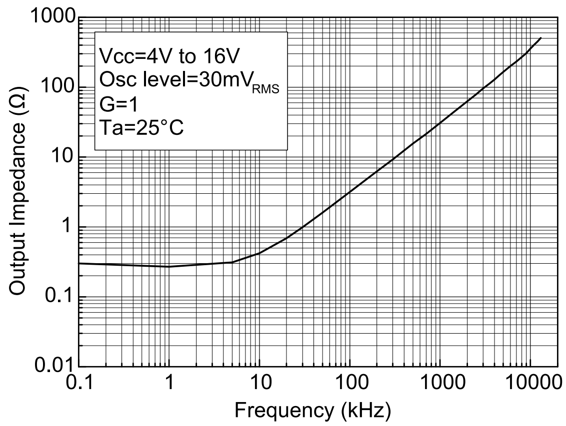


Figure 30: Noise vs. frequency with 16 V supply voltage

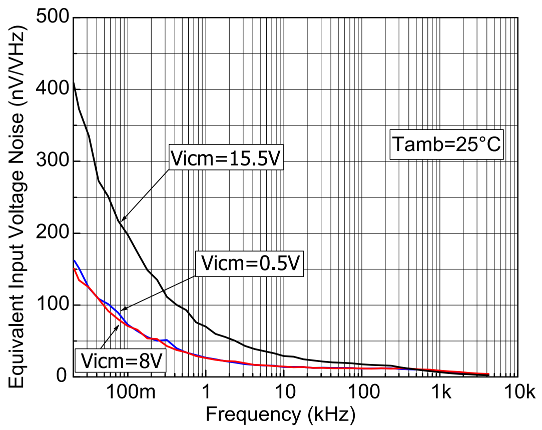


Figure 31: 0.1 to 10 Hz noise

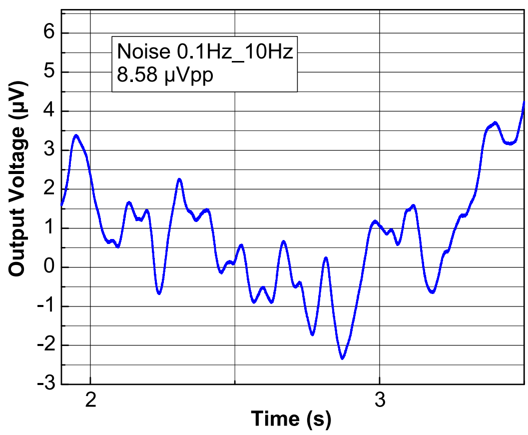


Figure 32: THD+N vs. frequency at VCC = 16 V

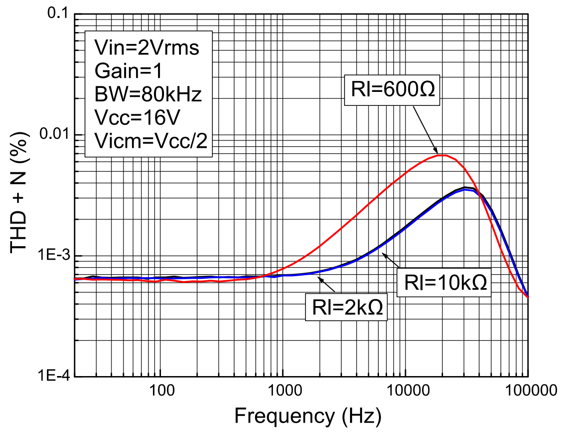


Figure 33: THD+N vs. output voltage at VCC = 16 V

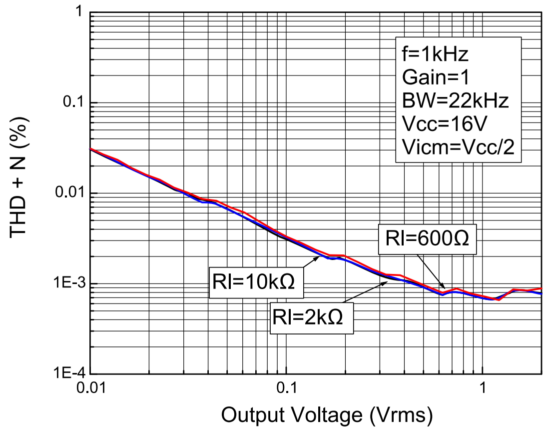


Figure 34: Power supply rejection ratio (PSRR) vs. frequency

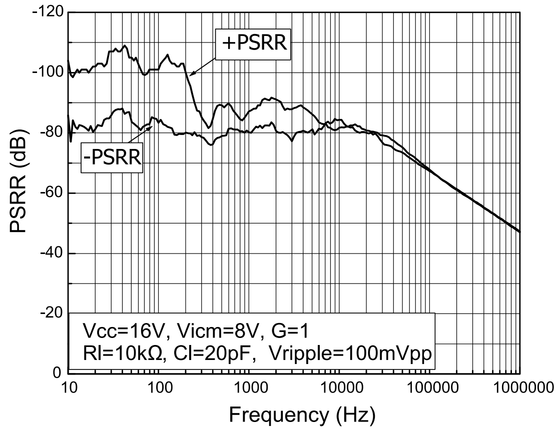


Figure 35: Crosstalk vs. frequency between operators on TSX922 at VCC = 16 V

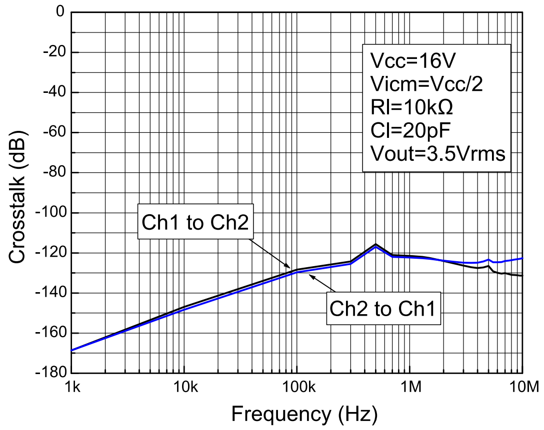


Figure 36: Startup time after standby released for VCC = 4 V

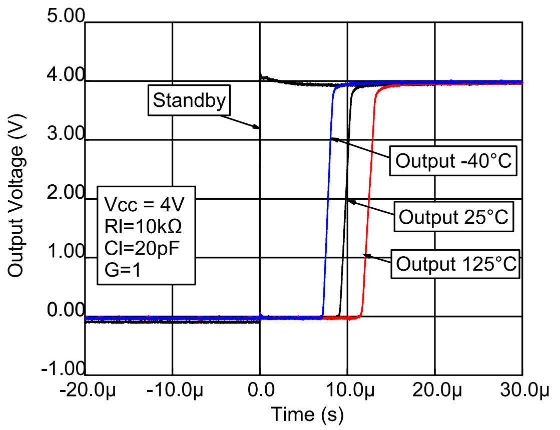
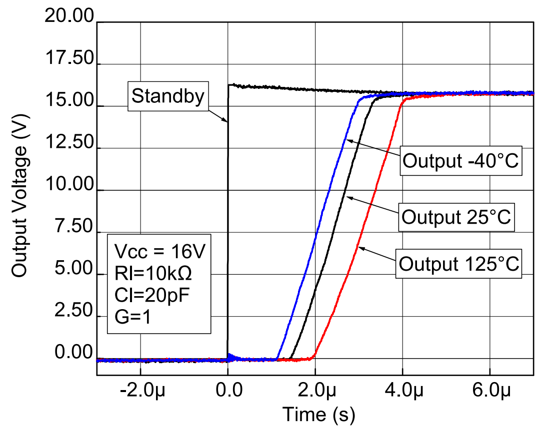


Figure 37: Startup time after standby released for VCC = 16 V



5 Application information

5.1 Operating voltages

The TSX92x operational amplifiers can operate from 4 V to 16 V. The parameters are fully specified at 4.5 V, 10 V, and 16 V power supplies. However, parameters are very stable in the full V_{CC} range. Additionally, main specifications are guaranteed in the extended temperature range from -40 to 125 °C.

5.2 Rail-to-rail input

The TSX92x series is designed with two complementary PMOS and NMOS input differential pairs. The device has a rail-to-rail input and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V. However, the performance of this device is clearly optimized for the PMOS differential pairs (which means from (V_{CC-}) - 0.1 V to (V_{CC+}) - 2 V).

Beyond (V_{CC+}) - 2 V, the operational amplifier is still functional but with downgraded performances (see *Figure 19*). Performances are still suitable for a large number of applications requiring the rail-to-rail input feature.

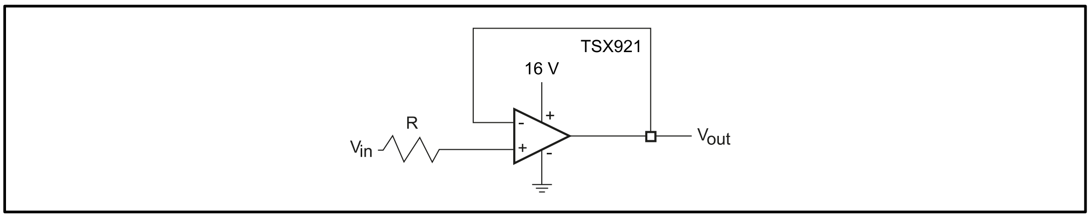
The TSX92x operational amplifiers are designed to prevent phase reversal.

5.3 Input pin voltage range

The TSX92x operational amplifiers have internal ESD diode protections on the inputs. These diodes are connected between the input and each supply rail to protect MOSFETs inputs from electrostatic discharges.

Thus, if the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current could flow through them. To prevent any permanent damage, this current must be limited to 10 mA. This can be done by adding a resistor in series with the input pin (*Figure 38: "Limiting input current with a series resistor"*). The resistor value has to be calculated for a 10 mA current limitation on the input pins.

Figure 38: Limiting input current with a series resistor



5.4 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 2.

5.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate k is the Boltzmann constant (8.6173×10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\text{ h} \times 12\text{ months} / (24\text{ h} \times 365.25\text{ days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \text{max}V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.6 Capacitive load

Driving a large capacitive load can cause stability issues. Increasing the load capacitance produces gain peaking in the frequency response, with overshooting and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB the op-amp might become unstable. Generally, the unity gain configuration is the worst configuration for stability and the ability to drive large capacitive loads. *Figure 39: "Stability criteria with a serial resistor"* shows the serial resistor (Riso) that must be added to the output, to make the system stable.

Figure 39: Stability criteria with a serial resistor

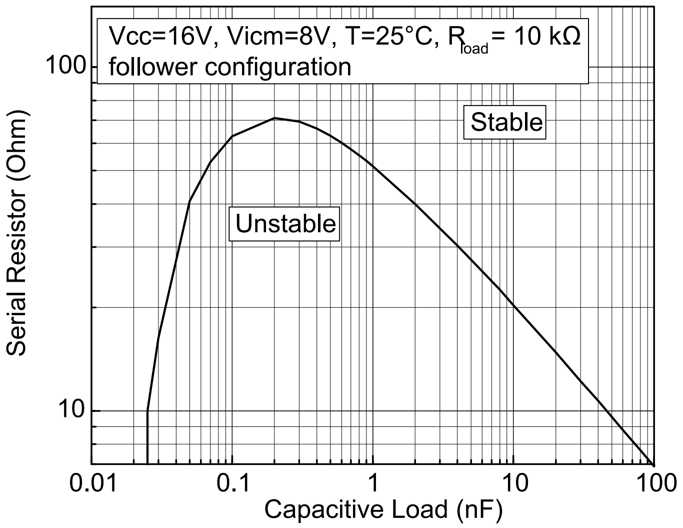
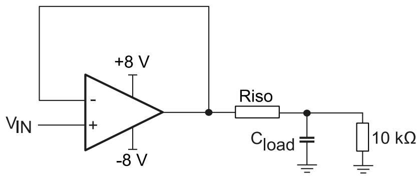


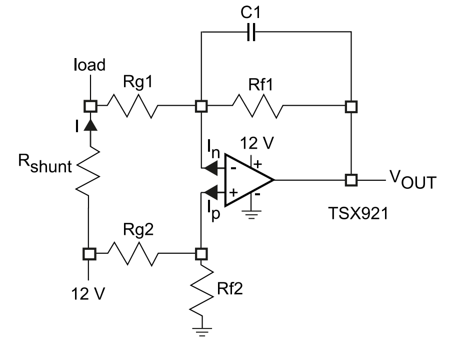
Figure 40: Test configuration for Riso



5.7 High-side current sensing

TSX92x rail to rail input devices can be used to measure a small differential voltage on a high side shunt resistor and translate it into a ground referenced output voltage. The gain is fixed by external resistance.

Figure 41: High-side current sensing configuration



V_{out} can be expressed as follows:

Equation 8

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2} \times R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \times R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, *Equation 8* can be simplified as follows:

Equation 9

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

With the TSX92x operational amplifiers, the high side current measurement must be made by respecting the common mode voltage of the amplifier: (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V. If the application requires a higher common voltage please refer to the TSC high side current sensing family.

5.8 High-speed photodiode

The TSX92x series is an excellent choice for current to voltage (I-V) conversions. Due to the CMOS technology, the input bias currents are extremely low. Moreover, the low noise and high unity-gain bandwidth of the TSX92x operational amplifiers make them particularly suitable for high-speed photodiode preamplifier applications.

The photodiode is considered as a capacitive current source. The input capacitance, C_{IN}, includes the parasitic input Common mode capacitance, C_{CM} (3pF), and the input differential mode capacitance, C_{DIFF} (8pF). C_{IN} acts in parallel with the intrinsic capacitance of the photodiode, C_D. At higher frequencies, the capacitors affect the circuit response. The output capacitance of a current sensor has a strong effect on the stability of the op-amp feedback loop.

C_F stabilizes the gain and limits the transimpedance bandwidth. To ensure good stability and to obtain good noise performance, C_F can be set as shown in *Equation 10*.

Equation 10

$$C_F > \sqrt{\frac{C_{IN} + C_D}{2 \cdot \pi \cdot R_F \cdot F_{GBP}}} - C_{SMR}$$

where,

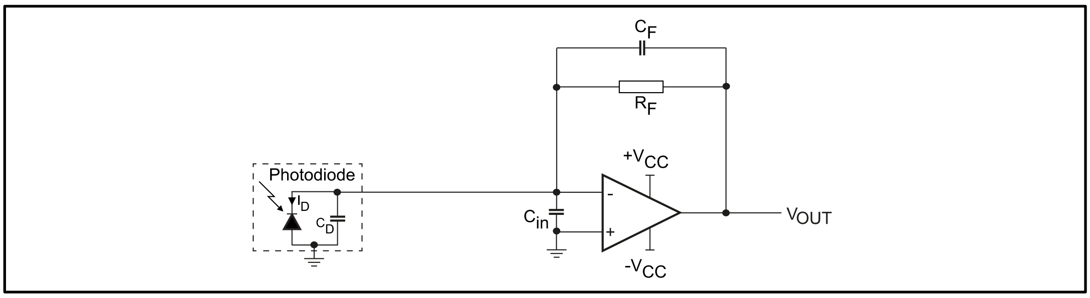
- $C_{IN} = C_{CM} + C_{DIFF} = 11$ pF
- C_{DIFF} is the differential input capacitance: 8 pF typical
- C_{CM} is the Common mode input capacitance: 3 pF typical
- C_D is the intrinsic capacitance of the photodiode
- C_{SMR} is the parasitic capacitance of the surface mount R_F resistor: 0.2 pF typical
- F_{GBP} is the gain bandwidth product: 10 MHz at 16 V

R_F fixes the gain as shown in Equation 11.

Equation 11

$$V_{OUT} = R_F \times I_D$$

Figure 42: High-speed photodiode



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 SOT23-5 package information

Figure 43: SOT23-5 package outline

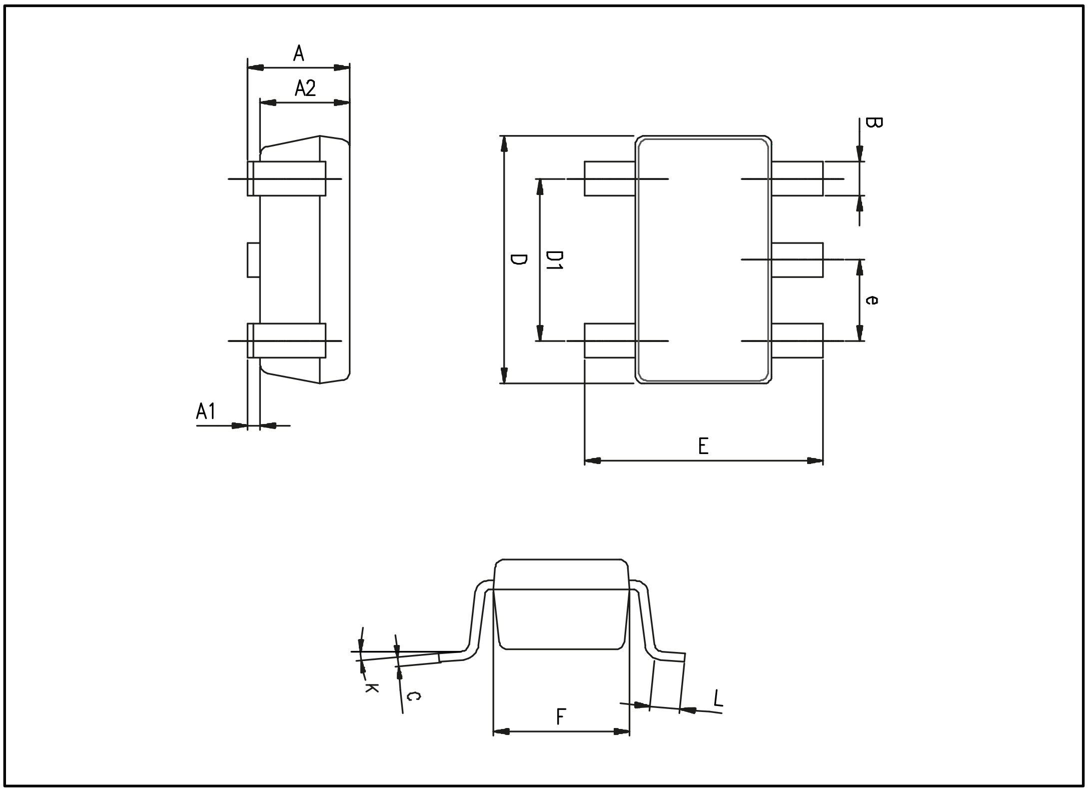


Table 7: SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 SOT23-6 package information

Figure 44: SOT23-6 package outline

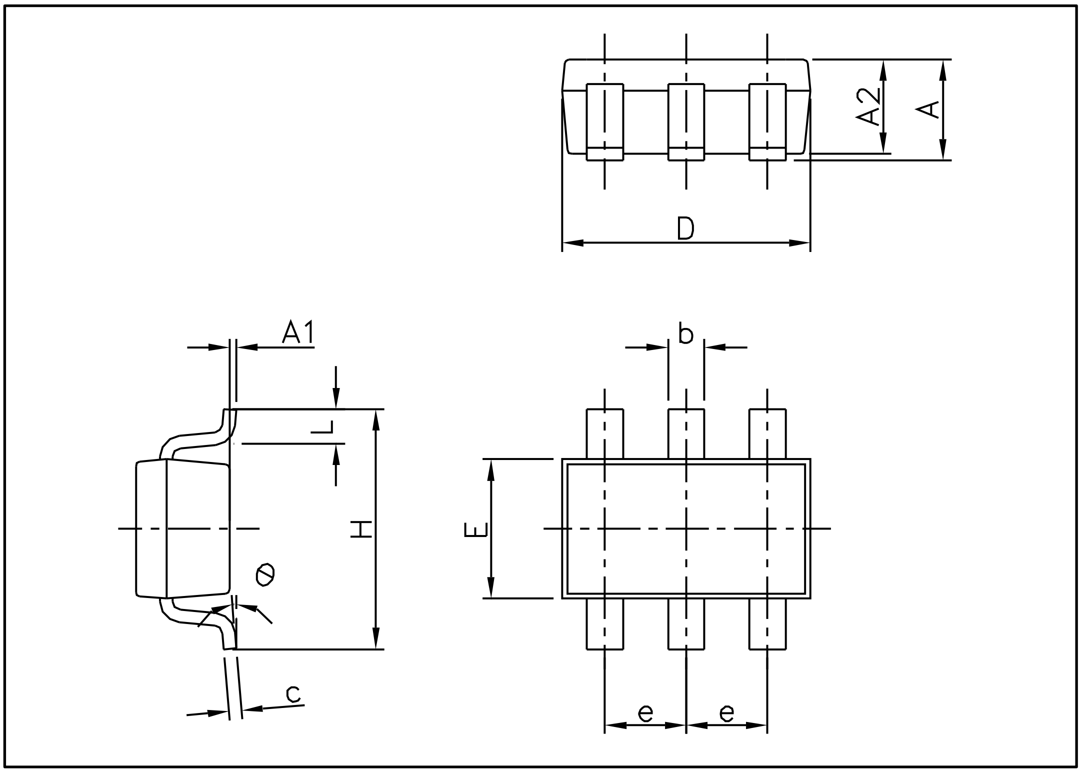


Table 8: SOT23-6 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1			0.10			0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.013		0.019
c	0.09		0.20	0.003		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.060		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0 °		10 °	0 °		10 °

6.3 MiniSO8 package information

Figure 45: MiniSO8 package outline

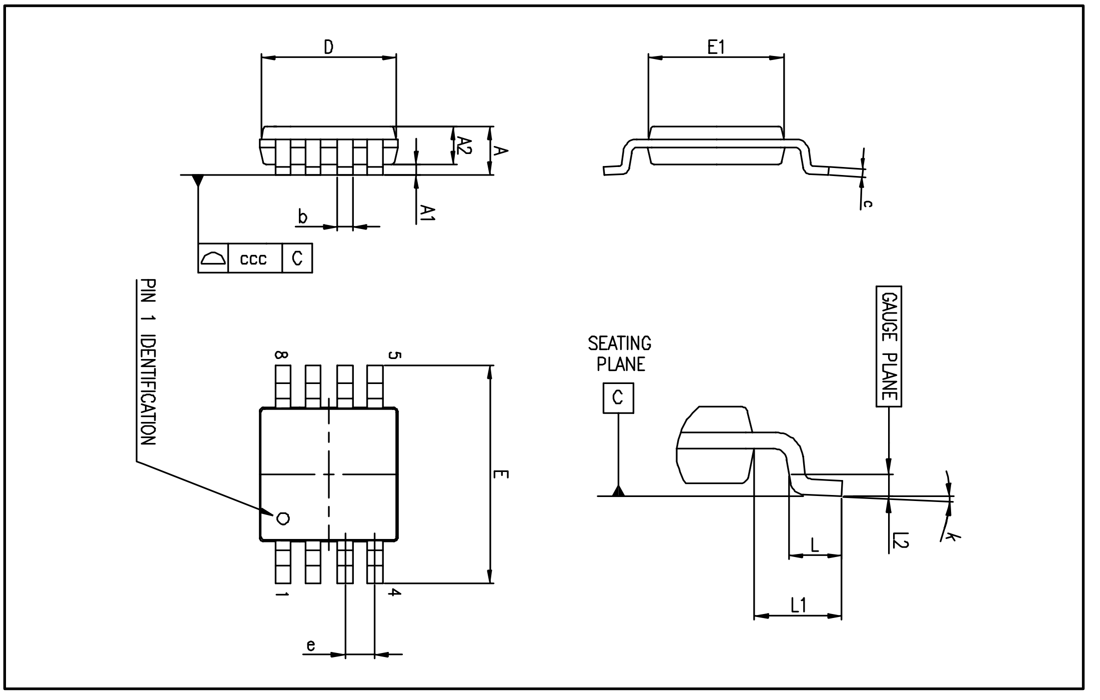


Table 9: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.4 SO8 package information

Figure 46: SO8 package outline

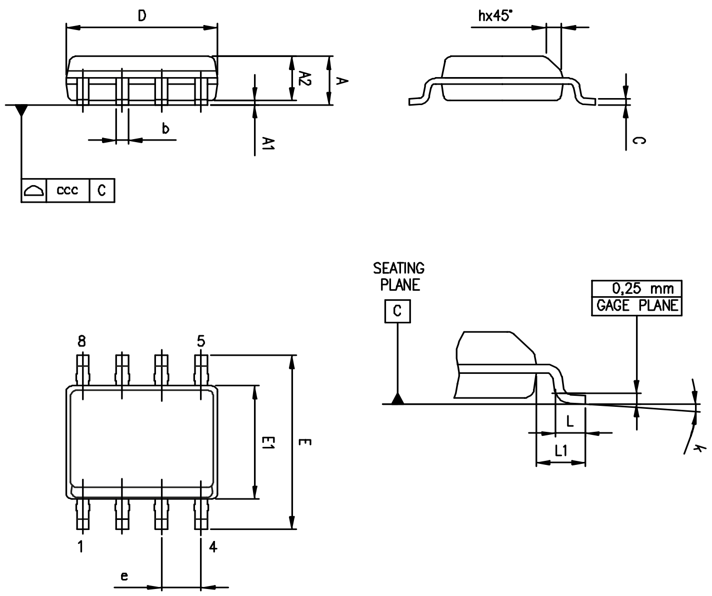


Table 10: SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

6.5 DFN8 2x2 package information

Figure 47: DFN8 2x2 package outline

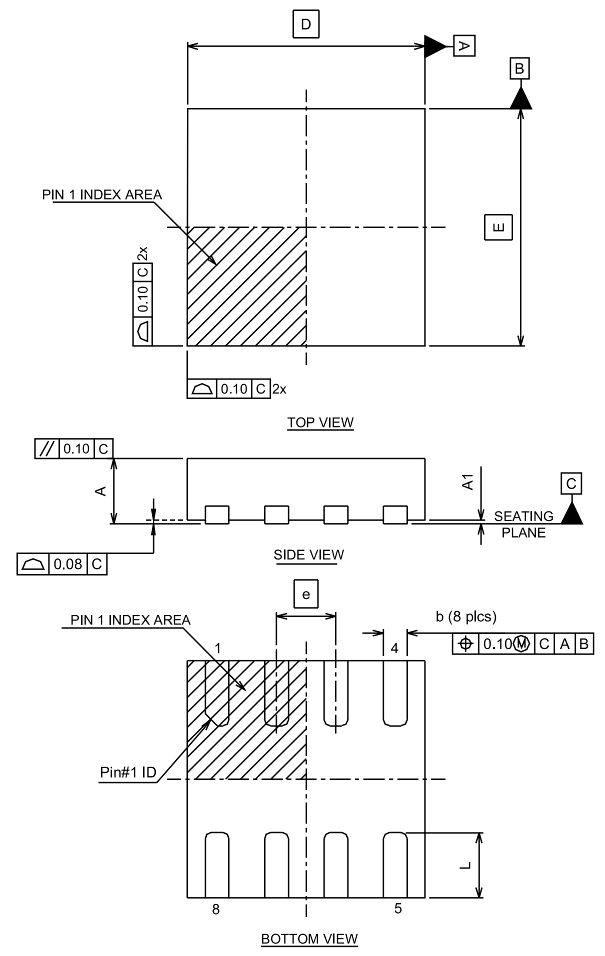


Table 11: DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8					

6.6 MiniSO10 package information

Figure 48: MiniSO10 package outline

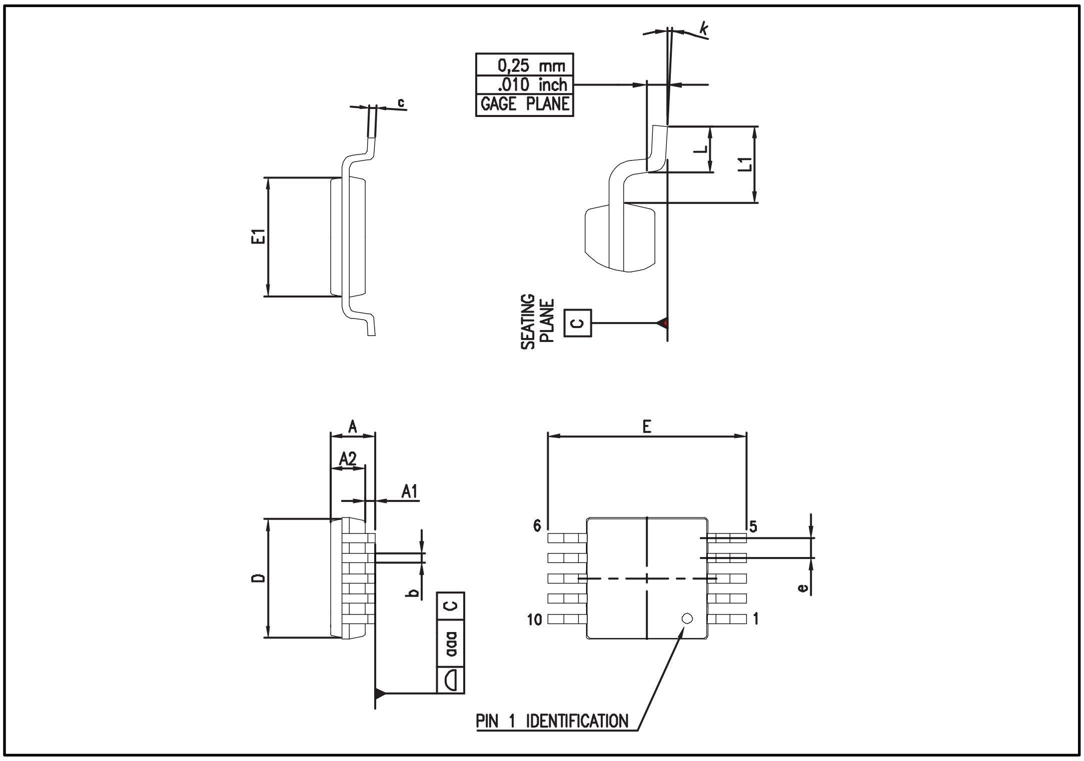


Table 12: MiniSO-10 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0°	3°	6°	0°	3°	6°
aaa			0.10			0.004

7 Ordering information

Table 13: Order codes

Order code	Temperature range	Package	Packing	Marking
TSX920ILT	-40 °C to 125 °C	SOT23-6	Tape and reel	K304
TSX921ILT		SOT23-5		
TSX921IYLT [(1)]				K305
TSX922IDT		SO8		TSX922I
TSX922IYDT [(1)]				SX922IY
TSX922IST		MiniSO8		K305
TSX922IQ2T		DFN8 2x2		K26
TSX922IYST [(1)]		MiniSO8 (automotive grade)		K312
TSX922IYDT [(1)]		SO8 (automotive grade)		SX922IY
TSX923IST		MiniSO10		K305

Notes:

[(1)]Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

8 Revision history

Table 14: Document revision history

Date	Revision	Changes
12-Apr-2013	1	Initial release
27-Jun-2013	2	Added TSX920,TSX922, TSX923 devices. Added packages for TSX920,TSX922, and TSX923. Added shutdown characteristics in Table 4, Table 5, and Table 6. Added Figure 35, Figure 36, and Figure 37. Updated Table 13 for new order codes.
10-Dec-2013	3	Added long-term input offset voltage drift parameter in Table 4, Table 5, and Table 6. Added Section 5.4: Input offset voltage drift over temperature in Section 5: Application information. Added Section 5.5: Long-term input offset voltage drift section in Section 5: Application information.
14-Jan-2016	4	Updated document layout *Table 4*, *Table 5*, and *Table 6*: updated V_{io} and DV_{io}/DT parameters *Table 7*: updated inches dimension "B" (typ) and "L" (typ and max) to align with rounded-off values of POA. *Table 10*: updated minimum mm dimensions for "k" *Table 13: "Order codes"*: added order codes TSX922IYST and TSX922IYDT.