

MPC8260A

PowerQUICC™ II Integrated Communications Processor

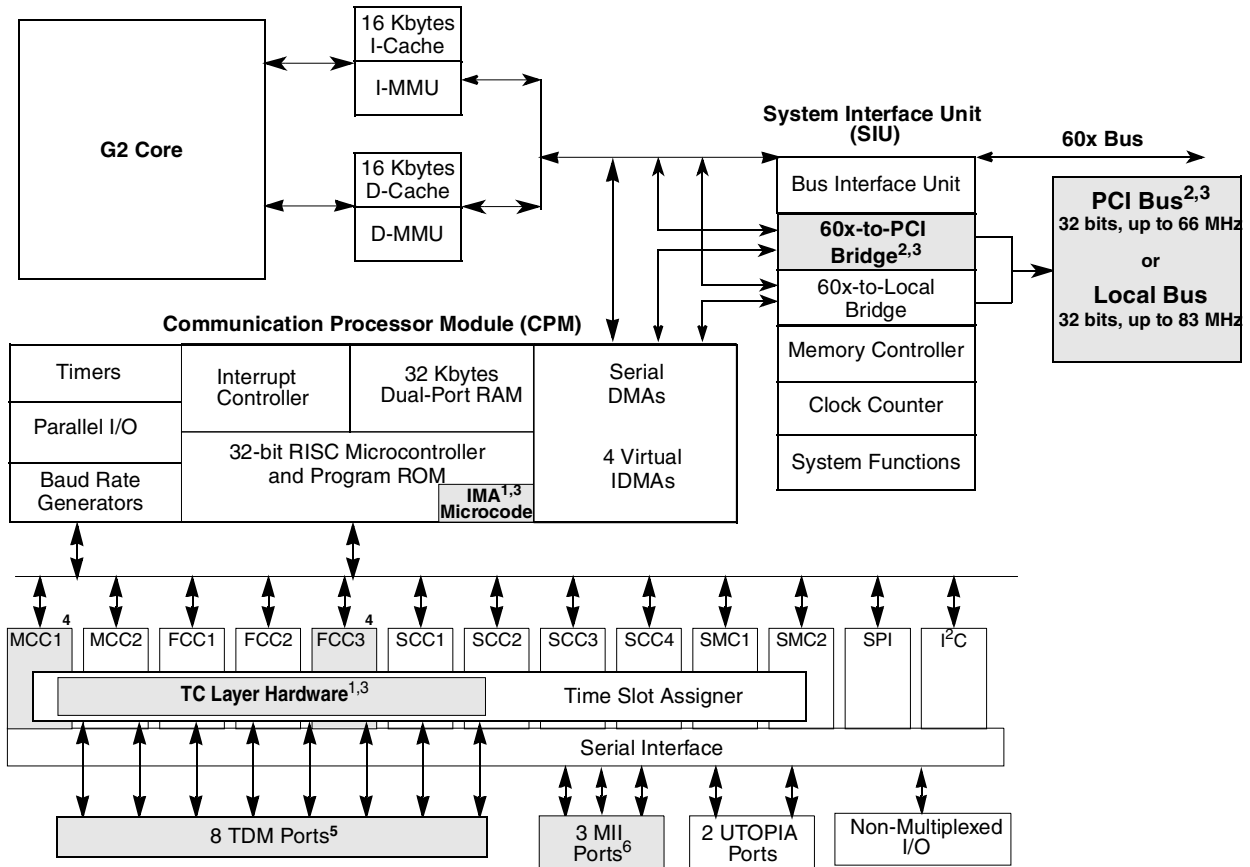
Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for .25μm (HiP4) devices in the PowerQUICC II™ MPC8260 communications processor family. These devices include the MPC8260, the MPC8255, the MPC8264, the MPC8265, and the MPC8266. Throughout this document, these devices are collectively referred to as the MPC826xA.

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Figure 1 shows the block diagram for the MPC8266, the HiP4 superset device. Shaded portions indicate functionality that is not available on all devices; refer to the notes.



- Notes:**
- ¹ MPC8264
 - ² MPC8265
 - ³ MPC8266
 - ⁴ Not on MPC8255
 - ⁵ 4 TDM ports on the MPC8255
 - ⁶ 2 MII ports on the MPC8255

Figure 1. MPC8266 Block Diagram

1 Features

The major features of the MPC826xA family are as follows:

- Dual-issue integer core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 150–300 MHz
 - Separate 16-Kbyte data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm

- PowerPC architecture-compliant memory management unit (MMU)
- Common on-chip processor (COP) test interface
- High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPS/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
 - Programmable host bridge and agent
 - 32-bit data bus, 66 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation

- 32-bit address decodes with programmable bank size
- Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
- Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
- Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
 - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
 - 10/100-Mbit Ethernet/IEEE Std. 802.3@ CDMA/CS interface through media independent interface (MII)
 - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
 - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
 - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
 - Two serial management controllers (SMCs), identical to those of the MPC860
 - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Transparent
- UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I²C) controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8255)
 - Supports two groups of four TDM channels for a total of eight TDMs
 - 2,048 bytes of SI RAM
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronization
 - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
 - 32-Kbyte dual-port RAM
 - Additional MCC host commands
 - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264 and MPC8266 only)
- CPM multiplexing
 - FCC2 can also be connected to the TC layer.
- TC layer (MPC8264 and MPC8266 only)
 - Each of the 8 TDM channels is routed in hardware to a TC layer block
 - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
 - Performing ATM TC layer functions (according to ITU-T I.432)
 - Transmit (Tx) updates
 - Cell HEC generation
 - Payload scrambling using self synchronizing scrambler (programmable by the user)
 - Coset generation (programmable by the user)
 - Cell rate by inserting idle/unassigned cells
 - Receive (Rx) updates
 - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
 - Payload descrambling using self synchronizing scrambler (programmable by the user)

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)
- Operates with FCC2 (UTOPIA 8)
- Provides serial loop back mode
- Cell echo mode is provided
- Supports both FCC transmit modes
 - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
 - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
- Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
- Cell counters for performance monitoring
 - 16-bit counters count
 - HEC error cells
 - HEC single bit error and corrected cells
 - Idle/unassigned cells filtered
 - Idle/unassigned cells transmitted
 - Transmitted ATM cells
 - Received ATM cells
 - Maskable interrupt is sent to the host when a counter expires
- Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported
- PCI bridge (MPC8265 and MPC8266 only)
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI to 60x memory and 60x memory to PCI streaming
 - PCI Host Bridge or Peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
 - Supports the I₂O standard

- Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
- Support for 66 MHz, 3.3 V specification
- 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
- Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. [Table 1](#) shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings¹

| Rating | Symbol | Value | Unit |
|----------------------------------|------------------|-----------------|------|
| Core supply voltage ² | VDD | -0.3 – 2.5 | V |
| PLL supply voltage ² | VCCSYN | -0.3 – 2.5 | V |
| I/O supply voltage ³ | VDDH | -0.3 – 4.0 | V |
| Input voltage ⁴ | VIN | GND(-0.3) – 3.6 | V |
| Junction temperature | T _j | 120 | °C |
| Storage temperature range | T _{STG} | (-55) – (+150) | °C |

¹ Absolute maximum ratings are stress ratings only; functional operation (see [Table 2](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

² **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

³ **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

⁴ **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions¹

| Rating | Symbol | Value | | | Unit |
|--------------------------------|----------------|------------------------|----------------------|------------------------|------|
| Core supply voltage | VDD | 1.7 – 1.9 ² | 1.7–2.1 ³ | 1.9 – 2.2 ⁴ | V |
| PLL supply voltage | VCCSYN | 1.7 – 1.9 ² | 1.7–2.1 ³ | 1.9–2.2 ⁴ | V |
| I/O supply voltage | VDDH | 3.135 – 3.465 | | | V |
| Input voltage | VIN | GND (–0.3) – 3.465 | | | V |
| Junction temperature (maximum) | T _j | 105 ⁵ | | | °C |
| Ambient temperature | T _A | 0–70 ⁵ | | | °C |

¹ **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

² CPU frequency less than or equal to 200 MHz.

³ CPU frequency greater than 200 MHz but less than 233 MHz.

⁴ CPU frequency greater than or equal to 233 MHz.

⁵ Note that for extended temperature parts the range is $(-40)_{T_A} - 105_{T_j}$.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

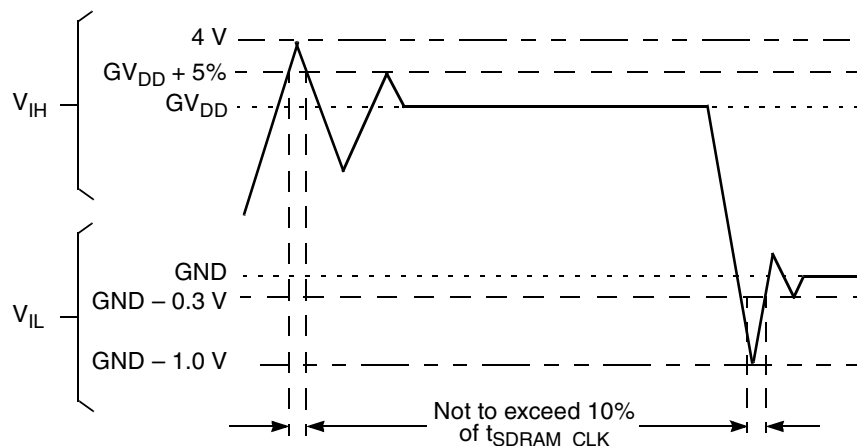


Figure 2. Overshoot/Undershoot Voltage

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics¹

| Characteristic | Symbol | Min | Max | Unit |
|---|-----------|-----|-------|---------|
| Input high voltage, all inputs except CLKIN | V_{IH} | 2.0 | 3.465 | V |
| Input low voltage | V_{IL} | GND | 0.8 | V |
| CLKIN input high voltage | V_{IHC} | 2.4 | 3.465 | V |
| CLKIN input low voltage | V_{ILC} | GND | 0.4 | V |
| Input leakage current, $V_{IN} = V_{DDH}^2$ | I_{IN} | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}^2$ | I_{OZ} | — | 10 | μA |
| Signal low input current, $V_{IL} = 0.8$ V | I_L | — | 1 | μA |
| Signal high input current, $V_{IH} = 2.0$ V | I_H | — | 1 | μA |
| Output high voltage, $I_{OH} = -2$ mA except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: $I_{OH} = -8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31] | V_{OH} | 2.4 | — | V |
| In UTOPIA mode: $I_{OL} = 8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31] | V_{OL} | — | 0.5 | V |

Table 3. DC Electrical Characteristics¹ (continued)

| Characteristic | Symbol | Min | Max | Unit |
|---|----------|-----|-----|------|
| $I_{OL} = 7.0 \text{ mA}$ $\overline{\text{BR}}$ $\overline{\text{BG}}$ $\overline{\text{ABB/IRQ2}}$ $\overline{\text{TS}}$ $\overline{\text{A[0-31]}}$ $\overline{\text{TT[0-4]}}$ $\overline{\text{TBST}}$ $\overline{\text{TSIZE[0-3]}}$ $\overline{\text{AACK}}$ $\overline{\text{ARTRY}}$ $\overline{\text{DBG}}$ $\overline{\text{DBB/IRQ3}}$ $\overline{\text{D[0-63]}}$ $\overline{\text{DP(0)/RSRV/EXT_BR2}}$ $\overline{\text{DP(1)/IRQ1/EXT_BG2}}$ $\overline{\text{DP(2)/TLBISYNC/IRQ2/EXT_DBG2}}$ $\overline{\text{DP(3)/IRQ3/EXT_BR3/CKSTP_OUT}}$ $\overline{\text{DP(4)/IRQ4/EXT_BG3/CORE_SREST}}$ $\overline{\text{DP(5)/TBEN/IRQ5/EXT_DBG3}}$ $\overline{\text{DP(6)/CSE(0)/IRQ6}}$ $\overline{\text{DP(7)/CSE(1)/IRQ7}}$ $\overline{\text{PSDVAL}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{GBL/IRQ1}}$ $\overline{\text{CI/BADDR29/IRQ2}}$ $\overline{\text{WT/BADDR30/IRQ3}}$ $\overline{\text{L2_HIT/IRQ4}}$ $\overline{\text{CPU_BG/BADDR31/IRQ5}}$ $\overline{\text{CPU_DBG}}$ $\overline{\text{CPU_BR}}$ $\overline{\text{IRQ0/NMI_OUT}}$ $\overline{\text{IRQ7/INT_OUT/APE}}$ $\overline{\text{PORESET}}$ $\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$ $\overline{\text{RSTCONF}}$ $\overline{\text{QREQ}}$ | V_{OL} | — | 0.4 | V |

Table 3. DC Electrical Characteristics¹ (continued)

| Characteristic | Symbol | Min | Max | Unit |
|--|----------|-----|-----|------|
| $I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ \overline{ALE} $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]^3$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}^3$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}^3$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}^3$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}^3$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}^3$ \overline{LWR} $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}^3$ $\overline{L_A15}/\overline{FRAME}^3/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}^3$ $\overline{L_A17}/\overline{IRDY}^3/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}^3$ $\overline{L_A19}/\overline{DEVSEL}^3$ $\overline{L_A20}/\overline{IDSEL}^3$ $\overline{L_A21}/\overline{PERR}^3$ $\overline{L_A22}/\overline{SERR}^3$ $\overline{L_A23}/\overline{REQ0}^3$ $\overline{L_A24}/\overline{REQ1}^3/\overline{HSEJSW}^3$ $\overline{L_A25}/\overline{GNT0}^3$ $\overline{L_A26}/\overline{GNT1}^3/\overline{HSLED}^3$ $\overline{L_A27}/\overline{GNT2}^3/\overline{HSENUM}^3$ $\overline{L_A28}/\overline{RST}^3/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTA}^3$ $\overline{L_A30}/\overline{REQ2}^3$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)/\overline{AD}(0-31)^3$ $\overline{LCL_DP}(0-3)/\overline{C}/\overline{BE}(0-3)^3$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ \overline{TDO} | V_{OL} | — | 0.4 | V |

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

² The leakage current is measured for nominal VDD, VCCSYN, and VDD.

³ MPC8265 and MPC8266 only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics for 480 TBGA Package

| Characteristics | Symbol | Value | Unit | Air Flow |
|--------------------------------|---------------|-----------------|------|-----------------|
| Junction to ambient | θ_{JA} | 13 ¹ | °C/W | NC ² |
| | | 10 ¹ | | 1 m/s |
| | | 11 ³ | | NC |
| | | 8 ³ | | 1 m/s |
| Junction to board ⁴ | θ_{JB} | 4 | °C/W | — |
| Junction to case ⁵ | θ_{JC} | 1.1 | °C/W | — |

¹ Assumes a single layer board with no thermal vias

² Natural convection

³ Assumes a four layer board

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J , in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K / (T_J + 273^\circ \text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ \text{C}) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3 \text{ W}$ (when the ambient temperature is 70°C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations¹

| Bus (MHz) | CPM Multiplier | Core CPU Multiplier | CPM (MHz) | CPU (MHz) | $P_{INT}(W)^2$ | | | |
|-----------|----------------|---------------------|-----------|-----------|----------------|---------|----------------|---------|
| | | | | | Vddl 1.8 Volts | | Vddl 2.0 Volts | |
| | | | | | Nominal | Maximum | Nominal | Maximum |
| 66.66 | 2 | 3 | 133 | 200 | 1.2 | 2 | 1.8 | 2.3 |
| 66.66 | 2.5 | 3 | 166 | 200 | 1.3 | 2.1 | 1.9 | 2.3 |
| 66.66 | 3 | 4 | 200 | 266 | — | — | 2.3 | 2.9 |
| 66.66 | 3 | 4.5 | 200 | 300 | — | — | 2.4 | 3.1 |
| 83.33 | 2 | 3 | 166 | 250 | — | — | 2.2 | 2.8 |
| 83.33 | 2 | 3 | 166 | 250 | — | — | 2.2 | 2.8 |
| 83.33 | 2.5 | 3.5 | 208 | 291 | — | — | 2.4 | 3.1 |

¹ Test temperature = room temperature (25°C)

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in [Table 6](#).

Table 6. Output Buffer Impedances¹

| Output Buffers | Typical Impedance (Ω) |
|-------------------|--------------------------------|
| 60x bus | 40 |
| Local bus | 40 |
| Memory controller | 40 |
| Parallel I/O | 46 |
| PCI | 25 |

¹ These are typical values at 65° C. The impedance may vary by $\pm 25\%$ with process and temperature.

[Table 7](#) lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs¹

| Spec Number | | Characteristic | Max Delay (ns) | | Min Delay (ns) | |
|-------------|-------|--|----------------|--------|----------------|--------|
| Max | Min | | 66 MHz | 83 MHz | 66 MHz | 83 MHz |
| sp36a | sp37a | FCC outputs—internal clock (NMSI) | 6 | 5.5 | 1 | 1 |
| sp36b | sp37b | FCC outputs—external clock (NMSI) | 14 | 12 | 2 | 1 |
| sp40 | sp41 | TDM outputs/SI | 25 | 16 | 5 | 4 |
| sp38a | sp39a | SCC/SMC/SPI/I2C outputs—internal clock (NMSI) | 19 | 16 | 1 | 0.5 |
| sp38b | sp39b | Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI) | 19 | 16 | 2 | 1 |
| sp42 | sp43 | TIMER/IDMA outputs | 14 | 11 | 1 | 0.5 |
| sp42a | sp43a | PIO outputs | 14 | 11 | 0.5 | 0.5 |

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs¹

| Spec Number | | Characteristic | Setup (ns) | | Hold (ns) | |
|-------------|-------|--|------------|--------|-----------|--------|
| Max | Min | | 66 MHz | 83 MHz | 66 MHz | 83 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 10 | 8 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 3 | 2.5 | 3 | 2 |
| sp20 | sp21 | TDM inputs/SI | 15 | 12 | 12 | 10 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 20 | 16 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 5 | 4 | 5 | 4 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 10 | 8 | 3 | 3 |

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

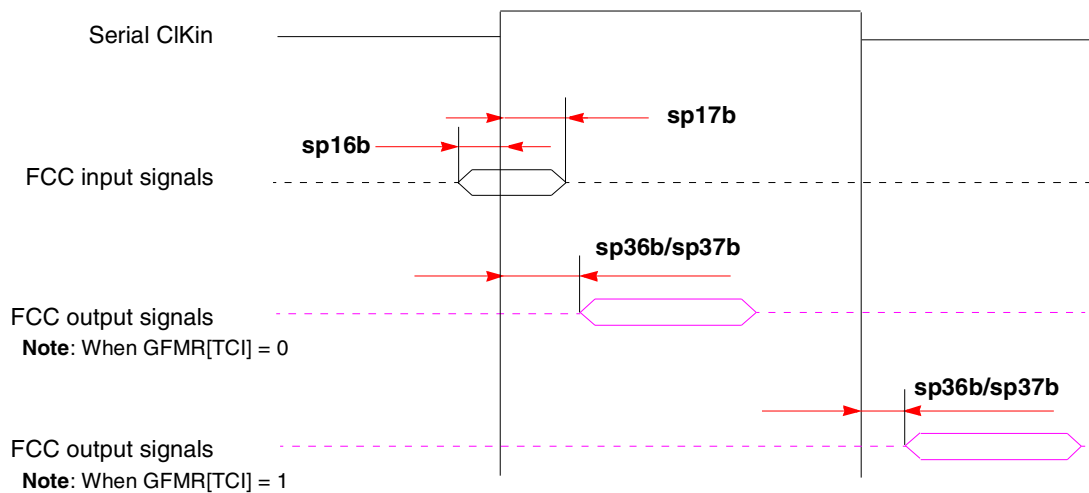


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

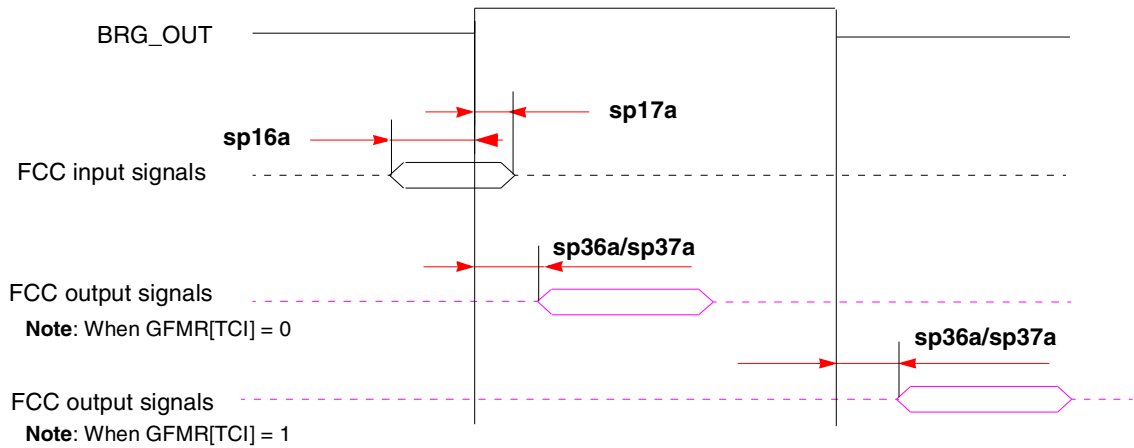
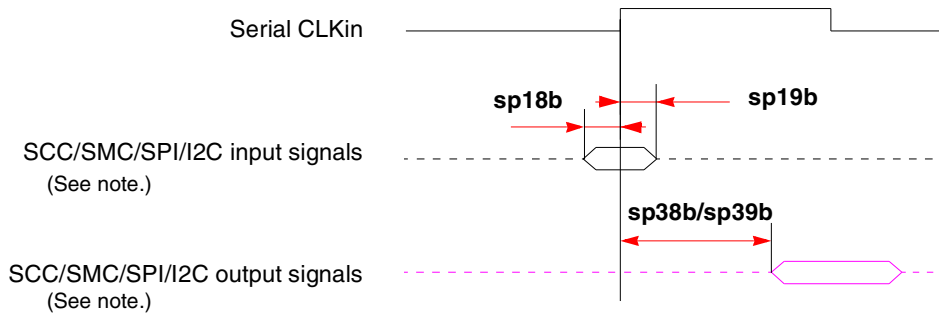


Figure 4. FCC Internal Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I²C external clock.

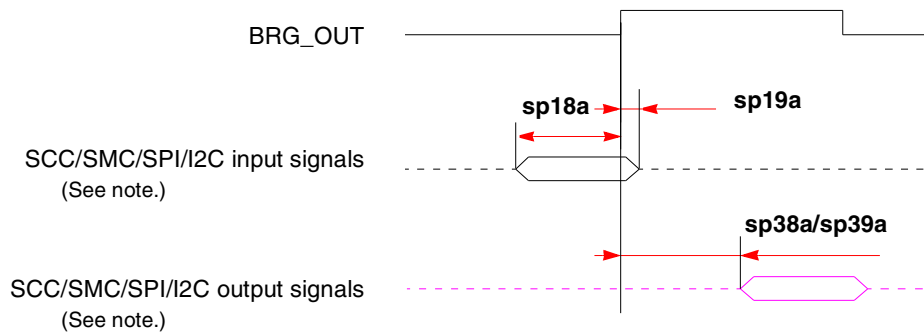


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I²C internal clock.

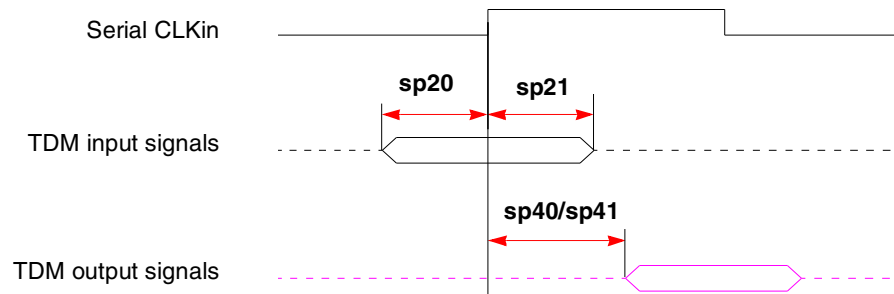


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

Figure 7 shows TDM input and output signals.

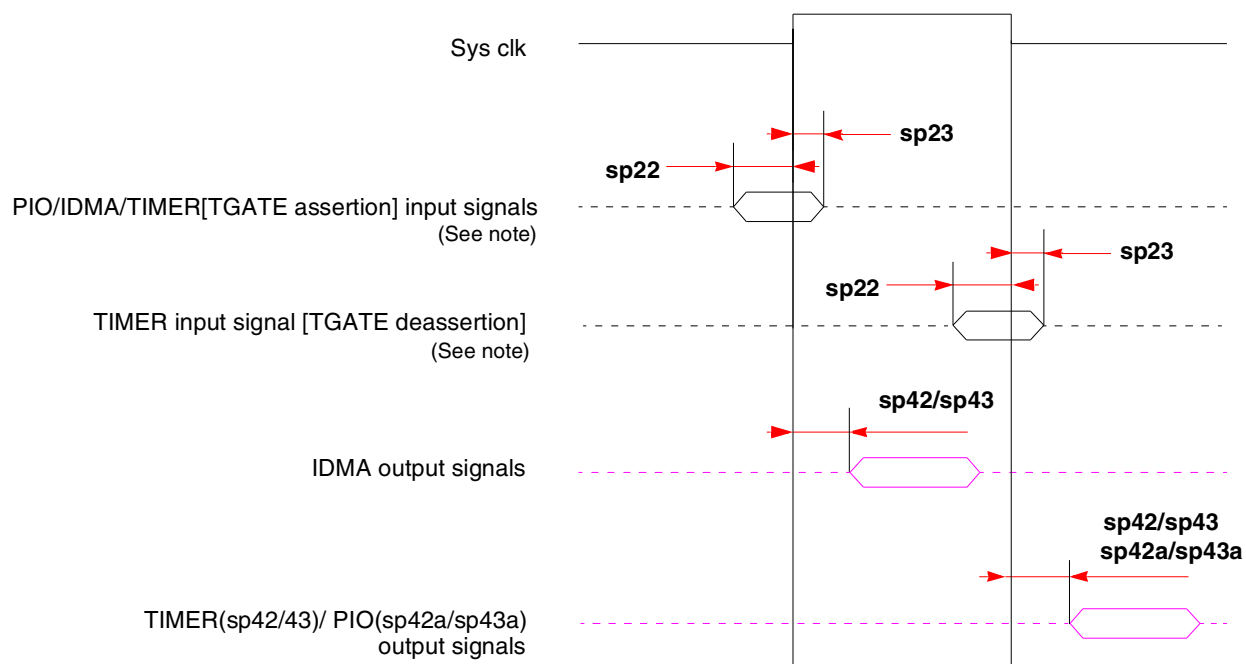


Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs¹

| Spec Number | | Characteristic | Setup (ns) | | Hold (ns) | |
|-------------|------|--|------------|--------|-----------|--------|
| Max | Min | | 66 MHz | 83 MHz | 66 MHz | 83 MHz |
| sp11 | sp10 | AACK/ARTRY/T \bar{A} /TS/TEA/DBG/BG/BR | 6 | 5 | 0.5 | 0.5 |
| sp12 | sp10 | Data bus in normal mode | 5 | 4 | 0.5 | 0.5 |
| sp13 | sp10 | Data bus in ECC and PARITY modes | 8 | 6 | 0.5 | 0.5 |
| sp14 | sp10 | DP pins | 7 | 6 | 0.5 | 0.5 |
| sp15 | sp10 | All other pins | 5 | 4 | 0.5 | 0.5 |

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs¹

| Spec Number | | Characteristic | Max Delay (ns) | | Min Delay (ns) | |
|-------------|------|-------------------------------|----------------|--------|----------------|--------|
| Max | Min | | 66 MHz | 83 MHz | 66 MHz | 83 MHz |
| sp31 | sp30 | PSDVAL/TEA/TA | 7 | 6 | 0.5 | 0.5 |
| sp32 | sp30 | ADD/ADD_atr./BADDR/CI/GBL/WT | 8 | 6.5 | 0.5 | 0.5 |
| sp33a | sp30 | Data bus | 6.5 | 6.5 | 0.5 | 0.5 |
| sp33b | sp30 | DP | 8 | 7 | 0.5 | 0.5 |
| sp34 | sp30 | Memory controller signals/ALE | 6 | 5 | 0.5 | 0.5 |
| sp35 | sp30 | All other signals | 6 | 5.5 | 0.5 | 0.5 |

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR_x[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 9 shows the interaction of several bus signals.

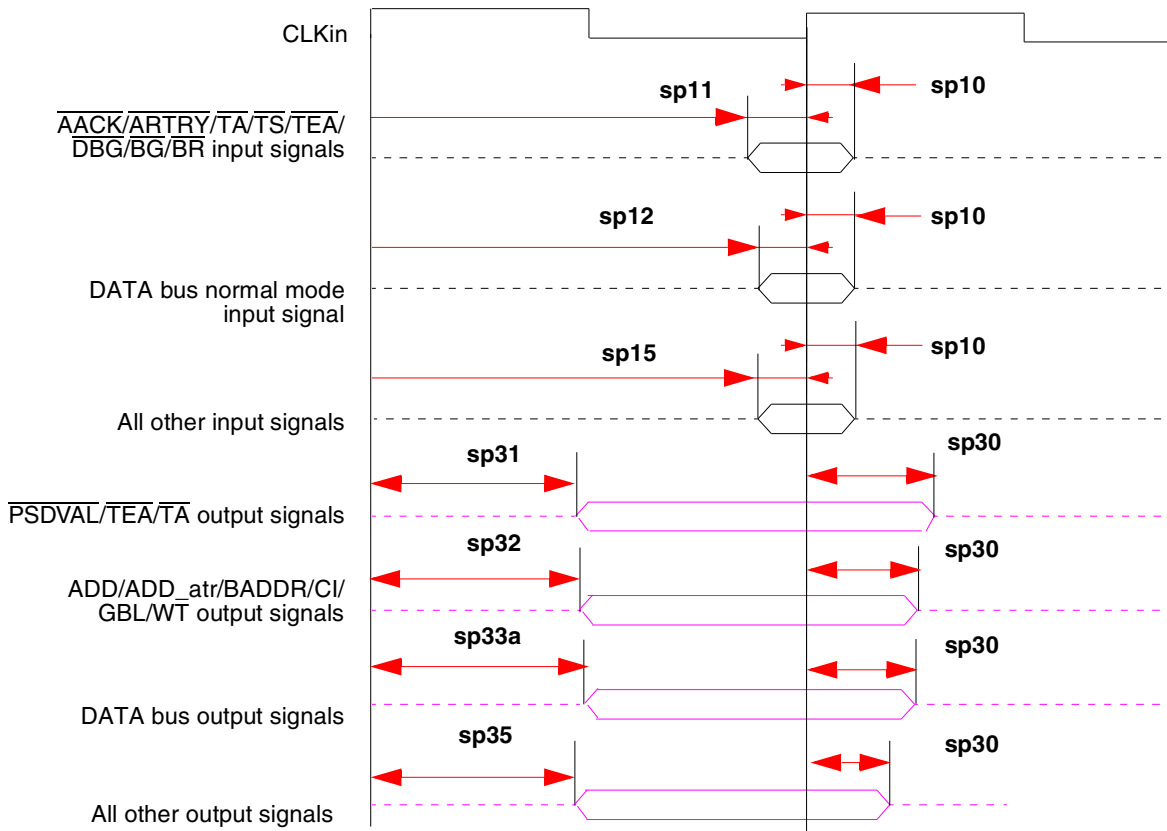


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

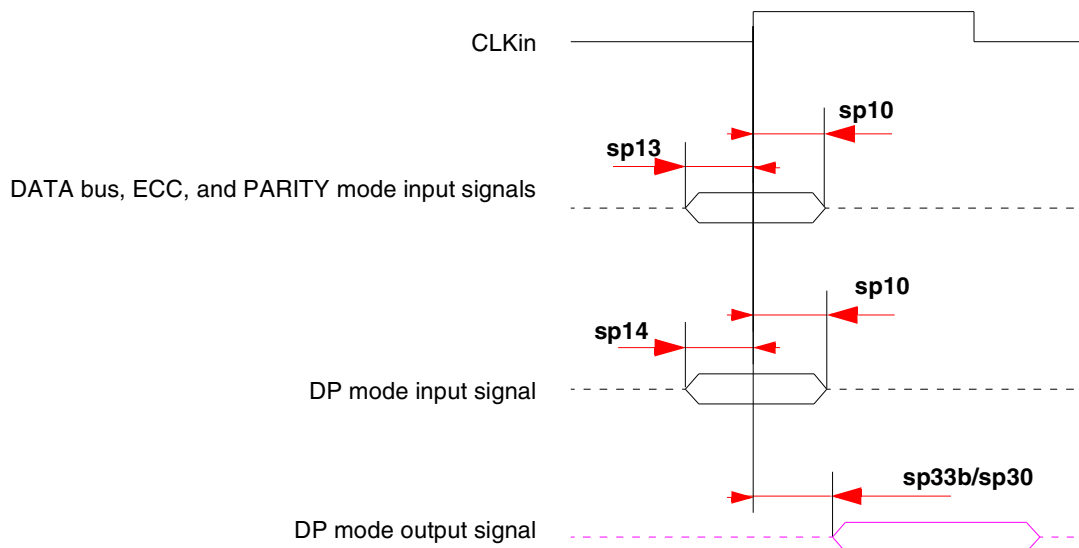


Figure 10. Parity Mode Diagram

Figure 11 shows signal behavior in MEMC mode.

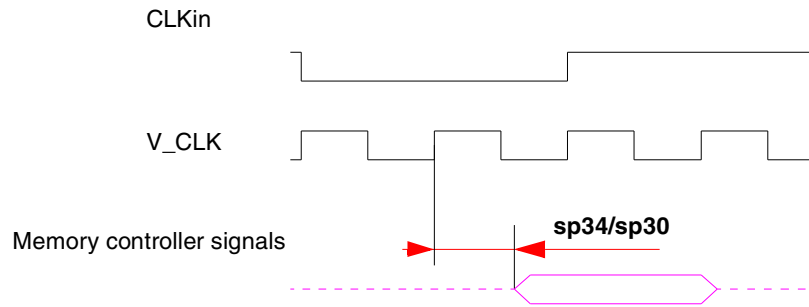


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC826xA bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of CLKIn) | | |
|-------------------------|--|-----------|-------------|
| | T2 | T3 | T4 |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 CLKIn | 1/2 CLKIn | 3/4 CLKIn |
| 1:2.5 | 3/10 CLKIn | 1/2 CLKIn | 8/10 CLKIn |
| 1:3.5 | 4/14 CLKIn | 1/2 CLKIn | 11/14 CLKIn |

Figure 12 is a graphical representation of Table 11.

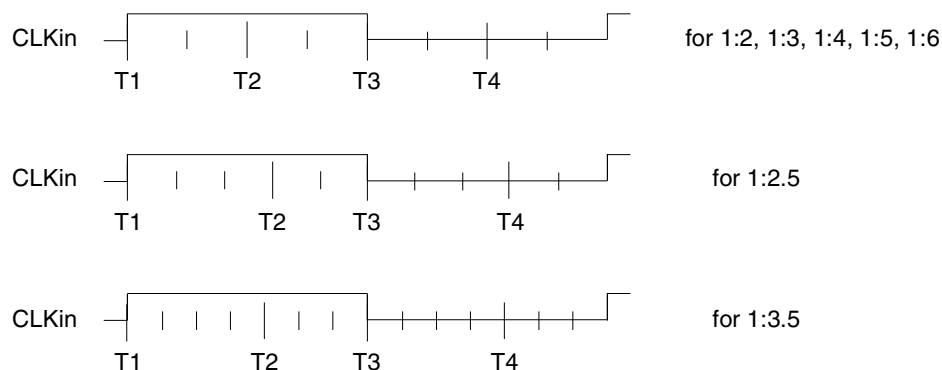


Figure 12. Internal Tick Spacing for Memory Controller Signals

Table 12 lists the JTAG timings.

Table 12. JTAG Timings¹

| Parameter | Symbol ² | Min | Max | Unit | Notes | |
|--|------------------------------|--------------|-----|------|-------|------|
| JTAG external clock frequency of operation | f_{JTG} | 0 | 25 | MHz | — | |
| JTAG external clock cycle time | t_{JTG} | 40 | — | ns | — | |
| JTAG external clock pulse width measured at 1.4V | t_{JTKHKL} | 20 | — | ns | — | |
| JTAG external clock rise and fall times | t_{JTGR} and t_{JTGF} | 0 | 5 | ns | 6 | |
| TRST assert time | t_{TRST} | 25 | — | ns | 3, 6 | |
| Input setup times | Boundary-scan data | t_{JTDVKH} | 4 | — | ns | 4, 7 |
| | TMS, TDI | t_{JTIVKH} | 4 | — | ns | 4, 7 |
| Input hold times | Boundary-scan data | t_{JTDXKH} | 10 | — | ns | 4, 7 |
| | TMS, TDI | t_{JTIXKH} | 10 | — | ns | 4, 7 |
| Output valid times | Boundary-scan data | t_{JTKLDV} | — | 25 | ns | 5, 7 |
| | TDO | t_{JTKLOV} | — | 25 | ns | 5, 7 |
| Output hold times | Boundary-scan data | t_{JTKLDX} | 1 | — | ns | 5, 7 |
| | TDO | t_{JTKLOX} | 1 | — | ns | 5, 7 |
| JTAG external clock to output high impedance | Boundary-scan data | t_{JTKLDZ} | 1 | 25 | ns | 5, 6 |
| | TDO | t_{JTKLOZ} | 1 | 25 | ns | 5, 6 |

¹ All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

² The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

³ TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

⁴ Non-JTAG signal input timing with respect to t_{TCLK} .

⁵ Non-JTAG signal output timing with respect to t_{TCLK} .

⁶ Guaranteed by design.

⁷ Guaranteed by design and device characterization.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin (RSTCONF) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

| MODCK[1–3] | Input Clock Frequency | CPM Multiplication Factor | CPM Frequency | Core Multiplication Factor | Core Frequency |
|------------|-----------------------|---------------------------|---------------|----------------------------|----------------|
| 000 | 33 MHz | 3 | 100 MHz | 4 | 133 MHz |
| 001 | 33 MHz | 3 | 100 MHz | 5 | 166 MHz |
| 010 | 33 MHz | 4 | 133 MHz | 4 | 133 MHz |
| 011 | 33 MHz | 4 | 133 MHz | 5 | 166 MHz |
| 100 | 66 MHz | 2 | 133 MHz | 2.5 | 166 MHz |
| 101 | 66 MHz | 2 | 133 MHz | 3 | 200 MHz |
| 110 | 66 MHz | 2.5 | 166 MHz | 2.5 | 166 MHz |
| 111 | 66 MHz | 2.5 | 166 MHz | 3 | 200 MHz |

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes¹

| MODCK_H–MODCK[1–3] | Input Clock Frequency ^{2,3} | CPM Multiplication Factor ² | CPM Frequency ² | Core Multiplication Factor ² | Core Frequency ² |
|--------------------|--------------------------------------|--|----------------------------|---|-----------------------------|
| 0001_000 | 33 MHz | 2 | 66 MHz | 4 | 133 MHz |
| 0001_001 | 33 MHz | 2 | 66 MHz | 5 | 166 MHz |
| 0001_010 | 33 MHz | 2 | 66 MHz | 6 | 200 MHz |
| 0001_011 | 33 MHz | 2 | 66 MHz | 7 | 233 MHz |
| 0001_100 | 33 MHz | 2 | 66 MHz | 8 | 266 MHz |

Table 14. Clock Configuration Modes¹ (continued)

| MODCK_H–MODCK[1–3] | Input Clock Frequency ^{2,3} | CPM Multiplication Factor ² | CPM Frequency ² | Core Multiplication Factor ² | Core Frequency ² |
|--------------------|--------------------------------------|--|----------------------------|---|-----------------------------|
| 0001_101 | 33 MHz | 3 | 100 MHz | 4 | 133 MHz |
| 0001_110 | 33 MHz | 3 | 100 MHz | 5 | 166 MHz |
| 0001_111 | 33 MHz | 3 | 100 MHz | 6 | 200 MHz |
| 0010_000 | 33 MHz | 3 | 100 MHz | 7 | 233 MHz |
| 0010_001 | 33 MHz | 3 | 100 MHz | 8 | 266 MHz |
| 0010_010 | 33 MHz | 4 | 133 MHz | 4 | 133 MHz |
| 0010_011 | 33 MHz | 4 | 133 MHz | 5 | 166 MHz |
| 0010_100 | 33 MHz | 4 | 133 MHz | 6 | 200 MHz |
| 0010_101 | 33 MHz | 4 | 133 MHz | 7 | 233 MHz |
| 0010_110 | 33 MHz | 4 | 133 MHz | 8 | 266 MHz |
| 0010_111 | 33 MHz | 5 | 166 MHz | 4 | 133 MHz |
| 0011_000 | 33 MHz | 5 | 166 MHz | 5 | 166 MHz |
| 0011_001 | 33 MHz | 5 | 166 MHz | 6 | 200 MHz |
| 0011_010 | 33 MHz | 5 | 166 MHz | 7 | 233 MHz |
| 0011_011 | 33 MHz | 5 | 166 MHz | 8 | 266 MHz |
| 0011_100 | 33 MHz | 6 | 200 MHz | 4 | 133 MHz |
| 0011_101 | 33 MHz | 6 | 200 MHz | 5 | 166 MHz |
| 0011_110 | 33 MHz | 6 | 200 MHz | 6 | 200 MHz |
| 0011_111 | 33 MHz | 6 | 200 MHz | 7 | 233 MHz |
| 0100_000 | 33 MHz | 6 | 200 MHz | 8 | 266 MHz |
| 0100_001 | Reserved | | | | |
| 0100_010 | | | | | |
| 0100_011 | | | | | |
| 0100_100 | | | | | |
| 0100_101 | | | | | |
| 0100_110 | | | | | |

Table 14. Clock Configuration Modes¹ (continued)

| MODCK_H–MODCK[1–3] | Input Clock Frequency ^{2,3} | CPM Multiplication Factor ² | CPM Frequency ² | Core Multiplication Factor ² | Core Frequency ² |
|--------------------|--------------------------------------|--|----------------------------|---|-----------------------------|
| 0100_111 | Reserved | | | | |
| 0101_000 | | | | | |
| 0101_001 | | | | | |
| 0101_010 | | | | | |
| 0101_011 | | | | | |
| 0101_100 | | | | | |
| 0101_101 | 66 MHz | 2 | 133 MHz | 2 | 133 MHz |
| 0101_110 | 66 MHz | 2 | 133 MHz | 2.5 | 166 MHz |
| 0101_111 | 66 MHz | 2 | 133 MHz | 3 | 200 MHz |
| 0110_000 | 66 MHz | 2 | 133 MHz | 3.5 | 233 MHz |
| 0110_001 | 66 MHz | 2 | 133 MHz | 4 | 266 MHz |
| 0110_010 | 66 MHz | 2 | 133 MHz | 4.5 | 300 MHz |
| 0110_011 | 66 MHz | 2.5 | 166 MHz | 2 | 133 MHz |
| 0110_100 | 66 MHz | 2.5 | 166 MHz | 2.5 | 166 MHz |
| 0110_101 | 66 MHz | 2.5 | 166 MHz | 3 | 200 MHz |
| 0110_110 | 66 MHz | 2.5 | 166 MHz | 3.5 | 233 MHz |
| 0110_111 | 66 MHz | 2.5 | 166 MHz | 4 | 266 MHz |
| 0111_000 | 66 MHz | 2.5 | 166 MHz | 4.5 | 300 MHz |
| 0111_001 | 66 MHz | 3 | 200 MHz | 2 | 133 MHz |
| 0111_010 | 66 MHz | 3 | 200 MHz | 2.5 | 166 MHz |
| 0111_011 | 66 MHz | 3 | 200 MHz | 3 | 200 MHz |
| 0111_100 | 66 MHz | 3 | 200 MHz | 3.5 | 233 MHz |
| 0111_101 | 66 MHz | 3 | 200 MHz | 4 | 266 MHz |
| 0111_110 | 66 MHz | 3 | 200 MHz | 4.5 | 300 MHz |
| 0111_111 | 66 MHz | 3.5 | 233 MHz | 2 | 133 MHz |
| 1000_000 | 66 MHz | 3.5 | 233 MHz | 2.5 | 166 MHz |

Table 14. Clock Configuration Modes¹ (continued)

| MODCK_H–MODCK[1–3] | Input Clock Frequency ^{2,3} | CPM Multiplication Factor ² | CPM Frequency ² | Core Multiplication Factor ² | Core Frequency ² |
|--------------------|--------------------------------------|--|----------------------------|---|-----------------------------|
| 1000_001 | 66 MHz | 3.5 | 233 MHz | 3 | 200 MHz |
| 1000_010 | 66 MHz | 3.5 | 233 MHz | 3.5 | 233 MHz |
| 1000_011 | 66 MHz | 3.5 | 233 MHz | 4 | 266 MHz |
| 1000_100 | 66 MHz | 3.5 | 233 MHz | 4.5 | 300 MHz |

¹ Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

² The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 150 MHz and the CPM ranges between 66–233 MHz.

³ Input clock frequency is given only for the purpose of reference. The user should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3.2 PCI Mode

The MPC8265 and the MPC8266 have three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 15.

Table 15. MPC8265 and MPC8266 Clocking Modes

| Pins | | | Clocking Mode | PCI Clock Frequency Range (MHZ) |
|----------|------------|-----------|---------------|---------------------------------|
| PCI_MODE | PCI_CFG[0] | PCI_MODCK | | |
| 1 | — | — | Local bus | — |
| 0 | 0 | 0 | PCI host | 50–66 |
| 0 | 0 | 1 | | 25–50 |
| 0 | 1 | 0 | PCI agent | 50–66 |
| 0 | 1 | 1 | | 25–50 |

In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.2.1 PCI Host Mode

The frequencies listed in [Table 16](#) and [Table 17](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

| MODCK[1–3] ¹ | Input Clock Frequency (Bus) | CPM Multiplication Factor | CPM Frequency | Core Multiplication Factor | Core Frequency | PCI Division Factor ² | PCI Frequency ² |
|-------------------------|-----------------------------|---------------------------|---------------|----------------------------|----------------|----------------------------------|----------------------------|
| 000 | 66 MHz | 2 | 133 MHz | 2.5 | 166 MHz | 2/4 | 66/33 MHz |
| 001 | 66 MHz | 2 | 133 MHz | 3 | 200 MHz | 2/4 | 66/33 MHz |
| 010 | 66 MHz | 2.5 | 166 MHz | 3 | 200 MHz | 3/6 | 55/28 MHz |
| 011 | 66 MHz | 2.5 | 166 MHz | 3.5 | 233 MHz | 3/6 | 55/28 MHz |
| 100 | 66 MHz | 2.5 | 166 MHz | 4 | 266 MHz | 3/6 | 55/28 MHz |
| 101 | 66 MHz | 3 | 200 MHz | 3 | 200 MHz | 3/6 | 66/33 MHz |
| 110 | 66 MHz | 3 | 200 MHz | 3.5 | 233 MHz | 3/6 | 66/33 MHz |
| 111 | 66 MHz | 3 | 200 MHz | 4 | 266 MHz | 3/6 | 66/33 MHz |

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to [Table 15](#).

[Table 17](#) describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

| MODCK_H – MODCK[1–3] | Input Clock Frequency ¹ (Bus) | CPM Multiplication Factor | CPM Frequency | Core Multiplication Factor | Core Frequency | PCI Division Factor ² | PCI Frequency ² |
|-----------------------|--|---------------------------|----------------|----------------------------|----------------|----------------------------------|----------------------------|
| 0001_000 | 33 MHz | 3 | 100 MHz | 5 | 166 MHz | 3/6 | 33/16 MHz |
| 0001_001 | 33 MHz | 3 | 100 MHz | 6 | 200 MHz | 3/6 | 33/16 MHz |
| 0001_010 | 33 MHz | 3 | 100 MHz | 7 | 233 MHz | 3/6 | 33/16 MHz |
| 0001_011 | 33 MHz | 3 | 100 MHz | 8 | 266 MHz | 3/6 | 33/16 MHz |
| | | | | | | | |
| 0010_000 | 33 MHz | 4 | 133 MHz | 5 | 166 MHz | 4/8 | 33/16 MHz |
| 0010_001 | 33 MHz | 4 | 133 MHz | 6 | 200 MHz | 4/8 | 33/16 MHz |
| 0010_010 | 33 MHz | 4 | 133 MHz | 7 | 233 MHz | 4/8 | 33/16 MHz |
| 0010_011 | 33 MHz | 4 | 133 MHz | 8 | 266 MHz | 4/8 | 33/16 MHz |
| | | | | | | | |
| 0011_000 ³ | 33 MHz | 5 | 166 MHz | 5 | 166 MHz | 5 | 33 MHz |
| 0011_001 ³ | 33 MHz | 5 | 166 MHz | 6 | 200 MHz | 5 | 33 MHz |
| 0011_010 ³ | 33 MHz | 5 | 166 MHz | 7 | 233 MHz | 5 | 33 MHz |

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

| MODCK_H – MODCK[1–3] | Input Clock Frequency¹ (Bus) | CPM Multiplication Factor | CPM Frequency | Core Multiplication Factor | Core Frequency | PCI Division Factor² | PCI Frequency² |
|-----------------------------|--|----------------------------------|----------------------|-----------------------------------|-----------------------|--|----------------------------------|
| 0011_011 ³ | 33 MHz | 5 | 166 MHz | 8 | 266 MHz | 5 | 33 MHz |
| 0100_000 ³ | 33 MHz | 6 | 200 MHz | 5 | 166 MHz | 6 | 33 MHz |
| 0100_001 ³ | 33 MHz | 6 | 200 MHz | 6 | 200 MHz | 6 | 33 MHz |
| 0100_010 ³ | 33 MHz | 6 | 200 MHz | 7 | 233 MHz | 6 | 33 MHz |
| 0100_011 ³ | 33 MHz | 6 | 200 MHz | 8 | 266 MHz | 6 | 33 MHz |
| 0101_000 | 66 MHz | 2 | 133 MHz | 2.5 | 166 MHz | 2/4 | 66/33 MHz |
| 0101_001 | 66 MHz | 2 | 133 MHz | 3 | 200 MHz | 2/4 | 66/33 MHz |
| 0101_010 | 66 MHz | 2 | 133 MHz | 3.5 | 233 MHz | 2/4 | 66/33 MHz |
| 0101_011 | 66 MHz | 2 | 133 MHz | 4 | 266 MHz | 2/4 | 66/33 MHz |
| 0101_100 | 66 MHz | 2 | 133 MHz | 4.5 | 300 MHz | 2/4 | 66/33 MHz |
| 0110_000 | 66 MHz | 2.5 | 166 MHz | 2.5 | 166 MHz | 3/6 | 55/28 MHz |
| 0110_001 | 66 MHz | 2.5 | 166 MHz | 3 | 200 MHz | 3/6 | 55/28 MHz |
| 0110_010 | 66 MHz | 2.5 | 166 MHz | 3.5 | 233 MHz | 3/6 | 55/28 MHz |
| 0110_011 | 66 MHz | 2.5 | 166 MHz | 4 | 266 MHz | 3/6 | 55/28 MHz |
| 0110_100 | 66 MHz | 2.5 | 166 MHz | 4.5 | 300 MHz | 3/6 | 55/28 MHz |
| 0111_000 | 66 MHz | 3 | 200 MHz | 2.5 | 166 MHz | 3/6 | 66/33 MHz |
| 0111_001 | 66 MHz | 3 | 200 MHz | 3 | 200 MHz | 3/6 | 66/33 MHz |
| 0111_010 | 66 MHz | 3 | 200 MHz | 3.5 | 233 MHz | 3/6 | 66/33 MHz |
| 0111_011 | 66 MHz | 3 | 200 MHz | 4 | 266 MHz | 3/6 | 66/33 MHz |
| 0111_100 | 66 MHz | 3 | 200 MHz | 4.5 | 300 MHz | 3/6 | 66/33 MHz |
| 1000_000 | 66 MHz | 3 | 200 MHz | 2.5 | 166 MHz | 4/8 | 50/25 MHz |
| 1000_001 | 66 MHz | 3 | 200 MHz | 3 | 200 MHz | 4/8 | 50/25 MHz |
| 1000_010 | 66 MHz | 3 | 200 MHz | 3.5 | 233 MHz | 4/8 | 50/25 MHz |
| 1000_011 | 66 MHz | 3 | 200 MHz | 4 | 266 MHz | 4/8 | 50/25 MHz |
| 1000_100 | 66 MHz | 3 | 200 MHz | 4.5 | 300 MHz | 4/8 | 50/25 MHz |
| 1001_000 | 66 MHz | 3.5 | 233 MHz | 2.5 | 166 MHz | 4/8 | 58/29 MHz |
| 1001_001 | 66 MHz | 3.5 | 233 MHz | 3 | 200 MHz | 4/8 | 58/29 MHz |

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

| MODCK_H – MODCK[1–3] | Input Clock Frequency ¹ (Bus) | CPM Multiplication Factor | CPM Frequency | Core Multiplication Factor | Core Frequency | PCI Division Factor ² | PCI Frequency ² |
|----------------------|--|---------------------------|---------------|----------------------------|----------------|----------------------------------|----------------------------|
| 1001_010 | 66 MHz | 3.5 | 233 MHz | 3.5 | 233 MHz | 4/8 | 58/29 MHz |
| 1001_011 | 66 MHz | 3.5 | 233 MHz | 4 | 266 MHz | 4/8 | 58/29 MHz |
| 1001_100 | 66 MHz | 3.5 | 233 MHz | 4.5 | 300 MHz | 4/8 | 58/29 MHz |
| | | | | | | | |
| 1010_000 | 100 MHz | 2 | 200 MHz | 2 | 200 MHz | 3/6 | 66/33 MHz |
| 1010_001 | 100 MHz | 2 | 200 MHz | 2.5 | 250 MHz | 3/6 | 66/33 MHz |
| 1010_010 | 100 MHz | 2 | 200 MHz | 3 | 300 MHz | 3/6 | 66/33 MHz |
| 1010_011 | 100 MHz | 2 | 200 MHz | 3.5 | 350 MHz | 3/6 | 66/33 MHz |
| 1010_100 | 100 MHz | 2 | 200 MHz | 4 | 400 MHz | 3/6 | 66/33 MHz |
| | | | | | | | |
| 1011_000 | 100 MHz | 2.5 | 250 MHz | 2 | 200 MHz | 4/8 | 62/31 MHz |
| 1011_001 | 100 MHz | 2.5 | 250 MHz | 2.5 | 250 MHz | 4/8 | 62/31MHz |
| 1011_010 | 100 MHz | 2.5 | 250 MHz | 3 | 300 MHz | 4/8 | 62/31 MHz |
| 1011_011 | 100 MHz | 2.5 | 250 MHz | 3.5 | 350 MHz | 4/8 | 62/31 MHz |
| 1011_100 | 100 MHz | 2.5 | 250 MHz | 4 | 400 MHz | 4/8 | 62/31 MHz |

¹ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to [Table 15](#).

³ In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in [Table 18](#) and [Table 19](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

| MODCK[1–3] ¹ | Input Clock Frequency (PCI) ² | CPM Multiplication Factor ² | CPM Frequency | Core Multiplication Factor | Core Frequency ³ | Bus Division Factor | 60x Bus Frequency ⁴ |
|-------------------------|--|--|---------------|----------------------------|-----------------------------|---------------------|--------------------------------|
| 000 | 66/33 MHz | 2/4 | 133 MHz | 2.5 | 166 MHz | 2 | 66 MHz |
| 001 | 66/33 MHz | 2/4 | 133 MHz | 3 | 200 MHz | 2 | 66 MHz |
| 010 | 66/33 MHz | 3/6 | 200 MHz | 3 | 200 MHz | 3 | 66 MHz |
| 011 | 66/33 MHz | 3/6 | 200 MHz | 4 | 266 MHz | 3 | 66 MHz |

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

| MODCK[1-3] ¹ | Input Clock Frequency (PCI) ² | CPM Multiplication Factor ² | CPM Frequency | Core Multiplication Factor | Core Frequency ³ | Bus Division Factor | 60x Bus Frequency ⁴ |
|-------------------------|--|--|---------------|----------------------------|-----------------------------|---------------------|--------------------------------|
| 100 | 66/33 MHz | 3/6 | 200 MHz | 3 | 240 MHz | 2.5 | 80 MHz |
| 101 | 66/33 MHz | 3/6 | 200 MHz | 3.5 | 280 MHz | 2.5 | 80 MHz |
| 110 | 66/33 MHz | 4/8 | 266 MHz | 3.5 | 300 MHz | 3 | 88 MHz |
| 111 | 66/33 MHz | 4/8 | 266 MHz | 3 | 300 MHz | 2.5 | 100 MHz |

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).

³ Core frequency = (60x bus frequency)(core multiplication factor)

⁴ Bus frequency = CPM frequency/bus division factor

[Table 19](#) describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

| MODCK_H – MODCK[1-3] | Input Clock Frequency (PCI) ^{1,2} | CPM Multiplication Factor ¹ | CPM Frequency | Core Multiplication Factor | Core Frequency ³ | Bus Division Factor | 60x Bus Frequency ⁴ |
|----------------------|--|--|----------------|----------------------------|-----------------------------|---------------------|--------------------------------|
| 0001_001 | 66/33 MHz | 2/4 | 133 MHz | 5 | 166 MHz | 4 | 33 MHz |
| 0001_010 | 66/33 MHz | 2/4 | 133 MHz | 6 | 200 MHz | 4 | 33 MHz |
| 0001_011 | 66/33 MHz | 2/4 | 133 MHz | 7 | 233 MHz | 4 | 33 MHz |
| 0001_100 | 66/33 MHz | 2/4 | 133 MHz | 8 | 266 MHz | 4 | 33 MHz |
| | | | | | | | |
| 0010_001 | 50/25 MHz | 3/6 | 150 MHz | 3 | 180 MHz | 2.5 | 60 MHz |
| 0010_010 | 50/25 MHz | 3/6 | 150 MHz | 3.5 | 210 MHz | 2.5 | 60 MHz |
| 0010_011 | 50/25 MHz | 3/6 | 150 MHz | 4 | 240 MHz | 2.5 | 60 MHz |
| 0010_100 | 50/25 MHz | 3/6 | 150 MHz | 4.5 | 270 MHz | 2.5 | 60 MHz |
| | | | | | | | |
| 0011_000 | 66/33 MHz | 2/4 | 133 MHz | 2.5 | 110MHz | 3 | 44 MHz |
| 0011_001 | 66/33 MHz | 2/4 | 133 MHz | 3 | 132 MHz | 3 | 44 MHz |
| 0011_010 | 66/33 MHz | 2/4 | 133 MHz | 3.5 | 154 MHz | 3 | 44 MHz |
| 0011_011 | 66/33 MHz | 2/4 | 133 MHz | 4 | 176MHz | 3 | 44 MHz |
| 0011_100 | 66/33 MHz | 2/4 | 133 MHz | 4.5 | 198 MHz | 3 | 44 MHz |
| | | | | | | | |
| 0100_000 | 66/33 MHz | 3/6 | 200 MHz | 2.5 | 166 MHz | 3 | 66 MHz |
| 0100_001 | 66/33 MHz | 3/6 | 200 MHz | 3 | 200 MHz | 3 | 66 MHz |
| 0100_010 | 66/33 MHz | 3/6 | 200 MHz | 3.5 | 233 MHz | 3 | 66 MHz |
| 0100_011 | 66/33 MHz | 3/6 | 200 MHz | 4 | 266 MHz | 3 | 66 MHz |

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

| MODCK_H – MODCK[1–3] | Input Clock Frequency (PCI) ^{1,2} | CPM Multiplication Factor ¹ | CPM Frequency | Core Multiplication Factor | Core Frequency ³ | Bus Division Factor | 60x Bus Frequency ⁴ |
|-----------------------|--|--|----------------|----------------------------|-----------------------------|---------------------|--------------------------------|
| 0100_100 | 66/33 MHz | 3/6 | 200 MHz | 4.5 | 300 MHz | 3 | 66 MHz |
| 0101_000 ⁵ | 33 MHz | 5 | 166 MHz | 2.5 | 166 MHz | 2.5 | 66 MHz |
| 0101_001 ⁵ | 33 MHz | 5 | 166 MHz | 3 | 200 MHz | 2.5 | 66 MHz |
| 0101_010 ⁵ | 33 MHz | 5 | 166 MHz | 3.5 | 233 MHz | 2.5 | 66 MHz |
| 0101_011 ⁵ | 33 MHz | 5 | 166 MHz | 4 | 266 MHz | 2.5 | 66 MHz |
| 0101_100 ⁵ | 33 MHz | 5 | 166 MHz | 4.5 | 300 MHz | 2.5 | 66 MHz |
| 0110_000 | 50/25 MHz | 4/8 | 200 MHz | 2.5 | 166 MHz | 3 | 66 MHz |
| 0110_001 | 50/25 MHz | 4/8 | 200 MHz | 3 | 200 MHz | 3 | 66 MHz |
| 0110_010 | 50/25 MHz | 4/8 | 200 MHz | 3.5 | 233 MHz | 3 | 66 MHz |
| 0110_011 | 50/25 MHz | 4/8 | 200 MHz | 4 | 266 MHz | 3 | 66 MHz |
| 0110_100 | 50/25 MHz | 4/8 | 200 MHz | 4.5 | 300 MHz | 3 | 66 MHz |
| 0111_000 | 66/33 MHz | 3/6 | 200 MHz | 2 | 200 MHz | 2 | 100 MHz |
| 0111_001 | 66/33 MHz | 3/6 | 200 MHz | 2.5 | 250 MHz | 2 | 100 MHz |
| 0111_010 | 66/33 MHz | 3/6 | 200 MHz | 3 | 300 MHz | 2 | 100 MHz |
| 0111_011 | 66/33 MHz | 3/6 | 200 MHz | 3.5 | 350 MHz | 2 | 100 MHz |
| 1000_000 | 66/33 MHz | 3/6 | 200 MHz | 2 | 160 MHz | 2.5 | 80 MHz |
| 1000_001 | 66/33 MHz | 3/6 | 200 MHz | 2.5 | 200 MHz | 2.5 | 80 MHz |
| 1000_010 | 66/33 MHz | 3/6 | 200 MHz | 3 | 240 MHz | 2.5 | 80 MHz |
| 1000_011 | 66/33 MHz | 3/6 | 200 MHz | 3.5 | 280 MHz | 2.5 | 80 MHz |
| 1000_100 | 66/33 MHz | 3/6 | 200 MHz | 4 | 320 MHz | 2.5 | 80 MHz |
| 1000_101 | 66/33 MHz | 3/6 | 200 MHz | 4.5 | 360 MHz | 2.5 | 80 MHz |
| 1001_000 | 66/33 MHz | 4/8 | 266 MHz | 2.5 | 166 MHz | 4 | 66 MHz |
| 1001_001 | 66/33 MHz | 4/8 | 266 MHz | 3 | 200 MHz | 4 | 66 MHz |
| 1001_010 | 66/33 MHz | 4/8 | 266 MHz | 3.5 | 233 MHz | 4 | 66 MHz |
| 1001_011 | 66/33 MHz | 4/8 | 266 MHz | 4 | 266 MHz | 4 | 66 MHz |
| 1001_100 | 66/33 MHz | 4/8 | 266 MHz | 4.5 | 300 MHz | 4 | 66 MHz |
| 1010_000 | 66/33 MHz | 4/8 | 266 MHz | 2.5 | 222 MHz | 3 | 88 MHz |

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

| MODCK_H – MODCK[1–3] | Input Clock Frequency (PCI) ^{1,2} | CPM Multiplication Factor ¹ | CPM Frequency | Core Multiplication Factor | Core Frequency ³ | Bus Division Factor | 60x Bus Frequency ⁴ |
|----------------------|--|--|---------------|----------------------------|-----------------------------|---------------------|--------------------------------|
| 1010_001 | 66/33 MHz | 4/8 | 266 MHz | 3 | 266 MHz | 3 | 88 MHz |
| 1010_010 | 66/33 MHz | 4/8 | 266 MHz | 3.5 | 300 MHz | 3 | 88 MHz |
| 1010_011 | 66/33 MHz | 4/8 | 266 MHz | 4 | 350 MHz | 3 | 88 MHz |
| 1010_100 | 66/33 MHz | 4/8 | 266 MHz | 4.5 | 400 MHz | 3 | 88 MHz |
| | | | | | | | |
| 1011_000 | 66/33 MHz | 4/8 | 266 MHz | 2 | 212MHz | 2.5 | 106 MHz |
| 1011_001 | 66/33 MHz | 4/8 | 266 MHz | 2.5 | 265 MHz | 2.5 | 106 MHz |
| 1011_010 | 66/33 MHz | 4/8 | 266 MHz | 3 | 318 MHz | 2.5 | 106 MHz |
| 1011_011 | 66/33 MHz | 4/8 | 266 MHz | 3.5 | 371 MHz | 2.5 | 106 MHz |
| 1011_100 | 66/33 MHz | 4/8 | 266 MHz | 4 | 424 MHz | 2.5 | 106 MHz |

¹ The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).

² Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

³ Core frequency = (60x bus frequency)(core multiplication factor)

⁴ Bus frequency = CPM frequency/bus division factor

⁵ In this mode, PCI_MODCK must be "1".

4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

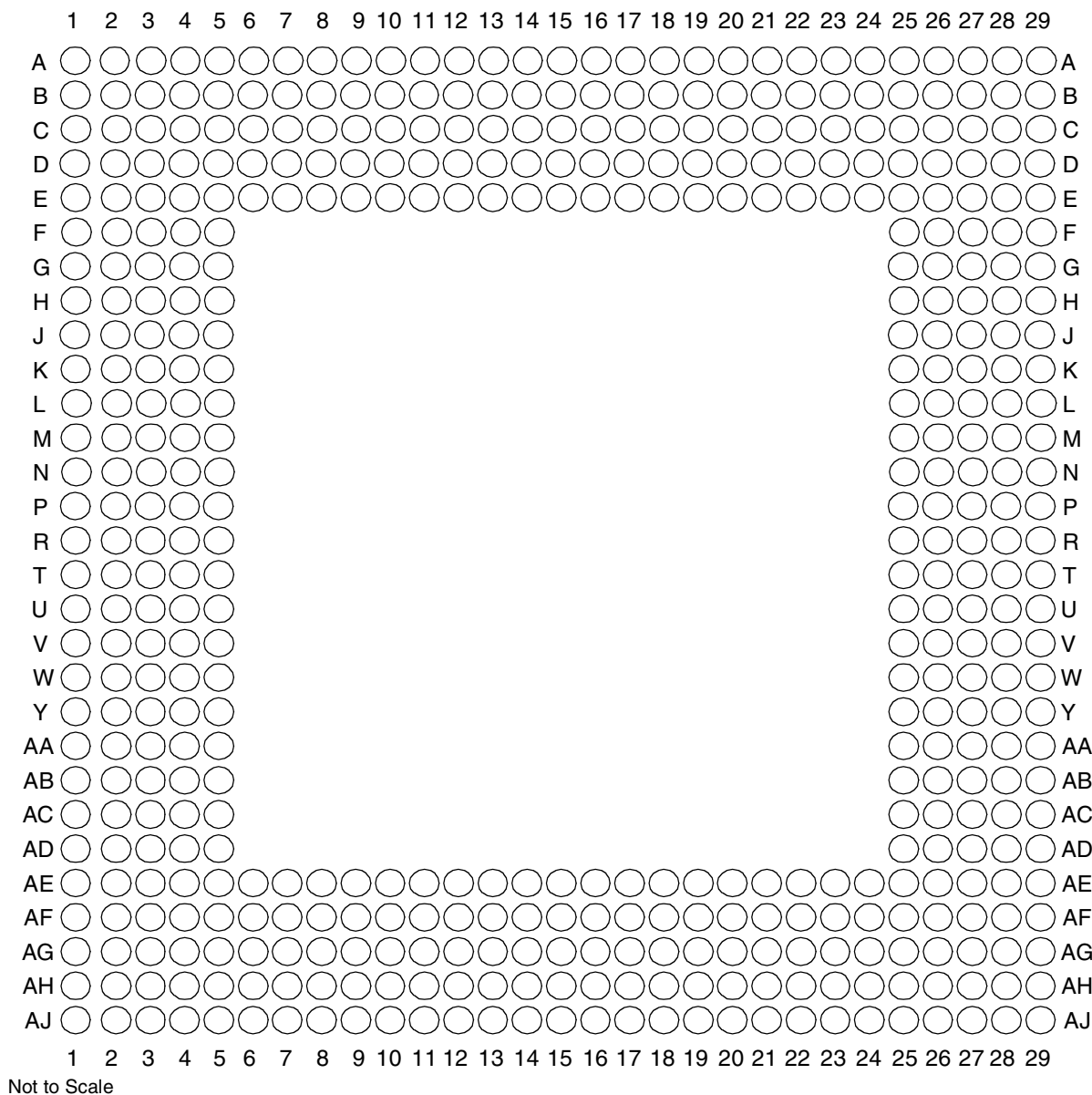


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

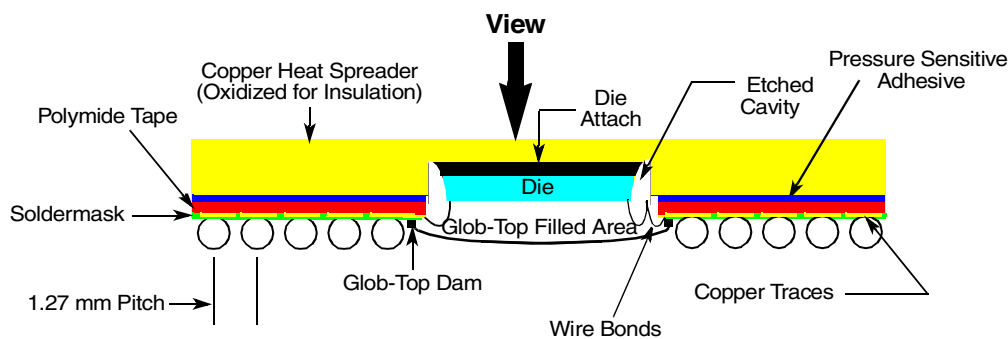


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

| Symbol | Meaning |
|---------|---|
| OVERBAR | Signals with overbars, such as \overline{TA} , are active low. |
| UTM | Indicates that a signal is part of the UTOPIA master interface. |
| UTS | Indicates that a signal is part of the UTOPIA slave interface. |
| UT8 | Indicates that a signal is part of the 8-bit UTOPIA interface. |
| UT16 | Indicates that a signal is part of the 16-bit UTOPIA interface. |
| MII | Indicates that a signal is part of the media independent interface. |

Table 21. Pinout List

| Pin Name | Ball |
|----------|------|
| BR | W5 |
| BG | F4 |
| ABB/IRQ2 | E2 |
| TS | E3 |
| A0 | G1 |
| A1 | H5 |
| A2 | H2 |
| A3 | H1 |
| A4 | J5 |
| A5 | J4 |
| A6 | J3 |
| A7 | J2 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|----------|------|
| A8 | J1 |
| A9 | K4 |
| A10 | K3 |
| A11 | K2 |
| A12 | K1 |
| A13 | L5 |
| A14 | L4 |
| A15 | L3 |
| A16 | L2 |
| A17 | L1 |
| A18 | M5 |
| A19 | N5 |
| A20 | N4 |
| A21 | N3 |
| A22 | N2 |
| A23 | N1 |
| A24 | P4 |
| A25 | P3 |
| A26 | P2 |
| A27 | P1 |
| A28 | R1 |
| A29 | R3 |
| A30 | R5 |
| A31 | R4 |
| TT0 | F1 |
| TT1 | G4 |
| TT2 | G3 |
| TT3 | G2 |
| TT4 | F2 |
| TBST | D3 |
| TSIZ0 | C1 |
| TSIZ1 | E4 |
| TSIZ2 | D2 |
| TSIZ3 | F5 |
| AACK | F3 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|----------|------|
| ARTRY | E1 |
| DBG | V1 |
| DBB/IRQ3 | V2 |
| D0 | B20 |
| D1 | A18 |
| D2 | A16 |
| D3 | A13 |
| D4 | E12 |
| D5 | D9 |
| D6 | A6 |
| D7 | B5 |
| D8 | A20 |
| D9 | E17 |
| D10 | B15 |
| D11 | B13 |
| D12 | A11 |
| D13 | E9 |
| D14 | B7 |
| D15 | B4 |
| D16 | D19 |
| D17 | D17 |
| D18 | D15 |
| D19 | C13 |
| D20 | B11 |
| D21 | A8 |
| D22 | A5 |
| D23 | C5 |
| D24 | C19 |
| D25 | C17 |
| D26 | C15 |
| D27 | D13 |
| D28 | C11 |
| D29 | B8 |
| D30 | A4 |
| D31 | E6 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|----------------------------|------|
| D32 | E18 |
| D33 | B17 |
| D34 | A15 |
| D35 | A12 |
| D36 | D11 |
| D37 | C8 |
| D38 | E7 |
| D39 | A3 |
| D40 | D18 |
| D41 | A17 |
| D42 | A14 |
| D43 | B12 |
| D44 | A10 |
| D45 | D8 |
| D46 | B6 |
| D47 | C4 |
| D48 | C18 |
| D49 | E16 |
| D50 | B14 |
| D51 | C12 |
| D52 | B10 |
| D53 | A7 |
| D54 | C6 |
| D55 | D5 |
| D56 | B18 |
| D57 | B16 |
| D58 | E14 |
| D59 | D12 |
| D60 | C10 |
| D61 | E8 |
| D62 | D6 |
| D63 | C2 |
| DP0/RSRV/EXT_BR2 | B22 |
| IRQ1/DP1/EXT_BG2 | A22 |
| IRQ2/DP2/TLBISYNC/EXT_DBG2 | E21 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|---|------|
| $\overline{\text{IRQ3}}/\text{DP3}/\overline{\text{CKSTP_OUT}}/\overline{\text{EXT_BR3}}$ | D21 |
| $\overline{\text{IRQ4}}/\text{DP4}/\overline{\text{CORE_SRESET}}/\overline{\text{EXT_BG3}}$ | C21 |
| $\overline{\text{IRQ5}}/\text{DP5}/\overline{\text{TBEN}}/\overline{\text{EXT_DBG3}}$ | B21 |
| $\overline{\text{IRQ6}}/\text{DP6}/\text{CSE0}$ | A21 |
| $\overline{\text{IRQ7}}/\text{DP7}/\text{CSE1}$ | E20 |
| PSDVAL | V3 |
| TA | C22 |
| TEA | V5 |
| GBL/IRQ1 | W1 |
| $\overline{\text{CI}}/\text{BADDR29}/\overline{\text{IRQ2}}$ | U2 |
| $\overline{\text{WT}}/\text{BADDR30}/\overline{\text{IRQ3}}$ | U3 |
| L2_HIT/IRQ4 | Y4 |
| $\overline{\text{CPU_BG}}/\text{BADDR31}/\overline{\text{IRQ5}}$ | U4 |
| CPU_DBG | R2 |
| CPU_BR | Y3 |
| CS0 | F25 |
| CS1 | C29 |
| CS2 | E27 |
| CS3 | E28 |
| CS4 | F26 |
| CS5 | F27 |
| CS6 | F28 |
| CS7 | G25 |
| CS8 | D29 |
| CS9 | E29 |
| $\overline{\text{CS10}}/\overline{\text{BCTL1}}$ | F29 |
| $\overline{\text{CS11}}/\text{AP0}$ | G28 |
| BADDR27 | T5 |
| BADDR28 | U1 |
| ALE | T2 |
| BCTL0 | A27 |
| PWE0/PSDDQM0/PBS0 | C25 |
| PWE1/PSDDQM1/PBS1 | E24 |
| PWE2/PSDDQM2/PBS2 | D24 |
| PWE3/PSDDQM3/PBS3 | C24 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|--|------|
| PWE4/PSDDQM4/PBS4 | B26 |
| PWE5/PSDDQM5/PBS5 | A26 |
| PWE6/PSDDQM6/PBS6 | B25 |
| PWE7/PSDDQM7/PBS7 | A25 |
| PSDA10/PGPL0 | E23 |
| PSDWE/PGPL1 | B24 |
| POE/PSDRAS/PGPL2 | A24 |
| PSDCAS/PGPL3 | B23 |
| PGTA/PUPMWAIT/PGPL4/PPBS | A23 |
| PSDAMUX/PGPL5 | D22 |
| LWE0/LSDDQM0/LBS0/PCI_CFG0 ¹ | H28 |
| LWE1/LSDDQM1/LBS1/PCI_CFG1 ¹ | H27 |
| LWE2/LSDDQM2/LBS2/PCI_CFG2 ¹ | H26 |
| LWE3/LSDDQM3/LBS3/PCI_CFG3 ¹ | G29 |
| LSDA10/LGPL0/PCI_MODCKH0 ¹ | D27 |
| LSDWE/LGPL1/PCI_MODCKH1 ¹ | C28 |
| LOE/LSDRAS/LGPL2/PCI_MODCKH2 ¹ | E26 |
| LSDCAS/LGPL3/PCI_MODCKH3 ¹ | D25 |
| LGTA/LUPMWAIT/LGPL4/LPBS | C26 |
| LGPL5/LSDAMUX/PCI_MODCK ¹ | B27 |
| LWR | D28 |
| L_A14/PAR ¹ | N27 |
| L_A15/FRAME ¹ /SMI | T29 |
| L_A16/TRDY ¹ | R27 |
| L_A17/IRDY ¹ /CKSTP_OUT | R26 |
| L_A18/STOP ¹ | R29 |
| L_A19/DEVSEL ¹ | R28 |
| L_A20/IDSEL ¹ | W29 |
| L_A21/PERR ¹ | P28 |
| L_A22/SERR ¹ | N26 |
| L_A23/REQ0 ¹ | AA27 |
| L_A24/REQ1 ¹ /HSEJSW ¹ | P29 |
| L_A25/GNT0 ¹ | AA26 |
| L_A26/GNT1 ¹ /HSLED ¹ | N25 |
| L_A27/GNT2 ¹ /HSENUM ¹ | AA25 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|-------------------------------------|------|
| L_A28/RST ¹ /CORE_SRESET | AB29 |
| L_A29/INTA ¹ | AB28 |
| L_A30/REQ2 ¹ | P25 |
| L_A31/DLLOUT ¹ | AB27 |
| LCL_D0/AD0 ¹ | H29 |
| LCL_D1/AD1 ¹ | J29 |
| LCL_D2/AD2 ¹ | J28 |
| LCL_D3/AD3 ¹ | J27 |
| LCL_D4/AD4 ¹ | J26 |
| LCL_D5/AD5 ¹ | J25 |
| LCL_D6/AD6 ¹ | K25 |
| LCL_D7/AD7 ¹ | L29 |
| LCL_D8/AD8 ¹ | L27 |
| LCL_D9/AD9 ¹ | L26 |
| LCL_D10/AD10 ¹ | L25 |
| LCL_D11/AD11 ¹ | M29 |
| LCL_D12/AD12 ¹ | M28 |
| LCL_D13/AD13 ¹ | M27 |
| LCL_D14/AD14 ¹ | M26 |
| LCL_D15/AD15 ¹ | N29 |
| LCL_D16/AD16 ¹ | T25 |
| LCL_D17/AD17 ¹ | U27 |
| LCL_D18/AD18 ¹ | U26 |
| LCL_D19/AD19 ¹ | U25 |
| LCL_D20/AD20 ¹ | V29 |
| LCL_D21/AD21 ¹ | V28 |
| LCL_D22/AD22 ¹ | V27 |
| LCL_D23/AD23 ¹ | V26 |
| LCL_D24/AD24 ¹ | W27 |
| LCL_D25/AD25 ¹ | W26 |
| LCL_D26/AD26 ¹ | W25 |
| LCL_D27/AD27 ¹ | Y29 |
| LCL_D28/AD28 ¹ | Y28 |
| LCL_D29/AD29 ¹ | Y25 |
| LCL_D30/AD30 ¹ | AA29 |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|---|-------------------|
| LCL_D31/AD31 ¹ | AA28 |
| LCL_DP0/C0 ¹ /BE0 ¹ | L28 |
| LCL_DP1/C1 ¹ /BE1 ¹ | N28 |
| LCL_DP2/C2 ¹ /BE2 ¹ | T28 |
| LCL_DP3/C3 ¹ /BE3 ¹ | W28 |
| IRQ0/NMI_OUT | T1 |
| IRQ7/INT_OUT/APE | D1 |
| TRST | AH3 |
| TCK | AG5 |
| TMS | AJ3 |
| TDI | AE6 |
| TDO | AF5 |
| TRIS | AB4 |
| PORESET | AG6 |
| HRESET | AH5 |
| SRESET | AF6 |
| QREQ | AA3 |
| RSTCONF | AJ4 |
| MODCK1/AP1/TC0/BNKSEL0 | W2 |
| MODCK2/AP2/TC1/BNKSEL1 | W3 |
| MODCK3/AP3/TC2/BNKSEL2 | W4 |
| XFC | AB2 |
| CLKIN1 | AH4 |
| PA0/RESTART1/DREQ3/FCC2_UTM_TXADDR2 | AC29 ² |
| PA1/REJECT1/FCC2_UTM_TXADDR1/DONE3 | AC25 ² |
| PA2/CLK20/FCC2_UTM_TXADDR0/DACK3 | AE28 ² |
| PA3/CLK19/FCC2_UTM_RXADDR0/DACK4/L1RXD1A2 | AG29 ² |
| PA4/REJECT2/FCC2_UTM_RXADDR1/DONE4 | AG28 ² |
| PA5/RESTART2/DREQ4/FCC2_UTM_RXADDR2 | AG26 ² |
| PA6/L1RSYNCA1 | AE24 ² |
| PA7/SMSYN2/L1TSYNCA1/L1GN1A1 | AH25 ² |
| PA8/SMRXD2/L1RXD0A1/L1RXDA1 | AF23 ² |
| PA9/SMTXD2/L1TXD0A1 | AH23 ² |
| PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5 | AE22 ² |
| PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4 | AH22 ² |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|--|-------------------|
| PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3 | AJ21 ² |
| PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2 | AH20 ² |
| PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3 | AG19 ² |
| PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2 | AF18 ² |
| PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1 | AF17 ² |
| PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD | AE16 ² |
| PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD | AJ16 ² |
| PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1 | AG15 ² |
| PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2 | AJ13 ² |
| PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3 | AE13 ² |
| PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11 | AF12 ² |
| PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10 | AG11 ² |
| PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1 | AH9 ² |
| PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0 | AJ8 ² |
| PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER | AH7 ² |
| PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV | AF7 ² |
| PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN | AD5 ² |
| PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER | AF1 ² |
| PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ FCC1_RTS | AD3 ² |
| PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL | AB5 ² |
| PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS | AD28 ² |
| PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2 | AD26 ² |
| PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2 | AD25 ² |
| PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2 | AE26 ² |
| PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1 | AH27 ² |
| PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1 | AG24 ² |
| PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1 | AH24 ² |
| PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1 | AJ24 ² |
| PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2 | AG22 ² |
| PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2 | AH21 ² |
| PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1 | AG20 ² |
| PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1 | AF19 ² |
| PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18 | AJ18 ² |
| PB17/FCC3_MII_RX_DV/L1RQA1/CLK17 | AJ17 ² |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|--|-------------------|
| PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2 | AE14 ² |
| PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2 | AF13 ² |
| PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1 | AG12 ² |
| PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GN2D2/ L1TXD2A1 | AH11 ² |
| PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2 | AH16 ² |
| PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2 | AE15 ² |
| PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2 | AJ9 ² |
| PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GN2C2/L1TXD3A1 | AE9 ² |
| PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2 | AJ7 ² |
| PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2 | AH6 ² |
| PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GN2B2/TXD1 | AE3 ² |
| PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/ FCC2_MII_TX_EN | AE2 ² |
| PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2 | AC5 ² |
| PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2 | AC4 ² |
| PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2 | AB26 ² |
| PC1/DREQ2/BRGO6/L1RQA2 | AD29 ² |
| PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2 | AE29 ² |
| PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4 | AE27 ² |
| PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD | AF27 ² |
| PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS | AF24 ² |
| PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR/ FCC1_UTM_RXCLAV1 | AJ26 ² |
| PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1 | AJ25 ² |
| PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3 | AF22 ² |
| PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GN2A2 | AE21 ² |
| PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3 | AF20 ² |
| PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2 | AE19 ² |
| PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1 | AE18 ² |
| PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1 | AH18 ² |
| PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0 | AH17 ² |
| PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0 | AG16 ² |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|---|-------------------|
| PC16/CLK16/TIN4 | AF15 ² |
| PC17/CLK15/TIN3/BRGO8 | AJ15 ² |
| PC18/CLK14/ $\overline{\text{TGATE2}}$ | AH14 ² |
| PC19/CLK13/BRGO7/SPICLK | AG13 ² |
| PC20/CLK12/ $\overline{\text{TGATE1}}$ | AH12 ² |
| PC21/CLK11/BRGO6 | AJ11 ² |
| PC22/CLK10/ $\overline{\text{DONE1}}$ | AG10 ² |
| PC23/CLK9/BRGO5/ $\overline{\text{DACK1}}$ | AE10 ² |
| PC24/FCC2_UT8_TXD3/CLK8/ $\overline{\text{TOUT4}}$ | AF9 ² |
| PC25/FCC2_UT8_TXD2/CLK7/BRGO4 | AE8 ² |
| PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK | AJ6 ² |
| PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3 | AG2 ² |
| PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ / $\overline{\text{CTS2}}$ /CLSN2 | AF3 ² |
| PC29/CLK3/TIN2/BRGO2/ $\overline{\text{CTS1}}$ /CLSN1 | AF2 ² |
| PC30/FCC2_UT8_TXD3/CLK2/ $\overline{\text{TOUT1}}$ | AE1 ² |
| PC31/CLK1/BRGO1 | AD1 ² |
| PD4/BRGO8/L1TSYNCD1/L1GNTD1/ $\overline{\text{FCC3_RTS}}$ /SMRXD2 | AC28 ² |
| PD5/FCC1_UT16_TXD3/ $\overline{\text{DONE1}}$ | AD27 ² |
| PD6/FCC1_UT16_TXD4/ $\overline{\text{DACK1}}$ | AF29 ² |
| PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2 | AF28 ² |
| PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5 | AG25 ² |
| PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3 | AH26 ² |
| PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4 | AJ27 ² |
| PD11/ $\overline{\text{L1RQB2}}$ /FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1 | AJ23 ² |
| PD12/SI1_L1ST2/L1RXDB1 | AG23 ² |
| PD13/SI1_L1ST1/L1TXDB1 | AJ22 ² |
| PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL | AE20 ² |
| PD15/FCC1_UT16_RXD1/ $\overline{\text{L1RQC2}}$ /I2CSDA | AJ20 ² |
| PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO | AG18 ² |
| PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI | AG17 ² |
| PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK | AF16 ² |
| PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1 | AH15 ² |
| PD20/ $\overline{\text{RTS4}}$ /TENA4/FCC1_UT16_RXD2/L1RSYNCA2 | AJ14 ² |

Table 21. Pinout List (continued)

| Pin Name | Ball |
|---|--|
| PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2 | AH13 ² |
| PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2 | AJ12 ² |
| PD23/ $\overline{\text{RTS3}}$ /TENA3/FCC1_UT16_RXD4/L1RSYNCD1 | AE12 ² |
| PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1 | AF10 ² |
| PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1 | AG9 ² |
| PD26/ $\overline{\text{RTS2}}$ /TENA2/FCC1_UT16_RXD6/L1RSYNCC1 | AH8 ² |
| PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1 | AG7 ² |
| PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1 | AE4 ² |
| PD29/ $\overline{\text{RTS1}}$ /TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4 | AG1 ² |
| PD30/ $\overline{\text{FCC2_UTM_TXENB}}$ /FCC2_UTS_TXENB/TXD1 | AD4 ² |
| PD31/RXD1 | AD2 ² |
| VCCSYN | AB3 |
| VCCSYN1 | B9 |
| GNDSYN | AB1 |
| CLKIN2 ^{1,3} | AE11 |
| SPARE4 ⁴ | U5 |
| $\overline{\text{PCI_MODE}}$ ^{1,5} | AF25 |
| SPARE6 ⁴ | V4 |
| THERMAL0 ⁶ | AA1 |
| THERMAL1 ⁶ | AG4 |
| I/O power | AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5 |
| Core Power | U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5 |
| Ground | AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3 |

¹ MPC8265 and MPC8266 only.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

Package Description

- ³ On PCI devices (MPC8265 and MPC8266) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled down or left floating.
- ⁴ Must be pulled down or left floating.
- ⁵ On PCI devices (MPC8265 and MPC8266) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled up or left floating.
- ⁶ For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

5.1 Package Parameters

Package parameters are provided in [Table 22](#). The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

Table 22. Package Parameters

| Parameter | Value |
|----------------------------------|--------------------------|
| Package Outline | 37.5 × 37.5 mm |
| Interconnects | 480 (29 × 29 ball array) |
| Pitch | 1.27 mm |
| Nominal unmounted package height | 1.55 mm |

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

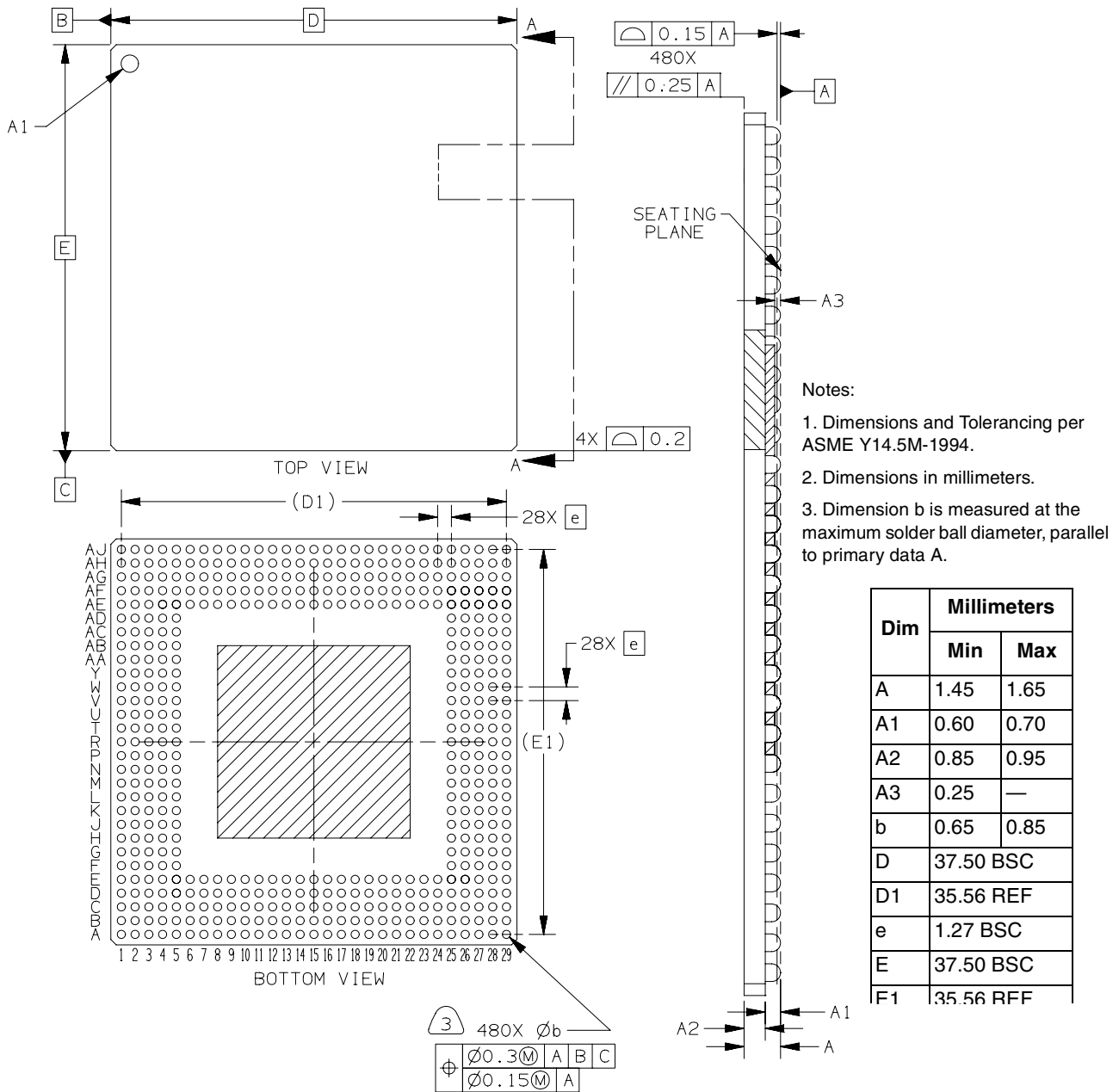


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

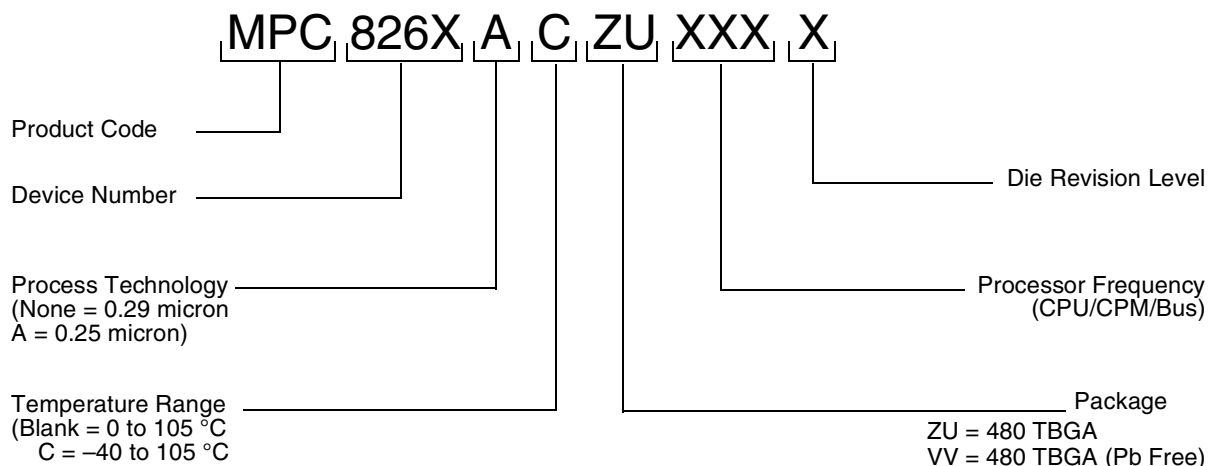


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

| Revision | Date | Substantive Changes |
|----------|---------|--|
| 2 | 06/2009 | <ul style="list-style-type: none"> Updated package values in Figure 16. |
| 1.1 | 02/2006 | <ul style="list-style-type: none"> Addition of Table 12. |
| 1.0 | 9/2005 | <ul style="list-style-type: none"> Document template update |

Table 23. Document Revision History (continued)

| Revision | Date | Substantive Changes |
|----------|---------|--|
| 0.9 | 8/2003 | <ul style="list-style-type: none"> Note: In revision 0.3, sp30 (Table 10) was changed. This change was not previously recorded in this “Document Revision History” Table. Removal of “HiP4 PowerQUICC II Documentation” table. These supplemental specifications have been replaced by revision 1 of the <i>MPC8260 PowerQUICC II™ Family Reference Manual</i>. Figure 1 and Section 1, “Features”: Addition of MPC8255 notes Addition of Figure 2 Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 Addition of note 1 to Table 3 Table 4: Changes to θ_{JA} and θ_{JB} and θ_{JC}. Addition of notes or modifications to Figure 6, Figure 7, and Figure 8 Table 9: Change of sp10. Addition of Table 15. Addition of note 2 to Table 21 Table 21: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. They are documented correctly in the parallel I/O ports chapter in the <i>MPC8260 PowerQUICC II™ Family Reference Manual</i> but had previously been omitted from Table 21. |
| 0.8 | 1/2003 | <ul style="list-style-type: none"> Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4. Table 4: Addition of θ_{JB} and θ_{JC}. Table 7, Figure 8: Addition of sp42a/sp43a. Figure 3, Figure 4: Addition of note for FCC output. Figure 5, Figure 6, Figure 7: Addition of notes. Table 14, Table 17, and Table 19: Removal of PLL bypass mode from clock tables. |
| 0.7 | 5/2002 | <ul style="list-style-type: none"> Section 1, “Features”: minimum supported core frequency of 150 MHz Section 1, “Features”: updated performance values (under “Dual-issue integer core”) Table 2: Note 2 (changes in italics): “...less than or equal to 233 MHz, 166 MHz CPM...” Table 2: Addition of note 3. |
| 0.6 | 3/2002 | <ul style="list-style-type: none"> Table 21: Modified notes to pins AE11 and AF25. |
| 0.5 | 3/2002 | <ul style="list-style-type: none"> Table 21: Modified notes to pins AE11 and AF25. Table 21: Addition of note to pins AA1 and AG4 (Therm0 and Therm1). |
| 0.4 | 2/2002 | <ul style="list-style-type: none"> Note 2 for Table 2 (changes in italics): “...greater than or equal to 266 MHz, 200 MHz CPM...” Table 19: Core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 Table 21: Notes added to pins at AE11, AF25, U5, and V4. |
| 0.3 | 11/2001 | <ul style="list-style-type: none"> Table 1: note 3 Section 2.1: Removal of “Warning” recommending use of bootstrap diodes. They are not needed. Table 9: Change to sp12. Table 10: Change to sp32. Note 2 for Table 16 and Table 17 Addition of note at beginning of Section 3.2 Note 1 for Table 18 and Table 19 Table 21: Additions to B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27 |
| 0.2 | 11/2001 | <ul style="list-style-type: none"> Revision of Table 5, “Power Dissipation” Modifications to Figure 9, Table 2, Table 10, Table 11, and Table 18 Modification to pinout diagram, Figure 13 Additional revisions to text and figures throughout |
| 0.1 | 8/2001 | <ul style="list-style-type: none"> Table 8: Change to sp20/sp21. |
| 0 | — | Initial version |

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