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Kind regards,

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74LVT04

3.3 V Hex inverter

Rev. 2 — 28 April 2014 Product data sheet

1. General description

The 74LVT04 is a high-performance product designed for V_{CC} operation at 3.3 V.

The 74LVT04 provides six inverting buffers.

2. Features and benefits

- TTL input and output switching levels
- Latch-up protection
  - JESD78 class II exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT04D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT04DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT04PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

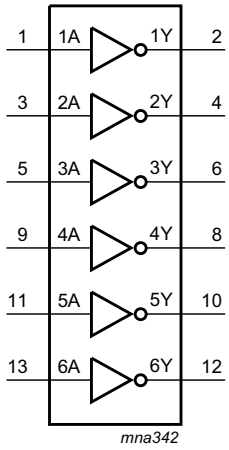


Fig 1. Logic symbol

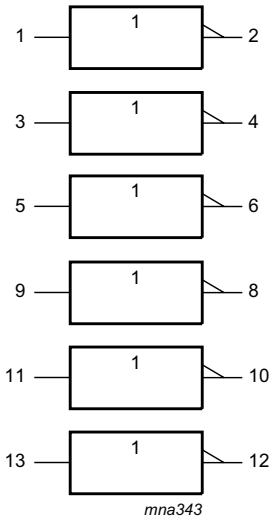


Fig 2. IEC logic symbol

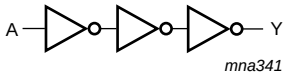


Fig 3. Logic diagram for one gate

5. Pinning information

5.1 Pinning

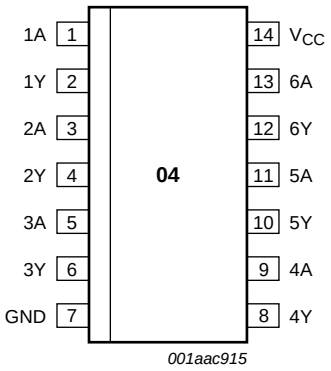


Fig 4. Pin configuration SOT108-1 (SO14), SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 3, 5, 9, 11, 13	data input
nY	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input	Output
nA	**nY**
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
V_I	input voltage	[1]	–0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	–50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	–50	-	mA
I_O	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-	–32	mA
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C [3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
I_{OH}	HIGH-level output current		-	–20	mA
I_{OL}	LOW-level output current		-	32	mA
T_{amb}	ambient temperature	in free air	–40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IK}	input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA	-	-	–1.2	V
V_{OH}	LOW-level input voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA	V_{CC} – 0.2	-	-	V
		V_{CC} = 2.7 V; I_{OH} = –6 mA	2.4	-	-	V
		V_{CC} = 3.0 V; I_{OH} = –20 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = –100 µA	-	-	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	-	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA	-	-	0.5	V
I_I	input leakage current	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	-	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	-	±1	µA
I_{OFF}	output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	-	±100	µA
I_{CCH}	quiescent supply current	V_{CC} = 3.6 V; outputs HIGH; V_I = GND or V_{CC}, I_O = 0 V	-	-	0.02	mA
I_{CCL}	quiescent supply current	V_{CC} = 3.6 V; outputs LOW; V_I = GND or V_{CC}; I_O = 0 V	-	1.5	3	mA
ΔI_{CC}	additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND	-	-	0.2	µA
C_I	input capacitance	V_I = 3 V or 0 V	-	3	-	pF

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

[2] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

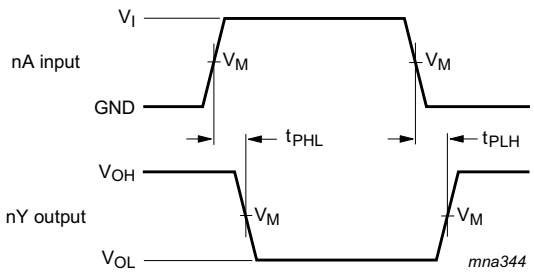
Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 6.

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{PLH}	LOW to OFF-state propagation delay	nA to nY; see Figure 5				
		V_{CC} = 2.7 V	-	-	4.7	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.6	3.9	ns
t_{PHL}	OFF-state to LOW propagation delay	nA to nY; see Figure 5				ns
		V_{CC} = 2.7 V	-	-	3.2	
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.5	3.5	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

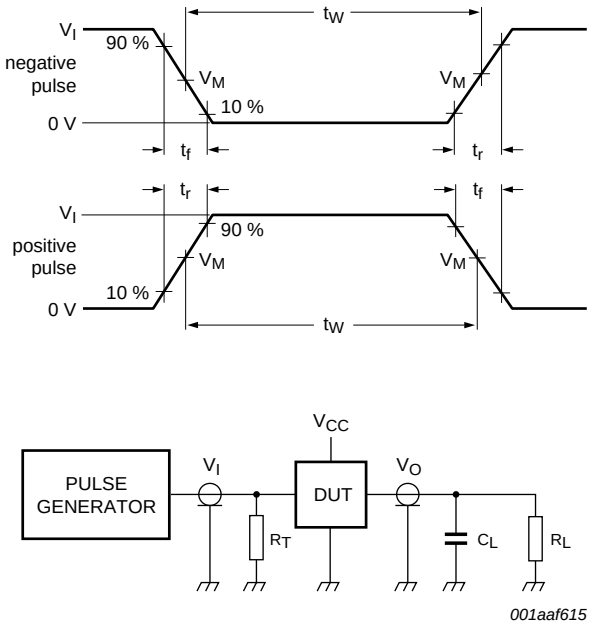
11. Waveforms



V_M = 50%; V_I = GND to V_{CC}.

V_M = 1.5 V; V_I = GND to 2.7 V

Fig 5. The input nA to output nY propagation delays



Test data is given in Table 8.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

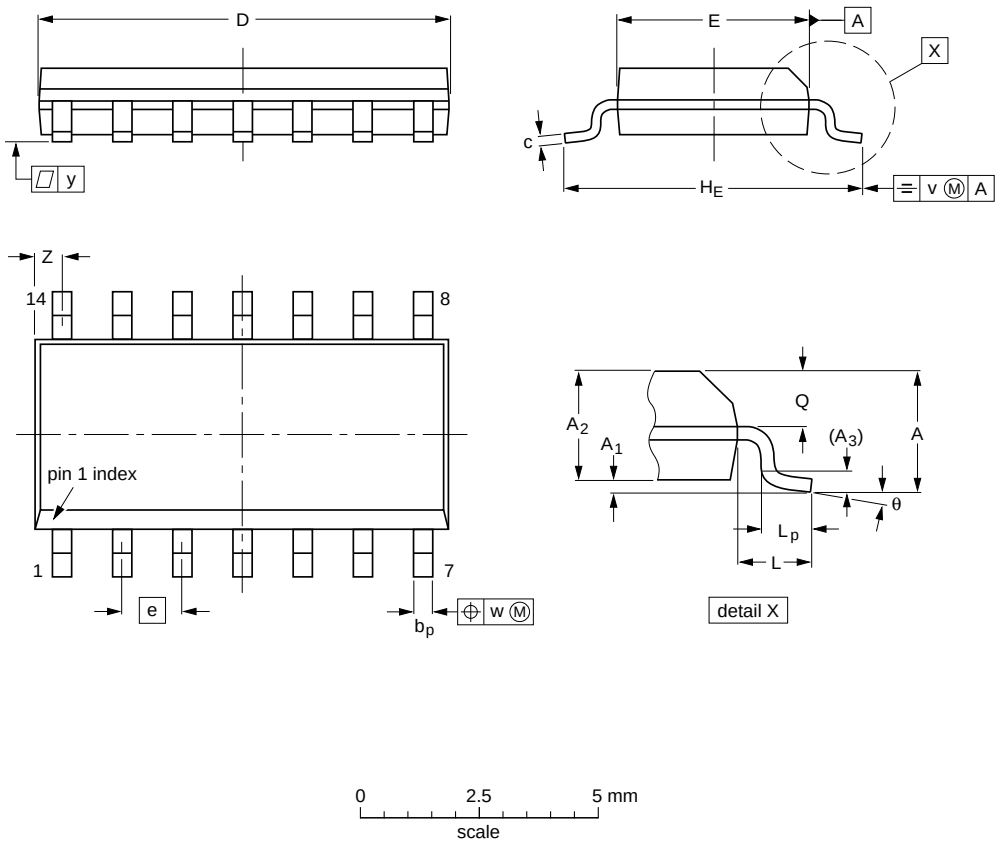
Fig 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load	
V_I	f_i	t_W	t_r, t_f	C_L	R_L
2.7 V	≤ 10 MHz	500 ns	≤2.5 ns	50 pF	500 Ω

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

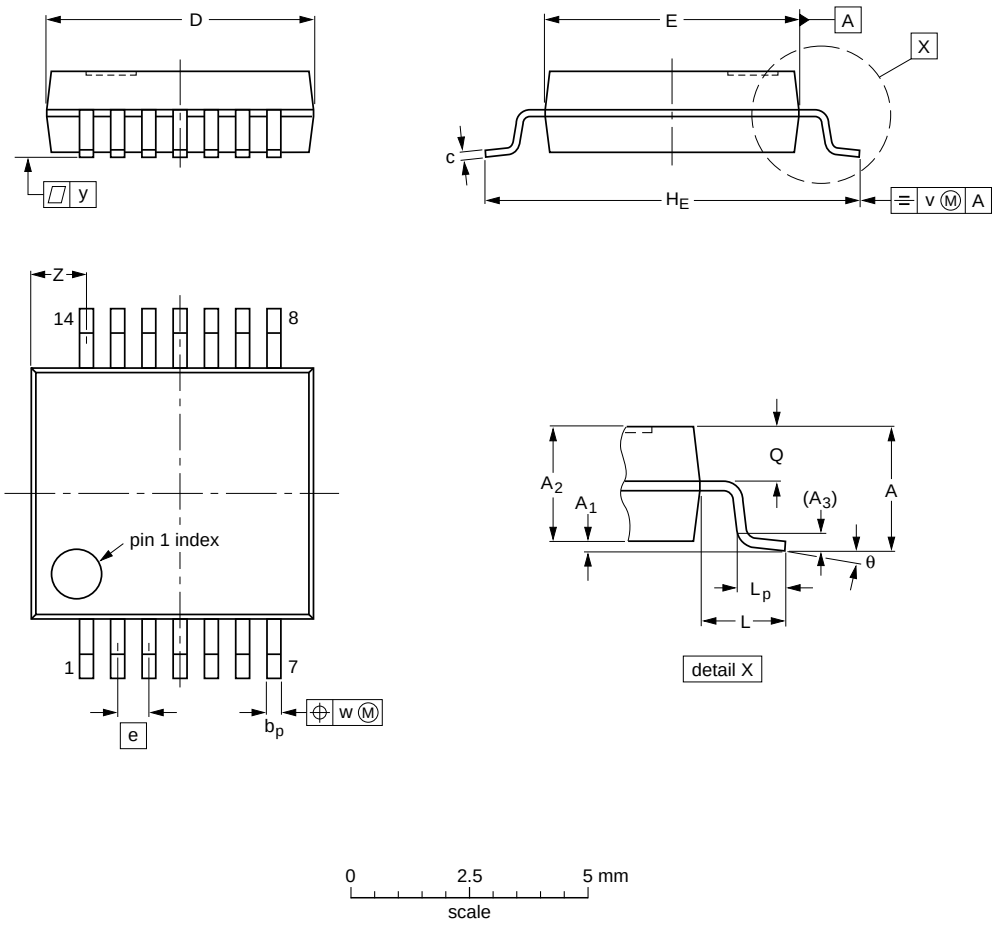
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

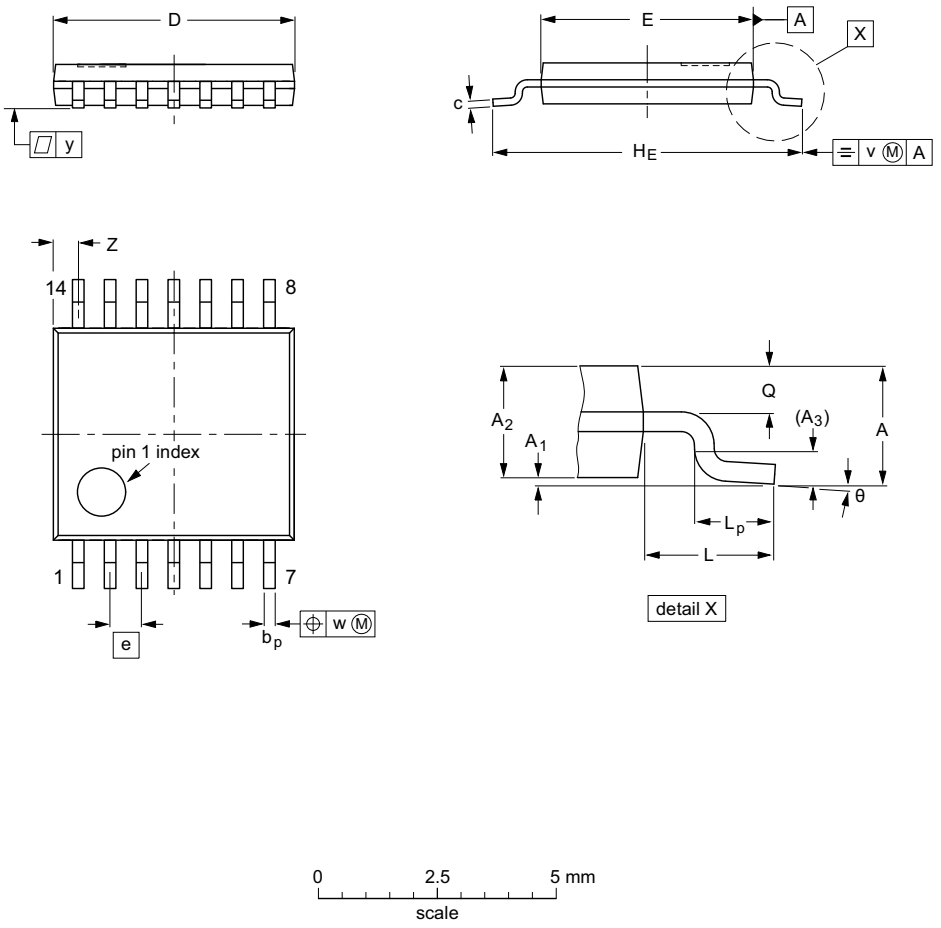
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT04 v.2	20140428	Product data sheet	-	74LVT04_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Imported the data sheet into the latest template			
74LVT04_1	19960828	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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