LTC3112

15V, 2.5A Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with V_{IN} Above, Below or Equal to V_{OUT}**
- **2.7V to 15V Input Voltage Range**
- **2.5V to 14V Output Voltage Range**
- **2.5A Continuous Output Current: $V_{IN} \geq 5V$, $V_{OUT} = 5V$, PWM Mode**
- **Output Current Monitor**
- Up to 95% Efficiency
- 750kHz Switching Frequency, Synchronizable Between 300kHz and 1.5MHz
- Internal N-Channel MOSFETs
- Selectable Burst Mode® Operation, $I_Q = 50\mu A$
- Shutdown Current < 1µA
- Overvoltage Protection
- Output Disconnect in Shutdown
- Internal Soft-Start
- Small, Thermally Enhanced 16-Lead (4mm × 5mm × 0.75mm) DFN and 20-Lead TSSOP Package

APPLICATIONS

- 3.3V or 5V from 1, 2 or 3 Li-Ion, Backup Capacitor Stack
- Hand Held Inventory Terminals
- RF Transmitters
- 12V Synchronous Boost Converter
- Multiple Power Input Systems
- LED Lighting with Current Regulation
- 12V Lead Acid Battery to 12V

DESCRIPTION

The LTC®3112 is a fixed frequency synchronous buck-boost DC/DC converter with an extended input and output range. The unique 4-switch, single inductor architecture provides low noise and seamless operation from input voltages above, below or equal to the output voltage.

With an input range of 2.7V to 15V, the LTC3112 is well-suited for a wide variety of single or multiple cell battery, backup capacitor or wall adapter source applications. Low $R_{DS(ON)}$ internal N-Channel MOSFET switches provide highly efficient operation in applications with higher load current requirements.

The LTC3112 features selectable PWM or Burst Mode operation, an easily synchronized oscillator and output disconnect in shutdown. An output current monitor circuit allows the load current to be controlled or measured. Other features include <1µA shutdown current, short circuit protection, soft-start, current limit and thermal shutdown.

The LTC3112 is offered in both a 16-pin (4mm × 5mm × 0.75mm) DFN and 20-pin TSSOP packages.

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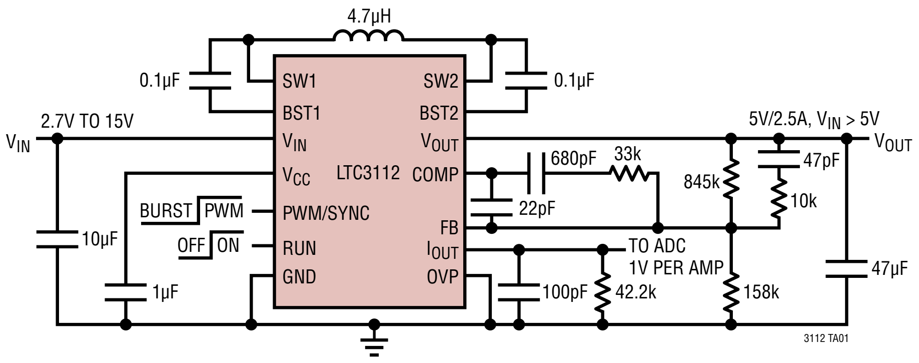
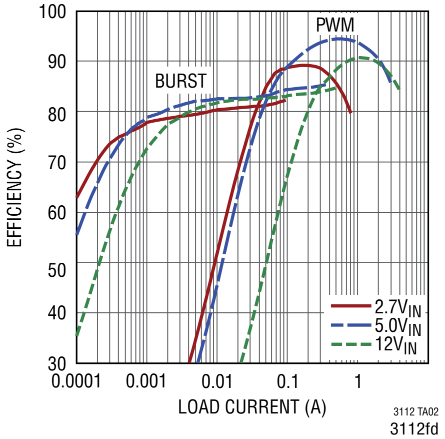
TYPICAL APPLICATION

5V, 750kHz Wide Input Voltage Range Buck-Boost Regulator



Efficiency at $5V_{OUT}$



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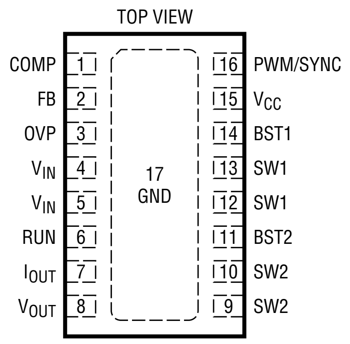
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

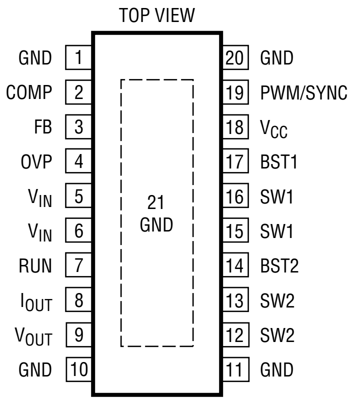
V_{IN} Voltage .... –0.3V to 16V
V_{OUT} Voltage .... –0.3V to 15V
SW1 Voltage (Note 4) .... –0.3V to (V_{IN} + 0.3V)
SW2 Voltage (Note 4) .... –0.3V to (V_{OUT} + 0.3V)
V_{BST1} Voltage.................. (V_{SW1} – 0.3V) to (V_{SW1} + 6V)
V_{BST2} Voltage.................. (V_{SW2} – 0.3V) to (V_{SW2} + 6V)
RUN Voltage... –0.3V to 16V
PWM/SYNC, V_{CC}, I_{OUT} Voltage .... –0.3V to 6V
FB, COMP, OVP Voltage .... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 6)
.... –55°C to 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10sec) TSSOP .... 300°C

PIN CONFIGURATION


TOP VIEW
COMP 1
FB 2
OVP 3
V_IN 4
V_IN 5
RUN 6
I_OUT 7
V_OUT 8
17 GND
16 PWM/SYNC
15 V_CC
14 BST1
13 SW1
12 SW1
11 BST2
10 SW2
9 SW2

DHD16 PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN

T_{JMAX}=150 °C, θ_{JA} = 43°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB


TOP VIEW
GND 1
COMP 2
FB 3
OVP 4
V_IN 5
V_IN 6
RUN 7
I_OUT 8
V_OUT 9
GND 10
21 GND
20 GND
19 PWM/SYNC
18 V_CC
17 BST1
16 SW1
15 SW1
14 BST2
13 SW2
12 SW2
11 GND

FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC3112#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3112EDHD#PBF	LTC3112EDHD#TRPBF	3112	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3112IDHD#PBF	LTC3112IDHD#TRPBF	3112	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3112HDHD#PBF	LTC3112HDHD#TRPBF	3112	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 150°C
LTC3112MPDHD#PBF	LTC3112MPDHD#TRPBF	3112	16-Lead (5mm × 4mm) Plastic DFN	–55°C to 150°C
LTC3112EFE#PBF	LTC3112EFE#TRPBF	3112FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3112IFE#PBF	LTC3112IFE#TRPBF	3112FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3112HFE#PBF	LTC3112HFE#TRPBF	3112FE	20-Lead Plastic TSSOP	–40°C to 150°C
LTC3112MPFE#PBF	LTC3112MPFE#TRPBF	3112FE	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = PWM/SYNC = RUN = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Range	0°C to 150°C –55°C to 0°C		2.7 2.85		15 15	V V
V_{IN} UVLO Threshold	Rising		1.75	2.3	2.7	V
V_{IN} UVLO Hysteresis				300		mV
V_{CC} UVLO Threshold	Rising	●	2.2	2.35	2.5	V
V_{CC} UVLO Hysteresis				150		mV
Output Voltage Adjust Range		●	2.5		14	V
$INTV_{CC}$ Clamp Voltage	V_{IN} = 5V or 15V	●	3.8	4.2	4.6	V
V_{CC} Voltage in Dropout	V_{IN} = 2.7V, I_{VCC} = 10mA			2.6		V
Quiescent Current – Burst Mode Operation	V_{FB} = 1V, $V_{PWM/SYNC}$ = 0V			50	75	µA
Quiescent Current – Shutdown	RUN = V_{OUT} = V_{CC} = 0V, Not Including Switch Leakage			0	1	µA
Feedback Voltage = PWM Mode Operation		●	0.778	0.8	0.818	V
Feedback Leakage	V_{FB} = 0.8V			0	50	nA
OVP Threshold	Rising Threshold		0.78	0.83	0.88	V
OVP Hysteresis	Measured at OVP Pin			20		mV
OVP Leakage	OVP = 0.8V			0	100	nA
NMOS Switch Leakage	Switch A, B, C, D, V_{IN} = V_{OUT} = 12V			1	10	µA
NMOS Switch On Resistance	Switch A			40		mΩ
NMOS Switch On Resistance	Switch B, C			50		mΩ
NMOS Switch On Resistance	Switch D			60		mΩ
Input Current Limit	L = 4.7µH	●	4.5	6	8.5	A
Peak Current Limit	L = 4.7µH		7	10	12	A
Burst Current Limit	L = 4.7µH		0.7	1.3	2	A
Burst Zero Current Threshold	L = 4.7µH			0.3		A
Reverse Current Limit	L = 4.7µH		–0.5	–1	–1.5	A
I_{OUT} Accuracy (Note 5)	SW2 to V_{OUT} Current = 1.5A SW2 to V_{OUT} Current = 1.0A SW2 to V_{OUT} Current = 0.5A		32 20 8	36 24 12	40 28 16	µA µA µA
Maximum Duty Cycle	Buck (Switch A On)	●	80	87		%
	Boost (Switch C On)	●	75	82		%
Minimum Duty Cycle	Buck (Switch A On)	●			0	%
	Boost (Switch C On)	●	5	12		%
Frequency	PWM/SYNC = 5V, V_{IN} = V_{OUT} = 12V	●	675	750	825	kHz
SYNC Frequency Range (Note 7)		●	300		1500	kHz
PWM/SYNC Threshold	V_{CC} = 2.7V or 5V	●	0.5	0.9	1.5	V
RUN Threshold	V_{IN} = 2.7V or 15V	●	0.35	0.75	1.5	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3112 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3112E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3112I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature, the LTC3112H is guaranteed to meet specifications over the –40°C to 150°C operating junction temperature range and the LTC3112MP is guaranteed and tested to meet specifications over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for temperature greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

ELECTRICAL CHARACTERISTICS

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Voltage transients on the switch pins beyond the DC limit specified in the Absolute Maximum Ratings, are non disruptive to normal operation when using good layout practices, as shown on the demo board or described in the data sheet and application notes.

Note 5: I_{OUT} current is tested in a non-switching DC state. In a switching environment I_{OUT} accuracy may exhibit variation with factors such as switching frequency, load current, input/output voltage, and temperature. See typical performance characteristic curves for predicted variation.

Note 6: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

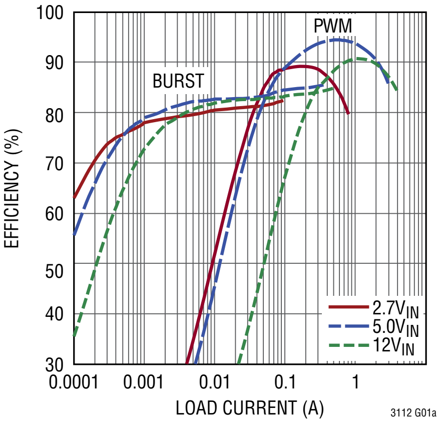
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 7: SYNC frequency range is tested with a square wave. Operation with 100ns minimum high or low times is assured by design.

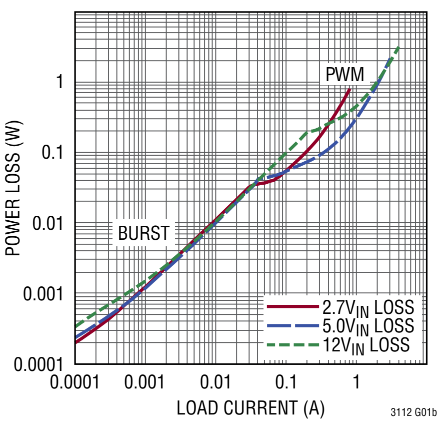
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{IN} = 5.0V$, $V_{OUT} = 5.0V$ unless otherwise specified

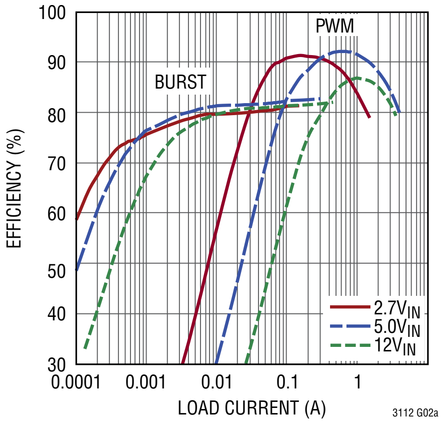
Wide V_{IN} to $5V_{OUT}$ Efficiency



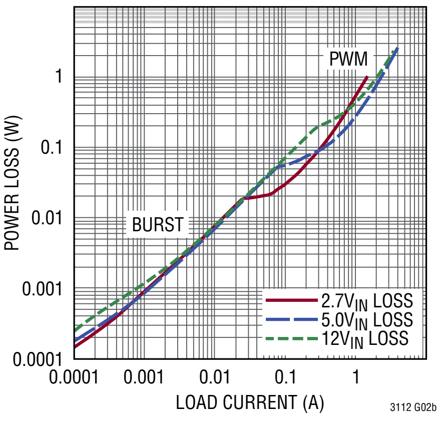
Wide V_{IN} to $5V_{OUT}$ Power Loss



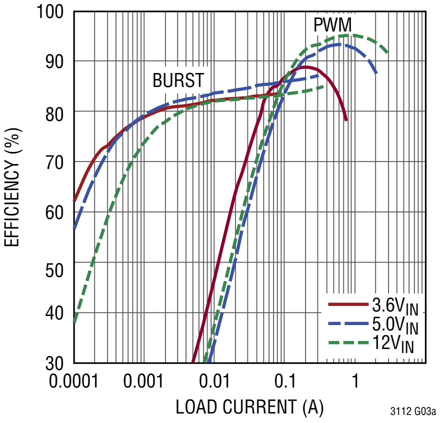
Wide V_{IN} to $3.3V_{OUT}$ Efficiency



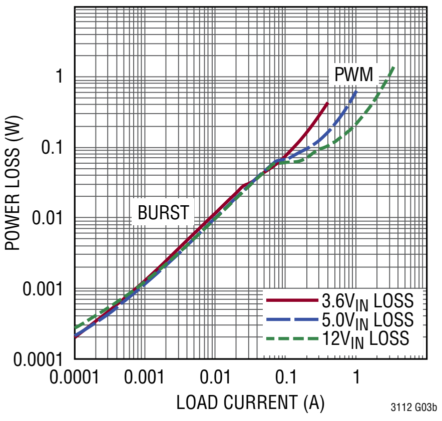
Wide V_{IN} to $3.3V_{OUT}$ Power Loss



Wide V_{IN} to $12V_{OUT}$ Efficiency



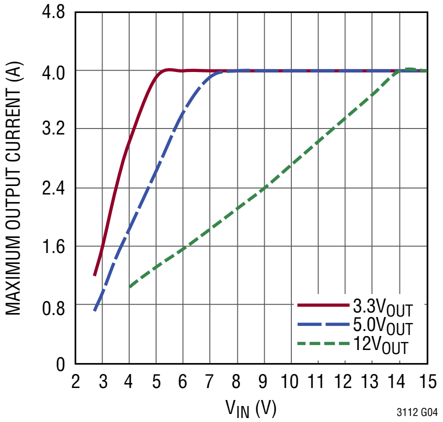
Wide V_{IN} to $12V_{OUT}$ Power Loss



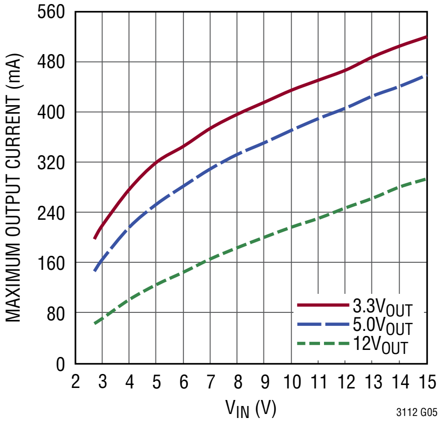
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5.0V, V_{OUT} = 5.0V unless otherwise specified

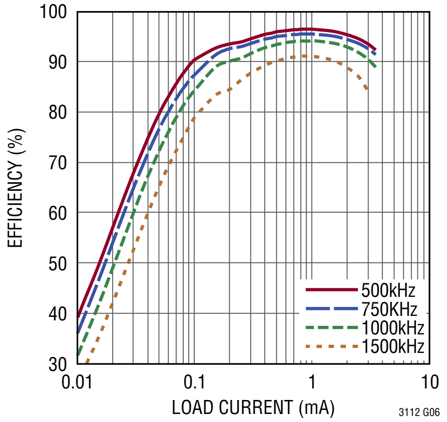
Maximum Output Current PWM Mode



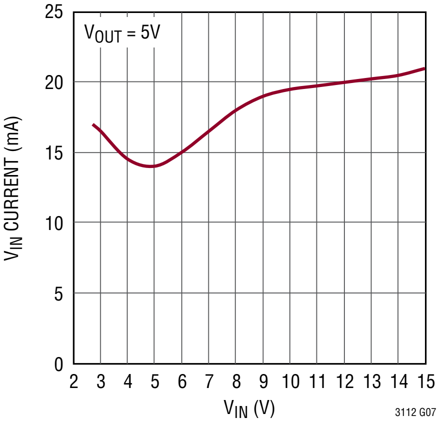
Maximum Output Current Burst Mode Operation



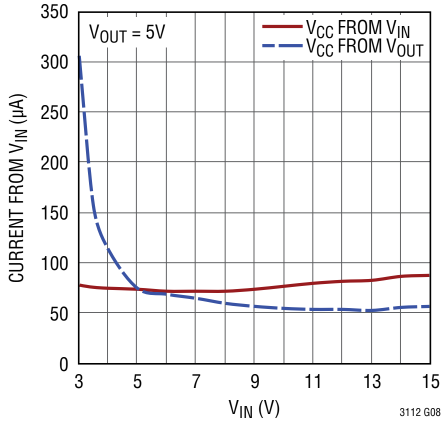
$12V_{IN}$ to $12V_{OUT}$ Efficiency vs Frequency with 4.7µH



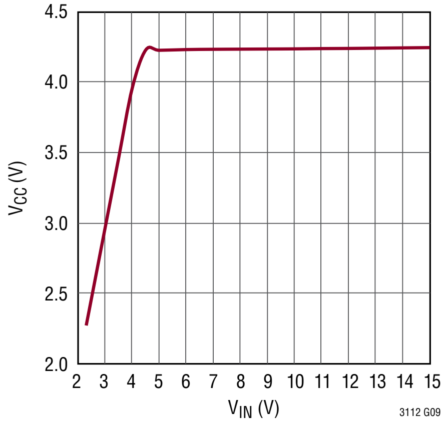
750kHz PWM Mode No-Load Input Current



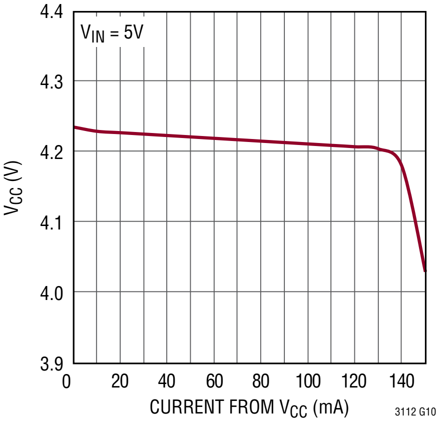
Burst Mode No-Load Input Current with V_{CC} from V_{IN} or Back-Fed from V_{OUT} with Optional Diode



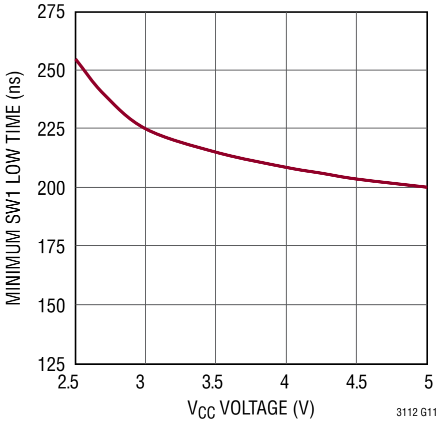
V_{CC} Voltage vs V_{IN} PWM Mode No Load



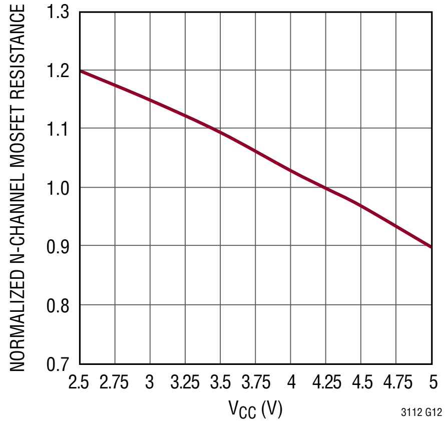
V_{CC} Voltage vs V_{CC} Current



Boost Mode Minimum SW1 Low Time vs V_{CC} Voltage

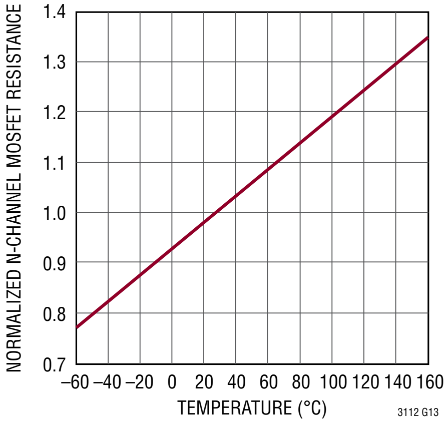


Normalized N-Channel MOSFET Resistance vs V_{CC}

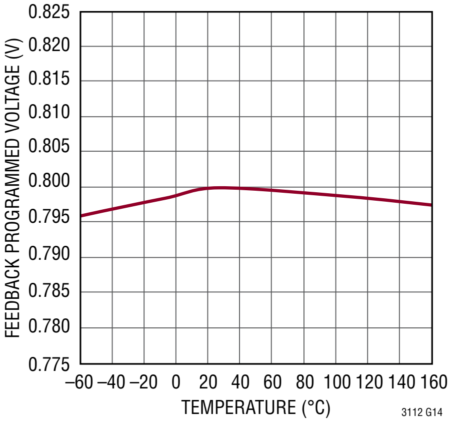


TYPICAL PERFORMANCE CHARACTERISTICS

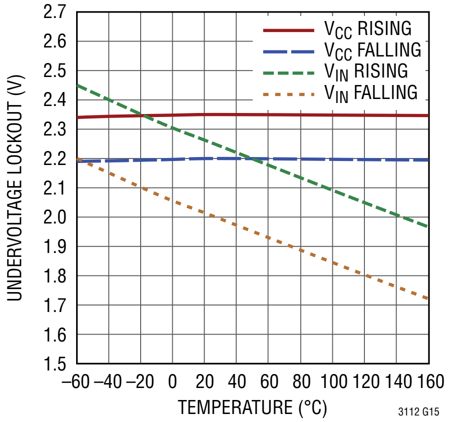
T_A = 25°C, V_{IN} = 5.0V, V_{OUT} = 5.0V unless otherwise specified



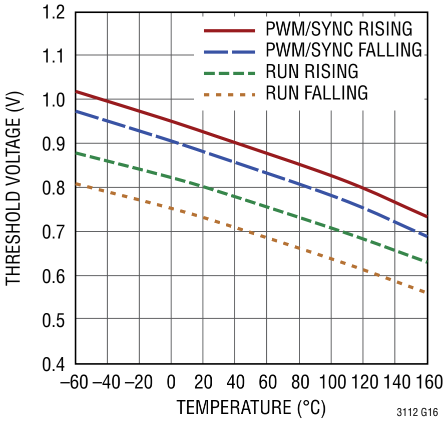
Normalized N-Channel MOSFET Resistance vs Temperature



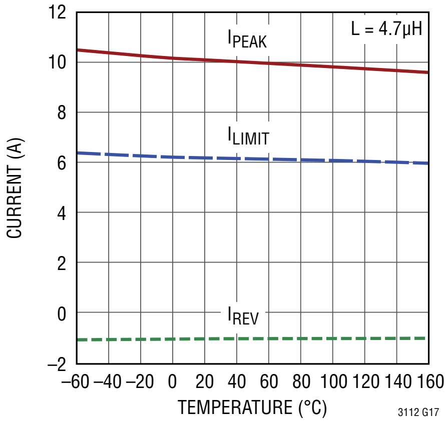
Feedback Pin Program Voltage vs Temperature



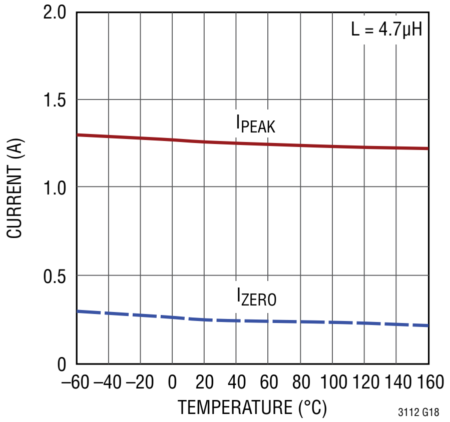
V_{CC} and V_{IN} UVLO vs Temperature



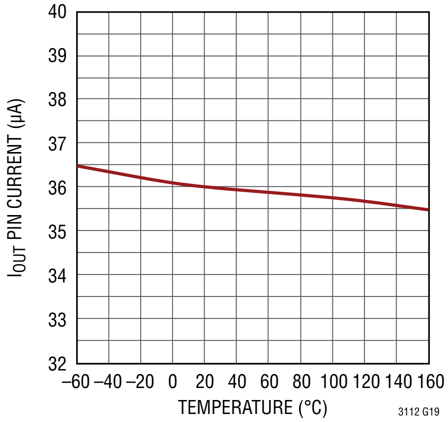
RUN and PWM/SYNC Threshold Voltage vs Temperature



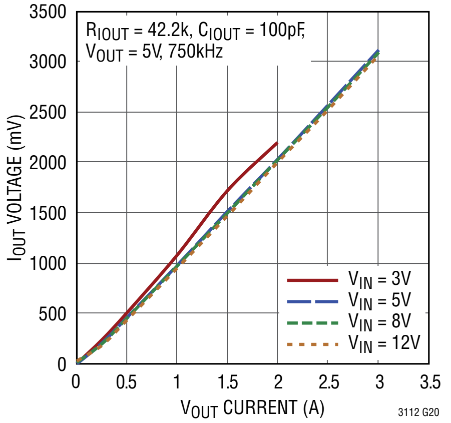
PWM Mode I_{LIMIT}, I_{PEAK}, I_{REV} vs Temperature



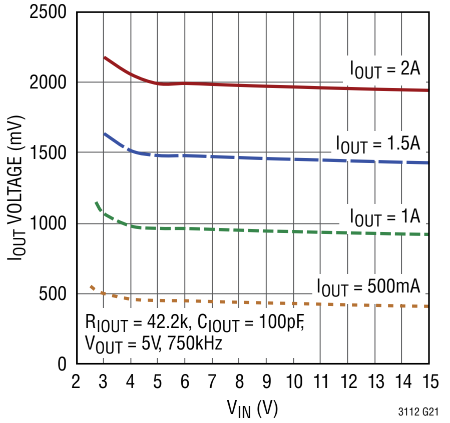
Burst Mode Operation I_{PEAK}, I_{ZERO} vs Temperature



I_{OUT} Pin Current vs Temperature 1.5A Load Current



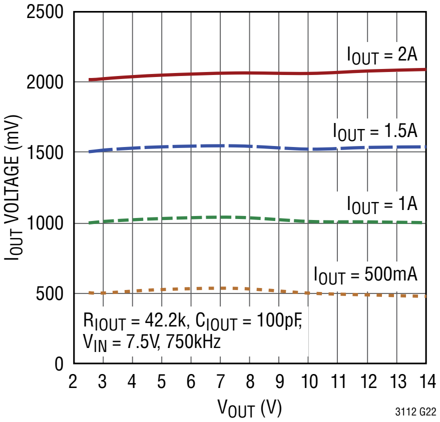
I_{OUT} Voltage vs V_{OUT} Current

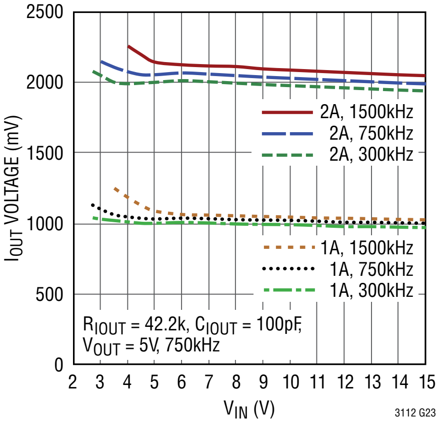


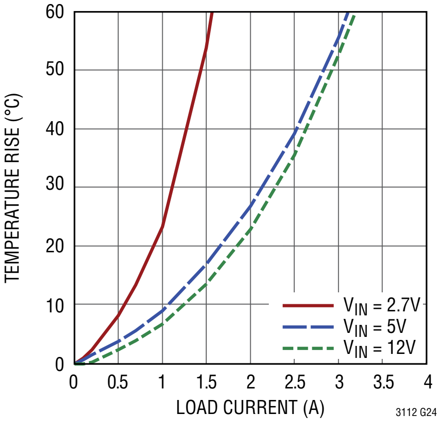
I_{OUT} Voltage vs V_{IN}

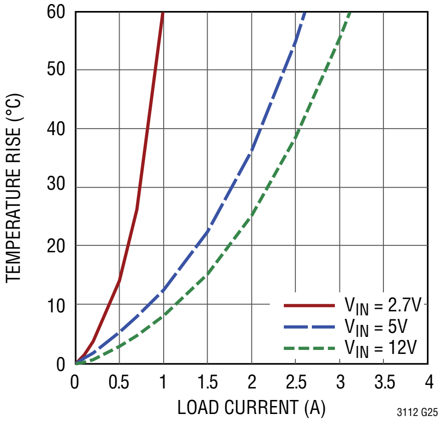
TYPICAL PERFORMANCE CHARACTERISTICS

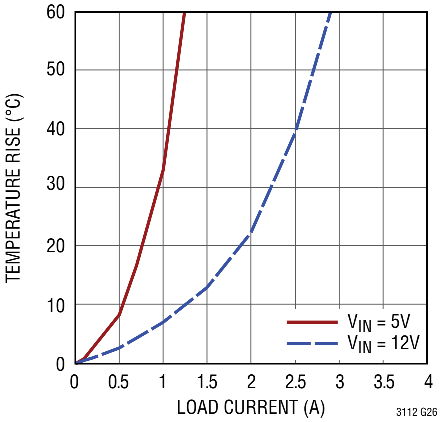
T_A = 25°C, V_{IN} = 5.0V, V_{OUT} = 5.0V unless otherwise specified

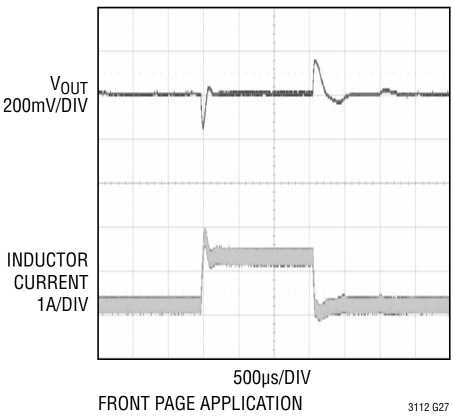

I_{OUT} Voltage vs V_{OUT}

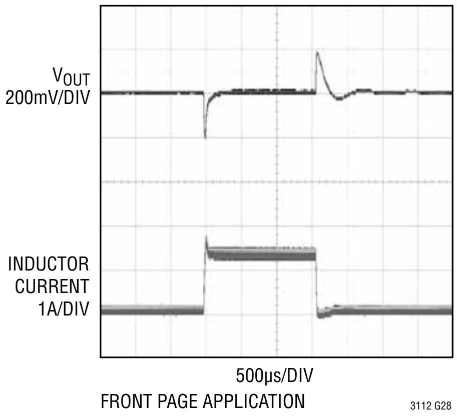

I_{OUT} Voltage vs V_{IN} and Switching Frequency

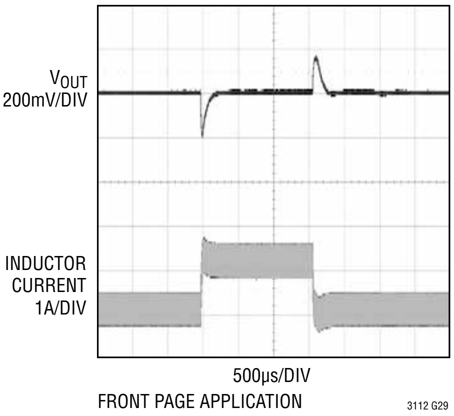

$3.3V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4 Layer Demo Board at 25°C

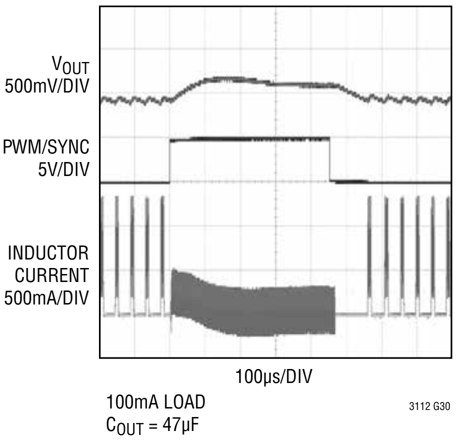

$5V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4 Layer Demo Board at 25°C


$12V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4 Layer Demo Board at 25°C


$3V_{IN}$ to $5V_{OUT}$ 0.1A to 0.6A Load Step


$5V_{IN}$ to $5V_{OUT}$ 0.1A to 1.0A Load Step

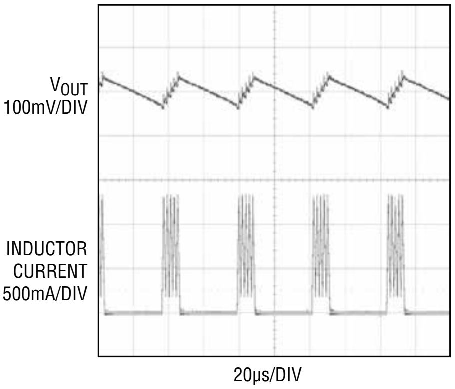

$12V_{IN}$ to $5V_{OUT}$ 0.1A to 1.0A Load Step


$5V_{IN}$ to $5.0V_{OUT}$ Burst to PWM Waveforms,

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5.0V, V_{OUT} = 5.0V unless otherwise specified

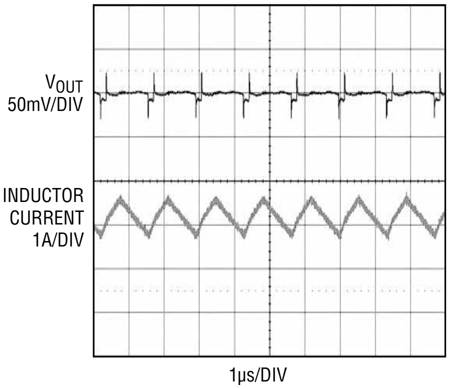
12V_{IN} to 5V_{OUT} Burst Mode Operation Waveforms



100mA LOAD
C_{OUT} = 47µF

3112 G31

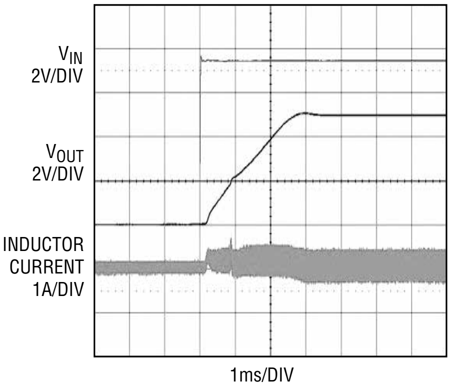
PWM V_{OUT} Ripple



12.0V_{IN} TO 5.0V_{OUT}
1A LOAD C_{OUT} = 47µF

3112 G32

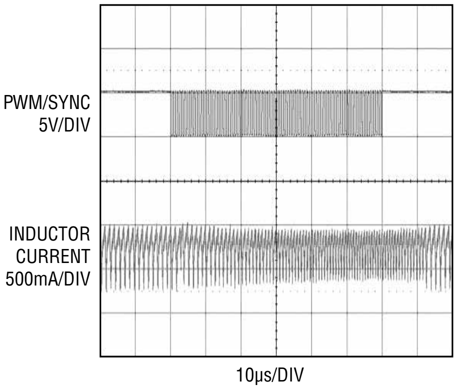
7.5V_{IN} to 5.0V_{OUT} Soft-Start Waveforms



I_L 1A/DIV

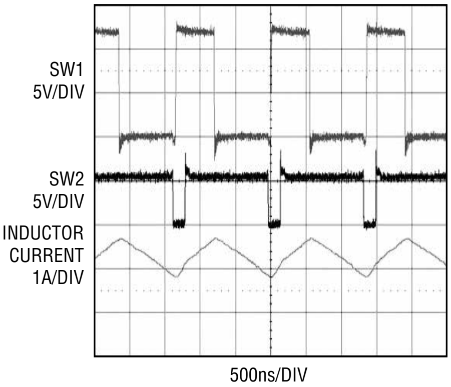
3112 G33

1500kHz SYNC Signal Capture and Release



3112 G34

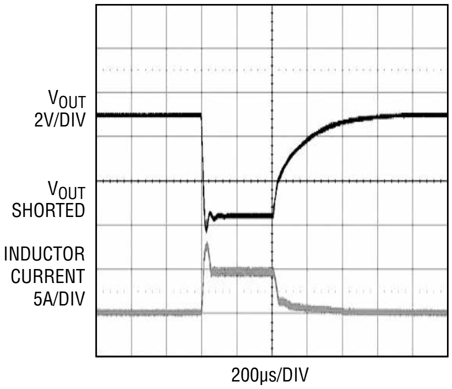
12V_{IN} to 5.0V_{OUT} SW1 and SW2 Waveforms



I_{LOAD} = 2A
750kHz

3112 G36

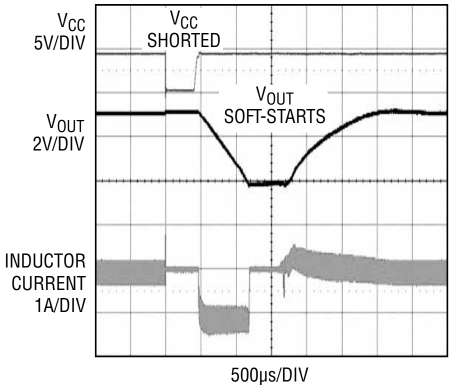
V_{OUT} Short Circuit Response



V_{IN} = 5V

3112 G37

V_{CC} Short Circuit Recovery



3112 G38

PIN FUNCTIONS (DFN/TSSOP)

COMP (Pin 1/Pin 2): Error Amp Output. An R-C network connected from this pin to FB sets the loop compensation for the voltage converter.

FB (Pin 2/Pin 3): Feedback Voltage Input. Connect V_{OUT} resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 14V by the following equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

where R1 is the resistor between V_{OUT} and FB and R2 is the resistor between FB and GND.

OVP (Pin 3/Pin 4): Overvoltage Protection Input. The common point of a resistor divider between V_{OUT} and GND can also be used to program the overvoltage protection to a lower voltage by the following equation:

$$V_{OVP} = 0.83V \bullet \left(1 + \frac{R3}{R4}\right)$$

where R3 is the resistor between V_{OUT} and OVP and R4 is the resistor between OVP and GND.

V_{IN} (Pins 4, 5/Pins 5, 6): Input Supply Voltage. This pin should be bypassed to the ground plane with at least 10µF of low ESR, low ESL ceramic capacitance. Place this capacitor as close to the pin as possible and have as short a return path to the ground plane as possible.

RUN (Pin 6/Pin 7): Shutdown Control Input. Operation will be disabled when the voltage is forced below 0.75V (typical) and less than 1µA of quiescent current will be consumed.

I_{OUT} (Pin 7/Pin 8): A Current approximately 24µA/A of the D Switch Output Current is Sourced from this Pin. An R-C circuit can be used to control the average output current or provide an analog output current monitor (see Applications Information section).

V_{OUT} (Pin 8/Pin 9): Regulated Output Voltage. This pin should be connected to a low ESR ceramic capacitor of at least 47µF. The capacitor should be placed as close to the pin as possible and have a short return to the ground plane.

SW2 (Pins 9, 10/Pins 12, 13): Internal switches C and D and the external inductor are connected here.

BST2 (Pin 11/Pin 14): Boosted Floating Driver Supply for D-Switch Driver. Connect a 0.1µF capacitor from this pin to SW2.

SW1 (Pins 12, 13/Pins 15, 16): Internal switches A and B and the external inductor are connected here.

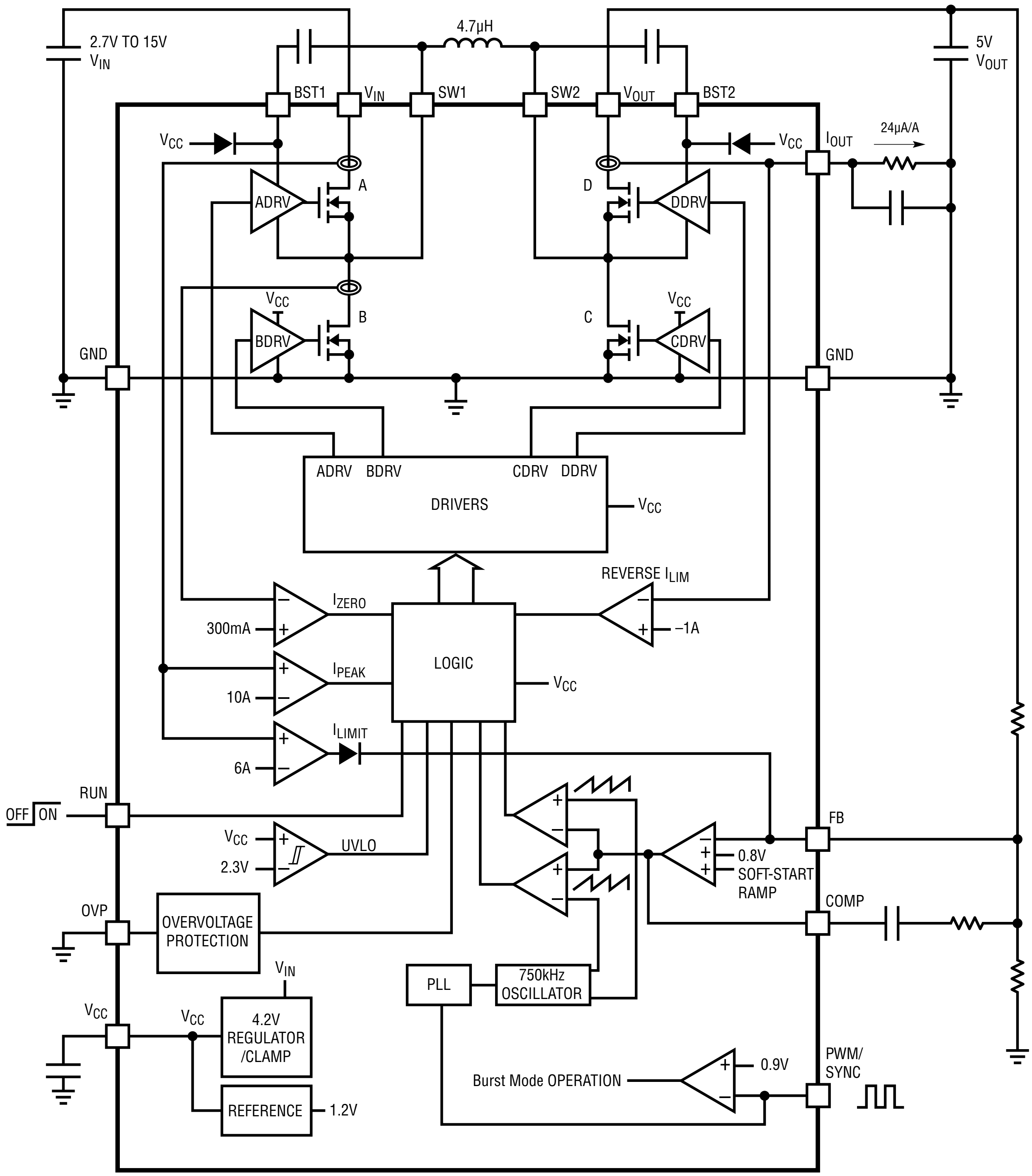
BST1 (Pin 14/Pin 17): Boosted Floating Driver Supply for A-Switch Driver. Connect a 0.1µF capacitor from this pin to SW1.

V_{CC} (Pin 15/Pin 18): External Capacitor Connection for the Regulated V_{CC} Supply. This supply is used to operate internal circuitry and switch drivers. V_{CC} will track V_{IN} up to 4.2V, but will maintain this voltage when V_{IN} > 4.2V. Connect a 1µF ceramic capacitor from this pin to GND.

PWM/SYNC (Pin 16/Pin 19): Burst Mode Control and Synchronization Input. A DC voltage <0.5V commands Burst Mode operation, >1.5V commands 750kHz fixed frequency mode. A digital pulse train between 300kHz and 1500kHz applied to this pin will override the internal oscillator and set the operating frequency. The pulse train should have minimum high or low times greater than 100ns (Note 7). Note the LTC3112 has reduced power capability when operating in Burst Mode operation. Refer to the Operation section of this data sheet for details.

GND (Exposed Pad Pin 17/Pins 1, 10, 11, 20, Exposed Pad Pin 21): Ground. Small-Signal and Power Ground for the IC. The exposed pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible. The bulk of the heat flow is through this pad, so printed circuit board design has an impact on the thermal performance of the IC. See PCB Layout and Thermal Considerations sections for more details.

BLOCK DIAGRAM


2.7V TO 15V
V_{IN}
4.7µH
5V
V_{OUT}
BST1
V_{IN}
SW1
SW2
V_{OUT}
BST2
V_{CC}
V_{CC}
I_{OUT}
24µA/A
A
D
ADRV
DDRV
V_{CC}
V_{CC}
B
C
BDRV
CDRV
GND
GND
ADRV
BDRV
CDRV
DDRV
DRIVERS
V_{CC}
REVERSE I_{LIM}
I_{ZERO}
300mA
−1A
LOGIC
I_{PEAK}
10A
V_{CC}
I_{LIMIT}
6A
RUN
OFF
ON
FB
V_{CC}
2.3V
UVLO
0.8V
SOFT-START
RAMP
OVP
OVERVOLTAGE
PROTECTION
COMP
V_{IN}
PLL
750kHz
OSCILLATOR
V_{CC}
V_{CC}
4.2V
REGULATOR
/CLAMP
PWM/
SYNC
0.9V
Burst Mode OPERATION
REFERENCE
1.2V

OPERATION

INTRODUCTION

The LTC3112 is an extended input and output range, high current synchronous buck-boost DC/DC converter optimized for a variety of demanding applications. The LTC3112 utilizes a proprietary switching algorithm, which allows its output voltage to be regulated above, below or equal to the input voltage. The error amplifier output on COMP determines the output duty cycle of the switches. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high efficiency pulse width modulation control. High efficiency is achieved at light loads when Burst Mode operation is commanded.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator, Phase-Locked Loop

An internal oscillator circuit sets the normal frequency of operation to 750kHz. A pulse train applied to the PWM/SYNC pin allows the operating frequency to be programmed between 300kHz to 1.5MHz via an internal phase-locked loop circuit. The pulse train must have a minimum high or low state of at least 100ns to guarantee operation (Note 7).

Error Amplifier

The error amplifier is a high gain voltage mode amplifier. The loop compensation components are configured around the amplifier (from FB to COMP and V_{OUT} to FB) to obtain stability of the converter and rapid response to load transients. Refer to the Applications Information section of this data sheet under Closing the Feedback Loop for information on selecting compensation type and components.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which sources current into the feedback divider network proportional to the extent that switch A current exceeds 6A typical. Due to the high gain of the feedback loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in current limit will have a dependency on the duty cycle (i.e. on the input and output voltages) in the overcurrent condition. For this current limit feature to be most effective, the Thevenin resistance from the FB to ground should exceed 100kΩ.

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it would be possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A if the current ever exceeds approximately 160% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Should the output become shorted, the average current limit is reduced to approximately one half of the normal operating current limit.

Reverse Current Limit

During fixed frequency operation, a reverse current comparator on switch D monitors the current entering the V_{OUT} pin. When this reverse current exceeds 1A (typical) switch D will be turned off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is above the regulation voltage.

Internal Soft-Start

The LTC3112 buck-boost converter has an independent internal soft-start circuit with a nominal duration of 2ms. The converter remains in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current during start-up.

OPERATION

THERMAL CONSIDERATIONS

For the LTC3112 to provide maximum output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct the heat away from the IC and into a copper plane with as much area as possible.

The efficiency and maximum output current capability of the LTC3112 will be reduced if the converter is required to continuously deliver large amounts of power or operate at high ambient temperatures. The amount of output current derating is dependent upon factors such as board ground plane or heat sink area, ambient operating temperature, and the input/output voltages of the application. A poor thermal design can cause excessive heating, resulting in impaired performance or reliability.

The temperature rise curves given in the Typical Performance Characteristics section can be used as a general guide to predict junction temperature rise from ambient. These curves were generated by mounting the LTC3112 to the 4-layer FR4 Demo Board printed circuit board layout shown in Figure 3. The curves were taken with the board at room temperature, elevated ambient temperatures will result in greater thermal rise rates due to increased initial $R_{DS(ON)}$ of the N-Channel MOSFETs. The die temperature of the LTC3112 should be kept below the maximum junction rating of 150°C.

In the event that the junction temperature gets too high (approximately 150ºC), the current limit will be linearly decreased from its typical value. If the junction temperature continues to rise and exceeds approximately 170°C the LTC3112 will be disabled. All power devices are turned off and all switch nodes put to a high impedance state. The soft-start circuit for the converter is reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. When the die temperature drops to approximately 160°C the LTC3112 will re-start.

UNDERVOLTAGE LOCKOUTS

The LTC3112 buck-boost converter is disabled and all power devices are turned off until the V_{CC} supply reaches 2.35V (typical). The soft-start circuit is reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold. A second UVLO circuit disables all power devices if V_{IN} is below 2.3V rising, 2.0V falling (typical). This can provide a lower V_{IN} operating range in applications where V_{CC} is powered from an alternate source or V_{OUT} after start-up.

INDUCTOR DAMPING

When the LTC3112 is disabled (RUN = 0V) or sleeping during Burst Mode operation (PWM/SYNC = 0V), active circuits "damp" the inductor voltage through a 250Ω (typical) impedance from SW1 and SW2 to GND to minimize ringing and reduce EMI.

PWM MODE OPERATION

When the PWM/SYNC pin is held high, the LTC3112 buck-boost converter operates in a fixed frequency pulse width modulation (PWM) mode using voltage mode control. Full output current capability is only available in PWM mode. A proprietary switching algorithm allows the converter to transition between buck, buck-boost, and boost modes without discontinuity in inductor current. The switch topology for the buck-boost converter is shown in Figure 1.

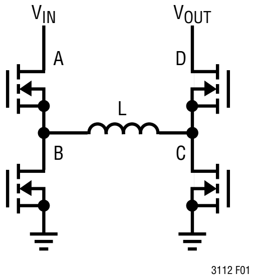


Figure 1. Buck-Boost Switch Topology

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on at maximum duty cycle and switch C turns on just long enough to refresh the voltage on the BST2 capacitor used to drive switch D. Switches A and B

OPERATION

are pulse width modulated to produce the required duty cycle to support the output regulation voltage.

As the input voltage nears the output voltage, switches A and D are on for a greater portion of the switching period, providing a direct current path from V_{IN} to V_{OUT}. Switches B and C are turned on only enough to ensure proper regulation and/or provide charging of the BST1 and BST2 capacitors. The internal control circuitry will determine the proper duty cycle in all modes of operation, which will vary with load current.

As the input voltage drops well below the output voltage, the converter operates solely in boost mode. Switch A turns on at maximum duty cycle and switch B turns on just long enough to refresh the voltage on the BST1 capacitor used to drive A. Switches C and D are pulse width modulated to produce the required duty cycle to regulate the output voltage.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout the operational modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

Powering V_{CC} from an External Source

The LTC3112's V_{CC} regulator can be powered or back-fed from an external source up to 5.5V. Advantages of back-feeding V_{CC} from a voltage above 4.2V include higher efficiency and improved maximum duty cycle at lower input voltages. These advantages are shown in the Typical Performance Characteristics curves "MOSFET Resistance vs V_{CC}" and "Minimum SW1 Low Times." For $5V_{OUT}$ applications, V_{CC} can be easily powered from V_{OUT} using an external low current Schottky diode as shown in several applications circuits in the Typical Applications section.

Back-feeding V_{CC} also improves a light load PWM mode output voltage ripple that occurs when the inductor passes through zero current. Back-feeding V_{CC} reduces the switch pin anti-cross conduction times, minimizing the V_{OUT} ripple during this light-load condition. One disadvantage of powering V_{CC} from V_{OUT} is that no-load quiescent current increases at low V_{IN} in Burst Mode operation as shown in the Typical Performance Characteristics curves (compared to V_{CC} powered from V_{IN}).

Considerations for Boost Applications

In boost mode, the maximum output current that can be supported at higher V_{OUT}/V_{IN} ratios is reduced. This effect is illustrated in the Maximum Output Current PWM Mode curves in the Typical Performance Characteristics section. For example at $12V_{OUT}$, the LTC3112 needs $V_{IN} >$ 4V to support 1A. As described previously, powering V_{CC} from a 5V source (if available) can improve output current capabilities at low input voltages.

At even lower input voltages (below 3.6V for $12V_{OUT}$), the LTC3112 can run into duty cycle limitations. This occurs since SW1 and SW2 maximum duty cycles are multiplied, giving an approximate 70% maximum duty cycle at the nominal 750kHz switching frequency. Reducing the switching frequency with the PWM/SYNC pin will increase the maximum duty cycle, allowing a higher boost ratio to be achieved. Do not attempt operating the LTC3112 beyond the duty cycle limitations described as this may result in unstable operation.

Burst Mode OPERATION

When the PWM/SYNC pin is held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses and as a result only a fraction of the maximum output current can be delivered when in Burst Mode operation.

These current pulses are repeated as often as necessary to maintain the output regulation voltage. The maximum output current, I_{MAX}, which can be supplied in Burst Mode operation is dependent upon the input and output voltage as approximated by the following formula:

$$I_{MAX} = \frac{0.5 \cdot V_{IN}}{V_{IN} + V_{OUT}} \text{ (A)}$$

If the buck-boost load exceeds the maximum Burst Mode current capability, the output rail will lose regulation. In

OPERATION

Burst Mode operation, the error amplifier is configured for low power operation and used to hold the compensation pin COMP, to reduce transients that may occur during transitions from and to burst and PWM mode.

OUTPUT CURRENT MONITOR

The LTC3112 includes a circuit that sources an approximate 24µA/A current replica of the V_{OUT} (or SWD) current. This current is typically passed through a resistor from I_{OUT} to GND and filtered to produce a DC voltage proportional to average load current. This voltage can be monitored by an A/D converter to track load conditions. The I_{OUT} pin voltage can also control LTC3112's feedback loop to regulate I_{OUT} current instead of V_{OUT} voltage. The accuracy of the I_{OUT} replica depends on factors such as duty cycle, V_{IN} and V_{OUT} voltages, operating frequency etc. The I_{OUT} pin's DC voltage must be less than V_{CC} - 1V to provide an accurate representation of output current.

APPLICATIONS INFORMATION

The basic LTC3112 application circuit is shown on the front page of this data sheet. The external component selection is dependent upon the required performance of the IC in each particular application given trade-offs such as PCB area, output voltages, output currents, ripple voltages and efficiency. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

V_{OUT} AND OVP PROGRAMMING

The buck-boost output voltage is set with an external resistor divider connected to the FB pin as shown in Figure 2.

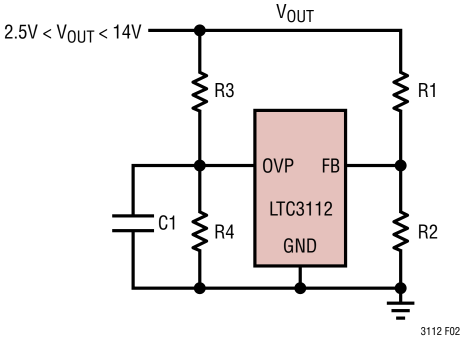


Figure 2. Setting the Output Voltage

The resistor divider values determine the buck-boost output voltage according to the following formula:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

If accurate overvoltage protection is required, a second resistor divider (R3 and R4) may be connected to the OVP pin to program the overvoltage protection threshold where the LTC3112 will stop switching.

$$V_{OVP} = 0.83V \bullet \left(1 + \frac{R3}{R4}\right)$$

A small capacitor, C1, in parallel with R4 may be needed to provide filtering to prevent nuisance trips during a load step. A soft-start cycle will be initiated if an overvoltage event occurs.

INDUCTOR SELECTION

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. In addition, the buck-boost inductor must have a saturation current rating that is greater than the worst case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple for buck or boost mode operation can be calculated from the following formulas:

$$\Delta I_{L,P-P,BUCK} = \frac{V_{OUT}}{f \bullet L}\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) A$$

$$\Delta I_{L,P-P,BOOST} = \frac{V_{IN}}{f \bullet L}\left(\frac{V_{OUT} - V_{IN}}{V_{OUT}}\right) A$$

APPLICATIONS INFORMATION

Where f is the switching frequency in Hz and L is the inductor value in Henries.

In addition to affecting output current ripple, the size of the inductor can also impact the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than 15µH if the converter is to be used in the boost region. For 750kHz operation, a 4.7µH inductor is recommended for 5V_{OUT} and a 10µH inductor for 12V_{OUT}.

The inductor DC resistance can impact the efficiency of the buck-boost converter as well as the maximum output current capability at low input voltage. In buck mode, the output current is limited only by the inductor current reaching the current limit value. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance, and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the graph in the Typical Performance Characteristics section of this data sheet.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3112 buck-boost converter applications. All inductor specifications are listed at an inductance value of 4.7µH for comparison purposes but other values within these inductor families are generally well suited to this application. Within each family (i.e. at a fixed size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Table 1. Representative Buck-Boost Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX I (A)	SIZE (mm) W × L × H
Coilcraft XPL7030-472ML	4.7	40.1	6.8	7 × 7 × 3
Coilcraft MSS1048-472NLB	4.7	12.3	6.46	10 × 10 × 4.8
Würth 744 311 470	4.7	24	6	7 × 6.9 × 3.8
Cooper Bussmann HC8-4R5-R	4.5	18.6	7.7	10.9 × 10.4 × 4

OUTPUT CAPACITOR SELECTION

A low-ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels. The minimum output capacitor needed for a given output voltage ripple (neglecting ESR and ESL) can be calculated by the following formulas:

$$C_{OUT} = \frac{1}{\Delta V_{P-P,\,BUCK}\, 8 \bullet L \bullet f^2} \bullet \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}}$$

$$C_{OUT} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{\Delta V_{P-P,\,BOOST}\; V_{OUT} \bullet f}$$

where f is the frequency in MHz, C_{OUT} is the capacitance in µF, L is the inductance in µH, and I_{LOAD} is the output current in Amps.

Given that the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. For most applications a 47µF or greater output capacitor is recommended.

INPUT CAPACITOR SELECTION

It is recommended that a low ESR ceramic capacitor with a value of at least 10µF be located as close to the V_{IN} and GND pins as possible. In addition, the return trace from each pin to the ground plane should be made as short as possible. For instances where the input source, such as a bench supply, is far away from the converter, a bulk capacitor of 100µF or greater is suggested to provide a low ripple input voltage especially in buck mode.

APPLICATIONS INFORMATION

CAPACITOR VENDOR INFORMATION

Both the input bypass capacitors and output capacitors used with the LTC3112 must be low ESR and designed to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce ripple on both the input and output. Many modern low voltage ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose 50% or more of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating then required in order to actually realize the intended capacitance at the full operating voltage. For details, consult the capacitor vendor's curve of capacitance versus DC bias voltage.

The capacitors listed in Table 2 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3112 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss overtemperature is minimized.

Table 2. Representative Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE (mm) L × W × H
AVX LD103D226MAB2A	22	25	3.2 × 2.5 × 2.79
Kemet C1210C476M4PAC7025	47	16	3.2 × 2.5 × 2.5
Murata GRM32ER61E226KE15L	22	25	3.6 × 2.5 × 2.5
Taiyo Yuden EMK325BJ476MM-T	47	16	3.2 × 2.5 × 2.5
TDK C5750X5RIC476M	47	16	5.7 × 5 × 2.3

PCB LAYOUT CONSIDERATIONS

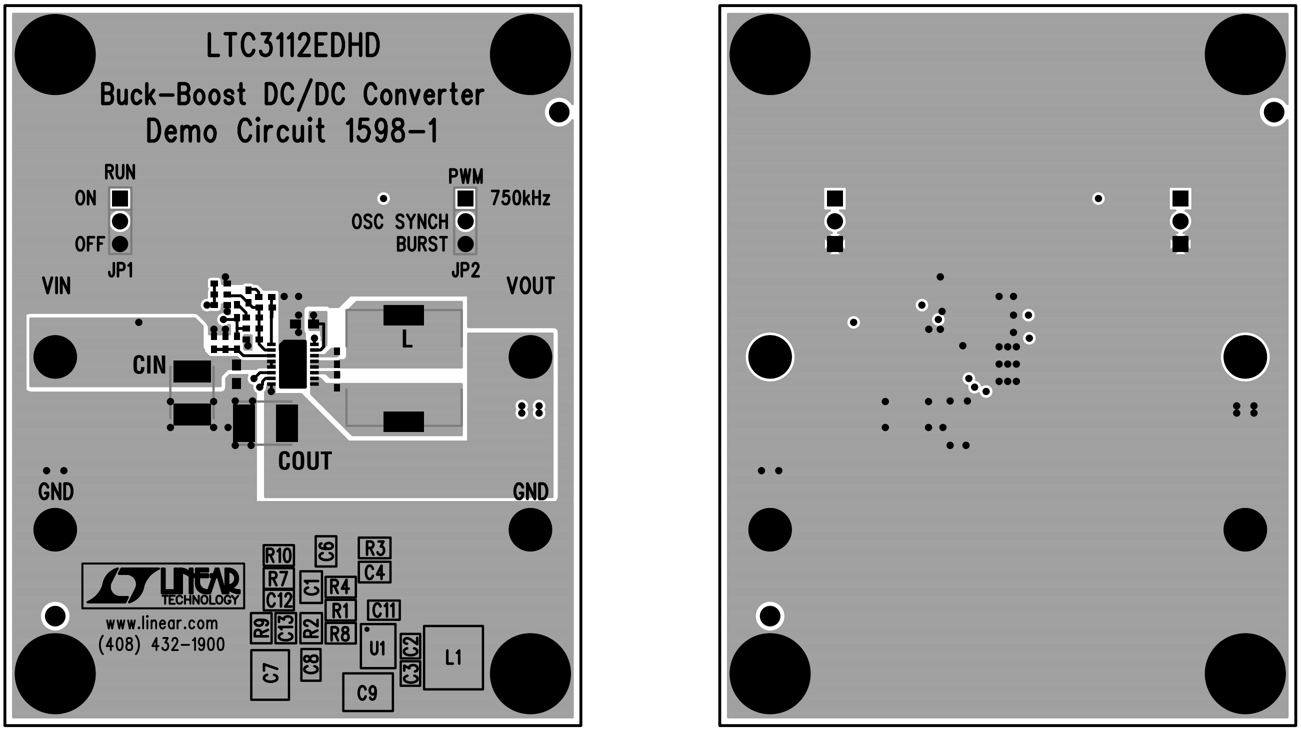
The LTC3112 switches large currents at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit. Figure 3 presents a representative 4-layer PCB layout to outline some of the primary considerations. A few key guidelines are outlined below:

1. A 4-layer board is highly recommended for the LTC3112 to ensure stable performance over the full operating voltage and current range. A dedicated/solid ground plane should be placed directly under the V_{IN}, V_{OUT}, SW1 and SW2 traces to provide a mirror plane to minimize noise loops from high dI/dt and dV/dt edges (see Figure 3, 2nd layer).
2. All circulating high current paths should be kept as short as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on V_{IN} should be placed as close to the IC as possible and should have the shortest possible paths to ground (see Figure 3, top layer).
3. The exposed pad is the power ground connection for the LTC3112. Multiple vias should connect the back pad directly to the ground plane. In addition maximization of the metallization connected to the back pad will improve the thermal environment and improve the power handling capabilities of the IC.
4. The high current components and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
5. Connections to all of the high current components should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
6. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned to the ground plane using a via placed close to the IC and away from the power connections.
7. Keep the connection from the resistor dividers to the feedback pins FB as short as possible and away from the switch pin connections.
8. Crossover connections should be made on inner copper layers if available. If it is necessary to place these on the ground plane, make the trace on the ground plane as short as possible to minimize the disruption to the ground plane (see Figure 3, 3rd layer).

APPLICATIONS INFORMATION

Top Layer

2nd Layer


LTC3112EDHD
Buck-Boost DC/DC Converter
Demo Circuit 1598-1
RUN
ON
OFF
JP1
PWM
750kHz
OSC SYNCH
BURST
JP2
VIN
VOUT
CIN
L
COUT
GND
GND
R10
C6
R3
C4
R7
C12
C1
R4
R1
C11
R9
C13
R2
R8
U1
C2
C3
L1
C7
C8
C9
TECHNOLOGY
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3rd Layer

Bottom Layer (Top View)

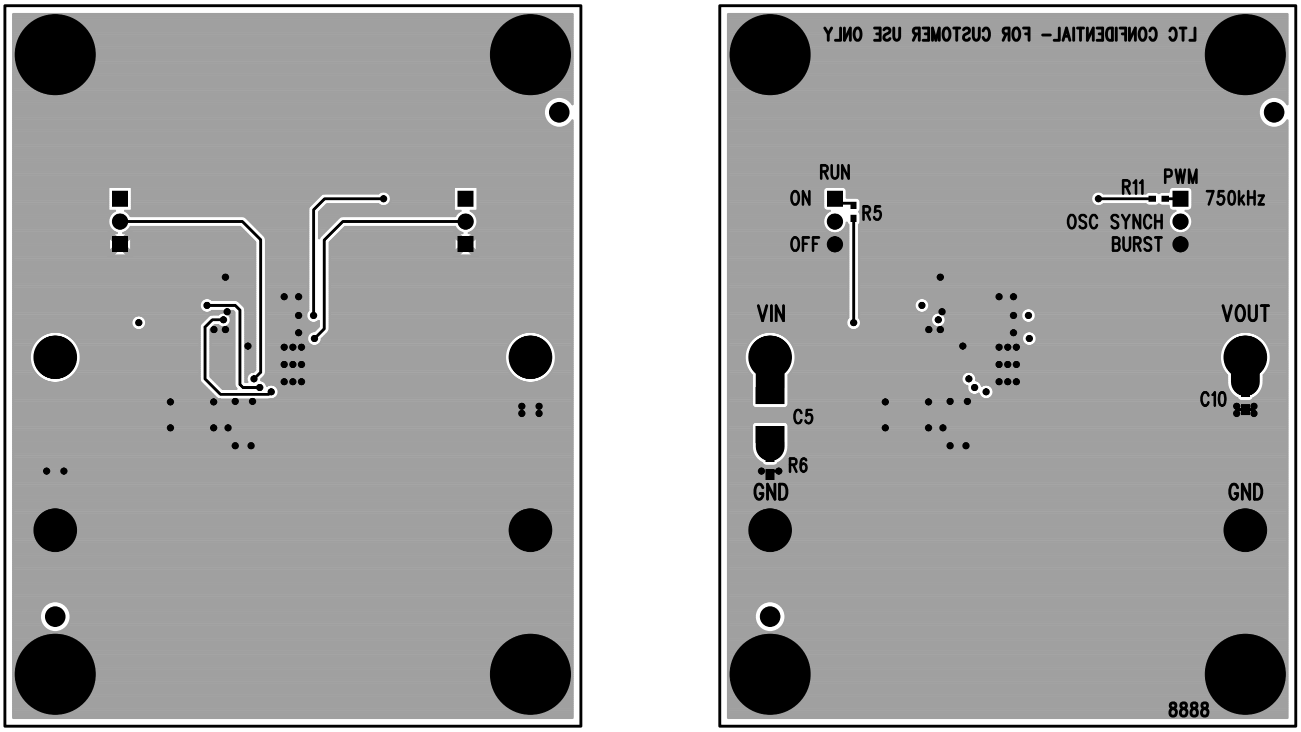
LTC CONFIDENTIAL- FOR CUSTOMER USE ONLY
RUN
ON
OFF
R5
R11
PWM
750kHz
OSC SYNCH
BURST
VIN
VOUT
C5
C10
R6
GND
GND
8888

Figure 3. Example PCB Layout

APPLICATIONS INFORMATION

Buck Mode Small Signal Model

The LTC3112 uses a voltage mode control loop to maintain regulation of the output voltage. An externally compensated error amplifier drives the COMP pin to generate the appropriate duty cycle of the power switches. Use of an external compensation network provides the flexibility for optimization of closed loop performance over the wide variety of output voltages, switching frequencies, and external component values supported by the LTC3112.

The small signal transfer function of the buck-boost converter is different in the buck and boost modes of operation and care must be taken to ensure stability in both operating regions. When stepping down from a higher input voltage to a lower output voltage, the converter will operate in buck mode and the small signal transfer function from the error amplifier output, V_{COMP}, to the converter output voltage is given by the following equation.

$$\left.\frac{V_O}{V_{COMP}}\right|_{BUCK\ MODE} = G_{BUCK}\frac{\left(1+\frac{s}{2\pi f_Z}\right)}{1+\frac{s}{2\pi f_O Q}+\left(\frac{s}{2\pi f_O}\right)^2}$$

The gain term, G_{BUCK}, is comprised of two different components: the gain of the pulse width modulator and the gain of the power stage as given by the following expressions where V_{IN} is the input voltage to the converter in volts, f is the switching frequency in Hz, R is the load resistance in ohms, and t_{LOW} is the switch pin minimum low time. A curve showing the switch pin minimum low time can be found in the Typical Performance Characteristics section of this data sheet. The parameter R_S represents the average series resistance of the power stage and can be approximated as twice the average power switch resistance plus the DC resistance of the inductor.

$$G_{BUCK} = G_{PWM} G_{POWER}$$

$$G_{PWM} = 2(1 - t_{LOW} f)$$

$$G_{POWER} = \frac{V_{IN} R}{(1 - t_{LOW} f)(R + R_S)}$$

The buck mode gain is well approximated by the following equation.

$$G_{BUCK} = \frac{2 \bullet V_{IN} \bullet R}{R + R_S} \cong 2 \bullet V_{IN}$$

The buck mode transfer function has a single zero which is generated by the ESR of the output capacitor. The zero frequency, f_Z, is given by the following expression where R_C and C_O are the ESR (in ohms) and value (in farads) of the output filter capacitor respectively.

$$f_Z = \frac{1}{2\pi R_C C_O}$$

In most applications, an output capacitor with a very low ESR is utilized in order to reduce the output voltage ripple to acceptable levels. Such low values of capacitor ESR result in a very high frequency zero and as a result the zero is commonly too high in frequency to significantly impact compensation of the feedback loop.

The denominator of the buck mode transfer function exhibits a pair of resonant poles generated by the LC filtering of the power stage. The resonant frequency of the power stage, f_O, is given by the following expression where L is the value of the inductor in henries.

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R + R_S}{LC_O(R + R_C)}} \cong \frac{1}{2\pi}\sqrt{\frac{1}{LC_O}}$$

The quality factor, Q, has a significant impact on compensation of the voltage loop since a higher Q factor produces a sharper loss of phase near the resonant frequency. The quality factor is inversely related to the amount of damping in the power stage and is substantially influenced by the average series resistance of the power stage, R_S. Lower values of R_S will increase the Q and result in a sharper loss of phase near the resonant frequency and will require more phase boost or lower bandwidth to maintain an adequate phase margin.

$$Q = \frac{\sqrt{LC_O(R + R_C)(R + R_S)}}{RR_C C_O + L + C_O R_S(R + R_C)} \cong \frac{\sqrt{LC_O}}{\frac{L}{R} + C_O R_S}$$

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Boost Mode Small Signal Model

When stepping up from a lower input voltage to a higher output voltage, the buck-boost converter will operate in boost mode where the small signal transfer function from control voltage, V_{COMP}, to the output voltage is given by the following expression.

$$\left.\frac{V_O}{V_{COMP}}\right|_{BOOST\ MODE} = G_{BOOST}\frac{\left(1+\frac{s}{2\pi f_Z}\right)\left(1-\frac{s}{2\pi f_{RHPZ}}\right)}{1+\frac{s}{2\pi f_O Q}+\left(\frac{s}{2\pi f_O}\right)^2}$$

In boost mode operation, the transfer function is characterized by a pair of resonant poles and a zero generated by the ESR of the output capacitor as in buck mode. However, in addition there is a right half plane zero which generates increasing gain and decreasing phase at higher frequencies. As a result, the crossover frequency in boost mode operation generally must be set lower than in buck mode in order to maintain sufficient phase margin.

The boost mode gain, G_{BOOST}, is comprised of two components: the pulse width modulator and the power stage. The gain of the power stage in boost mode is given by the following equation.

$$G_{POWER} \cong \frac{V_{OUT}^2}{(1-t_{LOW}\,f)V_{IN}}$$

By combining the individual terms, the total gain in boost mode can be reduced to the following expression. Notice that unlike in buck mode, the gain in boost mode is a function of both the input and output voltage.

$$G_{BOOST} \cong \frac{2 \bullet V_{OUT}^2}{V_{IN}}$$

In boost mode operation, the frequency of the right half plane zero, f_Z, is given by the following expression. The frequency of the right half plane zero decreases at higher loads and with larger inductors.

$$f_{RHPZ} = \frac{R(1-t_{LOW}\,f)^2\,V_{IN}^2}{2\pi L\,V_{OUT}^2}$$

In boost mode, the resonant frequency of the power stage has a dependence on the input and output voltage as shown by the following equation.

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R_S+\frac{RV_{IN}^2}{V_{OUT}^2}}{LC_O(R+R_C)}} \cong \frac{1}{2\pi}\bullet\frac{V_{IN}}{V_{OUT}}\sqrt{\frac{1}{LC}}$$

Finally, the magnitude of the quality factor of the power stage in boost mode operation is given by the following expression.

$$Q = \frac{\sqrt{LC_OR\left(R_S+\frac{RV_{IN}^2}{V_{OUT}^2}\right)}}{L+C_OR_SR}$$

Compensation of the Voltage Loop

The small signal models of the LTC3112 reveal that the transfer function from the error amplifier output, V_{COMP}, to the output voltage is characterized by a set of resonant poles and a possible zero generated by the ESR of the output capacitor as shown in the Bode plot of Figure 4. In boost mode operation, there is an additional right half plane zero that produces phase lag and increasing gain at higher frequencies. Typically, the compensation network is designed to ensure that the loop crossover frequency is low enough that the phase loss from the right half plane zero is minimized. The low frequency gain in buck mode is a constant, but varies with both V_{IN} and V_{OUT} in boost mode.

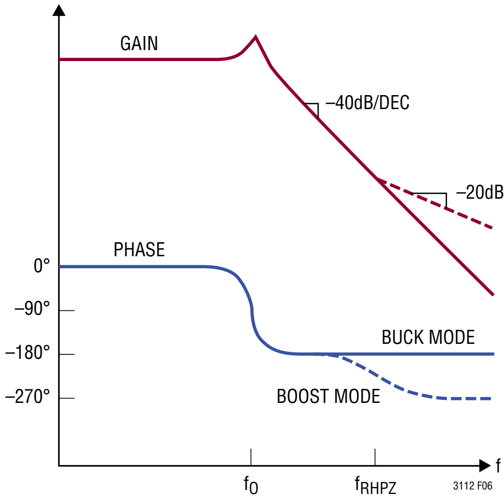

Figure 4. Buck-Boost Converter Bode Plot

APPLICATIONS INFORMATION

For charging, LED lighting, or other applications that do not require an optimized output voltage transient re-sponse, a simple Type I compensation network as shown in Figure 5 can be used to stabilize the voltage loop. To ensure sufficient phase margin, the gain of the error am-plifier must be low enough that the resultant crossover frequency of the control loop is well below the resonant frequency.

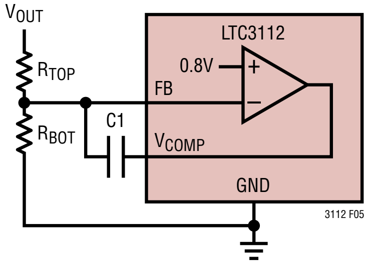

Figure 5. Error Amplifier with Type I Compensation

In most applications, the low bandwidth of the Type I com-pensated loop will not provide sufficient transient response performance. To obtain a wider bandwidth feedback loop, optimize the transient response, and minimize the size of the output capacitor, a Type III com-pensation network as shown in Figure 6 is required.

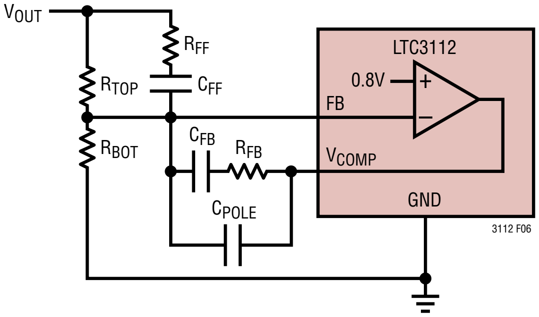

Figure 6. Error Amplifier with Type III Compensation

A Bode plot of the typical Type III compensation network is shown in Figure 7. The Type III compensation network provides a pole near the origin which produces a very high loop gain at DC to minimize any steady state error in the regulation voltage. Two zeros located at f_{ZERO1} and f_{ZERO2} provide sufficient phase boost to allow the loop crossover frequency to be set above the resonant frequency, f_O, of the power stage. The Type III compensation network also introduces a second and third pole. The second pole, at frequency f_{POLE2}, reduces the error amplifier gain to a zero slope to prevent the loop crossover from extending too high in frequency. The third pole at frequency f_{POLE3} provides attenuation of high frequency switching noise.

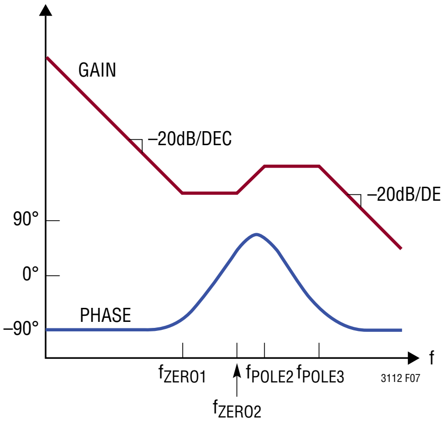

Figure 7. Type III Compensation Bode Plot.

The transfer function of the compensated Type III error amplifier from the input of the resistor divider to the output of the error amplifier, V_{COMP}, is:

$$\frac{V_{COMP}(s)}{V_{OUT}(s)} = G_{EA}\frac{\left(1+\frac{s}{2\pi f_{ZERO1}}\right)\left(1+\frac{s}{2\pi f_{ZERO2}}\right)}{s\left(1+\frac{s}{2\pi f_{POLE1}}\right)\left(1+\frac{s}{2\pi f_{POLE2}}\right)}$$

The error amplifier gain is given by the following equation. The simpler approximate value is sufficiently accurate in most cases since C_{FB} is typically much larger in value than C_{POLE}.

$$G_{EA} = \frac{1}{R_{TOP}(C_{FB}+C_{POLE})} \cong \frac{1}{R_{TOP}C_{FB}}$$

The pole and zero frequencies of the Type III compensation network can be calculated from the following equations where all frequencies are in Hz, resistances are in ohms, and capacitances are in farads.

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$$f_{ZERO1} = \frac{1}{2\pi R_{FB} C_{FB}}$$

$$f_{ZERO2} = \frac{1}{2\pi (R_{TOP} + R_{FF}) C_{FF}} \cong \frac{1}{2\pi R_{TOP} C_{FF}}$$

$$f_{POLE2} = \frac{C_{FB} + C_{POLE}}{2\pi C_{FB} C_{POLE} R_{FB}} \cong \frac{1}{2\pi C_{POLE} R_{FB}}$$

$$f_{POLE3} = \frac{1}{2\pi C_{FF} R_{FF}}$$

In most applications the compensation network is designed so that the loop crossover frequency is above the resonant frequency of the power stage, but sufficiently below the boost mode right half plane zero to minimize the additional phase loss. Once the crossover frequency is decided upon, the phase boost provided by the compensation network is centered at that point in order to maximize the phase margin. A larger separation in frequency between the zeros and higher order poles will provide a higher peak phase boost but may also increase the gain of the error amplifier which can push out the loop crossover to a higher frequency.

The Q of the power stage can have a significant influence on the design of the compensation network because it determines how rapidly the 180° of phase loss in the power stage occurs. For very low values of series resistance, R_S, the Q will be higher and the phase loss will occur sharply. In such cases, the phase of the power stage will fall rapidly to –180° above the resonant frequency and the total phase margin must be provided by the compensation network. However, with higher losses in the power stage (larger R_S) the Q factor will be lower and the phase loss will occur more gradually. As a result, the power stage phase will not be as close to –180° at the crossover frequency and less phase boost is required of the compensation network.

The LTC3112 error amplifier is designed to have a fixed maximum bandwidth in order to provide rejection of switching noise to prevent it from interfering with the control loop. From a frequency domain perspective, this can be viewed as an additional single pole as illustrated in Figure 8. The nominal frequency of this pole is 400kHz. For typical loop crossover frequencies below about 60kHz the phase contributed by this additional pole is negligible. However, for loops with higher crossover frequencies this additional phase loss should be taken into account when designing the compensation network.

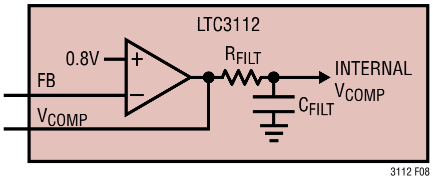

Figure 8. Internal Loop Filter.

Loop Compensation Example

This section provides an example illustrating the design of a compensation network for a typical LTC3112 application circuit. In this example a 5V regulated output voltage is generated with the ability to supply a 1A load from an input power source ranging from 3.5V to 15V. The nominal 750kHz switching frequency has been chosen. In this application the maximum inductor current ripple will occur at the highest input voltage. An inductor value of 4.7μH has been chosen to limit the worst case inductor current ripple to approximately 1A. A low ESR output capacitor with a value of 47μF is specified to yield a worst case output voltage ripple (occurring at the worst case step-up ratio and maximum load current) of approximately 10mV. In summary, the key power stage specifications for this LTC3112 example application are given below.

$f = 0.75\text{MHz}$, $t_{LOW} = 0.2\mu s$

$V_{IN} = 3.5V$ to $15V$

$V_{OUT} = 5V$ at $1A$

$C_{OUT} = 47\mu F$, $R_C = 5m\Omega$

$L = 4.7\mu H$, $R_L = 50m\Omega$

With the power stage parameters specified, the compensation network can be designed. In most applications, the most challenging compensation corner is boost mode operation at the greatest step-up ratio and highest load current since this generates the lowest frequency right half plane zero and results in the greatest phase loss. Therefore, a reasonable approach is to design the compensation network at this worst case corner and

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then verify that sufficient phase margin exists across all other operating conditions. In this example application, at V_{IN} = 3.5V and the full 1A load current, the right half plane zero will be located at 60kHz and this will be a dominant factor in determining the bandwidth of the control loop.

The first step in designing the compensation network is to determine the target crossover frequency for the compensated loop. A reasonable starting point is to assume that the compensation network will generate a peak phase boost of approximately 60°. Therefore, in order to obtain a phase margin of 60°, the loop crossover frequency, f_C, should be selected as the frequency at which the phase of the buck-boost converter reaches –180°. As a result, at the loop crossover frequency the total phase will be simply the 60° of phase provided by the error amplifier as shown below.

$$\text{Phase Margin} = \phi_{\text{BUCK-BOOST}} + \phi_{\text{ERRORAMPLIFIER}} + 180°$$
$$= -180° + 60° + 180° = 60°$$

Similarly, if a phase margin of 45° is required, the target crossover frequency should be picked as the frequency at which the buck-boost converter phase reaches –195° so that the combined phase at the crossover frequency yields the desired 45° of phase margin.

This example will be designed for a 60° phase margin to ensure adequate performance over parametric variations and varying operating conditions. As a result, the target crossover frequency, f_C, will be the point at which the phase of the buck-boost converter reaches –180°. It is generally difficult to determine this frequency analytically given that it is significantly impacted by the Q factor of the resonance in the power stage. As a result, it is best determined from a Bode plot of the buck-boost converter as shown in Figure 9. This Bode plot is for the LTC3112 buck-boost converter using the previously specified power stage parameters and was generated from the small signal model equations using LTSpice®. In this case, the phase reaches –180° at 35kHz making f_C = 35kHz the target crossover frequency for the compensated loop.

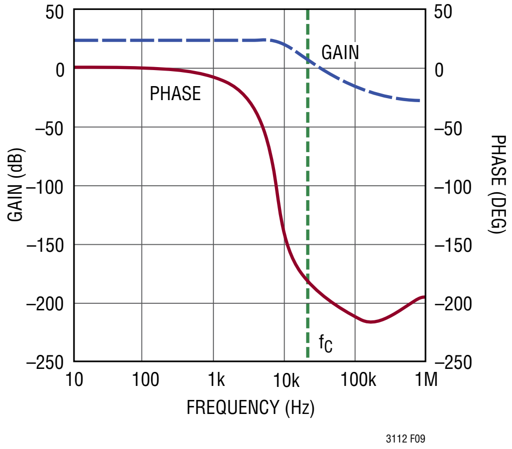

Figure 9. Converter Bode Plot, V_{IN} = 3.5V, I_{LOAD} = 1A

From the Bode plot of Figure 9 the gain of the power stage at the target crossover frequency is 7dB. Therefore, in order to make this frequency the crossover frequency in the compensated loop, the total loop gain at f_C must be adjusted to 0dB. To achieve this, the gain of the compensation network must be designed to be –7dB at the crossover frequency.

At this point in the design process, there are three constraints that have been established for the compensation network. It must have –7dB gain at f_C = 35kHz, a peak phase boost of 60° and the phase boost must be centered at f_C = 35kHz. One way to design a compensation network to meet these targets is to simulate the compensated error amplifier Bode plot in LTSpice for the typical compensation network shown on the front page of this data sheet. Then, the gain, pole frequencies and zero frequencies can be iteratively adjusted until the required constraints are met.

Alternatively, an analytical approach can be used to design a compensation network with the desired phase boost, center frequency and gain. In general, this procedure can be cumbersome due to the large number of degrees of freedom in a Type III compensation network. However the design process can be simplified by assuming that both compensation zeros occur at the same frequency, f_Z, and

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both higher order poles (f_{POLE2} and f_{POLE3}) occur at the common frequency, f_P. In most cases this is a reasonable assumption since the zeros are typically located between 1kHz and 10kHz and the poles are typically located near each other at much higher frequencies. Given this assumption, the maximum phase boost, ϕ_{MAX}, provided by the compensated error amplifier is determined simply by the amount of separation between the poles and zeros as shown by the following equation.

$$\phi_{MAX} = 4\tan^{-1}\left(\sqrt{\frac{f_P}{f_Z}}\right) - 270°$$

A reasonable choice is to pick the frequency of the poles, f_P, to be about 50 times higher than the frequency of the zeros, f_Z, which provides a peak phase boost of approximately $\phi_{MAX} = 60°$ as was assumed previously. Next, the phase boost must be centered so that the peak phase occurs at the target crossover frequency. The frequency of the maximum phase boost, f_{CENTER}, is the geometric mean of the pole and zero frequencies as shown below.

$$f_{CENTER} = \sqrt{f_P f_Z} = \sqrt{50} \bullet f_Z \cong 7f_Z$$

Therefore, in order to center the phase boost given a factor of 50 separation between the pole and zero frequencies, the zeros should be located at one seventh of the crossover frequency and the poles should be located at seven times the crossover frequency as given by the following equations.

$$f_Z = \frac{1}{7}f_C = \frac{1}{7}(35\text{kHz}) = 5\text{kHz}$$

$$f_P = 7f_C = 7(35\text{kHz}) = 250\text{kHz}$$

This placement of the poles and zeros will yield a peak phase boost of 60° that is centered at the crossover frequency, f_C. Next, in order to produce the desired target crossover frequency, the gain of the compensation network at the point of maximum phase boost, G_{CENTER}, must be set to –7dB. The gain of the compensated error amplifier at the point of maximum phase gain is given by the following equation.

$$G_{CENTER} = 10\log\left[\frac{2\pi f_P}{(2\pi f_Z)^3 (R_{TOP} C_{FB})^2}\right]\text{dB}$$

Assuming a multiple of 50 separation between the pole frequencies and zero frequencies this can be simplified to the following expression.

$$G_{CENTER} = 20\log\left[\frac{50}{2\pi f_C R_{TOP} C_{FB}}\right]\text{dB}$$

This equation completes the set of constraints needed to determine the compensation component values. Specifically, the two zeros, f_{ZERO1} and f_{ZERO2}, should be located near 5kHz. The two poles, f_{POLE2} and f_{POLE3}, should be located near 250kHz and the gain should be set to provide a gain at the crossover frequency of $G_{CENTER} = –7\text{dB}$.

The first step in defining the compensation component values is to pick a value for R_{TOP} that provides an acceptably low quiescent current through the resistor divider. A value of $R_{TOP} = 845\text{k}\Omega$ is a reasonable choice and is used in several applications circuits. Next, the value of C_{FB} can be found in order to set the error amplifier gain at the crossover frequency to –7dB as follows.

$$G_{CENTER} = -7\text{dB} = 20\log\left[\frac{50}{2\pi(35\text{kHz})(845\text{k}\Omega)C_{FB}}\right]$$

$$C_{FB} = \frac{50}{0.185 \bullet 10^{12} \bullet \text{antilog}\left(\frac{-7}{20}\right)} \cong 680\text{pF}$$

The compensation poles can be set at 250kHz and the zeros at 5kHz by using the expressions for the pole and zero frequencies given in the previous section. Setting the frequency of the first zero f_{ZERO1}, to 5kHz results in the following value for R_{FB}.

$$R_{FB} = \frac{1}{2\pi(680\text{pF})(5\text{kHz})} \cong 45\text{k}\Omega$$

A 33kΩ was selected to split the two zeros slightly apart, giving a higher zero frequency of 7kHz. This leaves the free parameter, C_{POLE}, to set the frequency f_{POLE1} to the common pole frequency of 250kHz.

APPLICATIONS INFORMATION

$$C_{POLE} = \frac{1}{2\pi(33k\Omega)(250kHz)} \cong 22pF$$

Next, C_{FF} can be chosen to set the second zero, f_{ZERO2}, to the common zero frequency of 5kHz.

$$C_{FF} = \frac{1}{2\pi(845k\Omega)(5kHz)} \cong 40pF$$

In this case C_{FF} was selected at 47pF giving a lower frequency of 4kHz for the second zero. Finally, the resistor value R_{FF} can be chosen to place the second pole.

$$R_{FF} = \frac{1}{2\pi(47pF)(250kHz)} \cong 13k\Omega$$

A 10kΩ is chosen giving a 325kHz pole frequency. Now that the pole frequencies, zero frequencies and gain of the compensation network have been established, the next step is to generate a Bode plot for the compensated error amplifier to confirm its gain and phase properties. A Bode plot of the error amplifier with the designed compensation component values is shown in Figure 10. The Bode plot confirms that the peak phase occurs near 30kHz and the phase boost at that point is around 60°. In addition, the gain at the peak phase frequency is –10db, close to the design target.

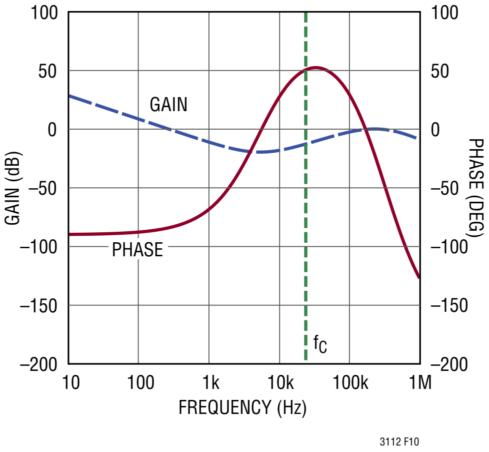


Figure 10. Compensated Error Amplifier Bode Plot.

The final step in the design process is to compute the Bode plot for the entire loop using the designed compensation network and confirm its phase margin and crossover frequency. The complete loop Bode plot for this example is shown in Figure 11. The resulting loop crossover frequency is 25kHz and the phase margin is approximately 60°. The crossover frequency is a bit lower than the design target of 35kHz, but farther away from the troublesome right half plane zero.

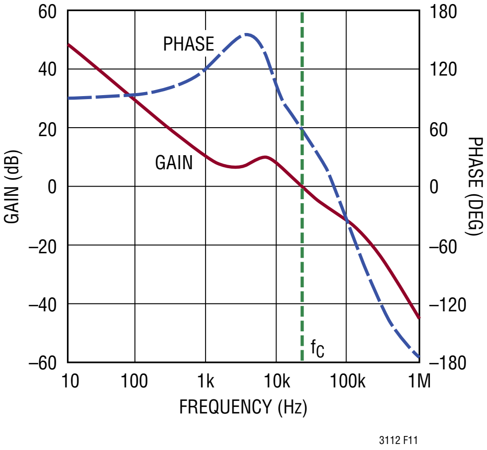


Figure 11. Complete Loop Bode Plot.

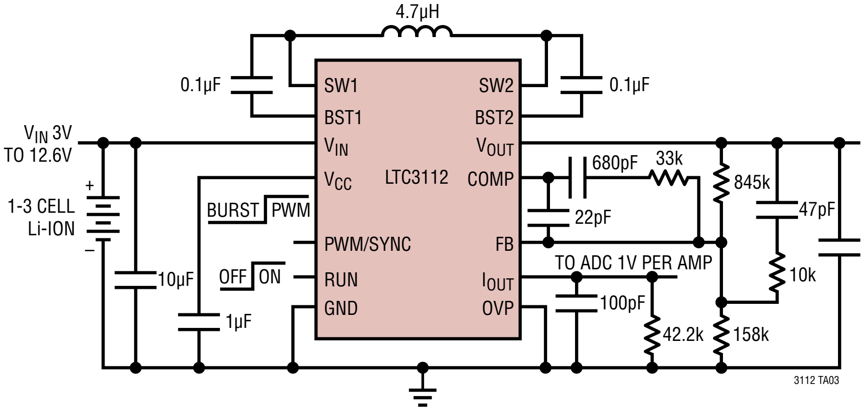
This feedback design example was done at $3.5V_{IN}$, $5V_{OUT}$, and a 1A load current. The phase margin in boost mode will decrease at lower V_{IN}s, higher V_{OUT}s, load currents, or inductor values due to the right half plane zero shifting to a lower frequency.

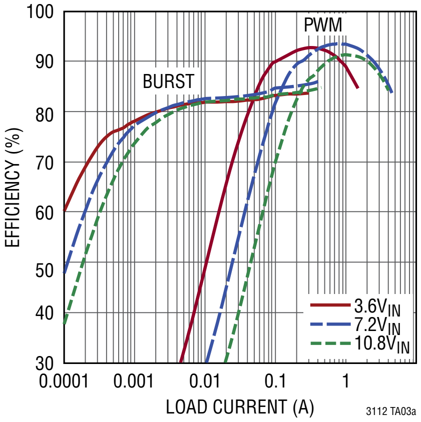
As a reminder, the amount of power stage Q at the L-C resonant frequency is highly dependent on the R_S term (series resistance) which includes the ESR of the inductor and the LTC3112's low R_{ON} MOSFETs. Lower total series resistances give a higher Q, making the feedback design more difficult. Higher series resistances lower the Q, resulting in a lower loop cross over frequency.

The Bode plot for the complete loop should be checked over all operating conditions and for variations in component values to ensure that sufficient phase margin exists in all cases. The stability of the loop should also be confirmed via time domain simulation and by evaluating the transient response of the converter in the actual circuit.

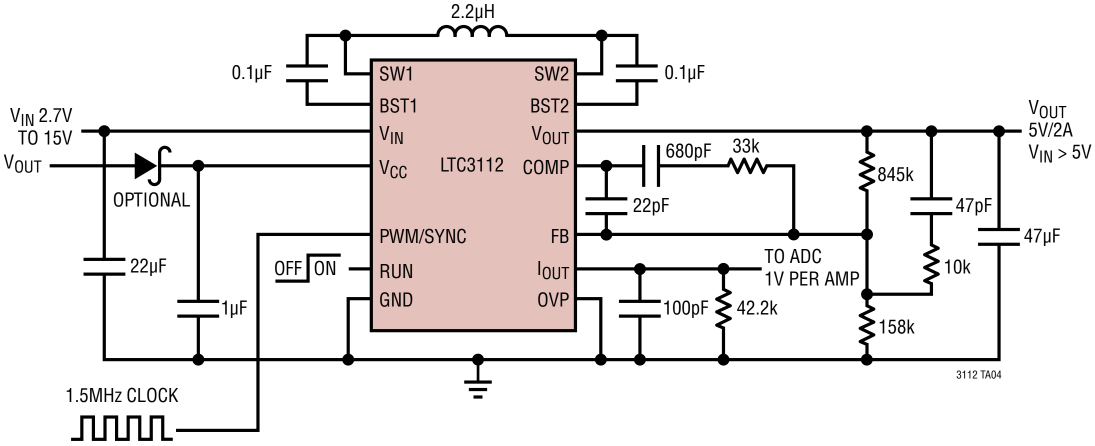
TYPICAL APPLICATIONS

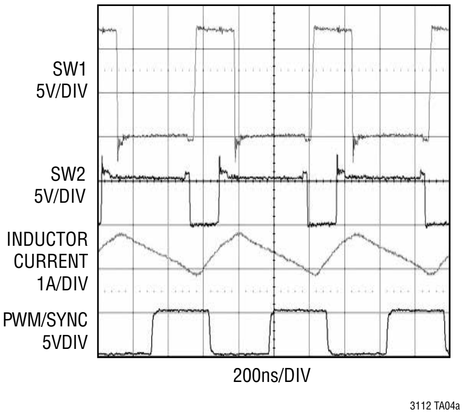
1,2 or 3 Li-Ion to 5V


4.7µH
0.1µF
0.1µF
SW1
SW2
BST1
BST2
V_{IN}
V_{OUT}
V_{CC}
LTC3112
COMP
V_{IN} 3V TO 12.6V
1-3 CELL Li-ION
+
–
BURST
PWM
PWM/SYNC
FB
OFF
ON
RUN
I_{OUT}
GND
OVP
10µF
1µF
680pF
33k
22pF
845k
47pF
10k
47µF
TO ADC 1V PER AMP
100pF
42.2k
158k
V_{OUT} 5V/1.5A
V_{IN} > 4V
3112 TA03



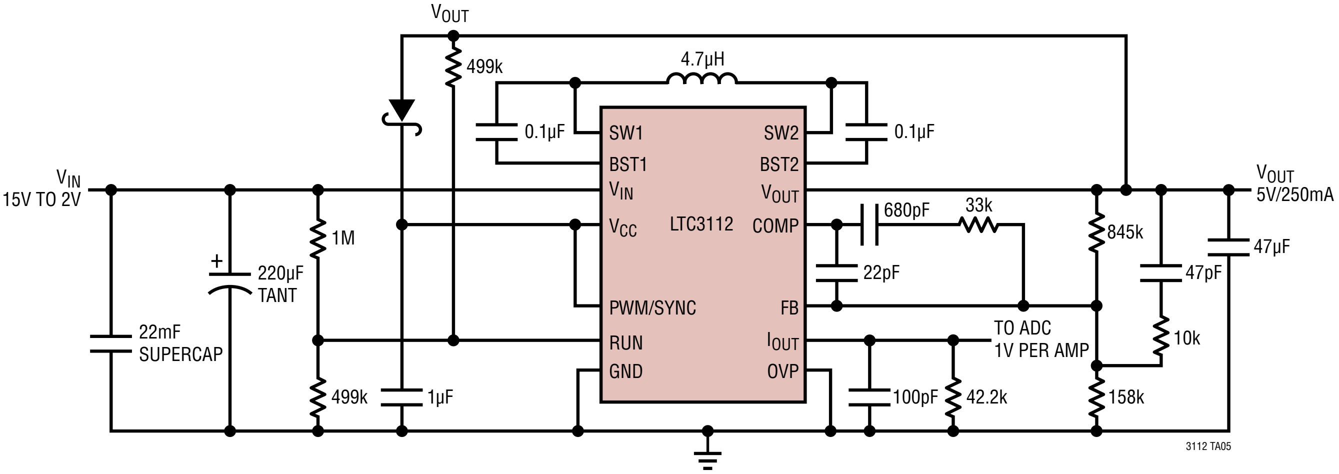
LTC3112 Synchronized to 1.5MHz Clock, 5V/2A Output

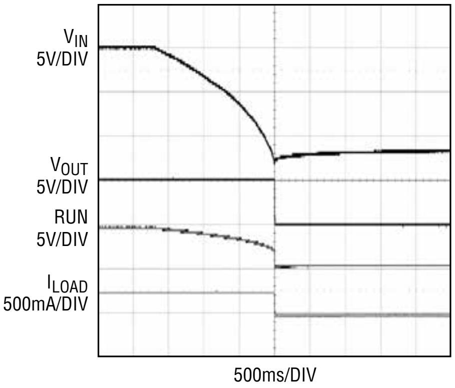

2.2µH
0.1µF
0.1µF
SW1
SW2
BST1
BST2
V_{IN}
V_{OUT}
V_{CC}
LTC3112
COMP
V_{IN} 2.7V TO 15V
V_{OUT}
OPTIONAL
22µF
1µF
PWM/SYNC
FB
OFF
ON
RUN
I_{OUT}
GND
OVP
680pF
33k
22pF
845k
47pF
10k
47µF
TO ADC 1V PER AMP
100pF
42.2k
158k
V_{OUT} 5V/2A
V_{IN} > 5V
1.5MHz CLOCK
3112 TA04



TYPICAL APPLICATIONS

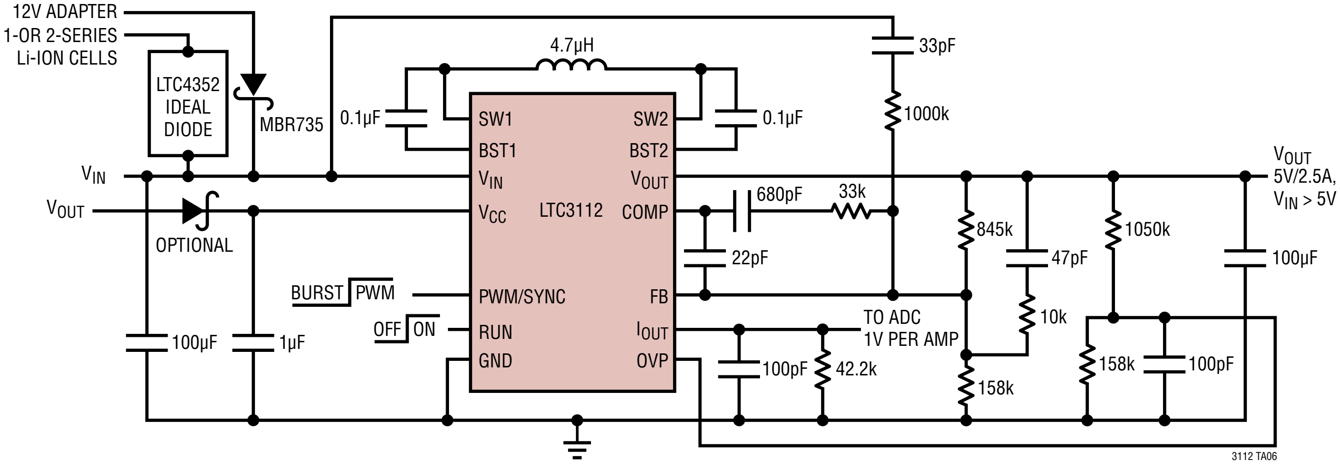
5V Backup Supply from Supercap Runs Down to V_{IN} = 2V with 250mA Load

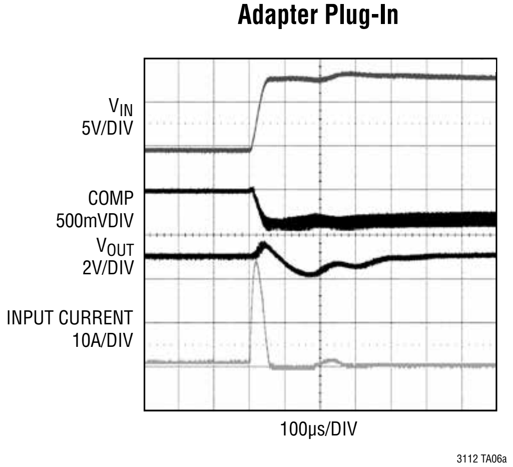

VOUT
499k
4.7µH
0.1µF
0.1µF
SW1
SW2
BST1
BST2
VIN
VOUT
VCC
LTC3112
COMP
PWM/SYNC
FB
RUN
IOUT
GND
OVP
VIN
15V TO 2V
VOUT
5V/250mA
1M
220µF
TANT
22mF
SUPERCAP
499k
1µF
680pF
33k
22pF
845k
47pF
47µF
TO ADC
1V PER AMP
10k
100pF
42.2k
158k
3112 TA05

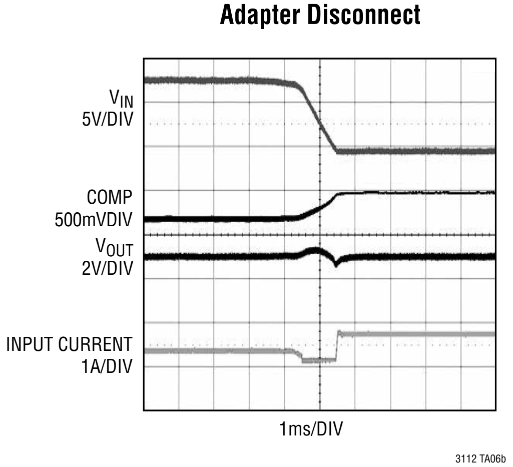


TYPICAL APPLICATIONS

Stepped Response from 1 or 2 Li-Ion to 12V Adapter Source with V_{IN} Feedforward Network

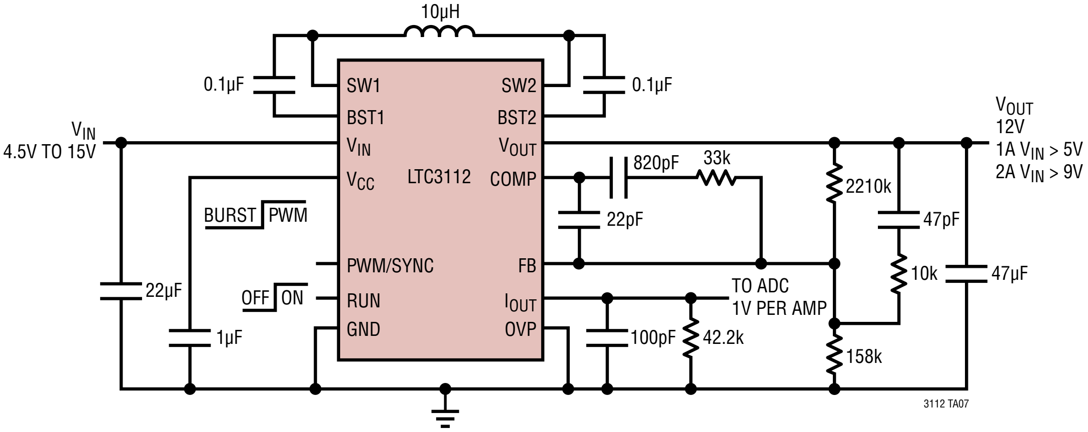

12V ADAPTER
1-OR 2-SERIES
Li-ION CELLS
LTC4352
IDEAL
DIODE
MBR735
V_{IN}
V_{OUT}
OPTIONAL
100µF
1µF
0.1µF
4.7µH
0.1µF
33pF
1000k
SW1
BST1
V_{IN}
V_{CC}
LTC3112
PWM/SYNC
RUN
GND
SW2
BST2
V_{OUT}
COMP
FB
I_{OUT}
OVP
BURST
PWM
OFF
ON
680pF
33k
22pF
TO ADC
1V PER AMP
100pF
42.2k
845k
47pF
10k
158k
1050k
158k
100pF
100µF
V_{OUT}
5V/2.5A,
V_{IN} > 5V
3112 TA06

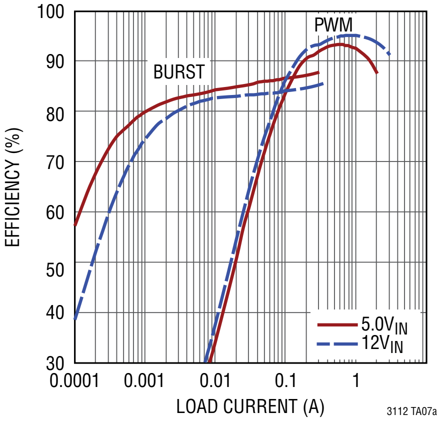




TYPICAL APPLICATIONS

Regulated 12V Output from Wide Input Supply Range


10µH
0.1µF
0.1µF
SW1
SW2
BST1
BST2
V_{IN}
V_{OUT}
V_{CC}
LTC3112
COMP
PWM/SYNC
FB
RUN
I_{OUT}
GND
OVP
V_{IN}
4.5V TO 15V
BURST
PWM
OFF
ON
22µF
1µF
820pF
33k
22pF
100pF
42.2k
TO ADC
1V PER AMP
2210k
47pF
10k
158k
47µF
V_{OUT}
12V
1A V_{IN} > 5V
2A V_{IN} > 9V
3112 TA07

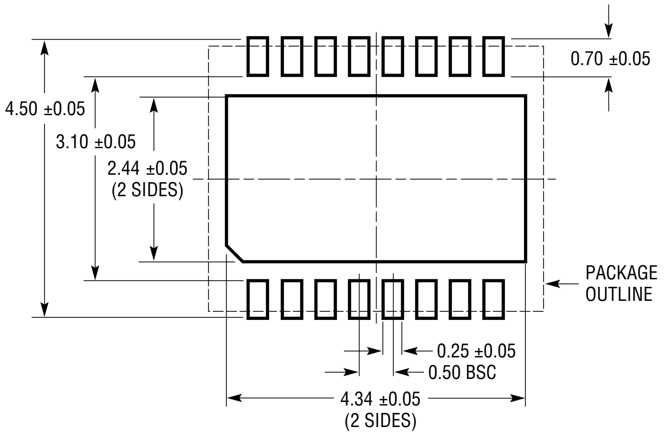


PACKAGE DESCRIPTION

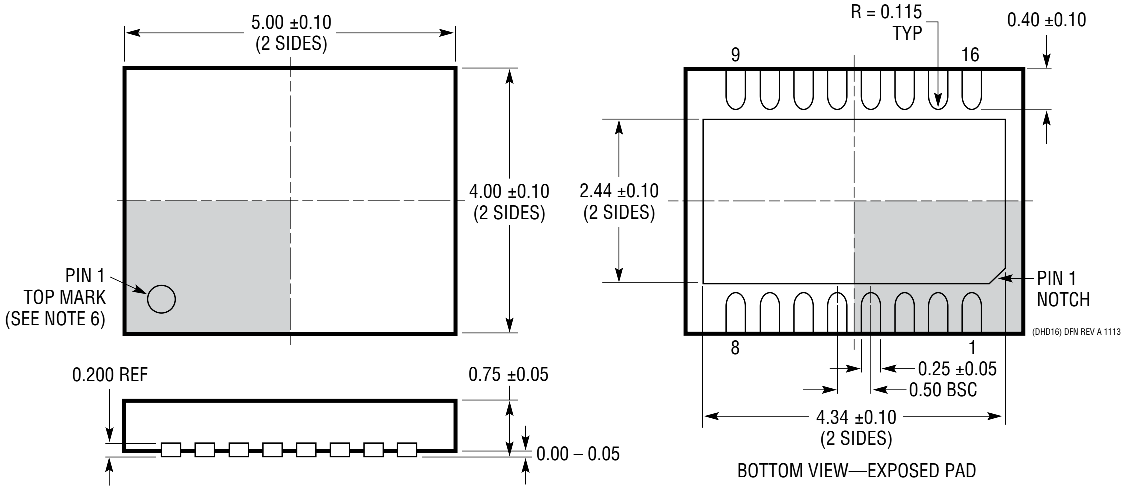
Please refer to http://www.linear.com/product/LTC3112#packaging for the most recent package drawings.

DHD Package
16-Lead Plastic DFN (5mm × 4mm)

(Reference LTC DWG # 05-08-1707 Rev A)


4.50 ±0.05
3.10 ±0.05
2.44 ±0.05
(2 SIDES)
0.70 ±0.05
PACKAGE
OUTLINE
0.25 ±0.05
0.50 BSC
4.34 ±0.05
(2 SIDES)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS


5.00 ±0.10
(2 SIDES)
4.00 ±0.10
(2 SIDES)
PIN 1
TOP MARK
(SEE NOTE 6)
0.200 REF
0.75 ±0.05
0.00 – 0.05
R = 0.115
TYP
0.40 ±0.10
9
16
2.44 ±0.10
(2 SIDES)
PIN 1
NOTCH
(DHD16) DFN REV A 1113
8
1
0.25 ±0.05
0.50 BSC
4.34 ±0.10
(2 SIDES)

BOTTOM VIEW—EXPOSED PAD

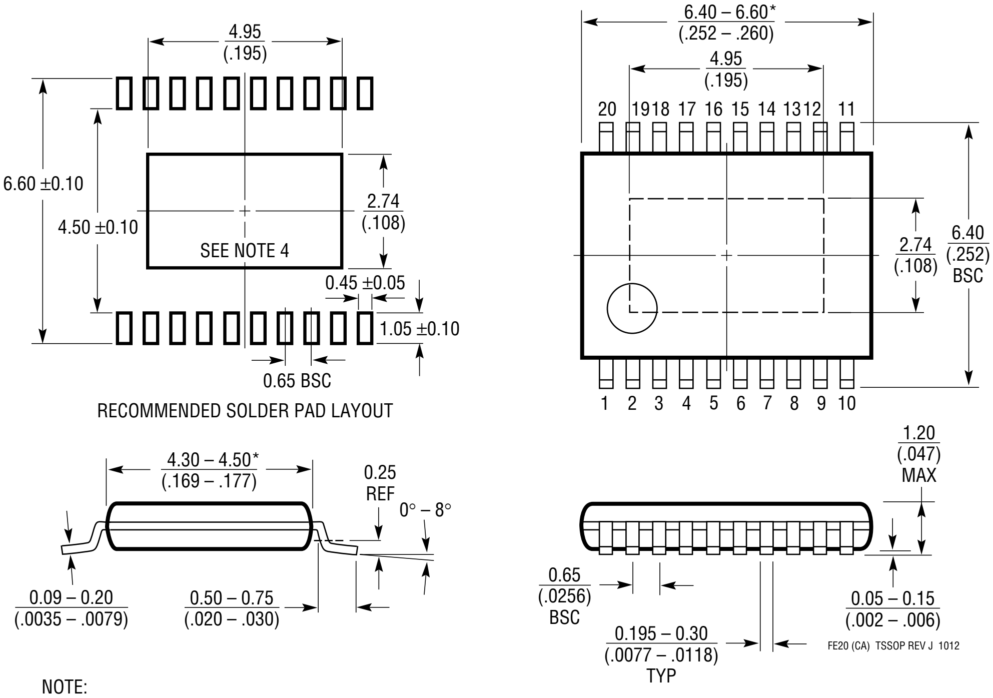
NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3112#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation CA


4.95
(.195)
6.60 ±0.10
4.50 ±0.10
SEE NOTE 4
2.74
(.108)
0.45 ±0.05
1.05 ±0.10
0.65 BSC
RECOMMENDED SOLDER PAD LAYOUT
6.40 – 6.60*
(.252 – .260)
4.95
(.195)
20 19 18 17 16 15 14 13 12 11
2.74
(.108)
6.40
(.252)
BSC
1 2 3 4 5 6 7 8 9 10
4.30 – 4.50*
(.169 – .177)
0.25
REF
0° – 8°
0.09 – 0.20
(.0035 – .0079)
0.50 – 0.75
(.020 – .030)
1.20
(.047)
MAX
0.65
(.0256)
BSC
0.195 – 0.30
(.0077 – .0118)
TYP
0.05 – 0.15
(.002 – .006)
FE20 (CA) TSSOP REV J 1012

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

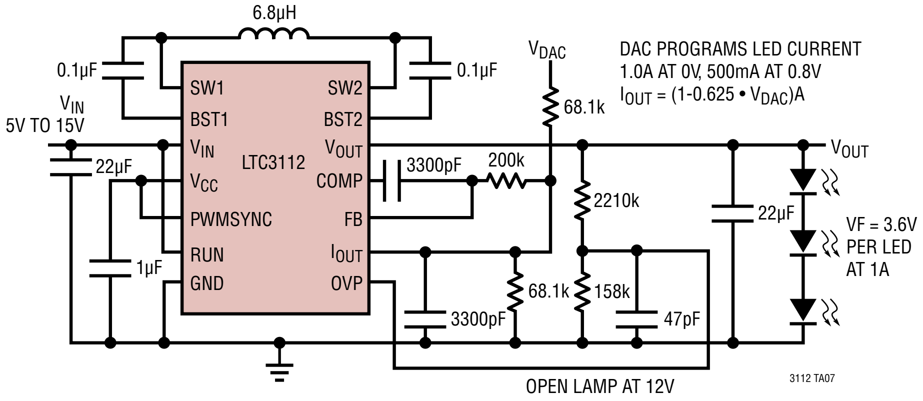
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/13	Clarified Absolute Maximum Rating: I_{OUT} voltage spec.	2
		Clarified RUN threshold specification.	3
		Clarified thermal considerations last paragraph.	12
		Clarified LTC4352 part designator.	28
		Clarified Related Parts list.	32
B	10/13	Clarified Buck Mode Small Signal Model Text	18
		Clarified C_{FB} Formula	23
C	06/14	Clarified Title of Typical Application	1
		Clarified Absolute Maximum Temperature Range and Ordering Information	2
		Clarified Note 2, 3 Temperature Range on Input Operating Range	3, 4
		Clarified Graphs Temperature Range	6
		Clarified Maximum Junction Temperature	12
D	09/16	Changed Minimum V_{IN} UVLO Threshold spec	3
		Fixed Block Diagram node error	10

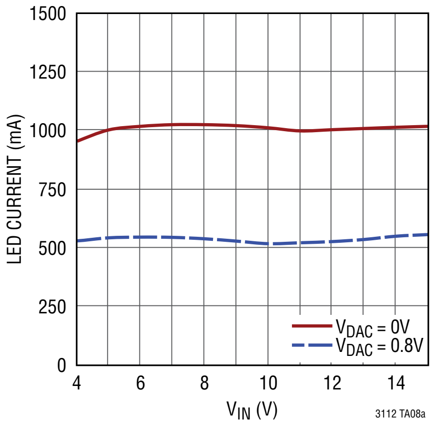
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

10W, 10V High Intensity LED Driver with Programmable Current and Low-Loss Sensing


6.8µH
0.1µF
0.1µF
V_{IN}
5V TO 15V
22µF
1µF
SW1
BST1
V_{IN}
V_{CC}
PWMSYNC
RUN
GND
LTC3112
SW2
BST2
V_{OUT}
COMP
FB
I_{OUT}
OVP
V_{DAC}
68.1k
DAC PROGRAMS LED CURRENT
1.0A AT 0V, 500mA AT 0.8V
I_{OUT} = (1-0.625 • V_{DAC})A
3300pF
200k
2210k
V_{OUT}
22µF
VF = 3.6V
PER LED
AT 1A
68.1k
158k
3300pF
47pF
OPEN LAMP AT 12V
3112 TA07

LED Current vs V_{IN} and DAC Voltage



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3531	200mA Buck-Boost Synchronous DC/DC Converter	V_{IN} = 1.8V to 5.5V, V_{OUT} = 3.3V, I_Q = 16µA, I_{SD} < 1µA , SOT23, DFN Package
LTC3129	15V, 200mA Synchronous Buck-Boost Converter	V_{IN} = 2.42V to 15V, V_{OUT} = 1.4V to 15.75V, I_Q = 1.3µA, I_{SD} < 10nA , QFN and MSOP Packages
LTC3533	2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN} = 1.8V to 5.5V, V_{OUT} = 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA , DFN Package
LTC3113	3A Low Noise Synchronous Buck-Boost DC/DC Converter	V_{IN} or V_{OUT} = 1.8V to 5.5V, I_Q = 40µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3534	7V, 500mA Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.4V to 7V, V_{OUT} = 1.8V to 7V, I_Q = 25µA, I_{SD} < 1µA , DFN, GN Package
LTC3538	800mA Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.4V to 5.5V, V_{OUT} = 1.8V to 5.25V, I_Q = 35µA, I_{SD} < 5µA , DFN Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.5V to 5.5V, V_{OUT} = 2.5V to 5.25V, I_Q = 25µA, I_{SD} < 1µA , MSOP and DFN Packages
LTC3441	1.2A (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.4V to 5.5V, V_{OUT} = 2.4V to 5.25V, I_Q = 25µA, I_{SD} < 1µA , DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter with Programmable Burst Mode Operation	V_{IN} = 2.4V to 5.5V, V_{OUT} = 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA , DFN Package
LTC3443	High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.4V to 5.5V, V_{OUT} = 1.5V to 5.25V, I_Q = 28µA, I_{SD} < 1µA , DFN Package
LTC3115-1	2A (I_{OUT}), 40V Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.7V to 40V, V_{OUT} = 2.7V to 40V, I_Q = 30µA, I_{SD} < 3µA , DFN and TSSOP Packages
LTC3780	High Efficiency, Synchronous, 4-Switch Buck-Boost Converter	V_{IN} = 4V to 36V, V_{OUT} = 0.8V to 30V, I_Q = 1500µA, I_{SD} < 55µA , QFN Package
LTC3785	10V, High Efficiency, Synchronous, No R_{SENSE}™ Buck-Boost Controller	V_{IN} = 2.7V to 10V, V_{OUT} = 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA , QFN Package
LTC3101	Wide V_{IN}, Multi-Output DC/DC Converter and PowerPath™ Controller	V_{IN} = 1.8V to 5.5V, V_{OUT} = 1.5V to 5.25V, I_Q = 38µA, I_{SD} < 15µA , QFN Package
LTC3522	Synchronous 400mA Buck-Boost and 200mA Buck	V_{IN} = 2.4V to 5.5V, V_{OUT} = 2.2V to 5.25V, I_Q = 25µA, I_{SD} < 1µA , QFN Package
LTC3530	Wide Input Voltage Synchronous Buck-Boost DC/DC Converter	V_{IN} = 1.8V to 5.5V, V_{OUT} = 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA , DFN Package

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