

# FDS6162N7

## 20V N-Channel PowerTrench® MOSFET

### General Description

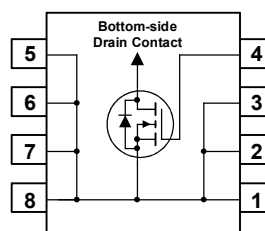
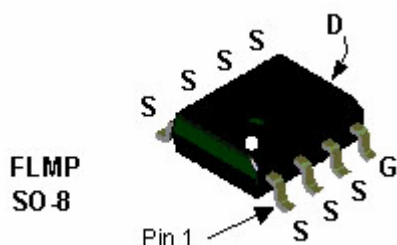
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low  $R_{DS(ON)}$  in a small package.

### Applications

- Synchronous rectifier
- DC/DC converter

### Features

- 23 A, 20 V  $R_{DS(ON)} = 3.5\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 5.0\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability
- Fast switching
- FLMP SO-8 package: Enhanced thermal performance in industry-standard package size



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a)	23	A
	– Pulsed	60	
$P_D$	Power Dissipation (Note 1a)	3.0	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6162N7	FDS6162N7	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 23\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 19\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 23\text{ A}, T_J = 125^\circ\text{C}$		2.9 3.6 4.1	3.5 5.0 6.2	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 23\text{ A}$		119		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		5521		pF
$C_{oss}$	Output Capacitance			1473		pF
$C_{riss}$	Reverse Transfer Capacitance			706		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.3		$\Omega$

### Switching Characteristics (Note 2)

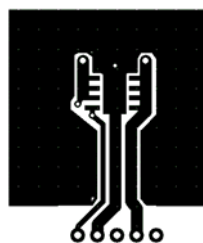
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		20	32	ns
$t_r$	Turn–On Rise Time			25	40	ns
$t_{d(off)}$	Turn–Off Delay Time			85	136	ns
$t_f$	Turn–Off Fall Time			55	88	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 23\text{ A},$ $V_{GS} = 4.5\text{ V}$		52	73	nC
$Q_{gs}$	Gate–Source Charge			9		nC
$Q_{gd}$	Gate–Drain Charge			14.5		nC

### Drain–Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			2.5	A	
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.5\text{ A}$ (Note 2)		0.6	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 23\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		42		nS
$Q_{rr}$	Diode Reverse Recovery Charge			52		nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $40^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $85^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

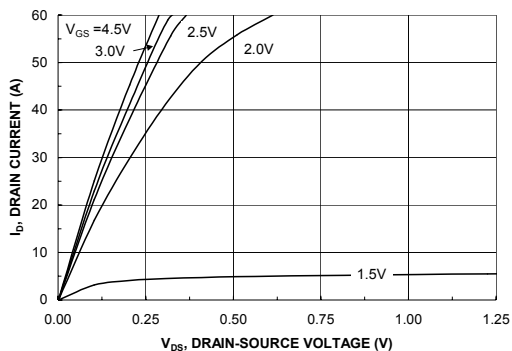


Figure 1. On-Region Characteristics.

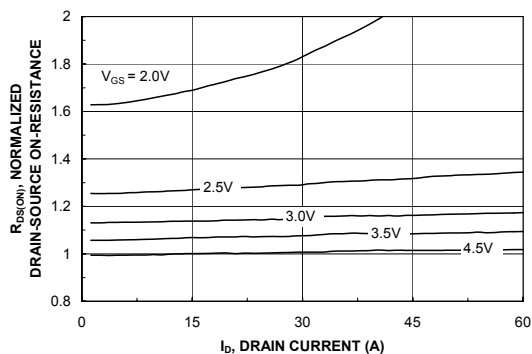


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

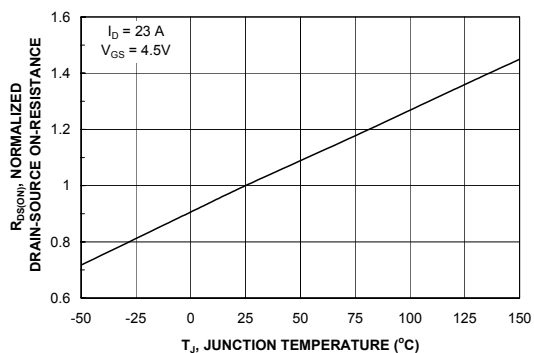


Figure 3. On-Resistance Variation with Temperature.

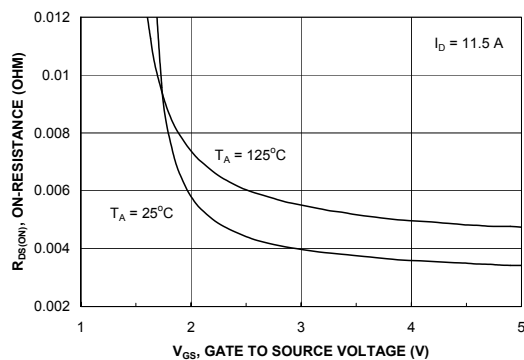


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

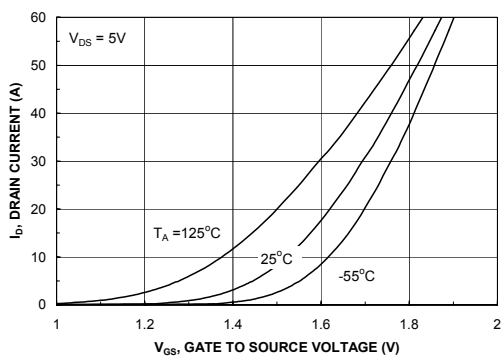


Figure 5. Transfer Characteristics.

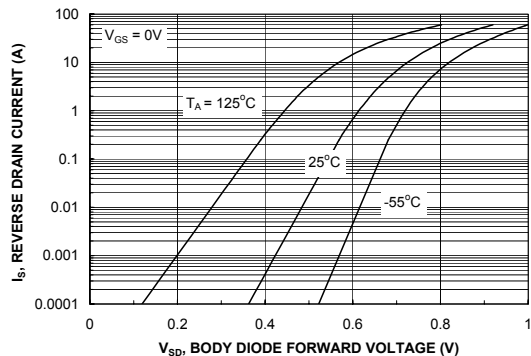
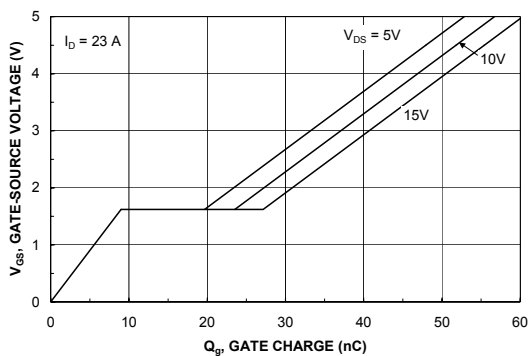
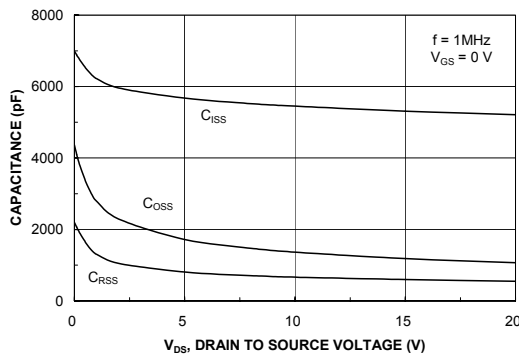


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

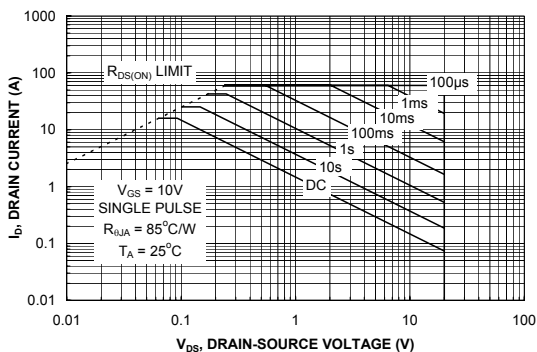
## Typical Characteristics



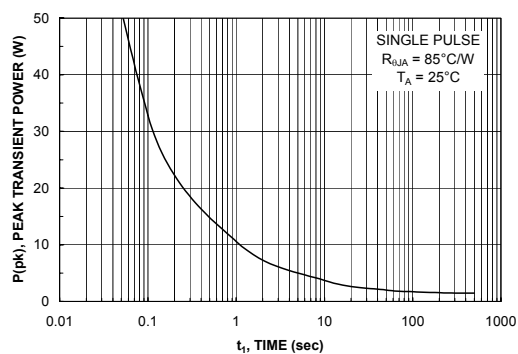
**Figure 7. Gate Charge Characteristics.**



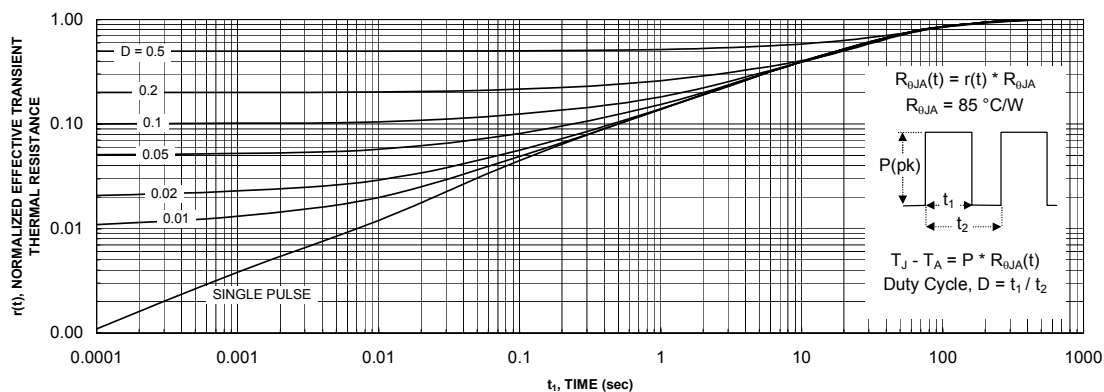
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



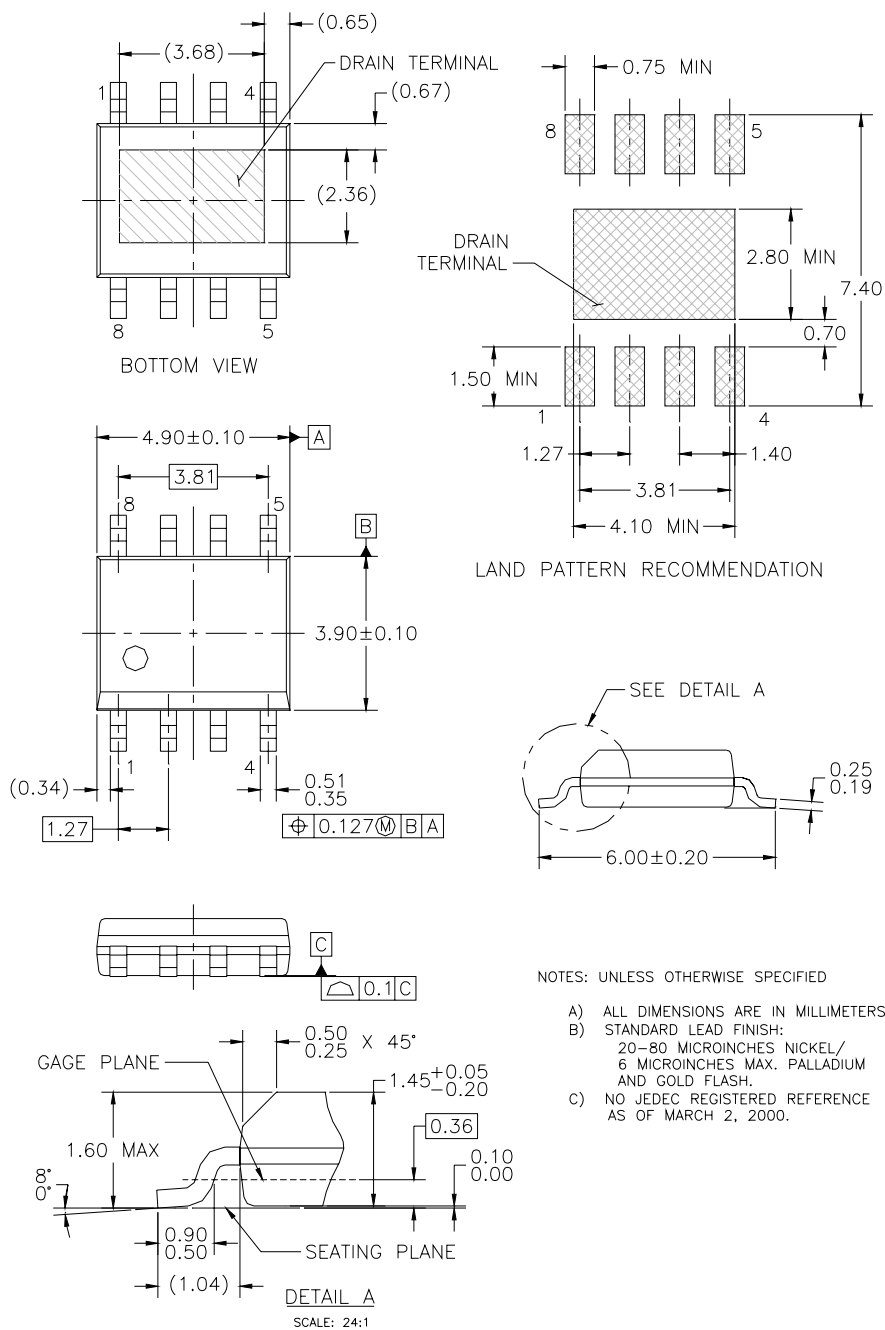
**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

## Dimensional Outline and Pad Layout



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CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
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