Evaluation Board for Transducer ADC

EVAL-AD7730EB

FEATURES

Operates from a Single +5V Supply

On-Board Reference and Digital Buffers

Various Linking Options

Direct Hook-Up to Printer Port of PC

PC Software for Control and Data Analysis

INTRODUCTION

This Application Note describes the evaluation board for the AD7730, Transducer ADC. The AD7730 is a complete analog front-end for weigh-scale and pressure measurement applications. The device accepts low-level signals directly from a transducer and outputs a serial digital word. The part features two buffered differential programmable gain analog inputs as well as a differential reference input. An on-chip 6-bit DAC allows the removal of TARE voltages. Clock signals for synchronizing ac excitation of the bridge are also provided. Full data on the AD7730 is available in the AD7730 data sheet available from Analog Devices and should be consulted in conjunction with this Application Note when using the Evaluation Board.

Included on the evaluation board, along with the AD7730, are an AD780, a +2.5 V ultra high precision bandgap reference, a 4.9152MHz crystal and digital buffers to buffer signals to and from the edge connectors.

Interfacing to this board is provided either through a 36-Way Centronics Connector or through a 9-way D-type connector. External sockets are provided for the analog inputs, an external reference input option and an external master clock option.

OPERATING THE AD7730 EVALUATION BOARD

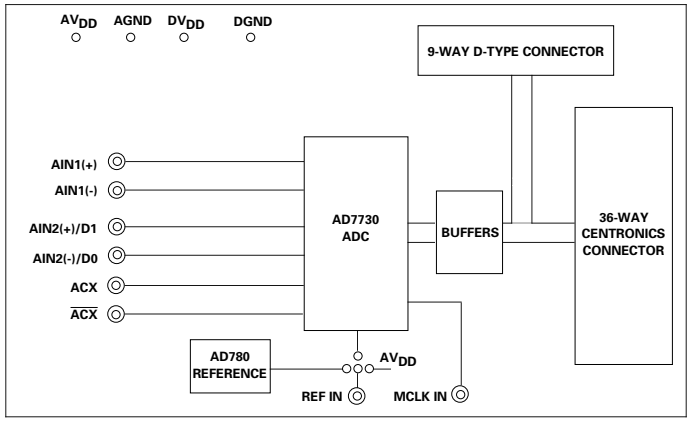
Power Supplies

The evaluation board has four power supply input pins: AV_{DD}, AGND, DV_{DD} and DGND. The AD7730 is specified with an AV_{DD} of +5V. Therefore, the AV_{DD} voltage supplied to the board must be +5V. This AV_{DD} voltage is also used to power the AD780 reference. To run the board from a single +5V supply, simply connect the AV_{DD} and DV_{DD} inputs together.

Both AGND and DGND inputs are provided on the board. AGND connects to the AD7730 AGND pin and also connects to the GND pin of the AD780. DGND connects to the DGND pin of the AD7730 and to the GND of the digital chips on the board. The AGND and DGND planes are connected at the AD7730. Therefore, it is recommended not to connect AGND and DGND elsewhere in the system to avoid ground loop problems. When using a single supply for both AV_{DD} and DV_{DD}, only one ground connection should be made to the board. This connection should be made to the board's AGND input terminal.

Both supplies are decoupled to their respective ground plane with 10µF tantalum and 0.1µF ceramic disc capacitors.

FUNCTIONAL BLOCK DIAGRAM



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Link Options

There are a number of link options on the evaluation board which should be set for the required operating setup before using the board. The functions of these link options are described in detail below.

Link No.	Function
LK1	This option selects the master clock option for the AD7730. The master clock source comes from the on-board crystal or from an external clock source via SKT11. This is a double link and both links must be moved together for correct operation. With both links in position A, the external clock option is selected and an externally applied clock to SKT 11 is routed to the MCLK IN pin of the AD7730. With both links in position B, the on-board crystal is selected and provides the master clock for the AD7730.
LK2	This link option is used to determine whether the AD7730 is in its normal operating mode or its $\overline{\text{STANDBY}}$ (power-down) mode. With this link in position A, the $\overline{\text{STANDBY}}$ input of the AD7730 is connected to a logic high thus configuring the part for normal operation. With this link in position B, the $\overline{\text{STANDBY}}$ input of the AD7730 is connected to a logic low and the AD7730 is placed in its power-down mode where its power dissipation is typically 100µW.
LK3	This link option is used to select the reference source for the AD7730's REF IN(-) input. With this link in position A, the REF IN(-) pin of the AD7730 is connected directly to AGND. With this link in position B, the REF IN(-) pin of the AD7730 is connected to SKT10. An external voltage connected to SKT10 can now be used for REF IN(-).
LK4	This link controls the polarity of the serial clock. With this link in position A, the POL pin of the AD7730 is connected to a logic high. With this input high, the first transition of the serial clock in a data transfer is from a high to a low. This link should be in position A when operating with the evaluation board software. With this link in position B, the POL pin of the AD7730 is connected to a logic low. With this input low, the first transition of the serial clock in a data transfer is from a low to a high.
LK5	This link option is used to select the reference source for the AD7730's REF IN(+) input. With this link in position A, the REF IN (+) pin of the AD7730 is connected directly to the output of the on-board reference, the AD780. With this link in position B, the REF IN (+) pin of the AD7730 is connected directly to AV_{DD}. With this link in position C, the REF IN(+) pin of the AD7730 is connected to SKT9. An external voltage connected to SKT9 can now be used for REF IN(+).
LK6	This link is in series with the $\overline{\text{ACX}}$ pin. With this link in place, SKT5 provides the $\overline{\text{ACX}}$ signal from the AD7730.
LK7	This link is in series with the ACX pin. With this link in place, SKT6 provides the ACX signal from the AD7730.
LK8	This link is in series with the AIN2(+)/D1 pin. With this link in place, SKT8 is connected directly to the AIN2(+)/D1 pin. This link may be removed so that an analog input signal at SKT8 can be connected to the component grid for signal conditioning before being applied to the AIN2(+) input of the AD7730.
LK9	This link is in series with the AIN2(-)/D0 pin. With this link in place, SKT7 is connected directly to the AIN2(-)/D0 pin. This link may be removed so that an analog input signal at SKT7 can be connected to the component grid for signal conditioning before being applied to the AIN2(-) input of the AD7730.

Link Options (ctnd)

Link No.	Function
LK10	This link is in series with the AIN1(+) analog input. With this link in place, the analog input on the SKT3 input is connected directly to the AIN1(+) input on the part. This link may be removed so that the input signal at SKT3 can be connected to the component grid for signal conditioning before being applied to the AIN1(+) input of the AD7730.
LK11	This link is in series with the AIN1(-) analog input. With this link in place, the analog input on the SKT4 input is connected directly to the AIN1(-) input on the part. This link may be removed so that the input signal at SKT4 can be connected to the component grid for signal conditioning before being applied to the AIN1(-) input of the AD7730.

Setup Conditions

Table I shows the position in which all the links are set when the evaluation board is sent out.

Table I. Initial Link Positions

Link No.	Position	Function.
LK1	B	Both links in position B to select the on-board crystal oscillator as the master clock for the board.
LK2	A	Normal Operating Mode.
LK3	A	REF IN(-) connected directly to AGND.
LK4	A	POL pin of AD7730 tied high.
LK5	B	REF IN(+) connected to the AV_{DD}.
LK6	IN	$\overline{ACX}$ connected to SKT5.
LK7	IN	ACX connected to SKT6.
LK8	IN	SKT8 connected to AIN2(+)/D1.
LK9	IN	SKT7 connected to AIN2(-)/D0.
LK10	IN	SKT3 connected to AIN1(+).
LK11	IN	SKT4 connected to AIN1(-).

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is either via a 9-way D-Type connector, SKT1, or a 36-way Centronics connector, SKT2. The pinout for the SKT1 connector is given in Figure 1 and its corresponding pin designations are given in Table II. The pinout for this SKT2 connector is shown in Figure 2 and its pin designations are given in Table III. The evaluation board should be powered up before a cable is connected to either of the connectors.

SKT2 is used to connect the evaluation board to the printer port (parallel port) of a PC. Connection between the two is direct via a standard parallel printer port cable. SKT1 is used to connect the evaluation board to any other system.

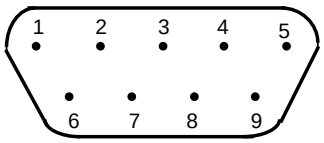

Figure 2. SKT1 Pin Configuration

Table II. SKT1 Pin Designations[1]

1	SCLK	Serial Clock. The signal on this pin is buffered before being applied to the SCLK pin of the AD7730.
2	$\overline{RDY}$	Logic Output. This is a buffered version of the signal on the AD7730's $\overline{DRDY}$ pin.
3	$\overline{CS}$	Chip Select. The signal on this pin is buffered before being applied to the $\overline{CS}$ pin of the AD7730.
4	$\overline{RESET}$	Reset Input. The signal on this pin is buffered before being applied to the $\overline{RESET}$ pin of the AD7730.
5	DIN	Serial Data Input. Data applied to this pin is buffered before being applied to the AD7730's DIN pin.
6	DGND	Ground reference point for digital circuitry. Connects to the DGND plane on the evaluation board.
7	DOUT	Serial Data Output. This is a buffered version of the signal on the AD7730's DOUT pin.
8	DV_{DD}	Digital Supply Voltage. The DV_{DD} voltage for the evaluation board can be supplied via this pin provided no voltage is applied to the main DV_{DD} terminal.
9	NC	No Connect. The signal on this pin is buffered before being applied to the $\overline{SYNC}$ pin of the AD7730.

NOTE

[1]An explanation of the AD7730 functions mentioned here is given in Table III as part of the SKT2 pin designations description.

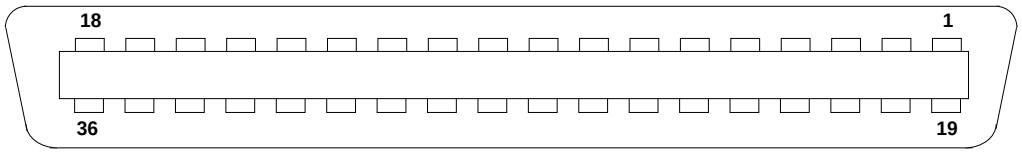

Figure 3. SKT2 Pin Configuration

Table III. SKT2 Pin Designations

1	NC	No Connect. This pin is not connected on the evaluation board.
2	DIN	Serial Data Input. Data applied to this pin is buffered before being applied to the AD7730's DIN pin. The serial data applied to the DIN pin is written to the input shift register on the part. Data from this input shift register is transferred to one of the on-chip registers depending on the register selection bits of the Communications Register.
3	$\overline{\text{RESET}}$	Reset Input. The signal on this pin is buffered before being applied to the $\overline{\text{RESET}}$ pin of the AD7730. $\overline{\text{RESET}}$ is an active low input which resets the control logic, interface logic, calibration coefficients, digital filter and all on-chip registers to power-on status.
4	$\overline{\text{CS}}$	Chip Select. The signal on this pin is buffered before being applied to the $\overline{\text{CS}}$ pin of the AD7730. $\overline{\text{CS}}$ is an active low logic input used to select the AD7730. With this input hard-wired low, the AD7730 operates in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{\text{CS}}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronisation signal in communicating with the AD7730.
5	SCLK	Serial Clock. The signal on this pin is buffered before being applied to the SCLK pin of the AD7730. An external serial clock is applied to this input to access serial data from the AD7730. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a non-continuous clock with the information being transmitted to the AD7730 in smaller batches of data.
6	$\overline{\text{SYNC}}$	Logic Input. The signal on this pin is buffered before being applied to the $\overline{\text{SYNC}}$ pin of the AD7730. The $\overline{\text{SYNC}}$ input allows for synchronisation of the digital filters and analog modulators across a number of AD7730s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset and the analog modulator is also held in its reset state.
7-8	NC	No Connect. These pins are not connected on the evaluation board.
9	DV_{DD}	Digital Supply Voltage. This provides the supply voltage for IC4, the buffer chip which buffers the output signals from the AD7730 before they are applied to SKT2.
10	$\overline{\text{RDY}}$	Logic output. This is a buffered version of the signal on the AD7730's $\overline{\text{RDY}}$ pin. $\overline{\text{RDY}}$ is used as a status output in both conversion and calibration mode. In conversion mode, a logic low on the $\overline{\text{RDY}}$ output indicates that a new output word is available from the AD7730 data register. The $\overline{\text{RDY}}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place after an output update, the $\overline{\text{RDY}}$ line will return high prior to the next output update, remain high while the update is taking place and return low again. This gives an indication of when a read operation should not be initiated to avoid reading from the data register as it is being updated. In calibration mode, $\overline{\text{RDY}}$ goes high when calibration is initiated and returns low to indicate that calibration is complete.
11-12	NC	No Connect. These pins are not connected on the evaluation board.
13	DOUT	Serial Data Output. This is a buffered version of the signal on the AD7730's DOUT pin. Serial data from the output shift register on the part is clocked out on this pin. This output shift register contains information from one of the nine on-chip registers depending on the register selection bits of the Communications Register.
14-18	NC	No Connect. These pins are not connected on the evaluation board.
19-30	DGND	Ground reference point for digital circuitry. Connects to the DGND plane on the evaluation board.
31-36	NC	No Connect. These pins are not connected on the evaluation board.

SOCKETS

There are eleven sockets on the AD7730 evaluation board. The function of these sockets is outlined in Table IV.

Table IV. Socket Functions

Socket	Function
SKT1	9-Way D-Type Connector which can be used for digital interfacing to the evaluation board.
SKT2	36-Way Centronics Connector which can be used for digital interfacing to the evaluation board. This connector should be used when connecting the board to the parallel printer port of the PC to use the evaluation software.
SKT3	Sub-Minature BNC (SMB) Connector. The analog input signal for the AIN1(+) input of the AD7730 is applied to this socket.
SKT4	Sub-Minature BNC (SMB) Connector. The analog input signal for the AIN1(-) input of the AD7730 is applied to this socket.
SKT5	Sub-Minature BNC (SMB) Connector. This socket provides the $\overline{ACX}$ ouput from the AD7730.
SKT6	Sub-Minature BNC (SMB) Connector. This socket provides the ACX ouput from the AD7730.
SKT7	Sub-Minature BNC (SMB) Connector. Connects to the AIN2(-)/D0 pin of the AD7730.
SKT8	Sub-Minature BNC (SMB) Connector. Connects to the AIN2(+)/D1 pin of the AD7730.
SKT9	Sub-Minature BNC (SMB) Connector. The reference voltage for the REF IN(+) input of the AD7730 is applied to this socket when the board is configured for an externally-applied reference voltage.
SKT10	Sub-Minature BNC (SMB) Connector. The reference voltage for the REF IN(-) input of the AD7730 is applied to this socket when the board is configured for an externally-applied reference voltage.
SKT11	Sub-Minature BNC (SMB) Connector. The master clock signal for the MCLK IN input of the AD7730 is applied to this socket when the board is configured for an externally-applied master clock..

RUNNING THE AD7730 INTERFACE SOFTWARE

Included in the evaluation board package is a PC-compatible disk which contains software for controlling and evaluating the performance of the AD7730 using the printer port of a PC. There are a total of thirteen files on the distribution disk.

To use the software, the user must have an IBM-compatible PC and Windows 3.1 must be installed. Start Windows and, using either the RUN command or the File Manager, start the program called SETUP.EXE on the distribution disk. This automatically installs the application and sets up a window called ANALOG DEVICES. The application ICON is found here. To start the application, double click on the ICON.

When the program starts, the user is asked to select a printer port. The correct selection depends on what type of computer is being used (Desktop, Laptop etc). LPT1 works for most machines. When using a Compaq laptop, select PRN. A different port can be selected at any time from the MAIN MENU.

After selecting the printer port, the program displays the Main Menu as outlined in Figure 4. There are a number of buttons on the Main Menu which select a variety of different functions. These are described below.

Program AD7730

Pressing this button calls up a second screen which displays the contents of the Status Register and provides another set of buttons allowing the user to program the on-chip registers. Figure 5 shows the "Program AD7730" screen. Pressing any of the buttons on this screen pulls up a further screen allowing all functions in a register to be programmed. Figure 6 gives an example of one of these screens (the screen for programming the Mode Register).

Read Data

The Read Data button allows the user access to the "read data" screen. On this screen, the user can choose whether the reading of data is for noise analysis or simply for display. It also allows the user to choose how many outputs of the AD7730 should be read for the noise analysis routines.

Noise Analysis

The Noise Analysis button gives the user access to the "noise analysis" screen. Here the user can look at the results of a data read in terms of rms code distribution, code spread etc. The user also has the facility to plot the data versus time and plot histogram results.

Reset AD7730

Pressing this button allows the user access to the reset menu where either a hardware reset (via the $\overline{RESET}$ pin) or an software/interface reset (via writing 32 1's) can be selected. The user also has a hardware reset button on the board.

Read from File
Pressing this button allows the user to read data from a file for noise analysis. The data to be read can either be in decimal or hexadecimal format.

Write to File
This button allows the user to store of output data from the AD7730 to a file in either decimal or hexadecimal format. This data can be used in other programs or can subsequently be read back to the AD7730 software.

Select Printer Port
This button allows the user to select the printer port to which the AD7730 evaluation is connected.

About
This provides details of the software revision.

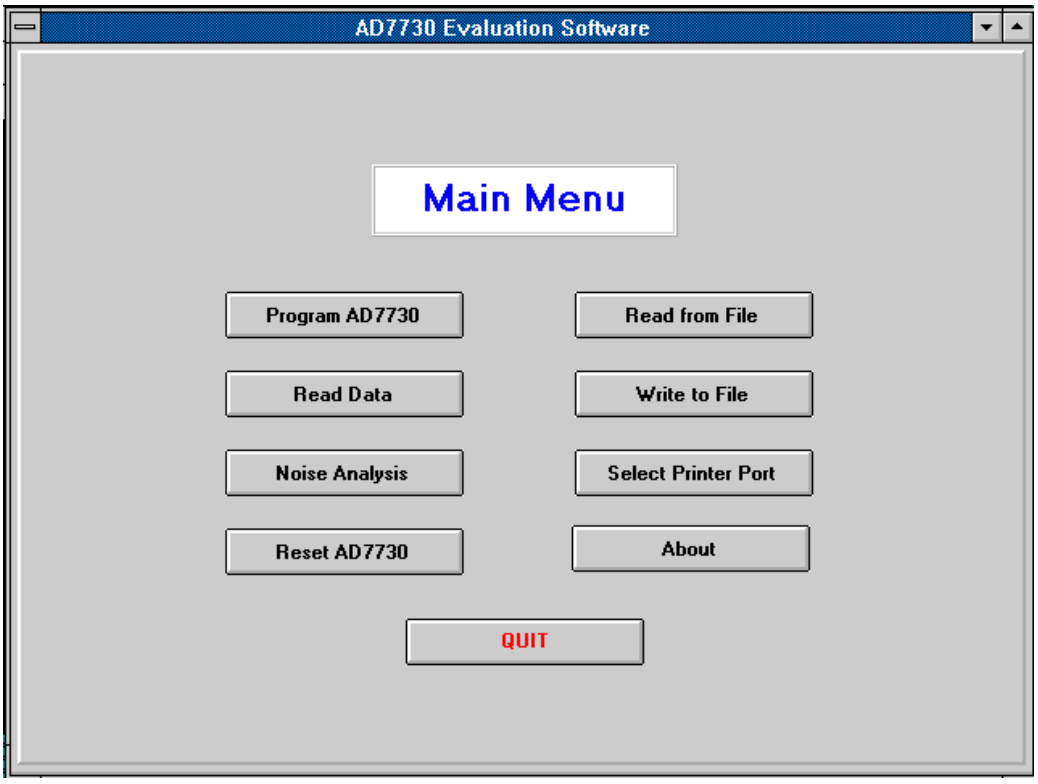

Figure 4. Main Screen

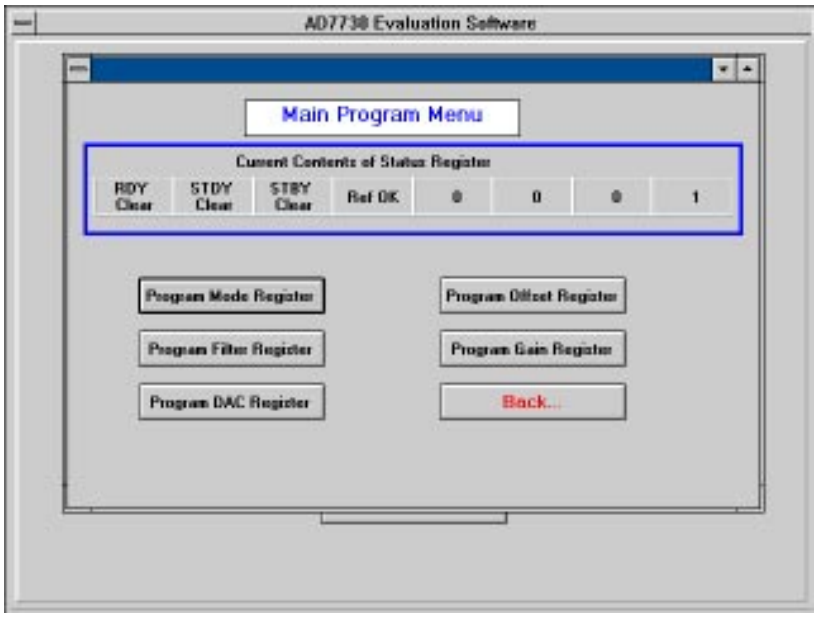

Figure 5. Program Screen

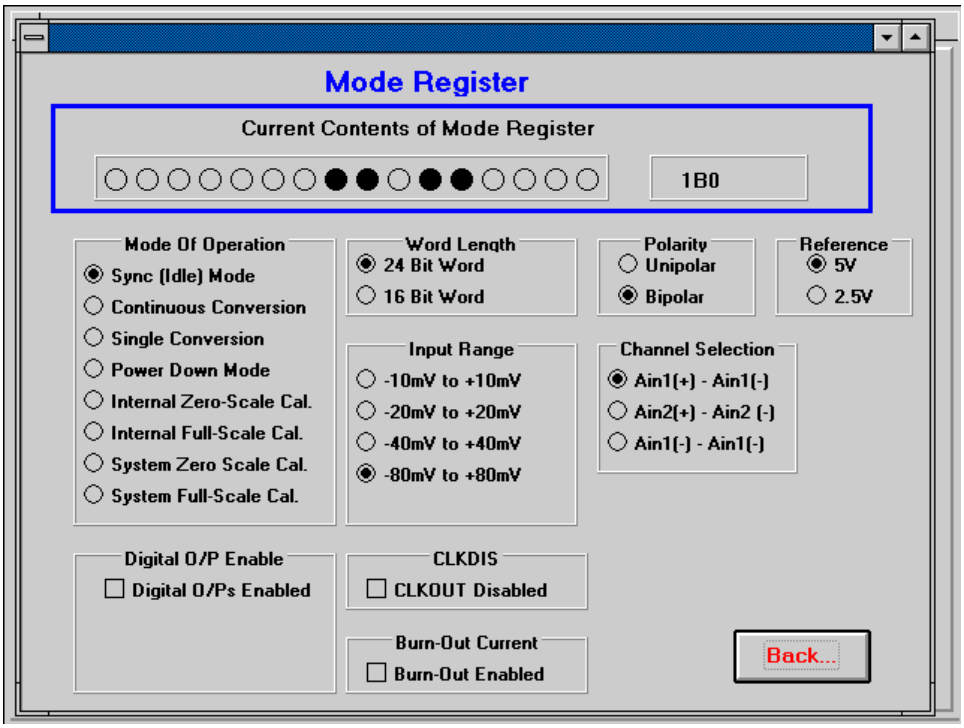

Figure 6. Mode Register Screen

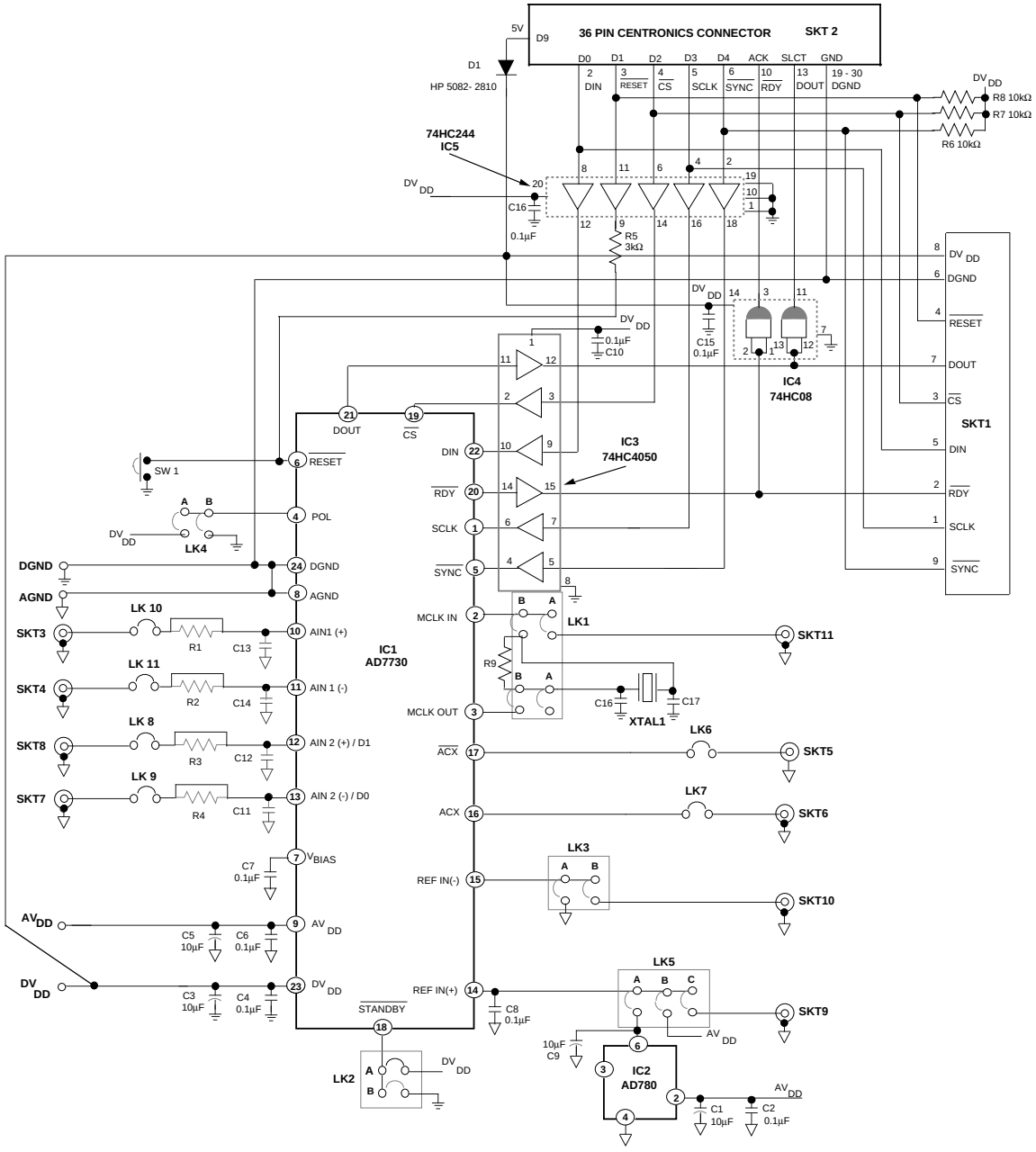

Figure 7. Evaluation Board Circuit Diagram