Secondary-Side Opto-Coupler Driver

FEATURES

- **600mV Reference (1.25% Over Temperature)**
- **Wide Input Supply Range: 3V to 20V**
- **Overshoot Control Function Prevents Output Overshoot on Start-Up and Short-Circuit Recovery**
- High Bandwidth Error Amplifier Permits Simple Loop Frequency Compensation
- Ground-Referenced Opto-Coupler Drive
- 10mA Opto-Coupler Drive with Current Limiting
- Low Profile (1mm) ThinSOT™ Package

APPLICATIONS

- 48V Input Isolated DC/DC Converters
- Isolated Telecommunication Power Systems
- Distributed Power Step-Down Converters
- Offline Isolated Power Supplies
- Industrial Control Systems
- Automotive and Heavy Equipment

DESCRIPTION

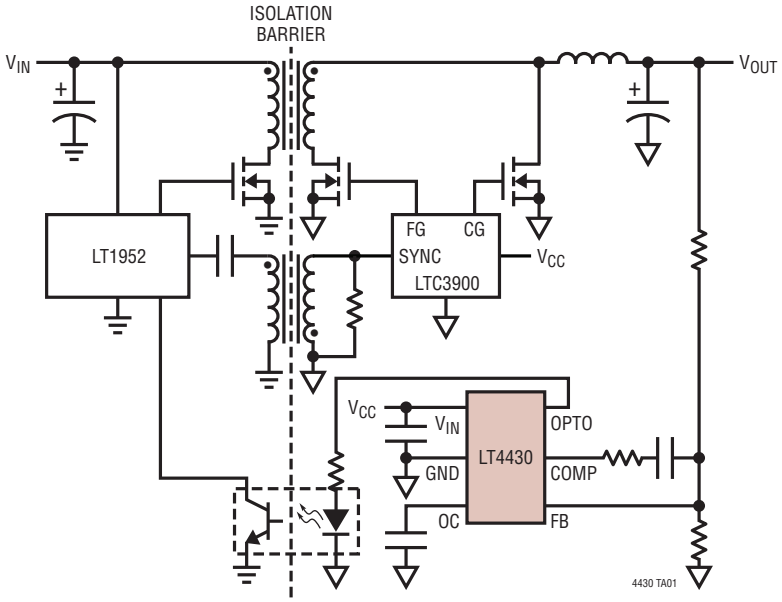
The LT®4430 drives the opto-coupler that crosses the galvanic barrier in an isolated power supply. The IC contains a precision-trimmed reference, a high bandwidth error amplifier, an inverting gain of 6 stage to drive the opto-coupler and unique overshoot control circuitry.

The LT4430's 600mV reference provides ±0.75% initial accuracy and ±1.25% tolerance over temperature. A high bandwidth 9MHz error amplifier permits simple frequency compensation and negligible phase shift at typical loop crossover frequencies. The opto-coupler driver provides 10mA of output current and is short-circuit protected. A unique overshoot control function prevents output overshoot on start-up and short-circuit recovery with a single capacitor.

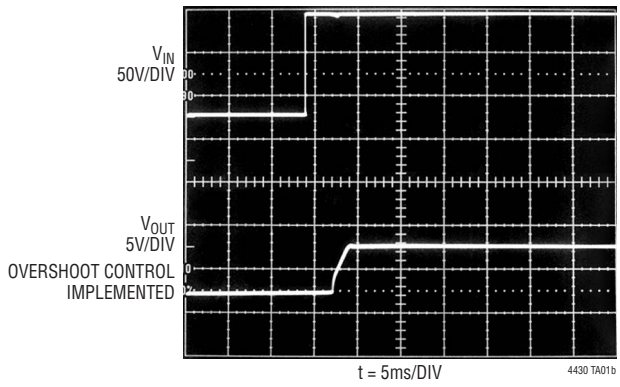
The LT4430 is available in the low profile 6-lead TSOT-23 package.

TYPICAL APPLICATION

Simplified Isolated Synchronous Forward Converter



Isolated Flyback Telecom Converter Start-Up with Overshoot Control (See Schematic on Back Page)



ABSOLUTE MAXIMUM RATINGS

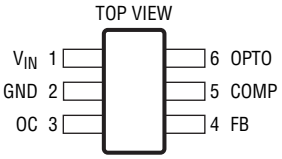
(Note 1)

Supply Voltage
- V_{IN} 20V

FB Voltage ..... –0.3V to 6V
OPTO Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 2)
- E-, I-Grades ..... –40°C to 125°C
- H-Grade ..... –40°C to 150°C
- MP-Grade ..... –55°C to 150°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4430ES6#PBF	LT4430ES6#TRPBF	LTBFY	6-Lead Plastic TSOT-23	–40°C to 125°C
LT4430IS6#PBF	LT4430IS6#TRPBF	LTBFY	6-Lead Plastic TSOT-23	–40°C to 125°C
LT4430HS6#PBF	LT4430HS6#TRPBF	LTBFY	6-Lead Plastic TSOT-23	–40°C to 150°C
LT4430MPS6#PBF	LT4430MPS6#TRPBF	LTBFY	6-Lead Plastic TSOT-23	–55°C to 150°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT4430ES6	LT4430ES6#TR	LTBFY	6-Lead Plastic TSOT-23	–40°C to 125°C
LT4430IS6	LT4430IS6#TR	LTBFY	6-Lead Plastic TSOT-23	–40°C to 125°C
LT4430HS6	LT4430HS6#TR	LTBFY	6-Lead Plastic TSOT-23	–40°C to 150°C
LT4430MPS6	LT4430MPS6#TR	LTBFY	6-Lead Plastic TSOT-23	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, FB = V_{FB}, COMP = 1V, unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	3		20	V
I_{IN}	Supply Current	3V ≤ V_{IN} ≤ 20V (E-, I-Grades) 3V ≤ V_{IN} ≤ 20V (H-, MP-Grades)	● 		1.9 1.9	3.9 4.3	mA mA
V_{UVLO}	Undervoltage Lockout Threshold	OC Held Low for V_{IN} < V_{UVLO} (E-, I-Grades) OC Held Low for V_{IN} < V_{UVLO} (H-Grade) OC Held Low for V_{IN} < V_{UVLO} (MP-Grade)	● ● ●	1.95 1.9 1.9	2.2 2.2 2.2	2.5 2.5 2.55	V V V
V_{FB}	Feedback Reference Voltage	 3V ≤ V_{IN} ≤ 20V	 ●	0.5955 0.5925	0.6 0.6	0.6045 0.6075	V V
	V_{FB} Line Regulation	3V ≤ V_{IN} ≤ 20V			0.02	0.1	%
I_{FB}	FB Input Bias Current	FB = V_{FB}		–150	–75		nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, FB = V_{FB}, COMP = 1V, unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OC}	Overshoot Control Charging Current	V_{OC} = 0V (E-, I-Grades) V_{OC} = 0V (H-Grade) V_{OC} = 0V (MP-Grade)	● ● ●	–15 –17 –17	–8.5 –8.5 –8.5	–5 –5 –4	µA µA µA
	OC Clamp Voltage				0.93		V
	OC Amplifier Offset Voltage	FB = 0.3V			48		mV
A_{VOL}	Error Amplifier Open-Loop DC Gain	V_{COMP} = 0.8V to 1V (E-, I-Grades) V_{COMP} = 0.8V to 1V (H-, MP-Grades)	● ●	60 55	80 80		dB dB
	Error Amplifier Unity-Gain Bandwidth	No Load (Note 4)			9		MHz
	Error Amplifier Output Swing Low	FB = 1V	●	0.1	0.35	0.55	V
	Error Amplifier Output Swing High	FB = 0V (E-, I-Grades) FB = 0V (H-Grade) FB = 0V (MP-Grade)	● ● ●	1.2 1.2 1.15	1.33 1.33 1.33	1.5 1.55 1.55	V V V
	Error Amplifier Output Source Current	FB = 0V, COMP = 1V (E-, I-Grades) FB = 0V, COMP = 1V (H-Grade) FB = 0V, COMP = 1V (MP-Grade)	● ● ●	–800 –825 –825	–450 –450 –450	–225 –225 –200	µA µA µA
	Error Amplifier Output Sink Current	FB = 1V, COMP = 1V			25		mA
	Opto Driver Inverting DC Gain			–6.4	–6	–5.6	V/V
	Opto Driver –3dB Bandwidth	No Load (Note 4)			600		kHz
	Opto Driver Output Swing Low	FB = 0V, COMP = Open (E-, I-Grades) FB = 0V, COMP = Open (H-, MP-Grades)	● ●		0.5 0.5	0.85 0.9	V V
	Opto Driver Output Swing High	V_{IN} = 3V, FB = 1V, COMP = Open, I_{OPTO} = 10mA (E-, I-, H-Grades) V_{IN} = 3V, FB = 1V, COMP = Open, I_{OPTO} = 10mA (MP-Grade)	● ●	V_{IN} – 1.25 V_{IN} – 1.3	V_{IN} – 1.05 V_{IN} – 1.05		V V
	Opto Driver Output Swing High	V_{IN} = 20V, FB = 1V, COMP = Open, I_{OPTO} = 10mA	●	4.2	5.6	7.5	V
I_{SC}	Opto Driver Output Short-Circuit Current (Sourcing)	FB = 1V, COMP = Open, OPTO = 0V (E-, I-, H-Grades) FB = 1V, COMP = Open, OPTO = 0V (MP-Grade)	● ●	10.5 9.5	22 22	45 45	mA mA
	Opto Driver Output Sink Current	FB = 0V, OPTO = 1.5V (E-, I-, H-Grades) FB = 0V, OPTO = 1.5V (MP-Grade)	● ●	150 135	350 350	650 650	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

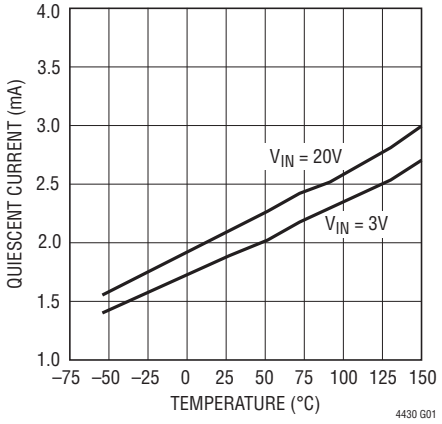
Note 2: The LT4430 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT4430E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT4430I is guaranteed over the –40°C to 125°C operating junction temperature range, the LT4430H is guaranteed over the –40°C to 150°C operating junction temperature range and the LT4430MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

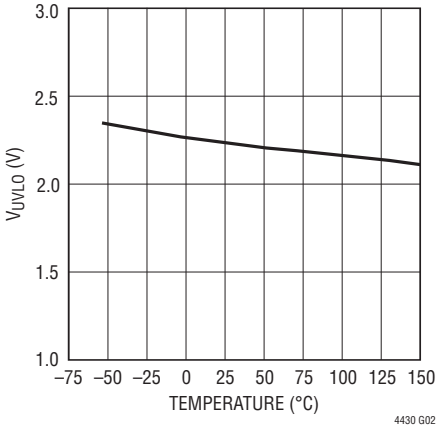
Note 4: This parameter is guaranteed by correlation and is not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

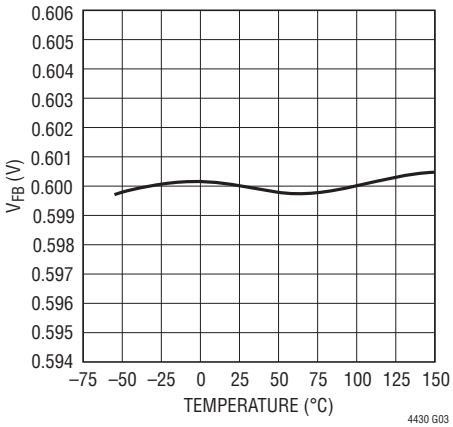
Quiescent Current vs Temperature



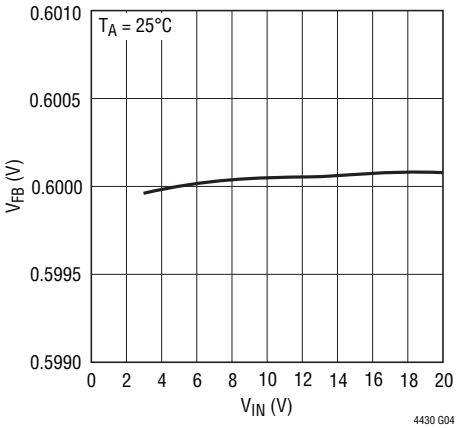
Undervoltage Lockout Threshold vs Temperature



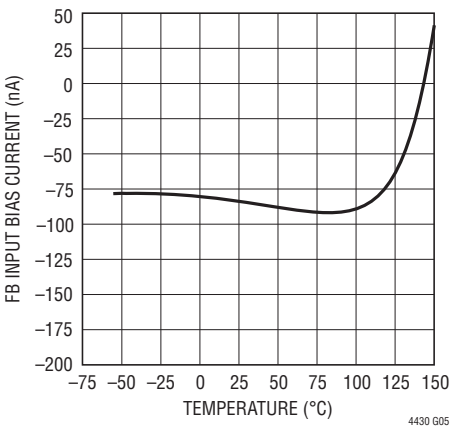
Feedback Reference Voltage vs Temperature



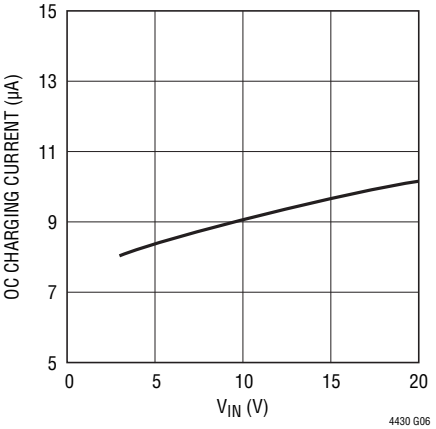
FB Voltage Line Regulation



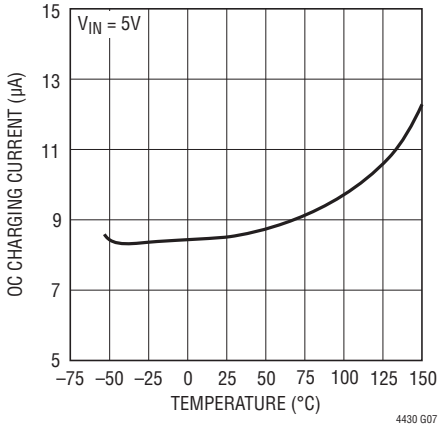
FB Input Bias Current vs Temperature



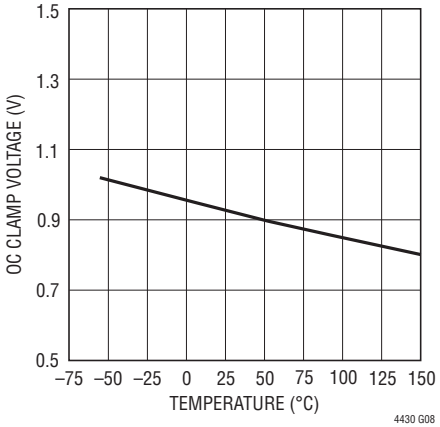
OC Charging Current vs Input Voltage



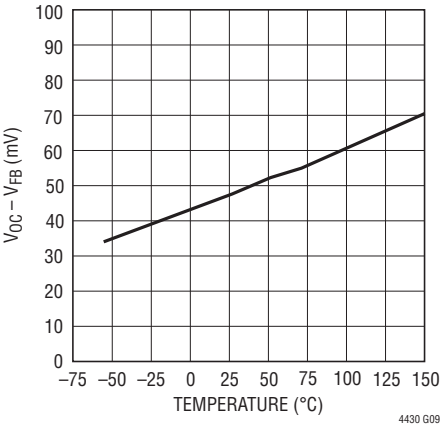
OC Charging Current vs Temperature



OC Clamp Voltage vs Temperature

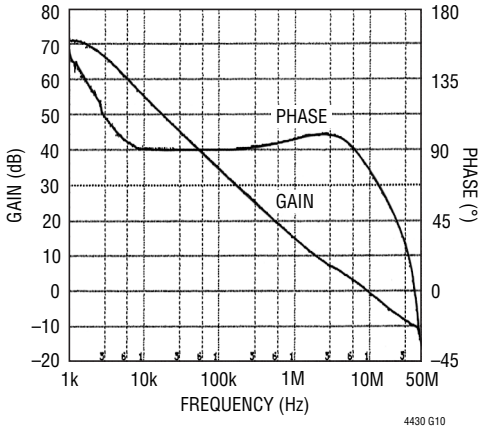


OC Amplifier Offset Voltage vs Temperature

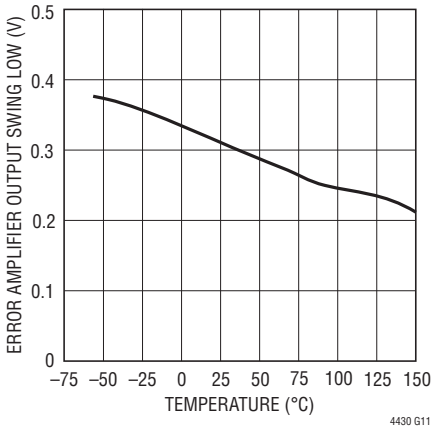


TYPICAL PERFORMANCE CHARACTERISTICS

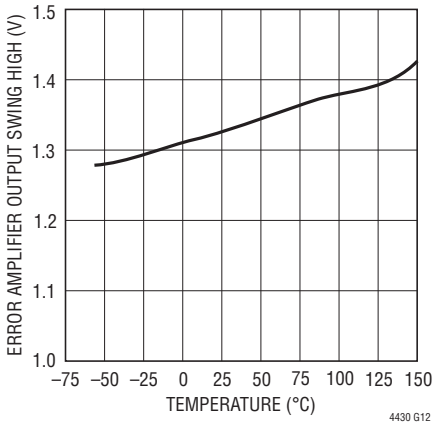
Error Amplifier Open Loop Gain and Phase vs Frequency



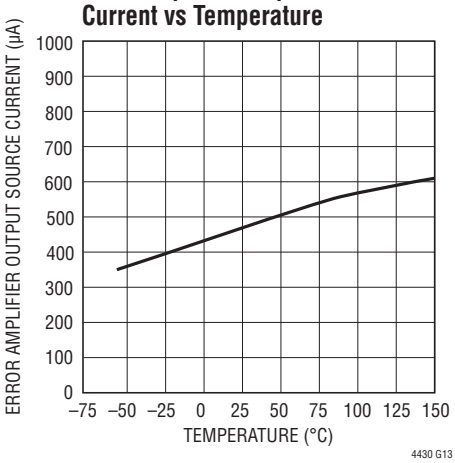
Error Amplifier Output Swing Low vs Temperature



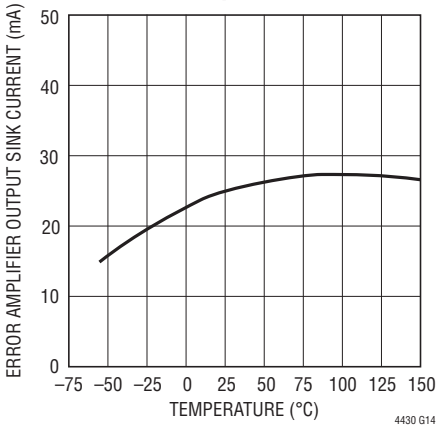
Error Amplifier Output Swing High vs Temperature



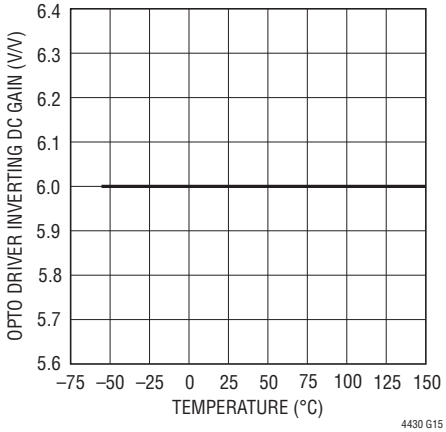
Error Amplifier Output Source Current vs Temperature



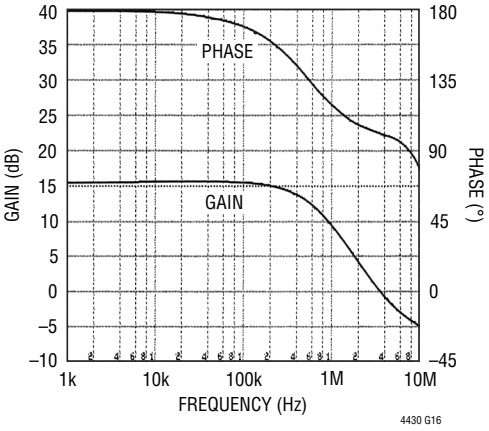
Error Amplifier Output Sink Current vs Temperature



Opto Driver Inverting DC Gain vs Temperature

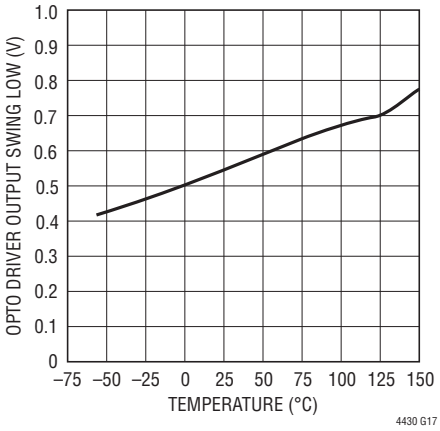


Opto Driver Inverting Closed Loop Gain and Phase vs Frequency

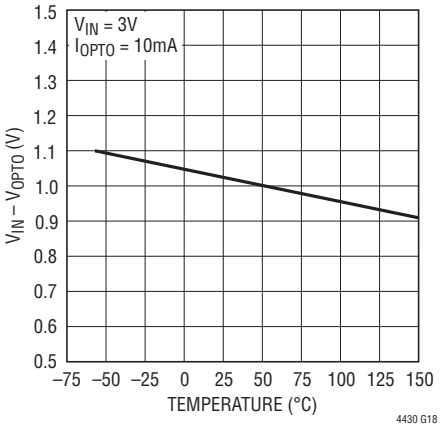


TYPICAL PERFORMANCE CHARACTERISTICS

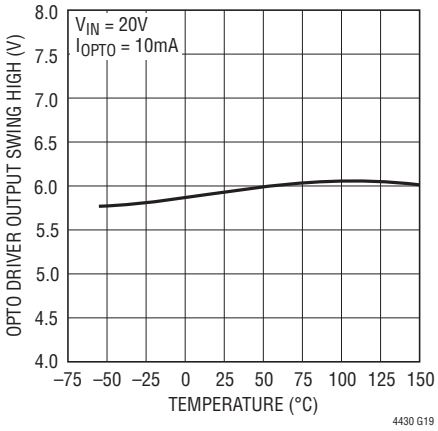
Opto Driver Output Swing Low vs Temperature



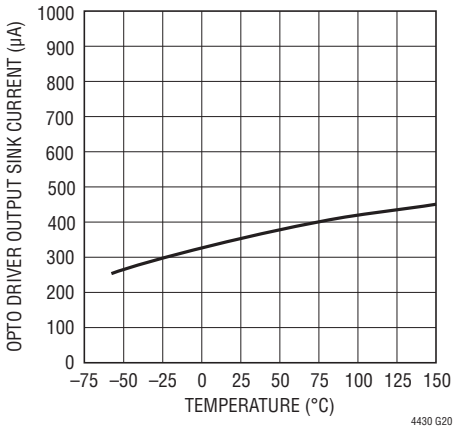
Opto Driver Output Swing High vs Temperature



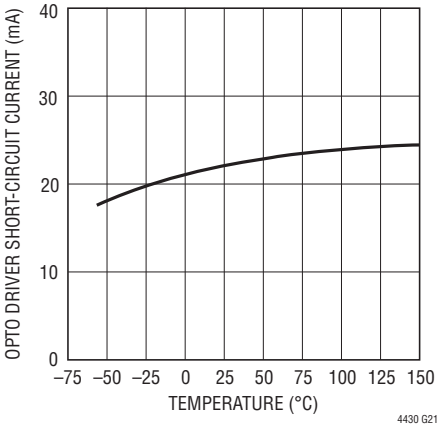
Opto Driver Output Swing High vs Temperature



Opto Driver Output Sink Current vs Temperature



Opto Driver Output Short-Circuit Current (Sourcing) vs Temperature



PIN FUNCTIONS

V_{IN} (Pin 1): This is the input supply that powers all internal circuitry. The input supply range is 3V minimum to 20V maximum and the typical input quiescent current is 1.9mA. Connect a 1µF bypass capacitor directly from V_{IN} to GND.

GND (Pin 2): Analog Ground Pin. It is also the negative sense terminal for the internal 0.6V reference. Connect the external feedback divider network that terminates to ground directly to this pin for best regulation and performance.

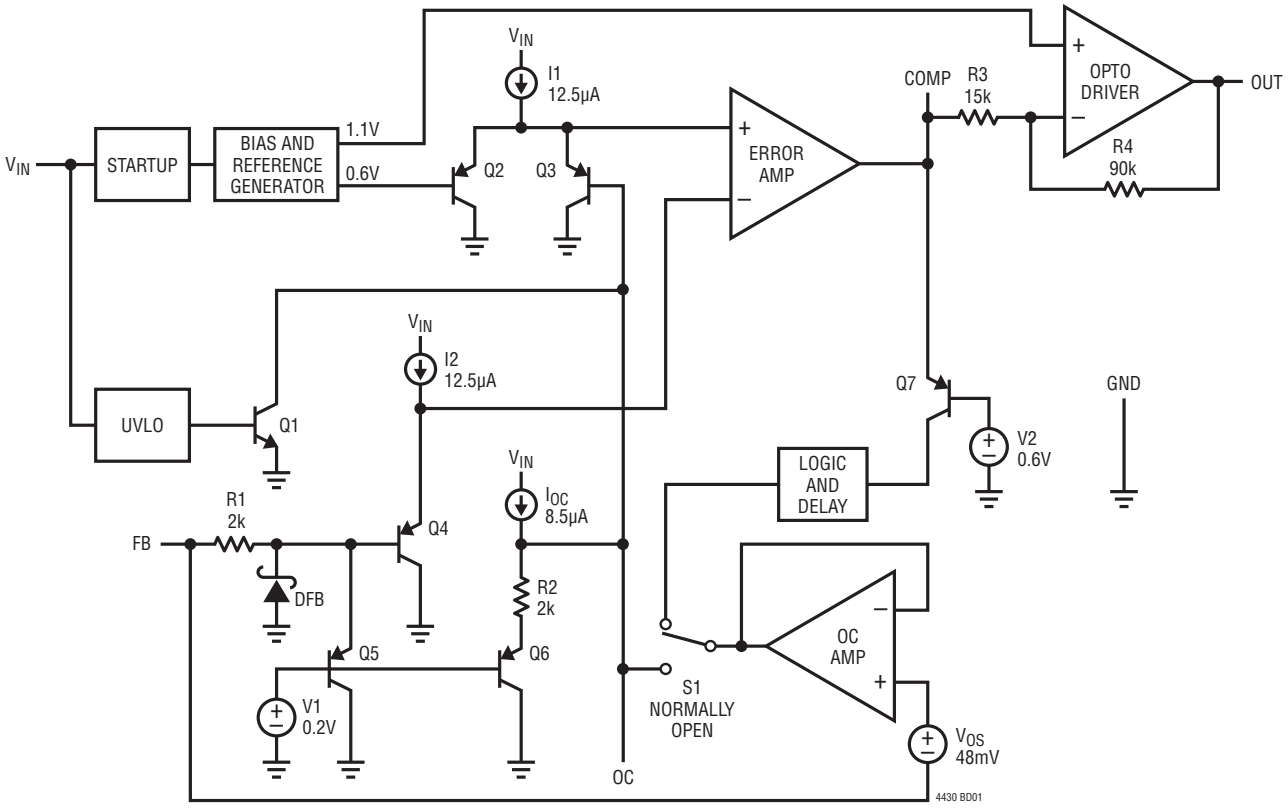
OC (Pin 3): Overshoot Control Pin. A typical 8.5µA current source and a capacitor placed from this pin to GND controls output voltage overshoot on start-up and recovery from short-circuit. The typical ramp time is (C_{OC} • 0.6V)/8.5µA. If V_{IN} is below V_{UVLO} (its undervoltage lockout threshold), the OC pin is actively held low. The OC pin also ties to the overshoot control amplifier output. This amplifier monitors the FB pin voltage and the error amplifier output. If FB is low due to a short-circuit fault condition, the COMP pin goes high. Logic detects the error amplifier COMP pin high state and activates the overshoot control amplifier. The amplifier responds by discharging the OC capacitor down to the FB voltage plus a built-in offset voltage of 48mV. If the short-circuit condition persists, the amplifier maintains the voltage on OC. If the short-circuit condition goes away, the FB pin recovers under the control of the OC pin.

FB (Pin 4): This is the inverting input of the error amplifier. The noninverting input is tied to the internal 0.6V reference. Input bias current for this pin is typically 75nA flowing out of the pin. This pin normally ties to a resistor divider network to set output voltage. Tie the top of the external resistor divider directly to the output voltage for best regulation performance.

COMP (Pin 5): This is the output of the error amplifier. The error amplifier is a true voltage-mode error amplifier and frequency compensation is performed around the amplifier. Typical LT4430 compensation schemes use series R-C in parallel with C networks from the COMP pin to the FB pin. COMP also ties to the overshoot control amplifier logic that detects if the COMP pin is at its high clamp level. The logic activates the overshoot control amplifier if COMP is at its clamp level for longer than 1µs.

OPTO (Pin 6): This is the output of the amplifier that drives the opto-coupler. The opto driver amplifier uses an inverting gain of six configuration to drive the opto-coupler referenced to ground. Driving the opto-coupler referenced to GND accommodates low output voltages and eases loop frequency compensation as the secondary feedback path with a traditional “431” topology is eliminated. The opto driver amplifier sources a maximum of 10mA, sinks 350µA typically and is short-circuit protected.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Block Diagram Operation

A precision voltage reference, a high-bandwidth error amplifier, an inverting opto-coupler driver and an overshoot control amplifier comprise the LT4430. Referring to the block diagram, a start-up circuit establishes all internal current and voltage biasing for the IC. A precision-trimmed bandgap generates the 600mV reference voltage and a 1.1V bias voltage for the opto-coupler driver. Room temperature reference voltage accuracy is specified at ±0.75% and operating temperature range tolerance is specified at ±1.25%. The 600mV reference ties to the noninverting input of the error amplifier.

The LT4430 error amplifier senses the output voltage through an external resistor divider and regulates the FB pin to 600mV. The FB pin ties to the inverting input of the error amplifier. The error amplifier's open loop DC gain is 80dB and its unity-gain crossover frequency of 9MHz provides negligible phase shift at typical feedback loop crossover frequencies. The error amplifier is a true voltage-mode amplifier and frequency compensation connects around the amplifier. Typical LT4430 compensation schemes use series R-C in parallel with C networks from the COMP pin to the FB pin.

The opto-coupler driver amplifies the voltage difference between the COMP pin and the 1.1V bias potential applied to its noninverting terminal with an inverting gain of 6. This signal drives the opto-coupler referenced to GND. Driving the opto-coupler referenced to GND accommodates low output voltages and simplifies loop frequency compensation as the secondary feedback path with a traditional "431" topology is eliminated. A resistor in series with the opto-coupler sets the opto-coupler's DC bias current. The opto driver amplifier sources a guaranteed maximum of 10mA, sinks 350µA typically and is short-circuit protected. The opto-coupler driver amplifier's typical –3dB bandwidth is 600kHz. The opto-coupler's output crosses the galvanic isolation barrier and closes the feedback loop to the primary-side controller.

The LT4430 incorporates a unique overshoot control function that allows the user to ramp the output voltage on start-up and recovery from short-circuit conditions, preventing overshoot. A capacitor, connected from the OC pin to GND and charged by internal 8.5µA current source I_{OC}, sets the ramp rate. On start-up, Q1 actively holds the OC capacitor low until V_{IN} of the LT4430 reaches its typical undervoltage lockout threshold of 2.2V. Q1 then turns off and the OC capacitor charges linearly. Q2 and Q3 OR the OC pin voltage and the 600mV reference voltage at the noninverting terminal of the error amplifier. The OC pin voltage is the reference voltage for the error amplifier until it increases above 600mV. If the feedback loop is in control, the FB pin voltage follows and regulates to the OC pin voltage. As the OC pin voltage increases past 600mV, the reference voltage takes control of the error amplifier and the FB pin regulates to 600mV. The OC pin voltage increases until it is internally clamped by R2, Q6 and V1. The OC pin's typical clamp voltage of 0.93V ensures that Q3 turns off. All of I1's current flows in Q2, matching I2's current in Q4.

In a short-circuit condition, the output voltage decreases to something well below the regulated level. The error amplifier reacts by increasing the COMP pin voltage, thereby decreasing the drive to the opto-coupler. The decreased opto-coupler bias signals the primary-side controller to increase the amount of power it delivers in an attempt to raise the output voltage back to its regulated value. As long as the fault persists, the output voltage remains low. The error amplifier's COMP pin voltage increases until it reaches a clamp level set by Q7 and V2. Q7's resultant collector current drives internal logic that closes normally open switch S1. This action activates the overshoot control amplifier which employs a unity-gain follower configuration. The overshoot control amplifier monitors the FB pin voltage and, on S1's closing, pulls the OC pin voltage down to the FB pin voltage plus a built-in offset voltage of typically 48mV. The built-in offset voltage serves two purposes. First, the offset voltage prevents the overshoot control amplifier from interfering with normal transient operating conditions. Second, the offset voltage biases the feedback loop so that if the short-circuit condition ends, the feedback loop immediately starts to increase the output voltage to its regulated value.

APPLICATIONS INFORMATION

If the fault condition ceases, the output voltage increases. In response, the error amplifier COMP pin's voltage decreases. This action opens switch S1, deactivates the overshoot control amplifier and allows the OC pin capacitor to charge. The FB pin voltage increases quickly until the FB pin voltage exceeds the OC pin voltage. The feedback loop increases the drive to the opto-coupler until the FB pin follows and regulates to the OC pin voltage. Again, as the OC pin voltage increases past 600mV, the reference voltage takes control of the error amplifier and the FB pin regulates to 600mV.

Generating a V_{IN} Bias Supply

Biasing an LT4430 is crucial to proper operation. If the overshoot control (OC) function is not being used and the output voltage is greater than 3.3V, the IC may be biased from V_{OUT}. In these cases, it is the user's responsibility to verify large-signal start-up and fault recovery behavior.

If the overshoot control function is being used or the output voltage is below the LT4430's minimum operating voltage of 3V, employing an alternate bias method is necessary. The LT4430's undervoltage lockout (UVLO) circuitry, controlled by V_{IN}, resets and holds the OC pin capacitor low for V_{IN} less than 2.2V. When V_{IN} increases above 2.2V, the circuit releases the OC pin capacitor. The LT4430's supply voltage must come up faster than the output voltage to assert loop control and limit output voltage overshoot. In most cases, a few simple components accomplish this task. Adding a few biasing components to control overshoot is advantageous. Let's examine bias circuits for different topologies.

Figures 1a to 1e illustrate bias supply circuits for the flyback converter. Figure 1a shows the typical flyback output connection. Figures 1b and 1c exhibit equivalent circuit performance but rotate the rectifier connection to the ground-referred side. This connection permits the user to take advantage of the transformer secondary's forward behavior when the primary-side switch is on.

Figures 1d to 1e illustrate the bias generator circuit. $V_{IN} \bullet N$ volts appear across the secondary winding when the primary-side switch is on. D2 forward biases and C1 charges. During this time, the secondary-voltage is in series with V_{OUT} and C1 ultimately charges to ($V_{IN} \bullet N + V_{OUT} – V_F$). V_F is the forward voltage of D2. When V_{OUT} is zero at start-up, $V_{IN} \bullet N$ volts exists to charge C1. C1 is generally much smaller in value than C_{OUT} and the bias supply starts up ahead of V_{OUT}. R1 in Figures 1d and 1e limits peak charging currents, lowering D2's current rating. R1 also filters C1 from peak-charging to the voltage spikes induced by the secondary winding's leakage inductance. Between 1Ω to 10Ω is generally sufficient. R1 is usually necessary if C1 is a low ESR ceramic capacitor or if the transformer has high leakage inductance. It may be possible to eliminate R1 if C1 is a low cost, high ESR, surface-mount tantalum.

V_{IN} variation changes the bias supply in Figure 1d. Depending on V_{OUT}, the transformer turns ratio N and V_{IN} range, the bias supply may exceed the LT4430's 20V V_{IN} absolute maximum rating. If this occurs, two solutions exist. One is to tap the secondary-side inductor to create a lower voltage from which to rectify as illustrated in Figure 2a. The bias voltage decreases to ($V_{IN} \bullet N1/N + V_{OUT} – V_F$). This solution relies on secondary-side pins being available for the tap point.

APPLICATIONS INFORMATION

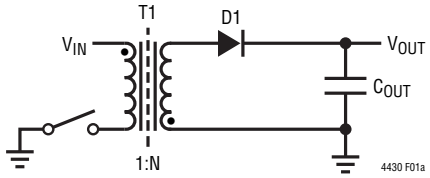


Figure 1a. Typical Flyback Converter Connection

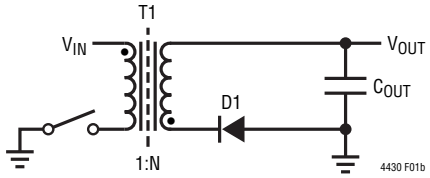


Figure 1b. Equivalent Flyback Converter Connection

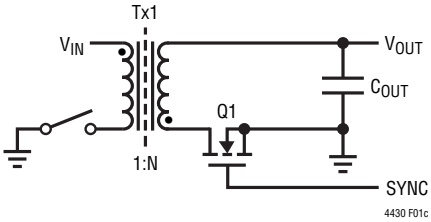


Figure 1c. Synchronous Flyback Converter Connection

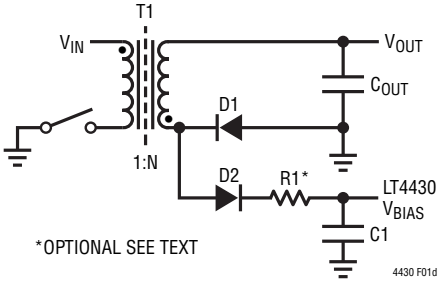


Figure 1d. Flyback Converter with Bias Generator

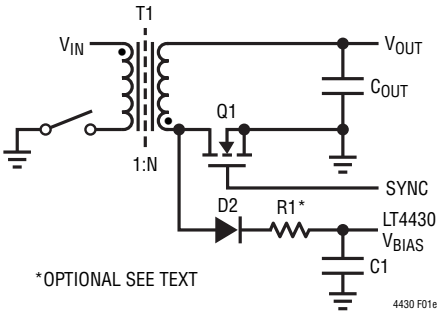


Figure 1e. Synchronous Flyback with Bias Generator

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The second solution is to make a preregulator as shown in Figure 2b. In this example, the bias supply equals (V_{Z1} – V_{BE}). Select R2 to bias Zener diode Z1 and to supply base current to QBS. Resistor R3 (on the order of a few hundred ohms), in series with Q5's base, suppresses possible high frequency oscillations depending on QBS's selection. The preregulator circuit has additional value for fully synchronous converters. Fully synchronous converters require gate drivers to control the secondary-side MOSFETs turn on and turnoff. The gate driver circuitry requires supply current in the range of 10mA to 100mA depending on the gate driver supply voltage, MOSFET size and switching frequency. The preregulator bias supply is ideal for powering both the LT4430 and the gate driver circuitry, especially since the gate drivers typically use a supply voltage between 5V to 12V. The preregulator circuit finds wide use in fully synchronous forward converters, push-pull converters and full-bridge converters.

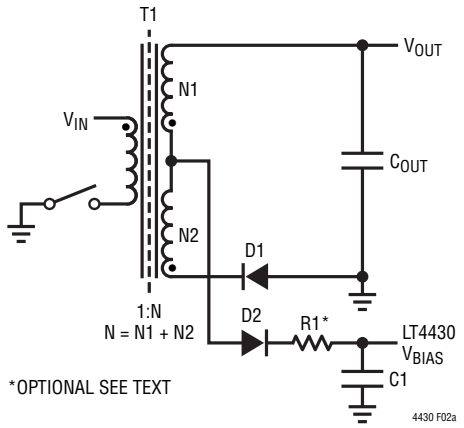

Figure 2a. Flyback Converter with Tapped Secondary Bias

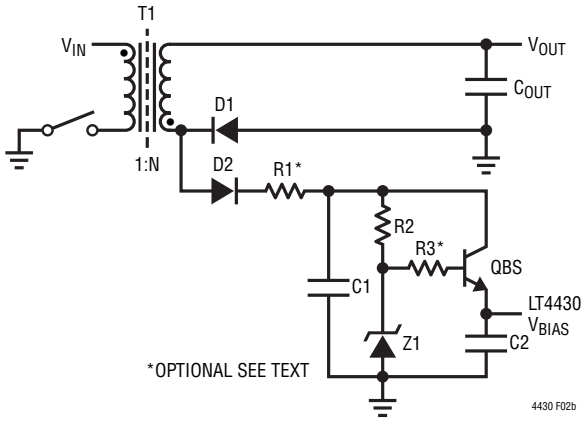

Figure 2b. Flyback Converter with Preregulator Bias

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Generate a bias supply for a forward converter using similar techniques to that of the flyback converter. Figure 3a to 3c detail the three common bias circuits for the synchronous single-switch forward converter. In the flyback converter of Figure 1d, the bias supply is proportional to V_{IN} and V_{OUT}. However, in the forward converter, L1's presence decouples the bias supply from V_{OUT}. In Figure 3a, the bias supply equals (V_{IN} • N – V_F). In Figure 3b, the bias supply equals (V_{IN} • N1/N – V_F). In Figure 3c, the bias supply equals (V_{Z1} – V_F).

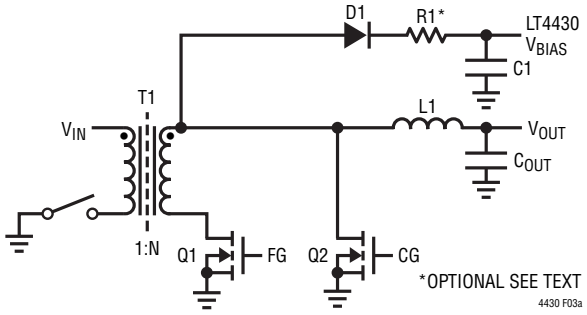

Figure 3a. Typical Single-Switch Synchronous Forward Converter with Bias Generator

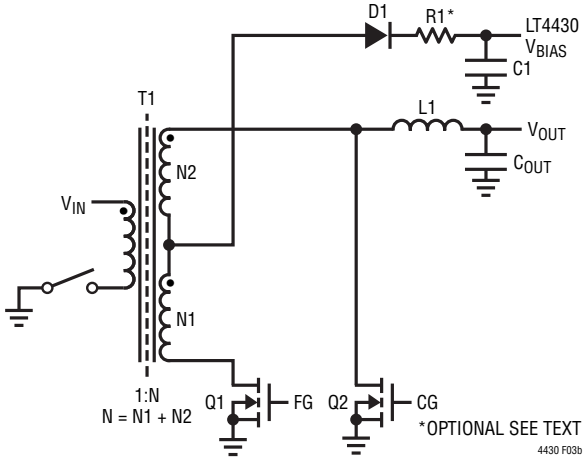

Figure 3b. Single-Switch Synchronous Forward Converter with Tapped Secondary Bias Generator

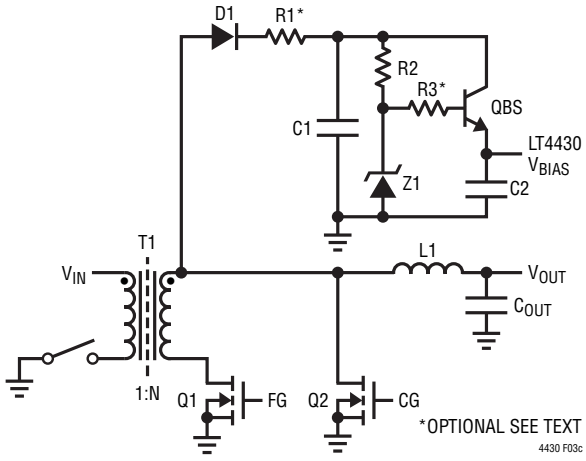

Figure 3c. Single-Switch Synchronous Forward Converter with Preregulator Bias Generator

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Figures 4a to 4d demonstrate bias supply circuits for the fully-synchronous push-pull topology. Biasing for full-bridge schemes is identical to the push-pull circuits with the obvious difference in the primary-side drive. In Figure 4a, the bias supply equals (V_{IN} • N – V_F). In Figure 4b and 4d, the bias supply equals (2 • V_{IN} • N – V_F). In Figure 4c and 4e, the bias supply equals (V_{Z1} – V_F).

In general, one of the simple, low-cost biasing schemes suffices for LT4430 applications. However, design constraints such as a very wide input voltage range may force employment of other biasing circuits. Other methods of generating the bias supply may include an additional transformer or output inductor winding, low-cost linear regulators, discrete or monolithic charge pumps and buck/boost regulators. However, if the bias supply gets this complicated, a quick chat with your local LTC applications engineer may result in a simpler solution.

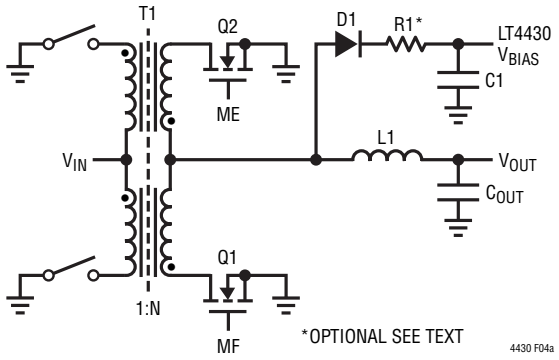

Figure 4a. Typical Synchronous Push-Pull Converter with Bias Generator

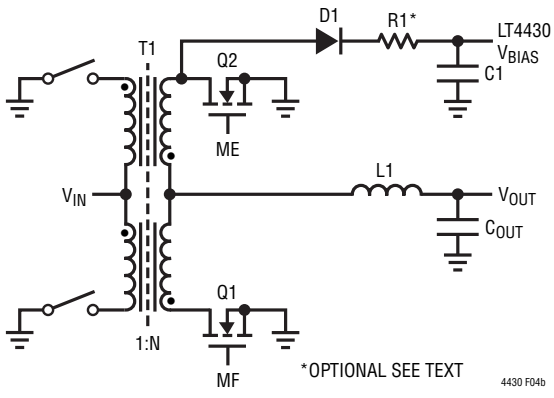

Figure 4b. Typical Synchronous Push-Pull Converter with 2x Bias Generator

APPLICATIONS INFORMATION

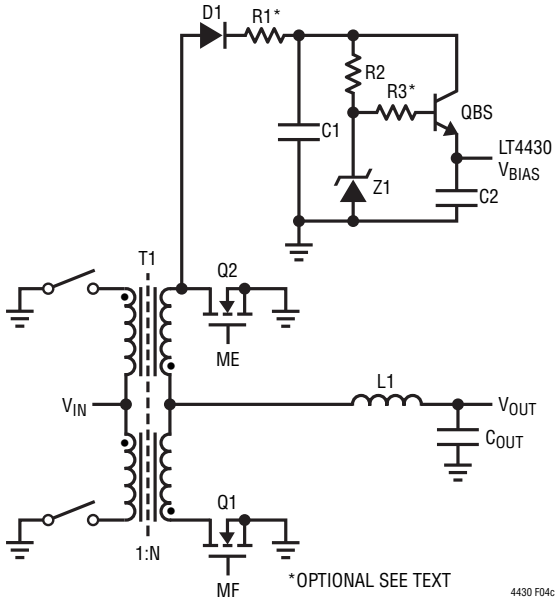

Figure 4c. Typical Synchronous Push-Pull Converter with Preregulator Bias

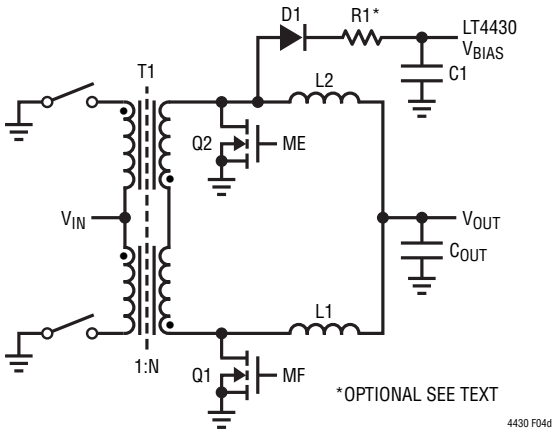

Figure 4d. Typical Synchronous Push-Pull Current-Doubler Converter with Bias Generator

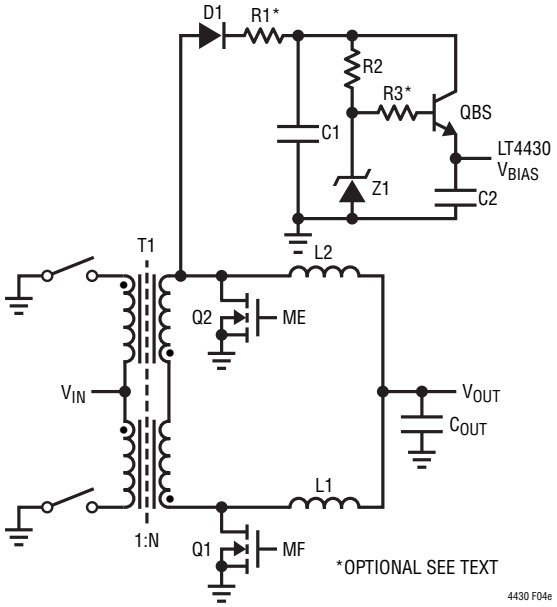

Figure 4e. Typical Synchronous Push-Pull Current-Doubler Converter with Preregulator Bias

APPLICATIONS INFORMATION

Setting Output Voltage

Figure 5 shows how to program the power supply output voltage with a resistor divider feedback network. Connect the top of R1 to V_{OUT}, the tap point of R1/R2 to FB and the bottom of R2 directly to GND of the LT4430. The FB pin regulates to 600mV and has a typical input pin bias current of 75nA flowing out of the pin.

The output voltage is set by the formula:

$$V_{OUT} = 0.6V \bullet (1 + R1/R2) – (75nA) \bullet R1$$

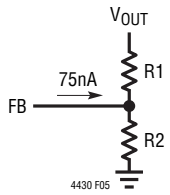

Figure 5. Setting Output Voltage

Opto-Coupler Feedback and Frequency Compensation

An isolated power supply with good line and load regulation generally employs the following strategy. Sense and compare the output voltage with an accurate reference potential. Amplify and feed back the error signal to the supply's control circuitry to correct the sensed error. Have the error signal cross the isolation barrier if the control circuitry resides on the primary-side. Coupling this signal requires an element that withstands the isolation potentials and still transfers the loop error signal.

Opto-couplers remain in prevalent use because of their ability to couple DC signals. Opto-couplers typically consist of an input infrared light emitting diode (LED) and an output phototransistor separated by an insulating gap. Most opto-coupler data sheets loosely specify the gain, or current transfer ratio (CTR), between the input diode and the output transistor. CTR is a strong function of the input diode current, temperature and time (aging). Aging degrades the LED's brightness and accelerates with higher operating current. CTR variation directly affects the overall system loop gain and the design must account for total variation. To make an effective optical detector, the output transistor design maximizes the base area to collect light energy. This constraint yields a transistor with a large collector-to-base capacitance. This capacitance can influence the circuit's performance based on the output transistor's hookup.

The two most common topologies for the output transistor of the opto-coupler are the common-emitter and common-collector configurations. Figure 6a illustrates the common-emitter design with the output transistor's collector connected to the output of the primary-side controller's error amplifier.

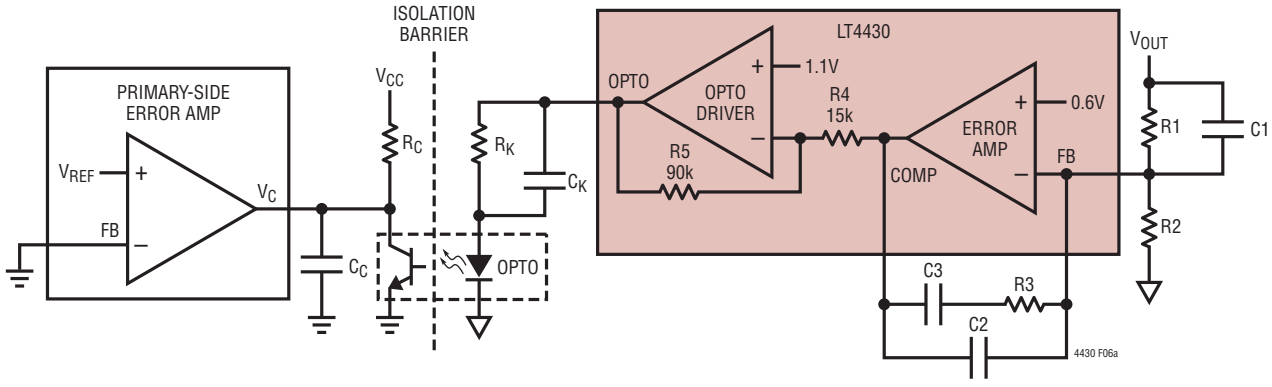

Figure 6a. Frequency Compensation with Opto-Coupler Common-Emitter Configuration

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In this example, the error amplifier is typically a transconductance amplifier with high output impedance and R_C dominates the impedance at the V_C node. Frequency compensation for this feedback loop is directly affected by the output transistor's collector-to-base capacitance as it introduces a pole into the feedback loop. This pole varies considerably with the transistor's operating conditions. In many cases, this pole limits the achievable loop bandwidth. Cascoding the output transistor significantly reduces the effects of this capacitance and increases achievable loop bandwidth. However, not all designs have the voltage headroom required for the cascode connection or can tolerate the additional circuit complexity. The open loop transfer function from the output voltage to the primary-side error amplifier's output is:

$$\frac{V_C}{V_{OUT}} = \frac{-A \bullet \left(\frac{R2}{R1+R2}\right) \bullet (1+s \bullet R1 \bullet C1) \bullet (1+s \bullet R3 \bullet C3)}{[s \bullet A \bullet R1 \bullet (C2+C3)] \bullet \left(1+s \bullet R3 \bullet \frac{(C2 \bullet C3)}{(C2+C3)}\right)} \bullet$$

$$6 \bullet \frac{(1+s \bullet R_K \bullet C_K)}{\left(1+s \bullet \frac{(R_K \bullet R_D)}{(R_K+R_D)} \bullet C_K\right)} \bullet \frac{CTR \bullet R_C}{(R_K+R_D)} \bullet$$

$$\frac{1}{\left(1+s \bullet r_\pi \bullet \left[\frac{(CTR \bullet R_C)}{(R_K+R_D)} \bullet C_{CB} + C_{BE}\right]\right)} \bullet$$

$$\frac{1}{(1+s \bullet R_C \bullet C_C)}$$

where:

A = LT4430 open loop DC Gain

R_D = Opto-coupler diode equivalent small-signal resistance

CTR = Opto-coupler AC current transfer ratio

C_{CB} = Opto-coupler nonlinear collector-to-base capacitor

C_{BE} = Opto-coupler nonlinear base-to-emitter capacitor

r_π = Opto-coupler small-signal base-to-emitter resistor

Figure 6a and its transfer function illustrate most of the possible poles and zeroes that can be set and are shown for the sake of completeness. In a practical application, the transfer function simplifies considerably because not all the poles and zeroes are used. Also, different combinations of poles and zeroes can result in the same small signal gain-phase characteristics but demonstrate dramatically different large-signal behavior.

The common-collector configuration eliminates the miller effect of the output transistor's collector-to-base capacitance and generally increases achievable loop bandwidth. Figure 6b illustrates the common-collector design with the output transistor's emitter connected to the inverting input of the primary-side controller's error amplifier.

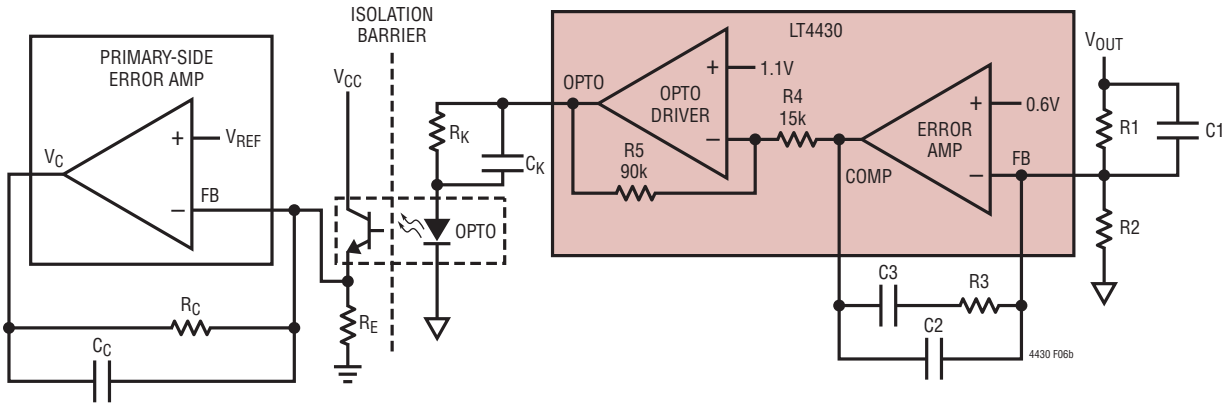

Figure 6b. Frequency Compensation with Opto-Coupler Common-Collector Configuration

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In this example, the error amplifier is typically a voltage error amplifier configured as a transimpedance amplifier. The opto-coupler transistor's emitter provides feedback information directly to the FB pin and the resistor R_E from FB to GND sets the DC bias condition for the opto-coupler. The open loop transfer function from the output voltage to the primary-side error amplifier's output is:

$$\frac{V_C}{V_{OUT}} = \frac{-A \bullet \left(\frac{R2}{R1+R2}\right) \bullet (1+s \bullet R1 \bullet C1) \bullet (1+s \bullet R3 \bullet C3)}{[s \bullet A \bullet R1 \bullet (C2+C3)] \bullet \left(1+s \bullet R3 \bullet \frac{(C2 \bullet C3)}{(C2+C3)}\right)} \bullet$$

$$6 \bullet \frac{(1+s \bullet R_K \bullet C_K)}{\left(1+s \bullet \frac{(R_K \bullet R_D)}{(R_K+R_D)} \bullet C_K\right)} \bullet \frac{CTR \bullet R_C}{(R_K+R_D)} \bullet$$

$$\frac{1}{(1+s \bullet r_\pi \bullet C_{BE})} \bullet \frac{1}{(1+s \bullet R_C \bullet C_C)}$$

Figure 6b and its transfer function illustrate most of the possible poles and zeroes that can be set and are shown for the sake of completeness. In a practical application, the transfer function simplifies considerably because not all the poles and zeroes are used.

In both configurations, the terms R_D, CTR, r_π, C_{CB} and C_{BE}. vary from part to part and also change with bias current. For most opto-couplers, R_D is 50Ω at a DC bias of 1mA, and 25Ω at a DC bias of 2mA. CTR is the small signal AC current transfer ratio. As an example, the Fairchild MOC207 opto-coupler has an AC CTR around 1, even though the DC CTR is much lower when biased at 1mA or 2mA. Most opto-coupler data sheets do not specify the terms C_{CB}, C_{BE} and r_π and values must be obtained from empirical measurements.

This frequency compensation discussion only addresses the transfer function from the output back to the control node on the primary-side. Compensation of the entire feedback loop must combine this transfer function with the transfer function of the power processing circuitry, commonly referred to as the modulator. In an isolated power supply, the modulator's transfer function depends on topology (flyback, forward, push-pull, bridge), current or voltage mode control, operation in discontinuous or continuous mode, input/output voltage, transformer turns ratio and output load current. It is beyond this data sheet's scope to detail the transfer functions for all of the various combinations. However, the power supply designer must fully characterize and understand the modulator's transfer function to successfully frequency compensate the feedback loop for all operating conditions.

Opto-Couplers

Opto-couplers are available in a wide variety of package styles and performance criteria including isolation rating, CTR, output transistor breakdown voltage, output transistor current capability, and response time. Table 1 lists several manufacturers of opto-coupler devices, although this is by no means a complete list.

Table 1. Opto-Coupler Vendors

VENDOR	PHONE	URL
Agilent Technologies	800-235-0312	www.agilent.com
Fairchild Semiconductor	207-775-8100	www.fairchildsemi.com
Isocom	214-495-0755	www.isocom.com
Kodenshi Korea Corp.	82-63-839-2111	www.kodenshi.co.kr
NEC	81-44-435-1588	www.ncsd.necel.com
Sharp Microelectronics	877-343-2181	www.sharpsma.com
Toshiba	949-455-2000	www.toshiba.com
Vishay	402-563-6866	www.vishay.com

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Setting Overshoot Control Time

Figure 7 shows how to calculate the overshoot time by connecting a capacitor from the OC pin to GND.

The overshoot control time, t_{OC}, is set by the formula:

$$t_{OC} = (C_{OC} \bullet 0.6V)/8.5\mu A$$

The OC pin requires a minimum capacitor of 100pF due to stability requirements with the overshoot control amplifier. This yields a minimum time of 7µs which is generally on the order of a few cycles of the switching regulator. Using the minimum capacitor value results in no influence on start-up characteristics. Larger OC capacitor values increase the overshoot control time and only increase the amplifier stability. **Do not** modulate the overshoot control time by externally increasing the OC charging current or by externally driving the OC pin.

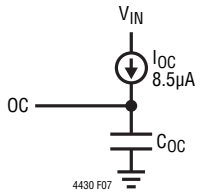

Figure 7. Setting Overshoot Control Time

Choosing the Overshoot Control (OC) Capacitor Value

As discussed in the frequency compensation section, the designer enjoys considerable freedom in setting the feedback loop's pole and zero locations for stability. Different pole and zero combinations can produce the same gain-phase characteristics, but result in noticeably different large-signal responses. Choosing frequency compensation values that optimize both small-signal and large-signal responses is difficult. Compromise values often result.

Power supply start-up and short-circuit recovery are the worst-case large signal conditions. Input voltage and output load characteristics heavily influence power supply behavior as it attempts to bring the output voltage into regulation. Frequency compensation values that provide stable response under normal operating conditions can allow severe output voltage overshoot to occur during start-up and short-circuit recovery conditions. Large overshoot often results in damage or destruction to the load circuitry being powered, not a desirable trait.

The LT4430's overshoot control circuitry plus one external capacitor (C_{OC}) provide independent control of start-up and short-circuit recovery response without compromising small-signal frequency compensation. Choosing the optimum C_{OC} value is a straightforward laboratory procedure. The following description and set of pictures explain this procedure.

Before choosing a value for the OC pin capacitor, complete the remainder of the power supply design. This process includes evaluating the chosen V_{IN} bias generator topology (**please consult prior applications information section**) and optimizing frequency compensation under all normal operating conditions. During this design phase, set C_{OC} to its minimum value of 100pF. This ensures negligible interaction from the overshoot control circuitry. Once these steps are complete, construct a test setup that monitors start-up and short-circuit recovery waveforms. Perform this testing with the output lightly loaded. Light load, following full slew operation, is the worst-case as the feedback loop transitions from full to minimal power delivery.

As an example, refer to the schematic on the last page illustrating the 5V, 2A isolated flyback converter. All of the following photos are taken with V_{IN} = 48V and I_{LD} = 20mA. Figure 8a demonstrates the power supply start-up and short-circuit recovery behavior with no overshoot control compensation (C_{OC} = 100pF minimum). The 5V output overshoots by several volts on both start-up and short-circuit recovery due to the conservative nature of the small-signal frequency compensation values.

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Next, increase C_{OC}'s value. Either use a capacitor substitution box or solder each new value into the circuit. Monitor the start-up and short-circuit recovery waveforms. Note any changes. Figures 8b to 8e illustrate what happens as C_{OC} increases. In general, overshoot decreases as C_{OC} increases.

C_{OC} = 0.0168µF in Figure 8b begins to affect loop dynamics, but start-up still exhibits about 1.5V of overshoot. Short-circuit recovery is considerably more damped. C_{OC} = 0.022µF in Figure 8c damps start-up overshoot to 0.5V and short-circuit recovery remains similar to that of Figure 8b. C_{OC} = 0.033µF in Figure 8d provides under 100mV of overshoot and short-circuit recovery is slightly more damped. C_{OC} = 0.047µF in Figure 8e achieves zero overshoot at the expense of additional damping and delay time in short-circuit recovery. In this example, C_{OC} = 0.033µF provides the best value for both start-up and short-circuit recovery. Figure 8f provides an expanded scale of the waveforms. After a C_{OC} value is selected, check start-up and short-circuit recovery over the V_{IN} supply range and with higher output load conditions. Modify the value as necessary.

Start-up and short-circuit recovery waveforms for various designs will differ from the photos shown in this example. Factors affecting these waveforms include the isolated topology chosen, the primary-side and secondary-side bias circuitry and input/output conditions. For instance, in many isolated power supplies, a winding on the main power transformer bootstraps the supply voltage for the primary-side control circuitry. Under short-circuit conditions, the primary-side control circuitry's supply voltage collapses, generating a restart cycle. Recovery from short-circuit is therefore identical to start-up. In the flyback example discussed, the primary-side control circuitry is always active. Switching never stops in short-circuit. The LT4430 error amplifier COMP pin changes from its low clamp level to its higher regulating value during start-up and changes from its high clamp level to its lower regulating point during short-circuit recovery. This large-signal behavior explains the observed difference in the start-up versus short-circuit recovery waveforms.

A final point of discussion involves the chosen C_{OC} value. LTC recommends that the designer use a value that controls overshoot to the acceptable level, but is not made overly large. The temptation arises to use the overshoot control function as a power supply "soft-start" feature. Larger values of C_{OC}, above what is required to control overshoot, do result in smaller dV/dt rates and longer start-up times. However, large values of C_{OC} may stall the feedback loop during start-up or short-circuit recovery, resulting in an extended period of time that the output voltage "flatspots". This voltage shelf may occur at an intermediate value of output voltage, promoting anomalous behavior with the powered load circuitry. If this situation occurs with the desired C_{OC} value, solutions may require circuit modifications. In particular, bias supply holdup times are a prime point of concern as switching stops during these output voltage flatspots. As a reminder, the purpose of this LT4430 circuitry is to control and prevent excessive output voltage overshoot that would otherwise induce damage or destruction, not to control power supply timing, sequencing, etc. It is ultimately the user's responsibility to define the acceptance criteria for any waveforms generated by the power supply relative to overall system requirements.

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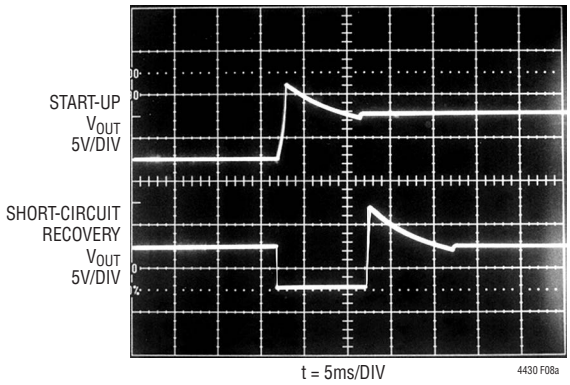
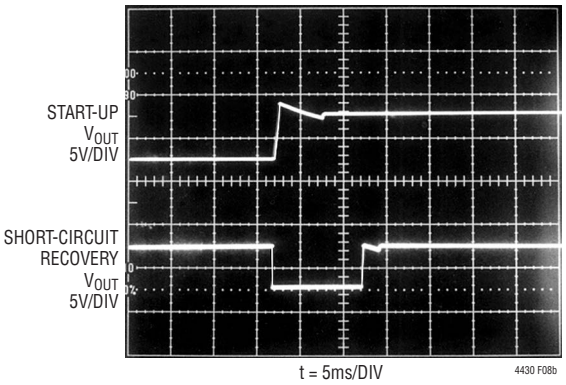


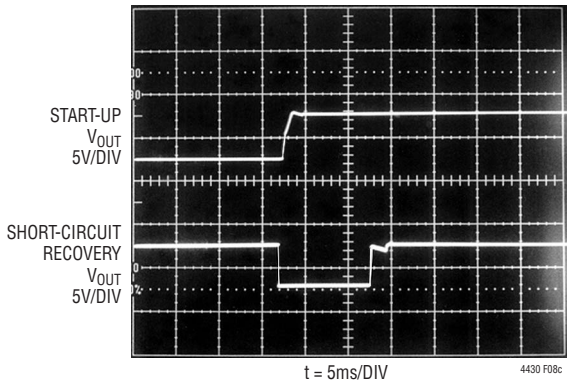
C_{OC} = 100pF

Figure 8a. Start-Up and Short-Circuit Recovery Waveforms



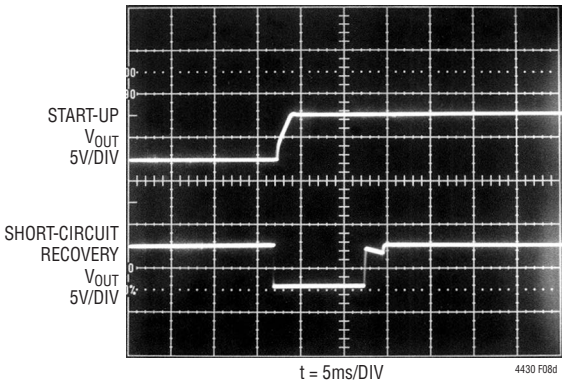
C_{OC} = 0.0168µF = 0.01µF + 6.8nF

Figure 8b. Start-Up and Short-Circuit Recovery Waveforms



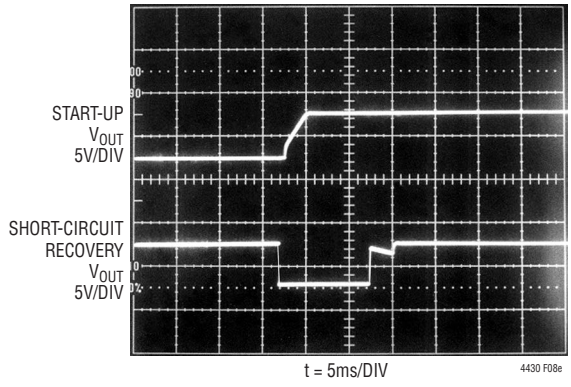
C_{OC} = 0.022µF

Figure 8c. Start-Up and Short-Circuit Recovery Waveforms



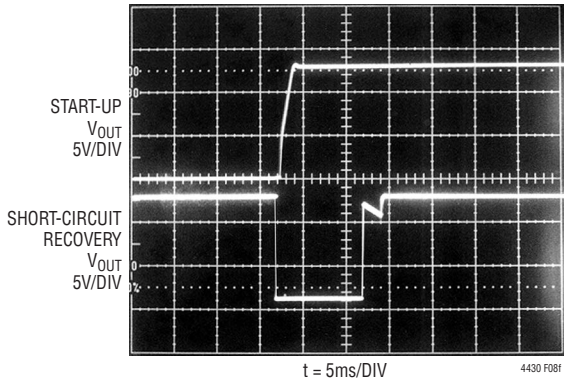
C_{OC} = 0.033µF

Figure 8d. Start-Up and Short-Circuit Recovery Waveforms



C_{OC} = 0.047µF

Figure 8e. Start-Up and Short-Circuit Recovery Waveforms

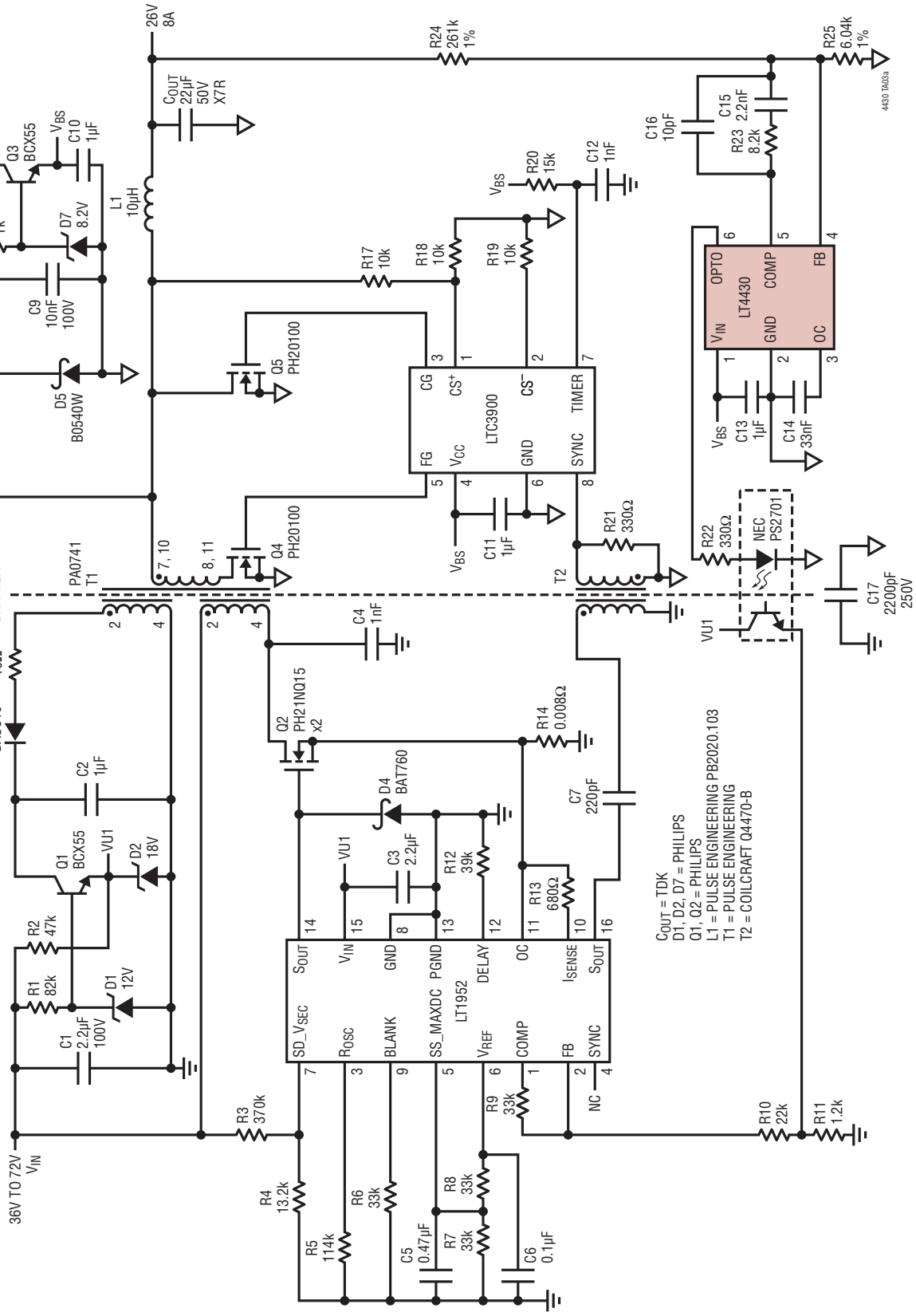


C_{OC} = 0.033µF

Figure 8f. Zoom In of Waveforms with Selected C_{OC} = 0.033µF

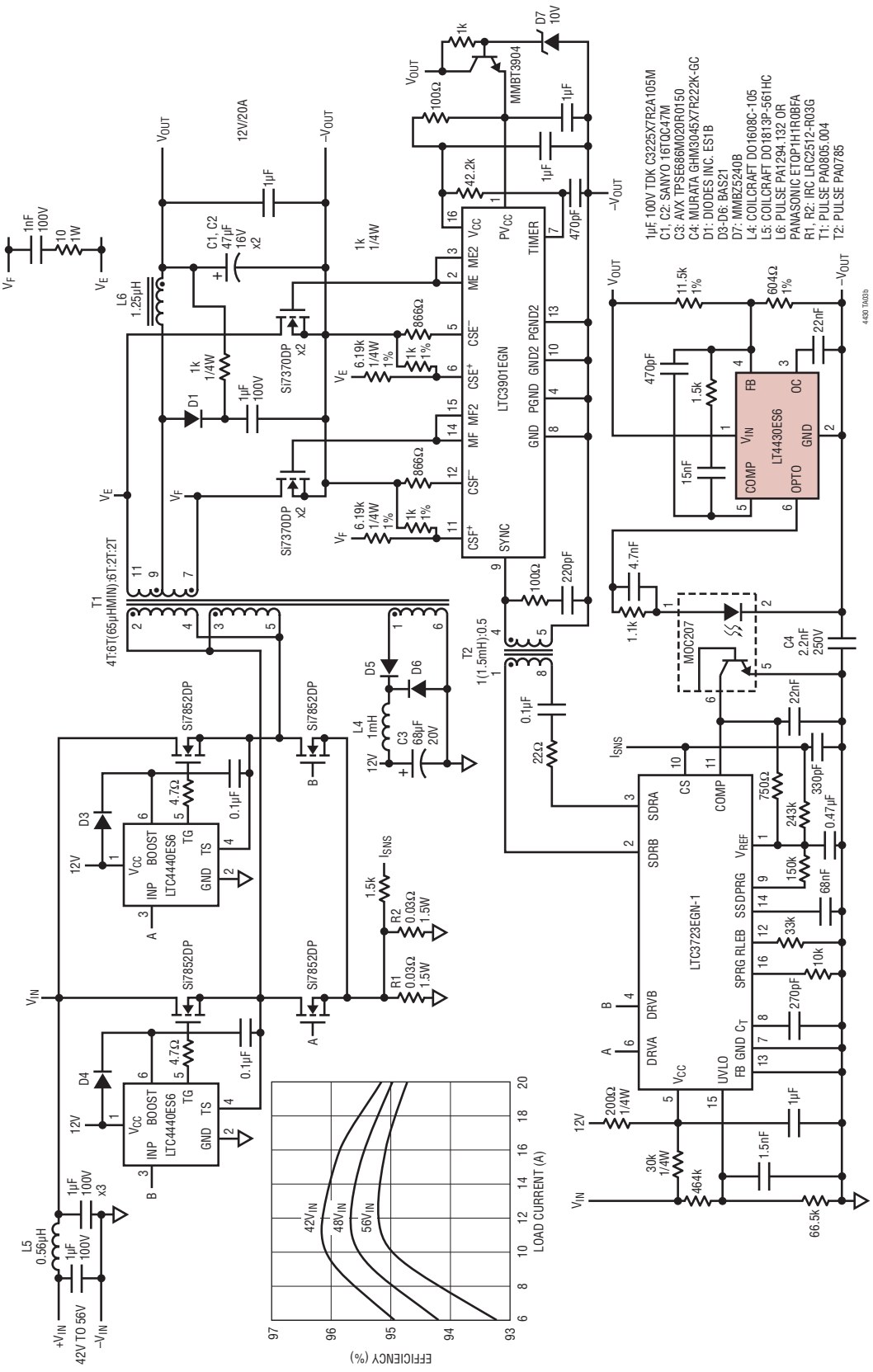
TYPICAL APPLICATIONS

200W, 26V, 95% Efficient Base Station Converter



TYPICAL APPLICATIONS

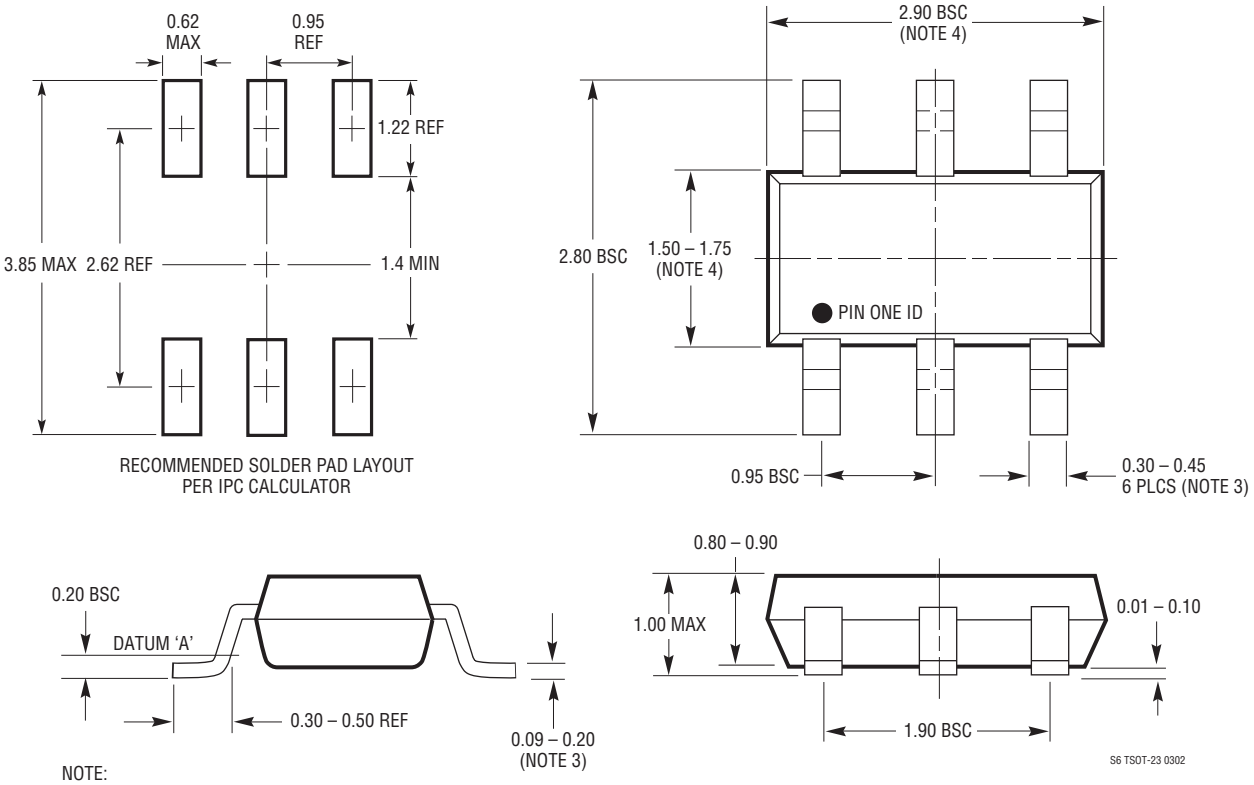
LTC3723-1 240W 42V$_{IN}$ to 56V$_{IN}$ to 12V/20A Isolated 1/4 Brick (2.3" × 1.45")



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



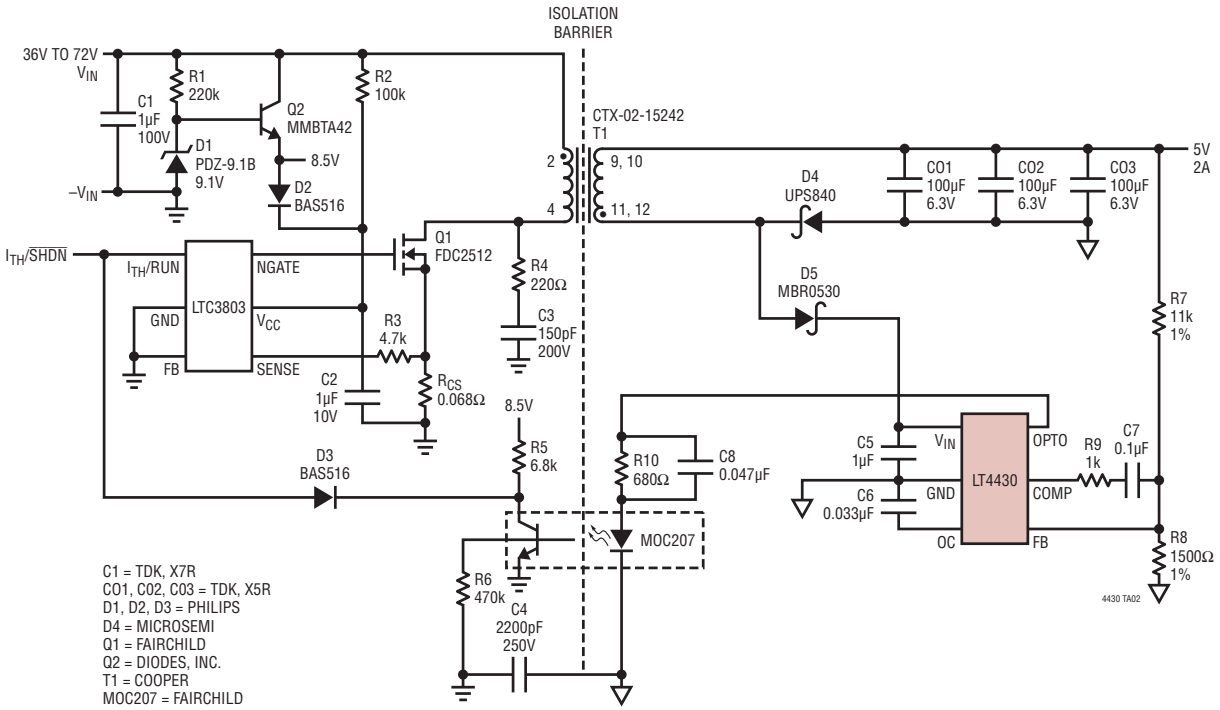
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/11	H-Grade and MP-Grade parts added. Reflected throughout the data sheet.	1-26
C	10/13	Corrected Q2 in Block Diagram from NPN to PNP.	8
		Changed R24 from 26.1k to 261k.	22
D	7/15	Corrected typos in formulas.	17, 18

TYPICAL APPLICATION

5V, 2A Isolated Flyback Telecom Converter Start-Up Waveforms with Overshoot Control Implemented



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1952/LT1952-1	Isolated Synchronous Forward Controllers	Ideal for Medium Power 24V and 48V Input Applications
LTC3765/LTC3766	Isolated Synchronous No-Opto Forward Controller Chip Set	Ideal for Medium Power 24V and 48V Input Applications
LTC3723-1/LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers
LTC3721-1/LTC3721-2	Non-Synchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LTC3722/LTC3722-2	Synchronous Isolated Full Bridge Controllers	Ideal for High Power 24V and 48V Input Applications
LTC3900	Synchronous Rectifier Driver for Forward Converters	Programmable Timeout, Synchronization Sequencer, Reverse Inductor Current Sense
LTC3901	Synchronous Rectifier Driver for Push-Pull and Full-Bridge	Programmable Timeout, Synchronization Sequencer, Reverse Inductor Current Sense
LTC3803/LTC3803-3/ LTC3803-5	Flyback DC/DC Controller with Fixed 200kHz or 300kHz Operating Frequency	V_{IN} and V_{OUT} Limited by External Components, 6-pin ThinSoT Package
LTC3805/LTC3805-5	Adjustable Constant Frequency (70KHz to 700kHz) Frequency Flyback DC/DC Controller	V_{IN} and V_{OUT} Limited by External Components, MSOP-10E and 3mm × 3mm DFN-10 Packages
LT3748	100V No Opto Flyback Controller	$5V \le V_{IN} \le 100V$, Boundary Mode Operation, MSOP-16 with Extra High Voltage Pin Spacing
LT3798	Off-Line Isolated No-Opto Flyback Controller with Active PFC	V_{IN} and V_{OUT} Limited by External Components

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