DATA SHEET

74ALVCH32501
36-bit universal bus transceiver with direction pin; 3-state

Product specification
Supersedes data of 2000 Mar 16

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Philips Semiconductors

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74ALVCH32501

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- Current drive ±24 mA at 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- CMOS low power consumption
- Direct interface with TTL levels
- All inputs have bus-hold circuitry
- Output drive capability 50 Ω transmission lines at 85 °C
- Plastic fine-pitch ball grid array package.

DESCRIPTION

The 74ALVCH32501 is a high-performance CMOS product designed for V_{CC} operation at 2.5 V and 3.3 V.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The 74ALVCH32501 can be used as two 18-bit transceivers or one 36-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OE_{AB} and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock inputs (CP_{AB} and CP_{BA}). For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is HIGH. When input LE_{AB} is LOW, the A data is latched if input CP_{AB} is held at a HIGH or LOW level. If input LE_{AB} is LOW, the A data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CP_{AB}. When input OE_{AB} is HIGH, the outputs are active. When input OE_{AB} is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B, but uses inputs $\overline{OE}_{BA}$, LE_{BA} and CP_{BA}. The output enables are complimentary (OE_{AB} is active HIGH, and $\overline{OE}_{BA}$ is active LOW).

To ensure the high-impedance state during power-up or power-down, pin $\overline{OE}_{BA}$ should be tied to V_{CC} through a pull-up resistor and pin OE_{AB} should be tied to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking or current-sourcing capability of the driver.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 30 pF; V_{CC} = 2.5 V	2.8	ns
		C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		8.0	pF
C_{PD}	power dissipation capacitance per latch	V_I = GND to V_{CC}; note 1		
		outputs enabled	21	pF
		outputs disabled	3	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = number of inputs switching;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

FUNCTION TABLE

See notes 1 and 2.

INPUT				INTERNAL REGISTERS	OUTPUT	OPERATING MODE
nOE_{AB}	nLE_{AB}	nCP_{AB}	nA_n		nB_n	
L	H	X	X	X	Z	disabled
L L	↓ ↓	X X	h l	H L	Z Z	disabled; latch data
L	L	H or L	X	NC	Z	disabled; hold data
L L	L L	↑ ↑	h l	H L	Z Z	disabled; clock data
H H	H H	X X	H L	H L	H L	transparent
H H	↓ ↓	X X	h l	H L	H L	latch data and display
H H	L L	↑ ↑	h l	H L	H L	clock data and display
H H	L L	H or L H or L	X X	H L	H L	hold data and display

Notes

1. A-to-B data flow is shown; B-to-A flow is similar but uses $n\overline{OE}_{BA}$, nLE_{BA} and nCP_{BA}.
2. H = HIGH voltage level;
   h = HIGH voltage level on set-up time prior to the enable or clock transition;
   L = LOW voltage level;
   l = LOW voltage level on set-up time prior to the enable or clock transition;
   NC = no change;
   X = don't care;
   ↑ = LOW-to-HIGH enable or clock transition;
   ↓ = HIGH-to-LOW enable or clock transition;
   Z = high impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH32501EC	–40 °C to +85 °C	114	LFBGA114	plastic	SOT537-1

PINNING

SYMBOL	DESCRIPTION
nA_n	data inputs
nB_n	data outputs
GND	ground (0 V)
V_{CC}	DC supply voltage
nOE_{AB}	output enable inputs A to B (active HIGH)
$n\overline{OE}_{BA}$	output enable inputs B to A (active LOW)
nLE_{AB}	latch enable inputs A to B
nLE_{BA}	latch enable inputs B to A
nCP_{AB}	clock input A to B
nCP_{BA}	clock input B to A

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
6	$1B_1$	$1B_3$	$1B_5$	$1B_7$	$1B_9$	$1B_{11}$	$1B_{13}$	$1B_{14}$	$1B_{16}$	n.c.	$2B_1$	$2B_3$	$2B_5$	$2B_7$	$2B_9$	$2B_{11}$	$2B_{13}$	2B14	$2B_{16}$
5	$1B_0$	$1B_2$	$1B_4$	$1B_6$	$1B_8$	$1B_{10}$	$1B_{12}$	$1B_{15}$	$1B_{17}$	$2CP_{AB}$	$2B_0$	$2B_2$	$2B_4$	$2B_6$	$2B_8$	$2B_{10}$	$2B_{12}$	$2B_{15}$	$2B_{17}$
4	$1CP_{AB}$	GND	GND	V_{CC}	GND	GND	V_{CC}	GND	$1CP_{BA}$	GND	GND	GND	V_{CC}	GND	GND	V_{CC}	GND	$2CP_{BA}$	GND
3	$1LE_{AB}$	$1OE_{AB}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$1\overline{OE}_{BA}$	$1LE_{BA}$	$2OE_{AB}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}_{BA}$	$2LE_{BA}$
2	$1A_0$	$1A_2$	$1A_4$	$1A_6$	$1A_8$	$1A_{10}$	$1A_{12}$	$1A_{15}$	$1A_{17}$	$2LE_{AB}$	$2A_0$	$2A_2$	$2A_4$	$2A_6$	$2A_8$	$2A_{10}$	$2A_{12}$	$2A_{15}$	$2A_{17}$
1	$1A_1$	$1A_3$	$1A_5$	$1A_7$	$1A_9$	$1A_{11}$	$1A_{13}$	$1A_{14}$	$1A_{16}$	n.c.	$2A_1$	$2A_3$	$2A_5$	$2A_7$	$2A_9$	$2A_{11}$	$2A_{13}$	$2A_{14}$	$2A_{16}$

MNA562

Fig.1 Pin configuration.

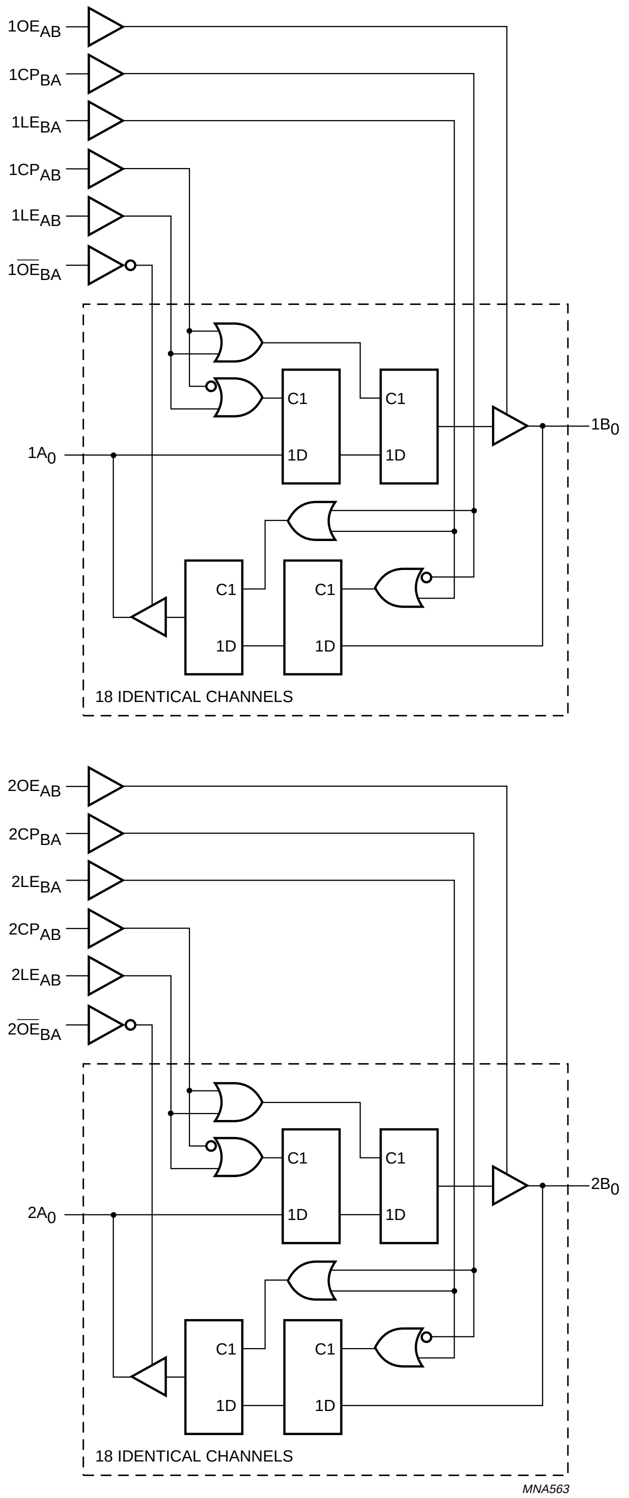


Fig.2 Logic symbol.

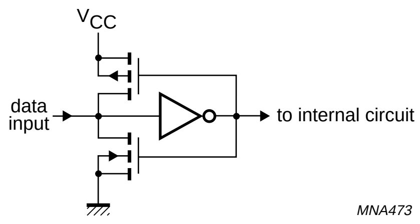


Fig.3 Bus-hold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	2.5 V range (for maximum speed performance at 30 pF output load)	2.3	2.7	V
		3.3 V range (for maximum speed performance at 50 pF output load)	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
T_{amb}	ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall time ratios ($\Delta t/\Delta V$)	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+4.6	V
V_I	input voltage	for control pins; note 1	–0.5	+4.6	V
		for data input pins; note 1	–0.5	V_{CC} + 0.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
I_{OK}	output clamping diode current	V_O < 0 V; note 1	–	50	mA
V_O	output voltage	see note 1	–0.5	V_{CC} + 0.5	V
I_O	output sink current	V_O = 0 V to V_{CC}	–	–50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +85 °C; note 2	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_{tot} derates linearly with 1.8 mW/K.

DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		2.3 to 2.7	1.7	1.2	–	V
			2.7 to 3.6	2.0	1.5	–	V
V_{IL}	LOW-level input voltage		2.3 to 2.7	–	1.2	0.7	V
			2.7 to 3.6	–	1.5	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	2.3 to 3.6	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –6 mA	2.3	V_{CC} – 0.3	V_{CC} – 0.08	–	V
		I_O = –12 mA	2.3	V_{CC} – 0.6	V_{CC} – 0.26	–	V
		I_O = –12 mA	2.7	V_{CC} – 0.5	V_{CC} – 0.14	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.6	V_{CC} – 0.09	–	V
		I_O = –24 mA	3.0	V_{CC} – 1.0	V_{CC} – 0.28	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	2.3 to 3.6	–	GND	0.20	V
		I_O = 6 mA	2.3	–	0.07	0.40	V
		I_O = 12 mA	2.3	–	0.15	0.70	V
		I_O = 12 mA	2.7	–	0.14	0.40	V
		I_O = 24 mA	3.0	–	0.27	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND	2.3 to 3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; note 2	2.3 to 3.6	–	0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	2.3 to 3.6	–	0.4	80	μA
ΔI_{CC}	additional quiescent supply current given per data I/O pin with bus-hold	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.7 to 3.6	–	150	750	μA
I_{BHL}	bus-hold LOW sustaining current	V_I = 0.7 V; note 3	2.3	45	–	–	μA
		V_I = 0.8 V; note 3	3.0	75	150	–	μA
I_{BHH}	bus-hold HIGH sustaining current	V_I = 1.7 V; note 3	2.3	–45	–	–	μA
		V_I = 2.0 V; note 3	3.0	–75	–175	–	μA
I_{BHLO}	bus-hold LOW overdrive current	note 3	3.6	500	–	–	μA
I_{BHHO}	bus-hold HIGH overdrive current	note 3	3.6	–500	–	–	μA

Notes

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.
3. Valid for data inputs of bus-hold parts.

AC CHARACTERISTICS

T_{amb} = –40 °C to +85 °C; GND = 0 V

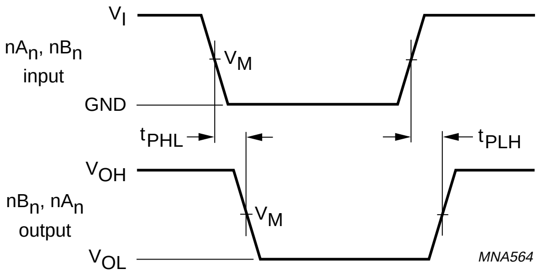
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L				
V_{CC} = 2.3 V to 2.7 V; $t_r = t_f \leq$ 2.0 ns; note 1							
t_{PHL}/t_{PLH}	propagation delay						
	nA_n to nB_n; nB_n to nA_n	see Figs 4 and 8	30 pF	1.0	2.8	5.1	ns
	nLE_{BA} to nA_n; nLE_{AB} to nB_n	see Figs 5 and 8	30 pF	1.1	3.5	6.1	ns
	nCP_{BA} to nA_n; nCP_{AB} to nB_n	see Figs 5 and 8	30 pF	1.0	3.3	6.1	ns
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	see Figs 6 and 8	30 pF	1.0	2.5	5.8	ns
	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	30 pF	1.3	2.8	6.3	ns
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	see Figs 6 and 8	30 pF	1.5	2.5	6.2	ns
	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	30 pF	1.3	2.5	5.3	ns
t_W	nLE_{AB} or nLE_{BA} pulse width HIGH	see Figs 5 and 8	30 pF	3.3	0.8	–	ns
	nCP_{AB} or nCP_{BA} pulse width HIGH or LOW	see Figs 5 and 8	30 pF	3.3	2.0	–	ns
t_{su}	set-up time nA_n before $nCP_{AB}\uparrow$ or nB_n before $nCP_{BA}\uparrow$	see Figs 7 and 8	30 pF	1.7	0.1	–	ns
	set-up time CP HIGH or LOW nA_n before $nLE_{AB}\downarrow$ or nB_n before $nLE_{BA}\downarrow$	see Figs 7 and 8	30 pF	1.1	0.1	–	ns
t_h	hold time nA_n after $nCP_{AB}\uparrow$ or nB_n after $nCP_{BA}\uparrow$	see Figs 7 and 8	30 pF	1.7	0.3	–	ns
	hold time CP HIGH or LOW nA_n after $nLE_{AB}\downarrow$ or nB_n after $nLE_{BA}\downarrow$	see Figs 7 and 8	30 pF	1.6	0.3	–	ns
f_{max}	maximum clock frequency	see Figs 5 and 8	30 pF	150	330	–	MHz
V_{CC} = 2.7 V; $t_r = t_f \leq$ 2.5 ns; note 2							
t_{PHL}/t_{PLH}	propagation delay						
	nA_n to nB_n; nB_n to nA_n	see Figs 4 and 8	50 pF	–	3.0	4.6	ns
	nLE_{BA} to nA_n; nLE_{AB} to nB_n	see Figs 5 and 8	50 pF	–	3.6	5.3	ns
	nCP_{BA} to nA_n; nCP_{AB} to nB_n	see Figs 5 and 8	50 pF	–	3.4	5.6	ns
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	see Figs 6 and 8	50 pF	–	2.7	5.3	ns
	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	50 pF	–	3.3	6.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	see Figs 6 and 8	50 pF	–	3.6	5.7	ns
	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	50 pF	–	3.3	4.6	ns
t_W	pulse width nLE_{AB} or nLE_{BA} HIGH	see Figs 5 and 8	50 pF	3.3	0.7	–	ns
	pulse width nCP_{AB} or nCP_{BA} HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.4	–	ns
t_{su}	set-up time nA_n before $nCP_{AB}\uparrow$ or nB_n before $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	+1.4	–0.1	–	ns
	set-up time CP HIGH or LOW nA_n before $nLE_{AB}\downarrow$ or nB_n before $nLE_{BA}\downarrow$	see Figs 7 and 8	50 pF	+1.0	–0.2	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L				
t_h	hold time nA_n after $nCP_{AB}\uparrow$ or nB_n after $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	1.6	0.3	–	ns
	hold time CP HIGH or LOW nA_n after $nLE_{AB}\downarrow$ or nB_n after $nLE_{BA}\downarrow$	see Figs 7 and 8	50 pF	1.5	0.1	–	ns
f_{max}	maximum clock frequency	see Figs 5 and 8	50 pF	150	333	–	MHz
V_{CC} = 3.0 V to 3.6 V; $t_r = t_f \leq$ 2.5 ns; note 3							
t_{PHL}/t_{PLH}	propagation delay						
	nA_n to nB_n; nB_n to nA_n	see Figs 4 and 8	50 pF	1.0	3.0	4.2	ns
	nLE_{BA} to nA_n; nLE_{AB} to nB_n	see Figs 5 and 8	50 pF	1.3	3.4	4.8	ns
	nCP_{BA} to nA_n; nCP_{AB} to nB_n	see Figs 5 and 8	50 pF	1.4	3.3	4.9	ns
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	see Figs 6 and 8	50 pF	1.0	2.4	4.6	ns
	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	50 pF	1.1	2.5	5.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	see Figs 6 and 8	50 pF	1.4	2.9	5.0	ns
	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	see Figs 6 and 8	50 pF	1.3	3.1	4.2	ns
t_W	pulse width nLE_{AB} or nLE_{BA} HIGH	see Figs 5 and 8	50 pF	3.3	0.9	–	ns
	pulse width nCP_{AB} or nCP_{BA} HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.1	–	ns
t_{su}	set-up time nA_n before $nCP_{AB}\uparrow$ or nB_n before $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	+1.3	–0.3	–	ns
	set-up time CP HIGH or LOW nA_n before $nLE_{AB}\downarrow$ or nB_n before $nLE_{BA}\downarrow$	see Figs 7 and 8	50 pF	1.0	0.3	–	ns
t_h	hold time nA_n after $nCP_{AB}\uparrow$ or nB_n after $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	+1.3	–0.4	–	ns
	hold time CP HIGH or LOW nA_n after $nLE_{AB}\downarrow$ or nB_n after $nLE_{BA}\downarrow$	see Figs 7 and 8	50 pF	1.2	0.1	–	ns
f_{max}	maximum clock frequency	see Figs 5 and 8	50 pF	150	340	–	MHz

Notes

1. All typical values are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
2. All typical values are measured at T_{amb} = 25 °C.
3. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

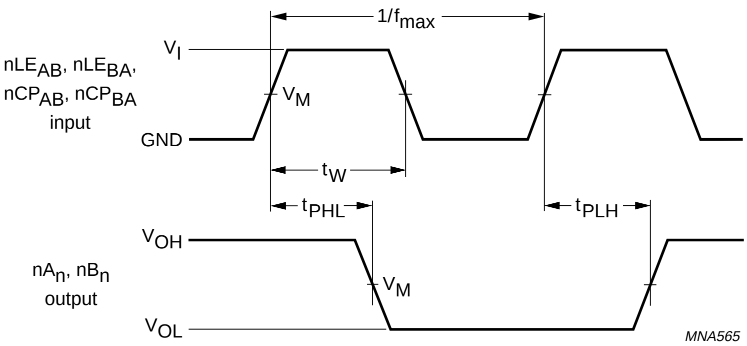
AC WAVEFORMS



V_{CC}	V_M	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

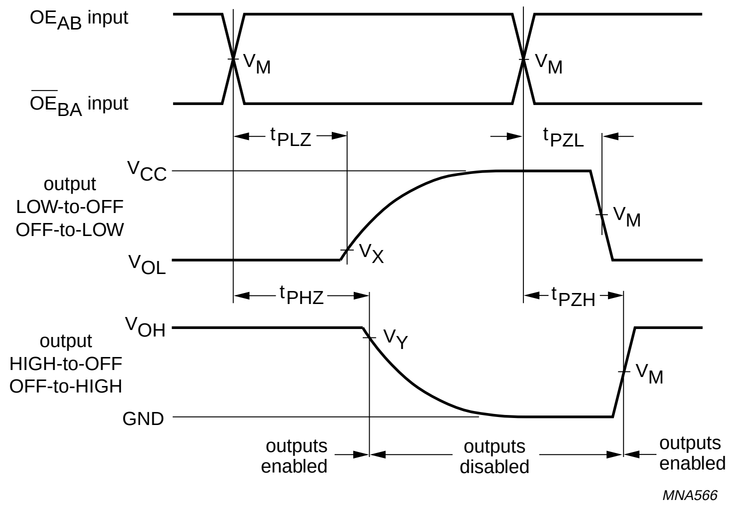
Fig.4 Input nA_n, nB_n to output nB_n, nA_n propagation delay times.



V_{CC}	V_M	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

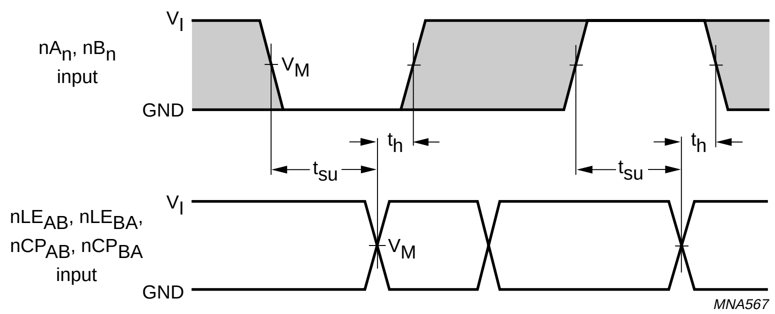
Fig.5 Latch enable input (nLE_{AB}, nLE_{BA}) and clock input (nCP_{AB}, nCP_{BA}) to output propagation delays and their pulse width.



V_{CC}	V_M	V_X	V_Y	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{OL} + 150 mV	V_{OH} – 150 mV	V_{CC}
2.7 V	1.5 V	V_{OL} + 300 mV	V_{OH} – 300 mV	2.7 V
3.0 V to 3.6 V	1.5 V	V_{OL} + 300 mV	V_{OH} – 300 mV	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.

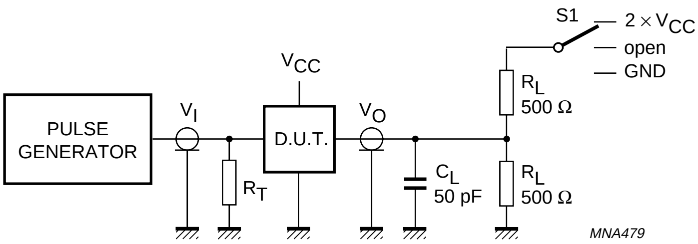


The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{CC}	V_M	V_I
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Data set-up and hold times for the nA_n and nB_n inputs to the nLE_{AB}, nLE_{BA}, nCP_{AB} and nCP_{BA} inputs.



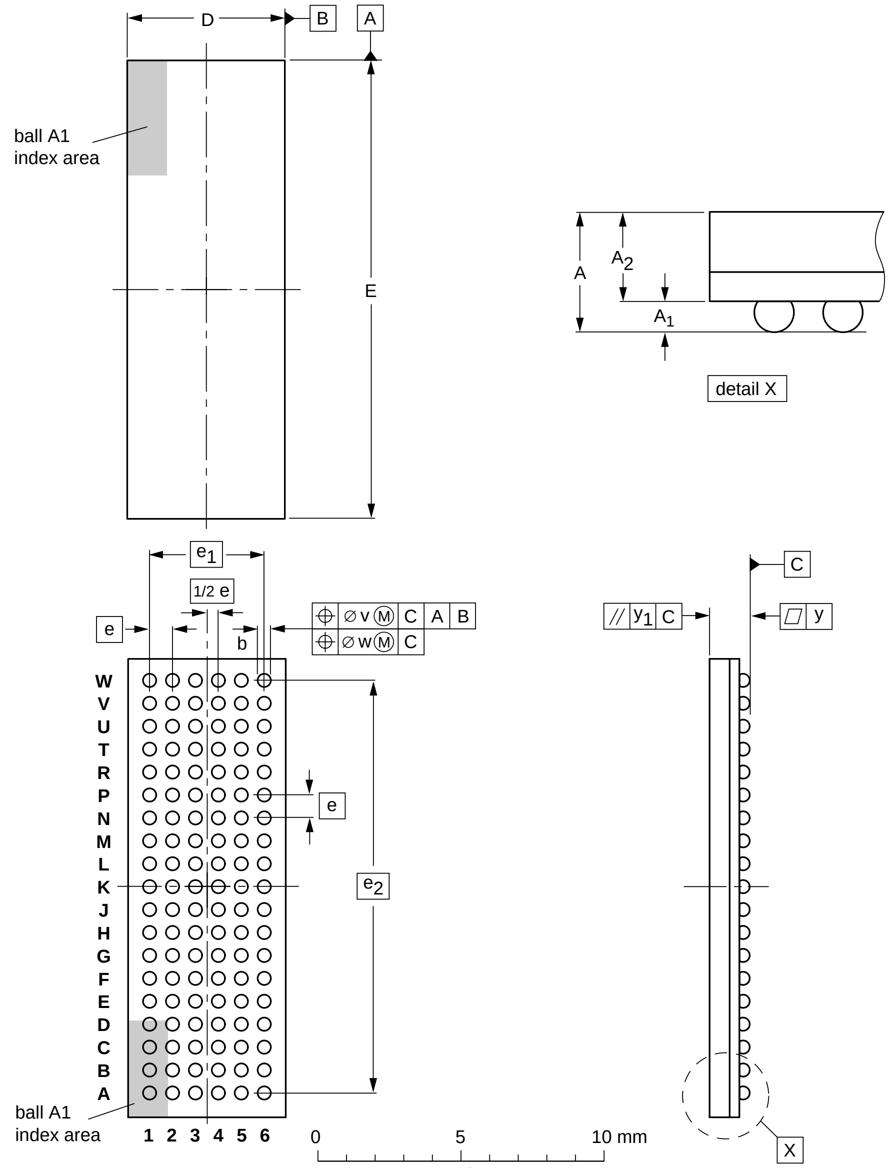
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINE

LFBGA114: plastic low profile fine-pitch ball grid array package; 114 balls; body 16 x 5.5 x 1.05 mm SOT537-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	16.1 15.9	0.8	4	14.4	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT537-1						~~00-03-04~~ 03-02-05

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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