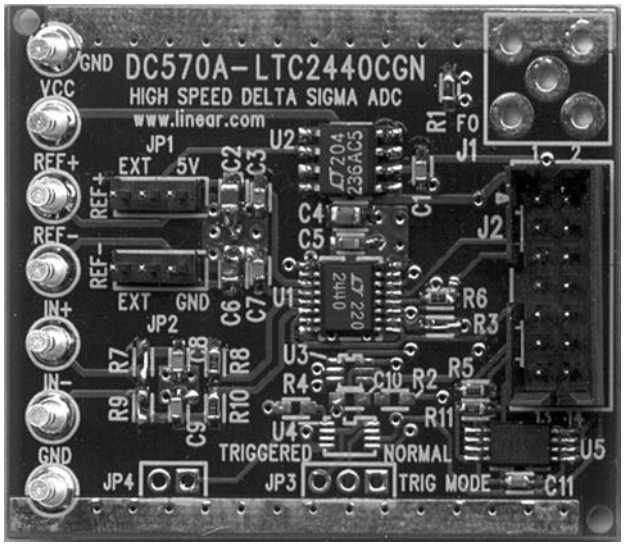
LTC2440
24-Bit High Speed Delta Sigma ADC

DESCRIPTION

The LTC®2440 is a high speed 24-bit ΔΣ ADC with 5ppm INL and 5μV offset. It uses a proprietary delta-sigma architecture enabling variable speed and resolution with no latency. Ten speed/resolution combinations (6.9Hz/200nV$_{RMS}$ to 3.5kHz/25μV$_{RMS}$) are programmed through a simple serial interface. Alternatively, by pulling the serial input pin HIGH or LOW, a fast (880Hz/2μV$_{RMS}$) or ultra low noise (6.9Hz, 200nV$_{RMS}$, 50Hz/60Hz rejection) speed/resolution combination can be easily selected. The accuracy (offset, full-scale, linearity, drift) and power dissipation are independent of the speed selected. Since there is no latency, a speed/resolution change may be made between conversions with no degradation in performance.

DC570A is a member of Linear Technology's QuikEval™ family of demonstration boards. It is designed to allow easy evaluation of the LTC2440 and may be connected directly to the target application's analog signals while using the DC590 USB Serial Controller board and supplied software to measure performance. The exposed ground planes allow proper grounding to prototype circuitry. After evaluating with LTC's software, the digital signals can be connected to the application's processor/controller for development of the serial interface.

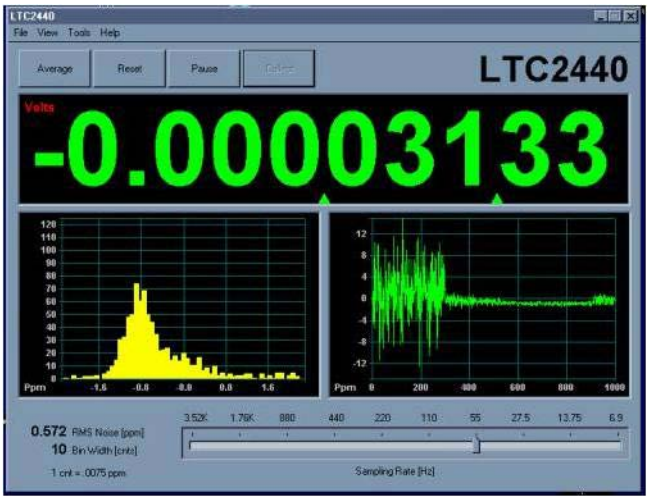
Design files for this circuit board are available at http://www.linear.com/demo/DC570A



QUICK START PROCEDURE

Connect DC570A to a DC590 USB Serial Controller using the supplied 14-conductor ribbon cable. Connect DC590 to host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or downloaded from www.linear.com/software. The correct program will be loaded automatically. Click the COLLECT button to start reading the input voltage. Click the slider at the bottom of the strip chart display to change the oversample ratio (OSR) which will in turn change the data output rate.

Tools are available for logging data, changing reference voltage, changing the number of points in the strip chart and histogram, and changing the number of points averaged for the DVM display.



HARDWARE SETUP

JUMPERS

JP1: Select the source for REF+, either external or 5.00V from the onboard LT1236 reference (default.)

JP2: Select the source for REF–, either external or Ground (0 volts, default.)

JP3: Trigger mode, either normal (default) or externally triggered.

JP4: Trigger input signal. Pin 1 is a 5V logic signal, pin 2 is ground. When triggered mode is selected on JP3, a rising edge starts a new conversion.

CONNECTION TO DC590 SERIAL CONTROLLER

J2 is the power and digital interface connector. Connect to DC590 serial controller with supplied 14-conductor ribbon cable.

ANALOG CONNECTIONS

Analog signal connections are made via the row of turret posts along the edge of the board. Also, if you are connecting the board to an existing circuit, the exposed ground planes along the edges of the board may be used to form a solid connection between grounds.

GND: Ground turrets are connected directly to the internal ground planes.

VCC: This is the supply for the ADC. Do not draw any power from this point. External power may be applied to this point after disabling the switching supply on DC590. If the DC590 serial controller is being used, the voltage must be regulated 5V only, as the isolation circuitry will also be powered from this supply.

REF+, REF–: These turrets are connected to the LTC2440 REF+ and REF– pins. If the onboard reference is being used, the reference voltage may be monitored from this point. An external reference may be connected to these terminals if JP1 and JP2 are configured for external reference.

Note: The REF+ and REF– terminals are decoupled to ground with 0.1µF and 10µF capacitors in parallel. Thus any source connected to these terminals must be able to drive a capacitive load and have very low impedance at DC. Examples are series references that require an output capacitor and C-load stable op amps such as the LT®1219 and LT1368.

IN+, IN–: These are the differential inputs to the LTC2440. These terminals have a filter consisting of a 1µF capacitor and 100Ω resistor to attenuate sampling glitches from the LTC2440 input network. These terminals should be driven by a low impedance source or op amp that is compensated to drive capacitive loads.

EXPERIMENTS

INPUT NOISE

Solder a short wire from the IN– turret post to the IN+ turret post. Set the demo software to OSR32768 (6.8 samples per second.) Noise should be approximately 0.04ppm of V_{REF} (200nV.) Next, select different oversample ratios. Measured noise for each oversample ratio should be close to values given in the LTC2440 data sheet.

COMMON MODE REJECTION

Tie the two inputs (still connected together from previous experiment) to ground through a short wire and note the indicated voltage. Tie the inputs to REF+; the difference should be less than 5µV due to the 120dB CMRR of the LTC2440.

RESOLVING MILLIAMPS WITH MILLIOHM SHUNTS

One application that can benefit greatly from the LTC2440's input resolution is current measurement. It is advantageous to use a very low resistance shunt to minimize the voltage drop. To demonstrate this, make a simple current shunt by soldering a 1 inch length of 24 gage copper wire from the IN+ turret to the IN– turret. This is a resistance of approximately 2.4 milliohms. Connect the IN– turret to the GND turret through a short wire. Start the demonstration software and note the initial voltage, which should be close to zero. Next, connect IN+ to REF+ through a 5k resistor, which will allow approximately 1mA to flow through the shunt. The indicated voltage should increase by approximately 2.4µV (The actual increase will depend on the tolerance of the wire material, diameter, and length.)

Since the common mode range of the inputs extends from ground to VCC, the current shunt can also be used at the high side. To demonstrate this, tie the IN+ turret to VCC and connect the resistor from IN– to ground. Thus the supply current of a circuit can be monitored with minimal impact on supply voltage and without breaking any ground connections.

BIPOLAR SYMMETRY

To demonstrate the symmetry of the ADCs transfer function, connect a stable, low noise, floating voltage source (with a voltage less than $V_{REF}/2$) from IN+ to IN– and note the indicated voltage. Reverse the polarity; the indicated voltage should be within 75µV of the first reading multiplied by –1, and will typically be much closer.

One convenient voltage source is a single alkaline battery. While a battery is fairly low noise, it is sensitive to temperature drift and will slowly discharge due to the LTC2440 input current. It is best to use a large (D-size) battery that is insulated from air currents. A better source is a battery powered series reference that can drive the 1µF input capacitor such as the LT1790. This part is available with output voltages of 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V.

INPUT NORMAL MODE REJECTION

The LTC2440's SINC4 digital filter is trimmed to strongly reject both 50Hz and 60Hz line noise when operated with the internal conversion clock and oversample ratio 32768 (6.8 samples per second.) To measure input normal mode rejection, connect IN– to a 2.5V source such as an LT1790-2.5 reference or a power supply. Apply a 10Hz, 2V peak-to-peak sine wave to IN+ through a 1µF capacitor. Note that this will form a 2:1 divider with the 1µF load capacitor on the board. A larger capacitor may be used to reduce this attenuation.

Select OSR32768 (6.8 samples per second) in the demo software and start taking data. The input noise will be quite large, and the graph of output vs time should show large variations.

EXPERIMENTS

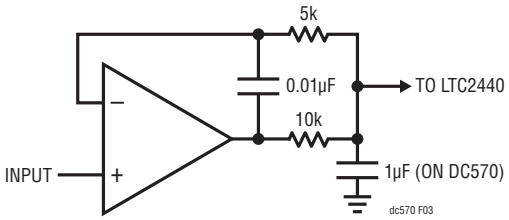
Next, slowly increase the frequency to 55Hz. The noise should be almost undetectable in the graph. Note that the indicated noise in ppm may still be above that of the data sheet specification because the inputs are not connected to a DC source.

Change the OSR to 16384 (13.75 samples per second;) the noise will increase substantially, as the first notch at this OSR is at 110Hz. Increase the signal generator frequency to 110Hz, the noise will drop again.

BUFFERING THE INPUTS

The input current of the LTC2440 may be as much as 63µA (depending on input and reference voltages; see applications information in the LTC2440 data sheet for details). If this produces unacceptable errors due to source impedance, a buffer may be necessary.

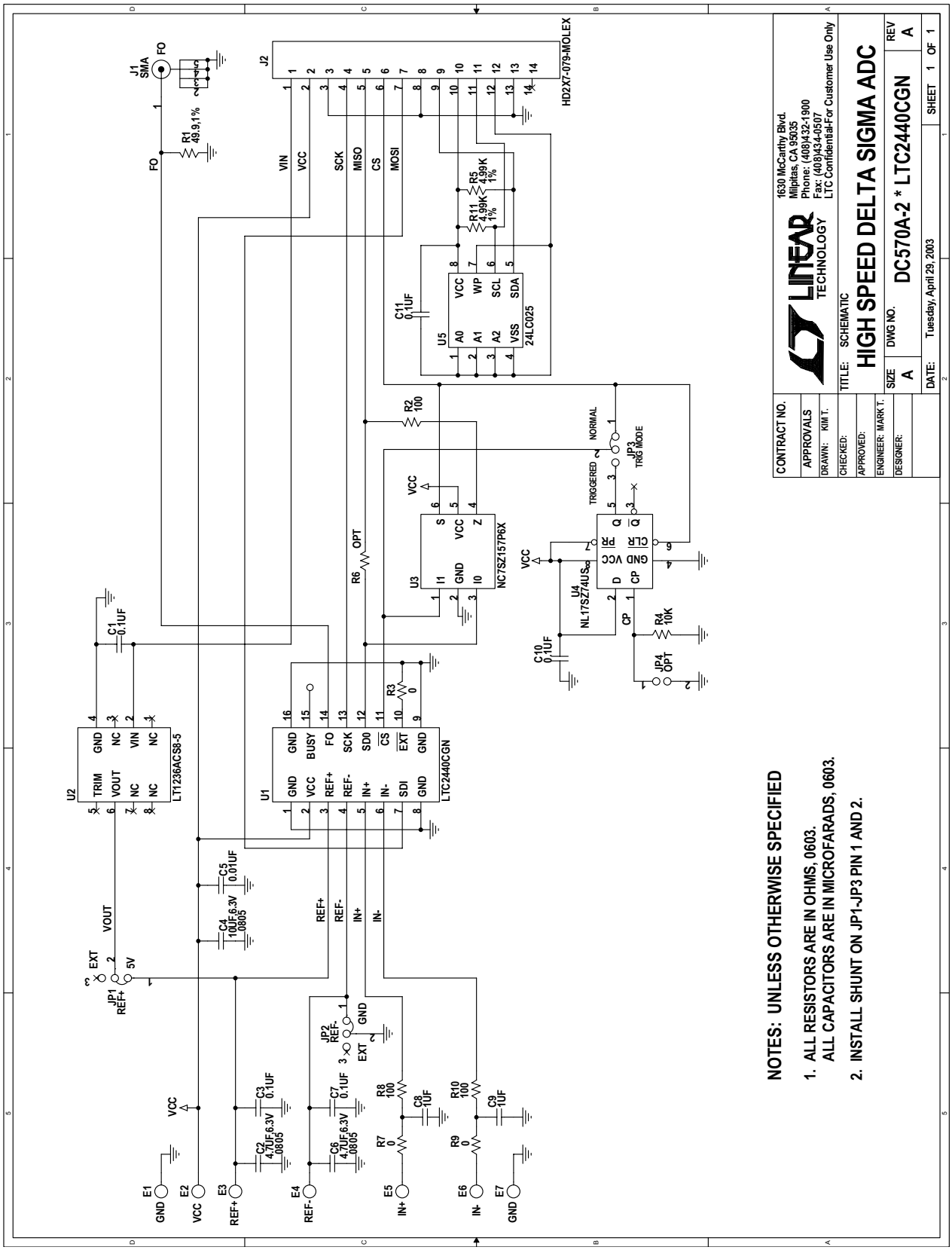
Most op amps will not drive a 1µF capacitor directly. The following schematic shows how to compensate almost any amplifier to drive the capacitors on the DC570A board while maintaining DC accuracy. The LTC2050HV (or the dual LTC2051HV) is a good general purpose autozero amplifier for use as a buffer in DC applications.



PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	5	C1, C3, C7, C10, C11	CAP., X7R 0.1µF 16V 20% 0603	AVX, 0603YC104MAT1A
2	2	C2, C6	CAP., X5R 4.7µF 6.3V 20% 0805	TAIYO YUDEN, JMK212BJ475MGT
3	1	C4	CAP., X5R 10µF 6.3V 20% 0805	TDK, C2012X5R0J106M
4	1	C5	CAP., X7R 0.01µF 16V 10% 0603	AVX, 0603YC103KAT1A 2rls
5	2	C8, C9	CAP., X5R 1µF 6.3V 20% 0603	TAIYO YUDEN, JMK107ABJ105MA-T
6	7	E1, E2, E3, E4, E5, E6, E7	TESTPOINT, TURRET, 0.061" PbF	MILL-MAX, 2308-2-00-80-00-00-07-0
7	3	JP1, JP2, JP3	HEADER, 3 PIN 0.079" SINGLE ROW	SAMTEC, TMM-103-02-L-S
8	3	SHUNTS FOR JP1-JP3	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
9	0	JP4	JMP, HD1X2-079	OPT
10	0	J1	CONN., 5 PIN GOLD, STRAIGHT	OPT
11	1	J2	HEADER, 2X7 PIN, 0.079CC	MOLEX, 87831-1420
12	1	R1	RES., CHIP 49.9Ω 1/16W 1% 0603	AAC, CR16-49R9FM
13	3	R2, R8, R10	RES., CHIP 100Ω 1/16W 5% 0603	AAC, CR16-101JM 3rls
14	3	R3, R7, R9	RES., CHIP 0Ω 1/16W 5% 0603	AAC, CJ06-000M
15	1	R4	RES., CHIP 10k 1/16W 5% 0603	AAC, CR16-103JM
16	2	R5, R11	RES., CHIP 4.99k 1/16W 1% 0603	AAC, CR16-4991FM
17	0	R6	RES., 0603	OPT
18	1	U1	I.C., LTC2440CGN#PBF, SSOP16GN	LINEAR TECH., LTC2440CGN#PBF
19	1	U2	I.C., LT1236ACS8-5, SO8	LINEAR TECH., LT1236ACS8-5#PBF
20	1	U3	I.C., NC7SZ157P6X, SC70-6P	FAIRCHILD SEMI., NC7SZ157P6X
21	1	U4	I.C., FLIP FLOP D-TYPE LOG US8	ON SEMI., NL17SZ74USG
22	1	U5	I.C., EEPROM 2k BIT 400kHz 8TSSOP	MICROCHIP, 24LC025-I /ST 3rls

SCHEMATIC DIAGRAM



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Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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