PTFA192401E
PTFA192401F

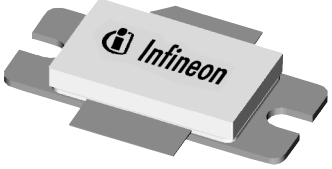
green Product

Thermally-Enhanced High Power RF LDMOS FETs
240 W, 1930 – 1990 MHz

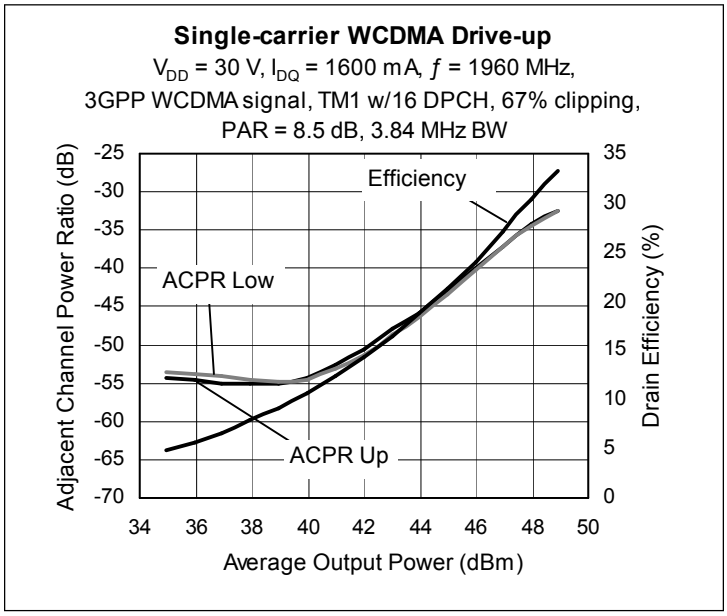
Description

The PTFA192401E and PTFA192401F are 240-watt LDMOS FETs intended for single- and two-carrier WCDMA and CDMA applications from 1930 to 1990 MHz. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA192401E
Package H-36260-2



PTFA192401F
Package H-37260-2



Features

- Pb-free, RoHS-compliant and thermally-enhanced packages
- Broadband internal matching
- Typical two-carrier WCDMA performance at 1960 MHz, 30 V
  - Average output power = 47.0 dBm
  - Linear Gain = 16 dB
  - Efficiency = 27.5%
  - Intermodulation distortion = –35 dBc
  - Adjacent channel power = –41 dBc
- Typical single-carrier WCDMA performance at 1960 MHz, 30 V, 3GPP signal, PAR = 8.5 dB
  - Average output power = 49 dBm
  - Linear Gain = 16 dB
  - Efficiency = 33%
  - Adjacent channel power = –33 dBc
- Typical CW performance, 1960 MHz, 30 V
  - Output power at P–1dB = 240 W
  - Efficiency = 54%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 5:1 VSWR @ 30 V, 240 W (CW) output power

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 50 W average
f_1 = 1955 MHz, f_2 = 1965 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15	16	—	dB
Drain Efficiency	η_D	25	27	—	%
Intermodulation Distortion	IMD	—	–36	–34	dBc

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 220 W PEP, f = 1960 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	15.8	—	dB
Drain Efficiency	η_D	—	40	—	%
Intermodulation Distortion	IMD	—	–28	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Drain Leakage Current	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.03	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1.6 A	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	761	W
Above 25°C derate by		4.35	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 50 W WCDMA)	$R_{\theta JC}$	0.23	°C/W

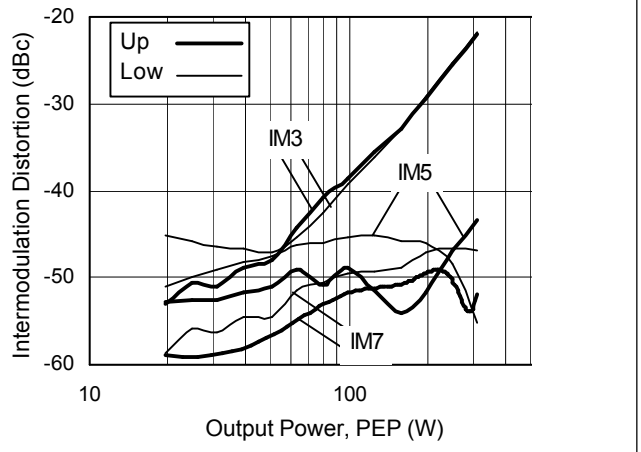
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA192401E V4	H-36260-2	Thermally-enhanced slotted flange, single-ended	PTFA192401E
PTFA192401F V4	H-37260-2	Thermally-enhanced earless flange, single-ended	PTFA192401F

Typical Performance (data taken in a production test fixture)

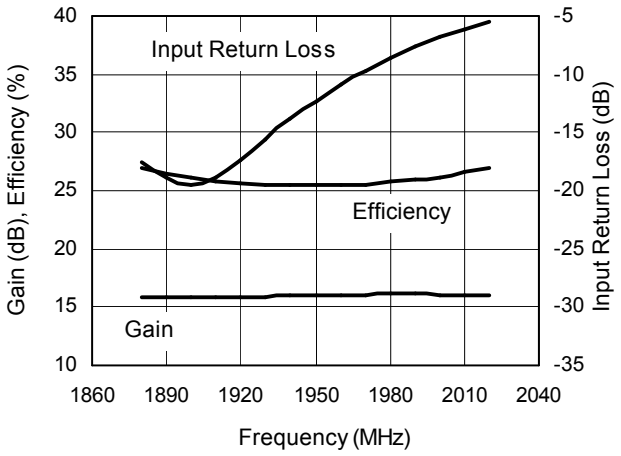
Intermodulation Distortion Products v. Output Power

V_{DD} = 30 V, I_{DQ} = 1600 mA,
f_1 = 1957.5 MHz, f_2 = 1962.5 MHz



Broadband Performance

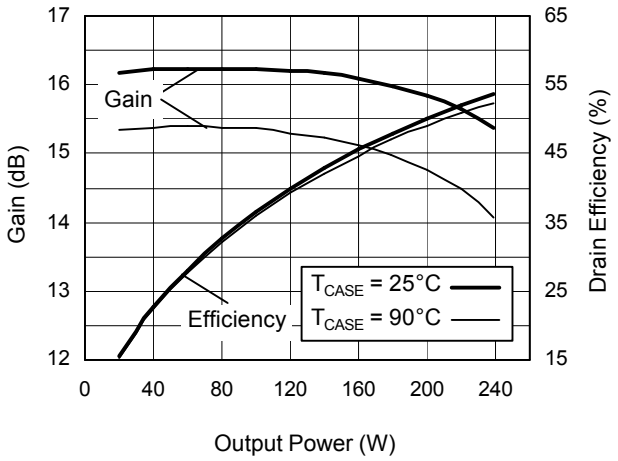
V_{DD} = 30 V, I_{DQ} = 1600 mA, P_{OUT} = 50 W



Typical Performance (cont.)

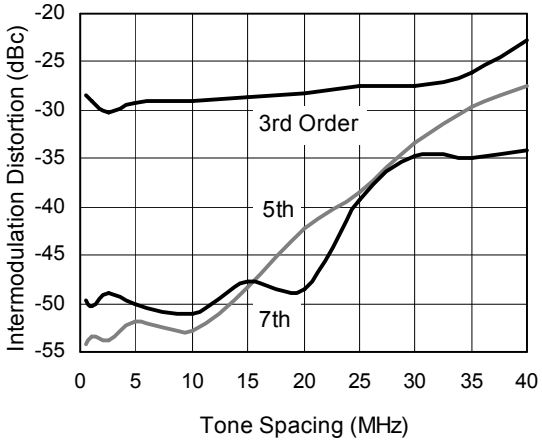
Power Sweep, CW Conditions

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1990 MHz



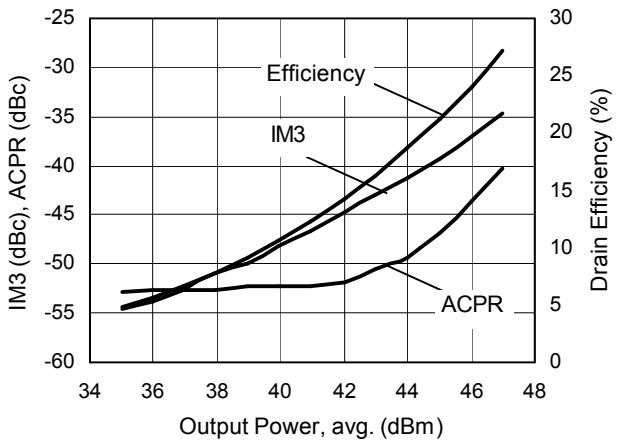
Intermodulation Distortion Products vs. Tone Spacing

V_{DD} = 30 V I_{DQ} = 1800 mA, f = 1960 MHz,
P_{OUT} = 53 dBm PEP



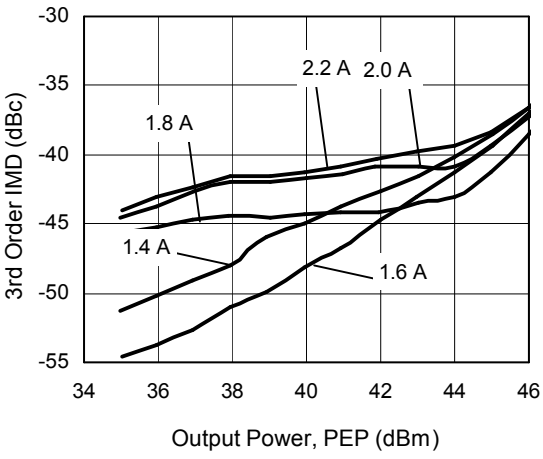
Two-carrier WCDMA Drive-up

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1960 MHz, 3GPP WCDMA signal, PAR = 8 dB, 10 MHz carrier spacing



Two-carrier WCDMA at Selected Biases

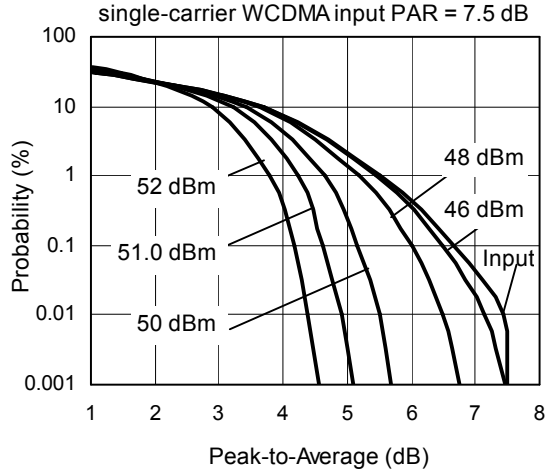
V_{DD} = 30 V, f = 1960 MHz, 3GPP WCDMA signal, PAR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



Typical Performance (cont.)

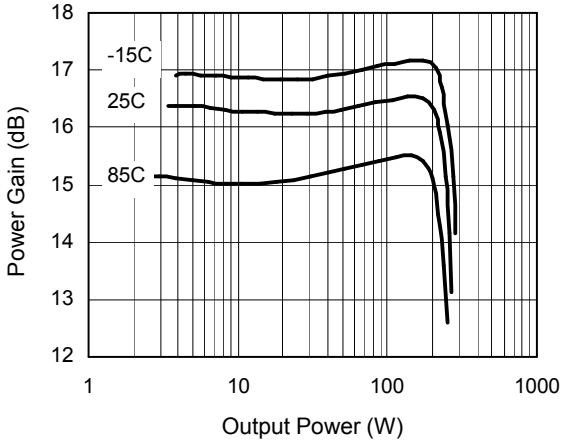
Output Peak-to-Average Ratio Compression (PARC) at various Power levels

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1990 MHz, single-carrier WCDMA input PAR = 7.5 dB



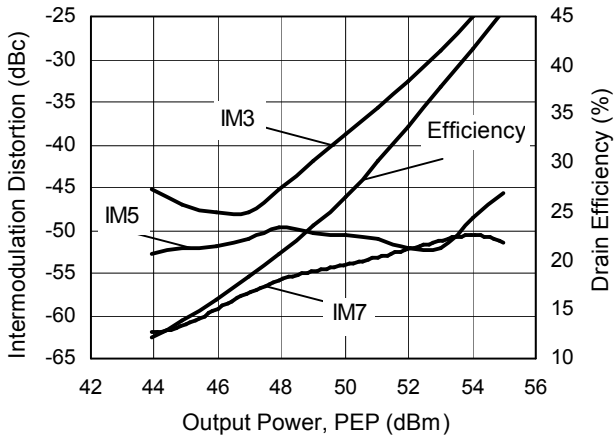
Power Gain vs. Power Sweep (CW) over Temperature

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 1990 MHz



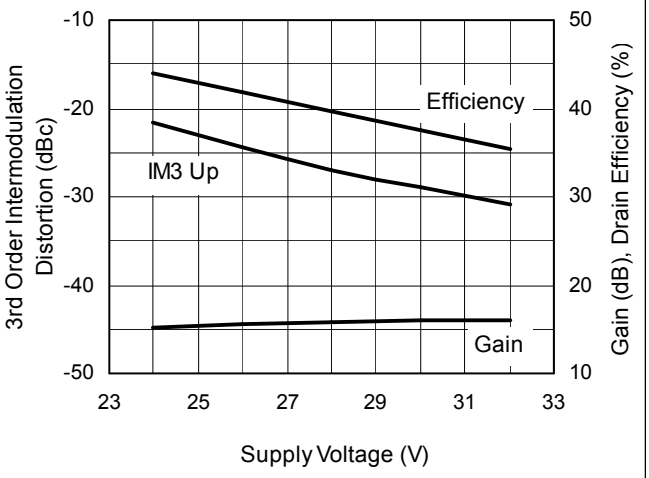
Two-tone Drive-up

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 1960 MHz, tone spacing = 1 MHz

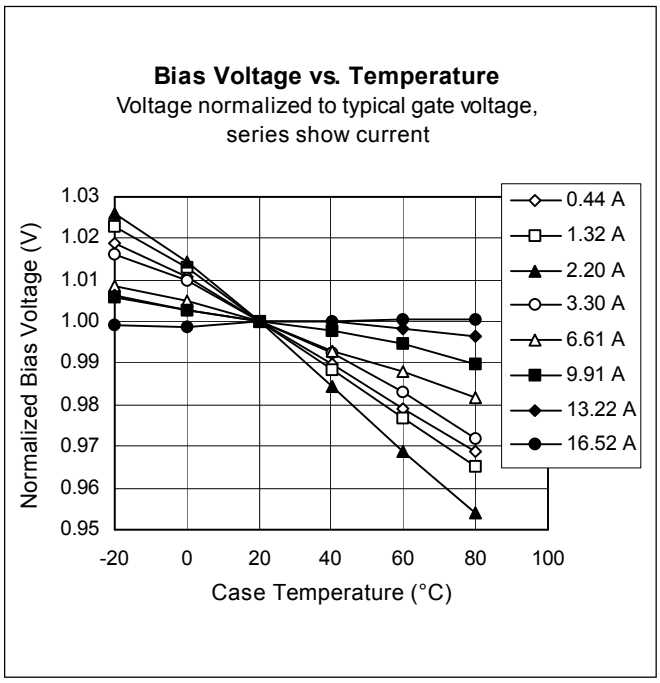


Voltage Sweep

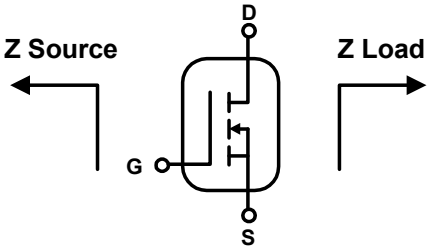
I_{DQ} = 1600 mA, f = 1960 MHz, tone spacing = 1 MHz, Output Power (PEP) = 53 dBm



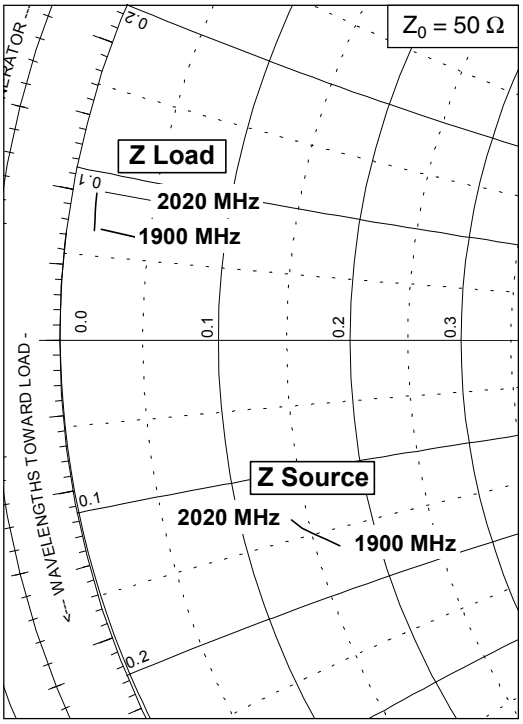
Typical Performance (cont.)



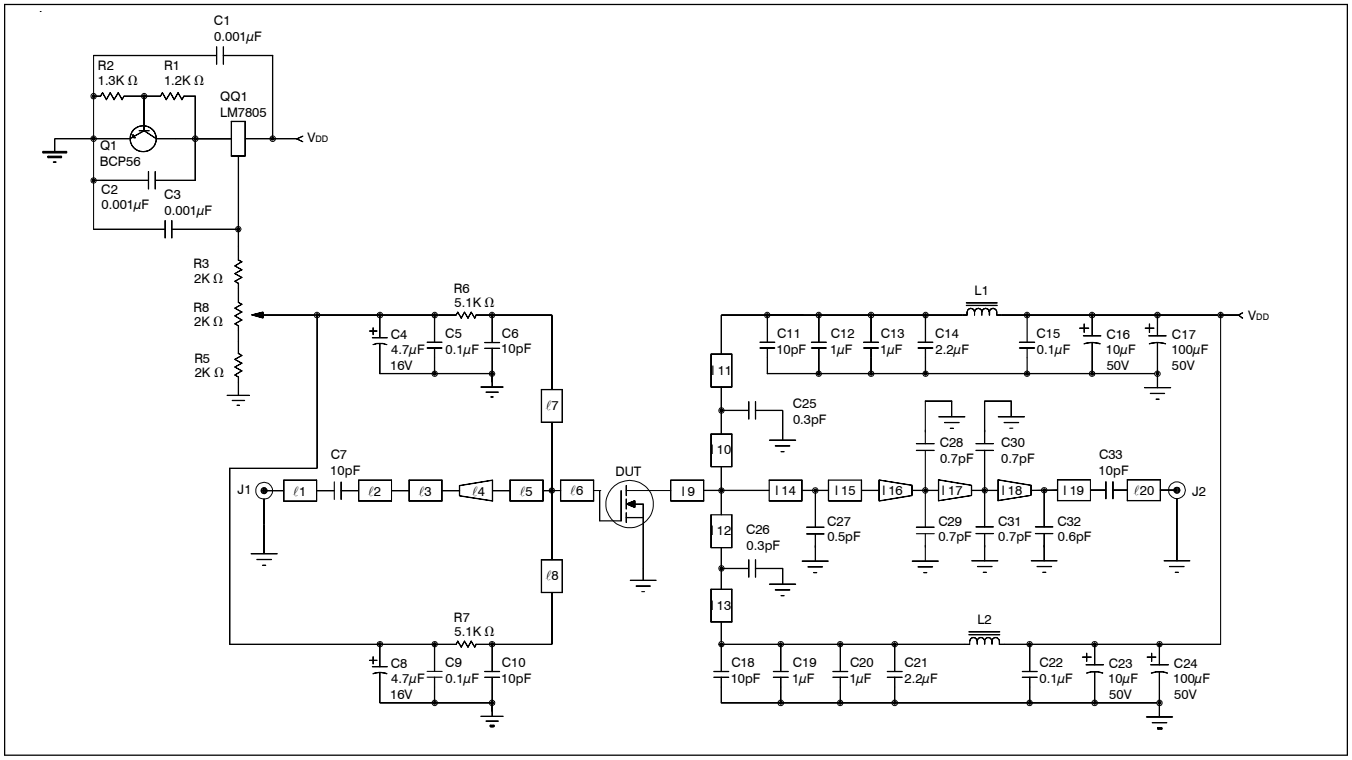
Broadband Circuit Impedance



Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
1900	8.43	–8.22	0.80	3.26
1930	8.00	–7.86	0.78	3.56
1960	7.57	–7.51	0.76	3.84
1990	7.19	–7.17	0.73	4.12
2020	6.86	–6.77	0.72	4.38



Reference Circuit

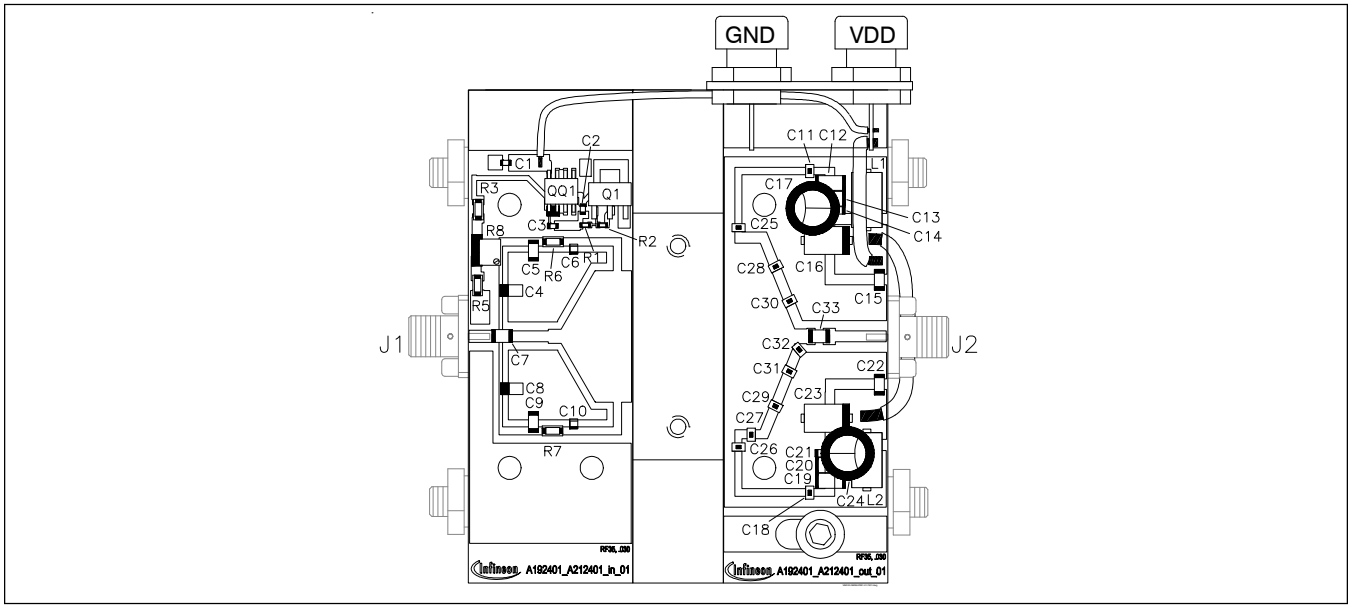


Reference circuit schematic for ƒ = 1960 MHz

Circuit Assembly Information			
DUT	PTFA192401E or PTFA192401F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, RF35, ε_r = 3.48	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 1960 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.038 λ, 50.0 Ω	3.51 x 1.70	0.138 x 0.067
ℓ2	0.071 λ, 50.0 Ω	6.60 x 1.70	0.260 x 0.067
ℓ3	0.022 λ, 43.1 Ω	2.01 x 2.16	0.079 x 0.085
ℓ4	0.060 λ, 43.1 Ω / 6.9 Ω	5.28 x 2.16 / 20.32	0.208 x 0.085 / 0.800
ℓ5	0.040 λ, 6.9 Ω	3.33 x 20.32	0.131 x 0.800
ℓ6	0.026 λ, 6.9 Ω	2.21 x 20.32	0.087 x 0.800
ℓ7, l8	0.123 λ, 59.9 Ω	11.48 x 1.24	0.452 x 0.049
ℓ9	0.010 λ, 5.0 Ω	0.84 x 28.91	0.033 x 1.138
ℓ10, l12	0.027 λ, 51.0 Ω	2.54 x 1.65	0.100 x 0.065
ℓ11, l13	0.228 λ, 51.0 Ω	21.03 x 1.65	0.828 x 0.065
ℓ14, l15	0.028 λ, 5.0 Ω	2.36 x 28.91	0.093 x 1.138
ℓ16	0.011 λ, 5.0 Ω / 6.0 Ω	0.89 x 28.91 / 23.65	0.035 x 1.138 / 0.931
ℓ17	0.030 λ, 6.0 Ω / 12.3 Ω	2.54 x 23.65 / 10.67	0.100 x 0.931/ 0.420
ℓ18	0.019 λ, 12.3 Ω / 41.2 Ω	1.78 x 10.67 / 2.29	0.070 x 0.420 / 0.090
ℓ19	0.033 λ, 41.2 Ω	3.05 x 2.29	0.120 x 0.090
ℓ20	0.096 λ, 50.0 Ω	8.99 x 1.70	0.354 x 0.067

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C8	Capacitor, 4.7 µF, 16V	Digi-Key	PCS3475CT-ND
C5, C9, C15, C22	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C10	Ceramic capacitor, 10 pF	ATC	100A 100
C7, C33	Ceramic capacitor, 10 pF	ATC	100B 100
C11, C18	Capacitor, 10 pF	AVX	08051J100GBTTR
C12, C13, C19, C20	Ceramic capacitor, 1 µF	Digi-Key	445-1411-1-ND
C14, C21	Capacitor, 2.2 µF	Digi-Key	445-1447-2-ND
C16, C23	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C17, C24	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	P5571-ND
C25, C26	Capacitor, 0.3 pF	AVX	08051J0R3BBTTR
C27	Capacitor, 0.5 pF	AVX	08051J0R5BBTTR
C28, C29, C30, C31	Capacitor, 0.7 pF	AVX	08051J0R7BBTTR
C32	Capacitor, 0.6 pF	ATC	600S0R6BT
L1, L2	Ferrite, 8.9mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2k ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3k ohms	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor 2k ohms	Digi-Key	P2KECT-ND
R4	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor 5.1k ohms	Digi-Key	P5.1KECT-ND
R8	Potentiometer 2k ohms	Digi-Key	3224W-202ETR-ND

**Gerber files for this circuit available on request*

Package Outline Specifications

Package H-36260-2

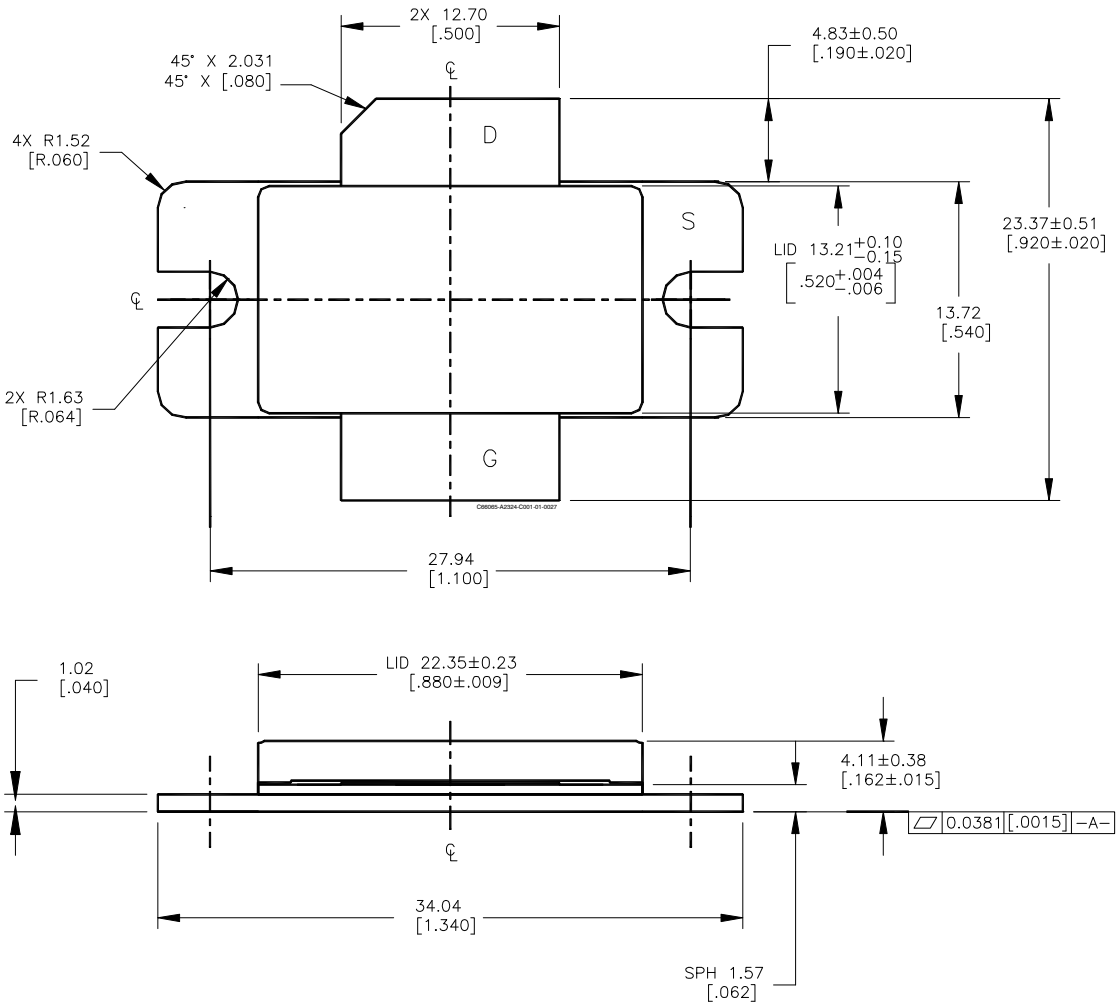


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: D = drain, S = source, G = gate.
3. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
4. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]
5. All tolerances ± 0.127 [.005] unless specified otherwise.
6. Primary dimensions are mm. Alternate dimensions are inches.

Find the latest and most complete information about products and packaging at the Infineon Internet page ***http://www.infineon.com/rfpower***

Package Outline Specifications (cont.)

Package H-37260-2

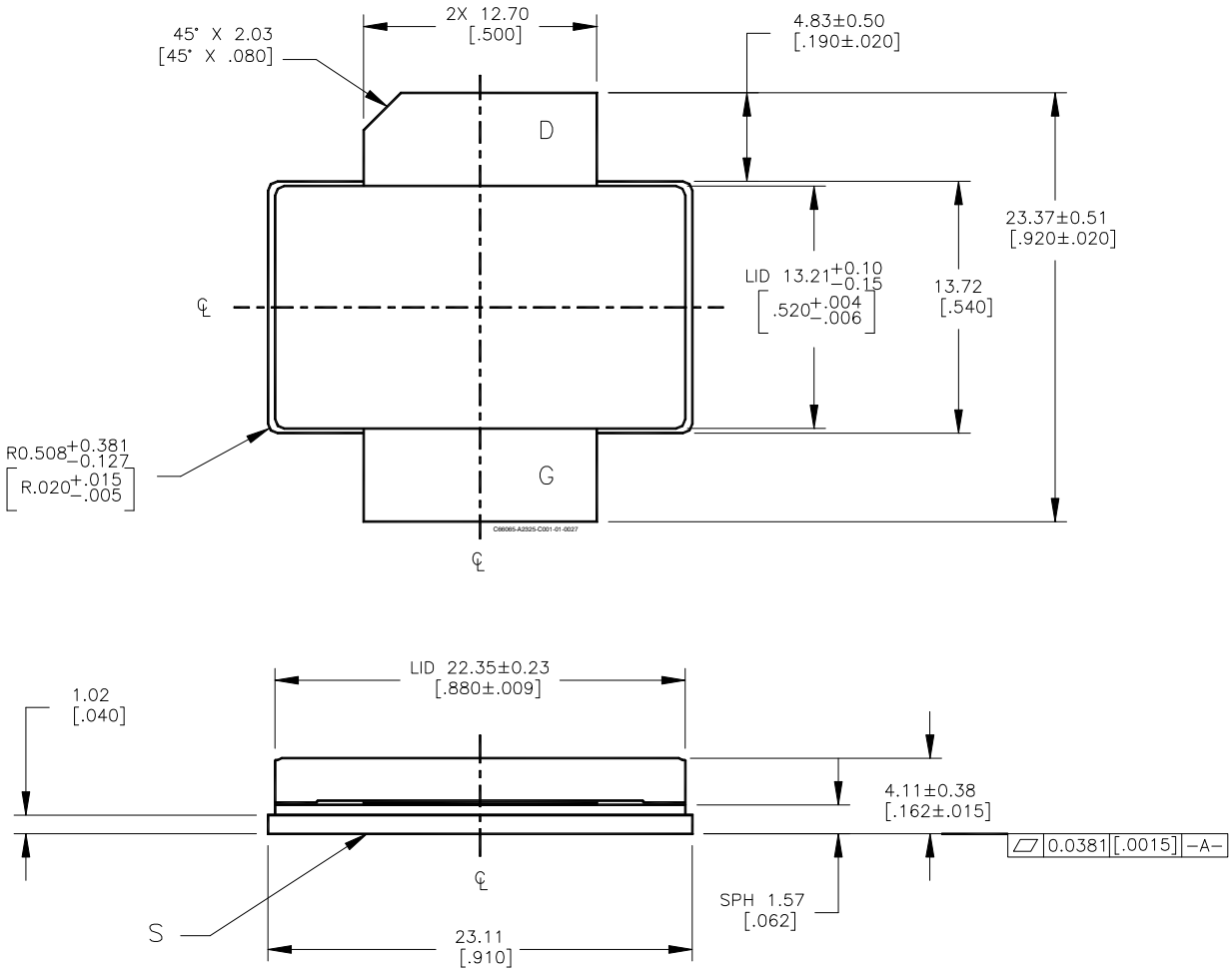


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: D = drain, S = source, G = gate.
3. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
4. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]
5. All tolerances ± 0.127 [.005] unless specified otherwise.
6. Primary dimensions are mm. Alternate dimensions are inches.

Find the latest and most complete information about products and packaging at the Infineon Internet page ***http://www.infineon.com/rfpower***

Revision History:	2009-04-01	Data Sheet
Previous Version:	2008-10-06	

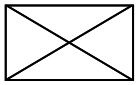
Page	**Subjects (major changes since last revision)**
9, 10	Update package information

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:

highpowerRF@infineon.com

To request other information, contact us at:
+1 877 465 3667 (1-877-GO-LDMOS) USA
or +1 408 776 0600 International



GOLDMOS® is a registered trademark of Infineon Technologies AG.

Edition 2009-04-01

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com/rfpower**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.