N0413N

R07DS0555EJ0100
Rev.1.00
Nov 07, 2011

N-CHANNEL MOSFET FOR SWITCHING

Description

The N0413N is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  $R_{DS\,(on)}$ = 3.3 mΩ MAX. (V_{GS} = 10 V, I_D = 50 A)
- Low input capacitance
  C_{iss} = 5550 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- High current
  $I_{D(DC)}$ = ±100 A
- RoHS Compliant

Ordering Information

Part No.	Lead Plating	Packing	Package
N0413N-ZK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	TO-263 1.39 g TYP.
N0413N-ZK-E2-AY *1			

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C, all terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±100	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±400	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	119	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current *2	I_{AS}	55	A
Single Avalanche Energy *2	E_{AS}	300	mJ

Thermal Resistance

Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.05	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W

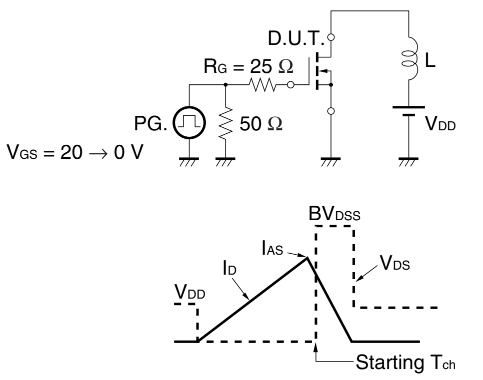
Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{DD} = 25 V, V_{GS} = 20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C, all terminals are connected)

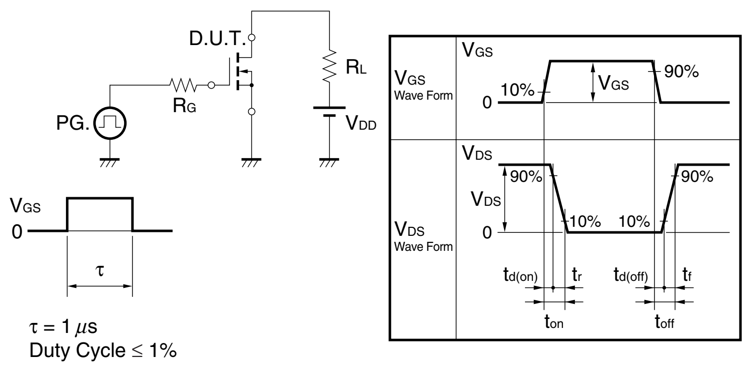
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Cut-off Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	$\mid y_{fs} \mid$	26			S	V_{DS} = 10 V, I_D = 50 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$		2.3	3.3	mΩ	V_{GS} = 10 V, I_D = 50 A
Input Capacitance	C_{iss}		5550		pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		580		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		320		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		29.0		ns	V_{DD} = 20 V, I_D = 50 A,
Rise Time	t_r		15.0		ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		64.0		ns	R_G = 0 Ω
Fall Time	t_f		13.0		ns	
Total Gate Charge	Q_G		100		nC	V_{DD} = 32 V,
Gate to Source Charge	Q_{GS}		26		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		32		nC	I_D = 100 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$			1.5	V	I_F = 100 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		40		ns	I_F = 50 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		44		nC	di/dt = 100 A/μs

Note: *1. Pulsed

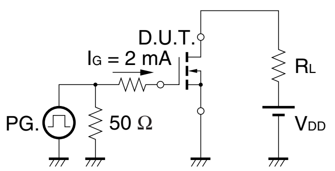
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

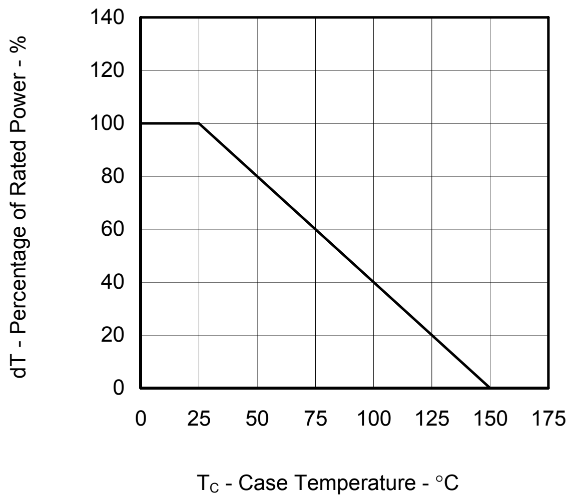


TEST CIRCUIT 3 GATE CHARGE

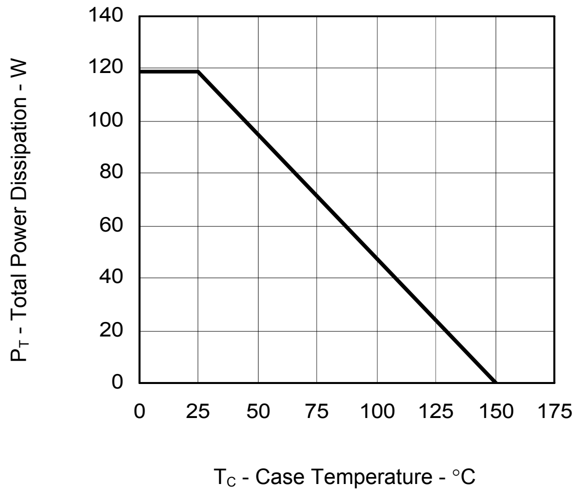


Typical Characteristics (T_A = 25°C)

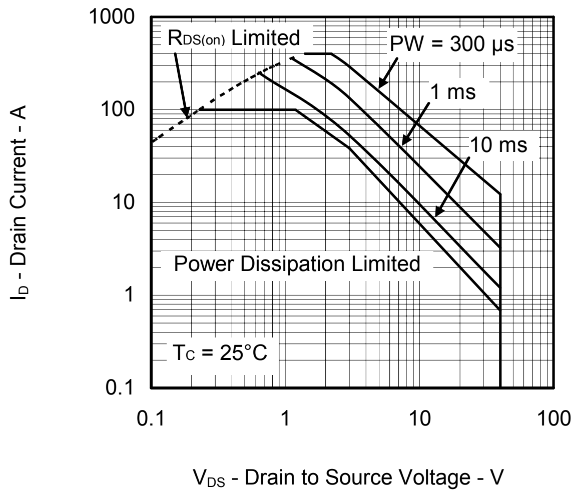
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



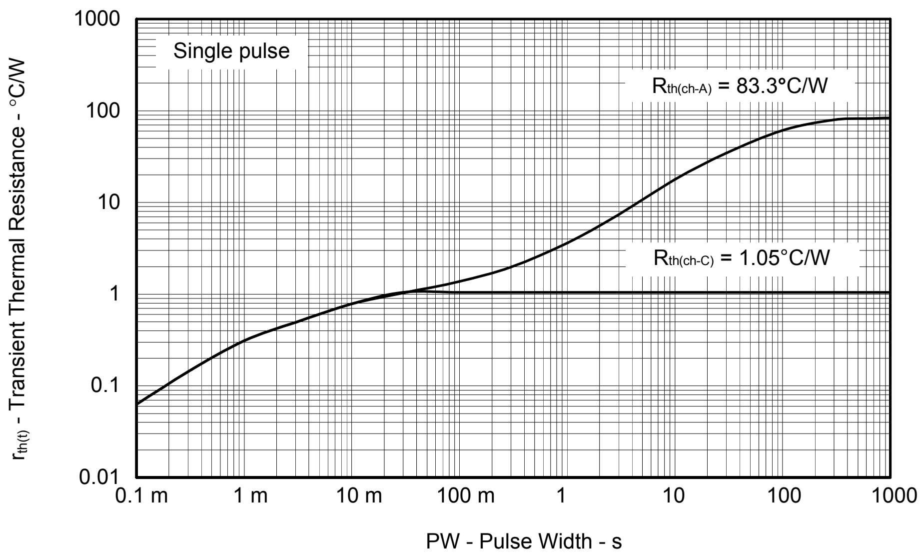
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



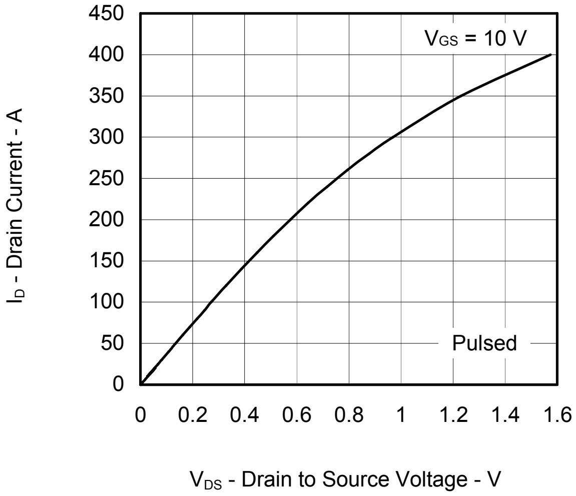
FORWARD BIAS SAFE OPERATING AREA



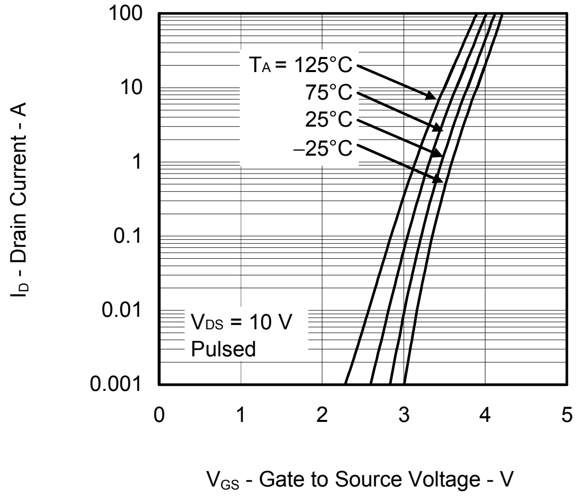
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



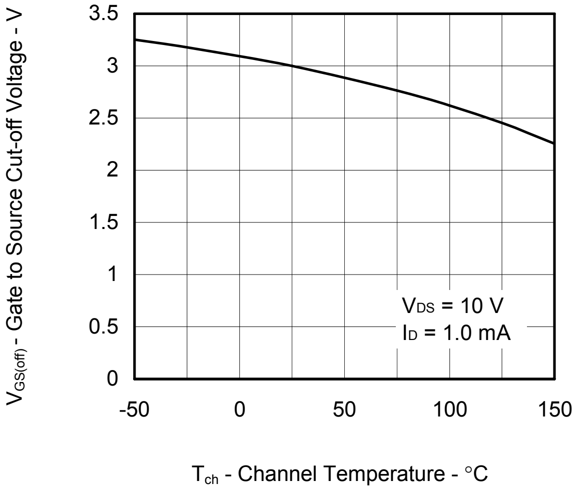
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



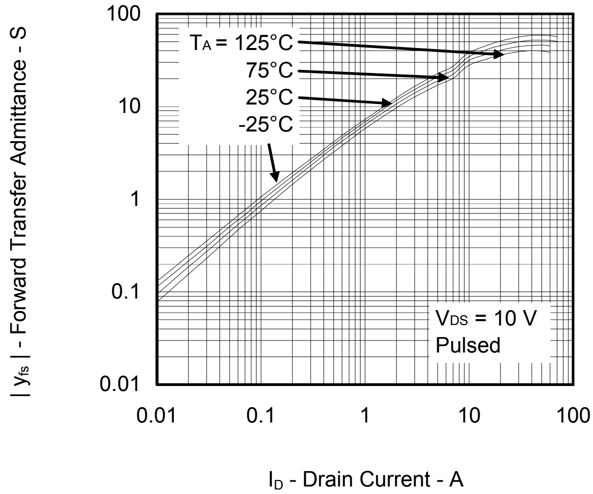
FORWARD TRANSFER CHARACTERISTICS



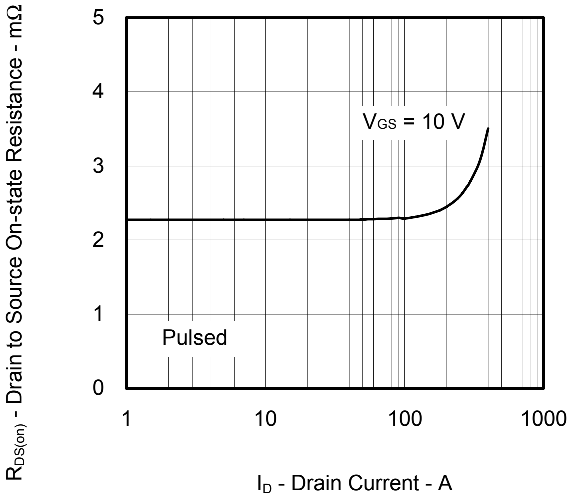
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



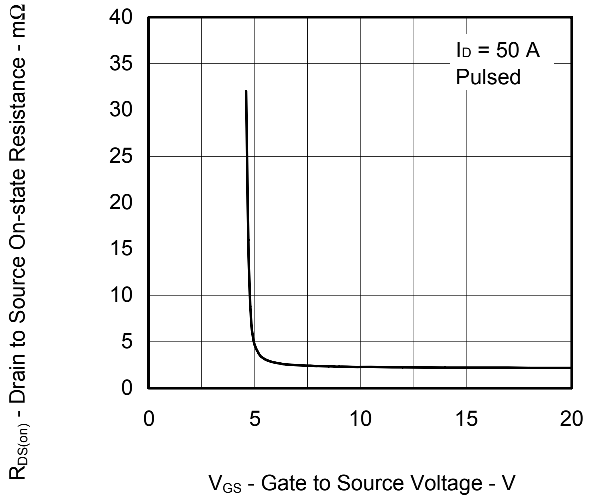
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



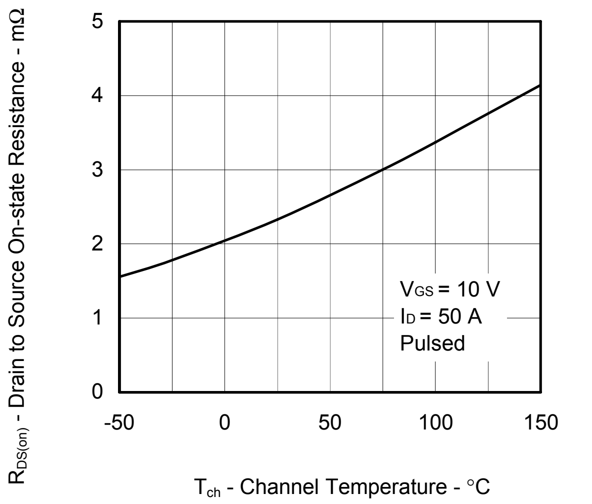
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



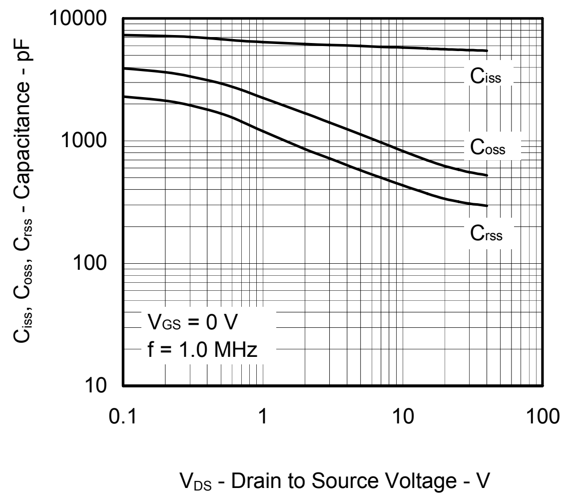
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



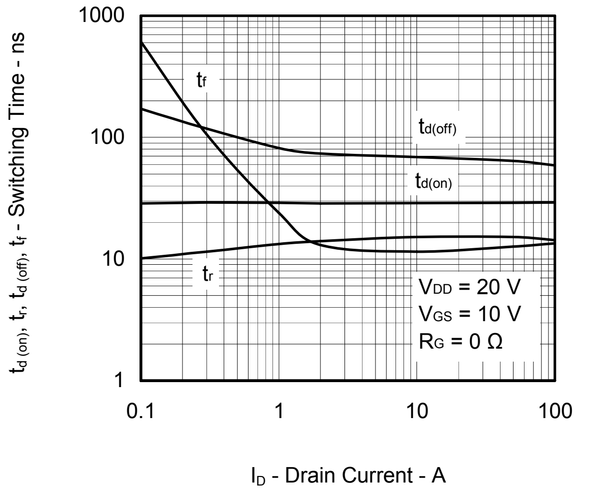
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



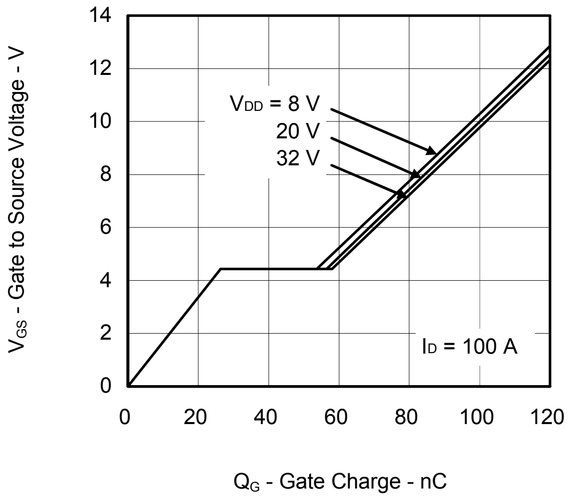
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



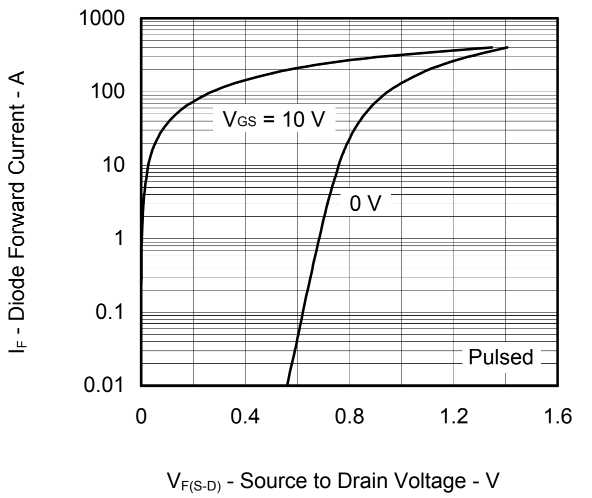
SWITCHING CHARACTERISTICS



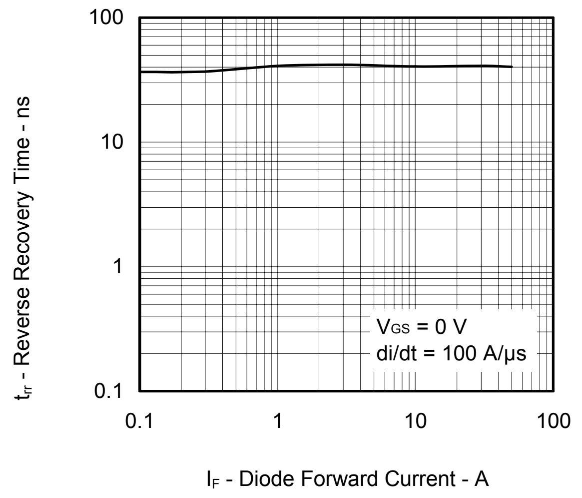
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

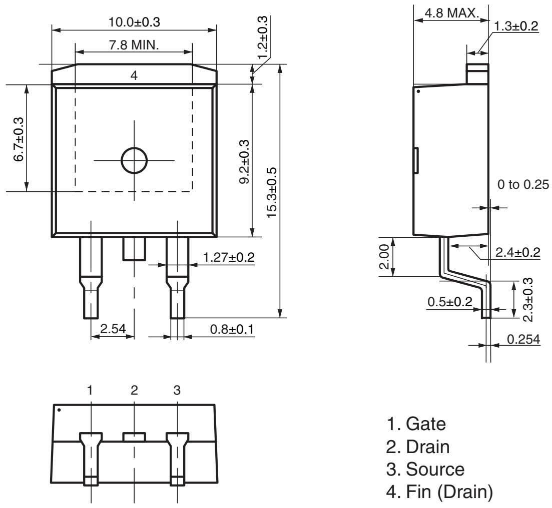


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



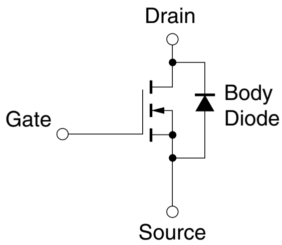
Package Drawing (Unit: mm)

TO-263



1. Gate
2. Drain
3. Source
4. Fin (Drain)

Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	N0413N Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 07, 2011	–	First Edition Issued

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