NB3L853141

2.5V/3.3V 1:5 LVPECL Fanout Buffer

ON Semiconductor®

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Description

The NB3L853141 is a low skew 1:5 LVPECL Clock fanout buffer designed explicitly for low output skew applications.

The NB3L853141 features a multiplexed input which can be driven by either a differential or single−ended input to allow for the distribution of a lower speed clock along with the high speed system clock.

The SEL pin will select the differential clock inputs, CLK0 & $\overline{CLK0}$, when LOW (or left open and pulled LOW by the internal pull−down resistor). When SEL is HIGH, the single−ended CLK1 input is selected.

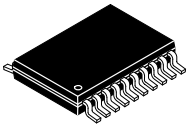
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Features

- 700 MHz Maximum Clock Output Frequency
- CLK0 and $\overline{CLK0}$ can Accept Differential LVPECL, LVDS, HCSL, LVHSTL, SSTL, LVCMOS
- CLK1 can Accept LVCMOS and LVTTL
- Five Differential LVPECL Clock Outputs
- 1.5 ns Maximum Propagation Delay
- Operating Range: V_{CC} = 2.375 V to 3.8 V
- LVCMOS Compatible Control Inputs
- Selectable Differential or LVCMOS Clock Inputs
- Synchronous Clock Enable
- 30 ps Max. Skew Between Outputs
- −40°C to +85°C Ambient Operating Temperature Range
- TSSOP−20 Package
- These are Pb−Free Devices

Applications

- Computing and Telecom
- Routers, Servers and Switches
- Backplanes



TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

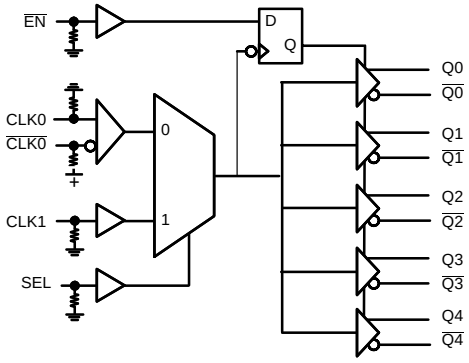
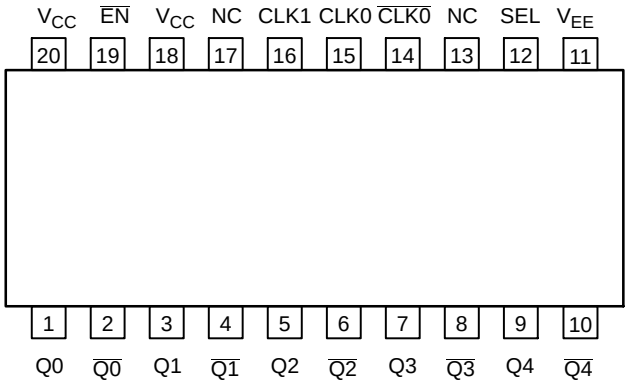


Figure 1. Simplified Logic Diagram of NB3L853141

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.



Note: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout (Top View) **and Logic Diagram**

Table 1. FUNCTION TABLE

CLK0	CLK1	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

*On next negative transition of CLK0 or CLK1
X = Don't Care

Table 2. PIN DESCRIPTION

Pin Number	Name	I/O	Open Default	Description
1	Q0	LVPECL Output		Non−Inverted Differential Clock Output
2	$\overline{Q0}$	LVPECL Output		Inverted Differential Clock Output
3	Q1	LVPECL Output		Non−Inverted Differential Clock Output
4	$\overline{Q1}$	LVPECL Output		Inverted Differential Clock Output
5	Q2	LVPECL Output		Non−Inverted Differential Clock Output
6	$\overline{Q2}$	LVPECL Output		Inverted Differential Clock Output
7	Q3	LVPECL Output		Non−Inverted Differential Clock Output
8	$\overline{Q3}$	LVPECL Output		Inverted Differential Clock Output
9	Q4	LVPECL Output		Non−Inverted Differential Clock Output
10	$\overline{Q4}$	LVPECL Output		Inverted Differential Clock Output
11	VEE	Power		Negative Supply Voltage
12	SEL	LVCMOS / LVTTL Input	Low	Clock Select Input. When HIGH, selects CLK1 input. When LOW, selects CLK0, $\overline{CLK0}$ inputs. Internal Pull−down Resistor.
13	NC			No Connect
14	$\overline{CLK0}$	Multi−Level Input	High	Inverted Differential Clock Input. Internal Pull−up Resistor.
15	CLK0	Multi−Level Input	Low	Non−Inverted Differential Clock Input. Internal Pull−down Resistor.
16	CLK1	LVCMOS/LVTTL Input	Low	Single−ended Clock Input. Internal Pull−down Resistor.
17	NC			No Connect
18	VCC	Power		Positive Supply Voltage
19	$\overline{EN}$	LVCMOS/LVTTL Input	Low	Synchronous Clock Enable Input. When Low, outputs are enabled. When High, outputs are disabled Low. Internal Pull−down Resistor.
20	VCC	Power		Positive Supply Voltage

All VCC and VEE pins must be externally connected to a power supply to guarantee proper operation. Bypass each supply pin with 0.01 μF to GND.

Table 3. ATTRIBUTES (Note 1)

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R_{PU} − Pull−up Resistor		50 kΩ
R_{PD} − Pull−down Resistor		50 kΩ
Moisture Sensitivity (Note 1)	TSSOP−20	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL*94 code V*0 @ 0.125 in
Transistor Count		300
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	LVPECL Mode Power Supply	V_{EE} = 0 V		4.6	V
V_I	LVPECL Mode Input Voltage	V_{EE} = 0 V	$V_I \le V_{CC}$	−0.5 to V_{CC} + 0.5	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−20 TSSOP−20	140 50	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−20	23 to 41	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. DC CHARACTERISTICS V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 2); T_A = −40°C to +85°C

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY						
V_{CC}	Power Supply Voltage		2.375		3.8	V
I_{EE}	Power Supply Current (Outputs Open)			40	55	mA
LVPECL OUTPUTS (Note 3)						
V_{OH}	Output HIGH Voltage		V_{CC}−1.4		V_{CC}−0.9	V
V_{OL}	Output LOW Voltage		V_{CC}−2.0		V_{CC}−1.7	V
V_{SWING}	Output Voltage Swing, Peak−to−Peak		0.6		1.0	V
DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED (Note 4) (Figures 3 and 4)						
V_{IH}	Single−ended Input HIGH Voltage		0.5		V_{CC}+0.3	V
V_{IL}	Single−ended Input LOW Voltage		−0.3		V_{CC}−1.0	V
V_{th}	Input Threshold Reference Voltage Range (Note 5)		0.35		V_{CC}−0.85	V
V_{ISE}	Single−ended Input Voltage (V_{IH} − V_{IL})		0.3		V_{CC}	V
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 5 and 6) (Note 6)						
V_{IHD}	Differential Input HIGH Voltage		0.5		V_{CC}−0.85	mV
V_{ILD}	Differential Input LOW Voltage		0		V_{IHD}−150	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; (Note 7)		0.5		V_{CC}–0.85	
I_{IH}	Input HIGH Current	V_{CC} = V_{IN} = 3.8 V CLK0 $\overline{CLK0}$			150 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.8V, V_{IN} = 0 V CLK0 $\overline{CLK0}$	−5 −150			µA
SINGLE−ENDED INPUTS (SEL, $\overline{EN}$, CLK1)						
V_{IH}	Input HIGH Voltage	SEL, $\overline{EN}$ CLK1	2.0 2.0		V_{CC}+0.3 V_{CC}+0.3	V
V_{IL}	Input LOW Voltage	SEL, $\overline{EN}$ CLK1	−0.3 −0.3		0.8 V_{CC}x0.35	V
I_{IH}	Input HIGH Current VCC = V_{IN} = 3.8 V	CLK1, SEL, $\overline{EN}$			150	µA
I_{IL}	CLK1, SEL, $\overline{EN}$	CLK1, SEL, $\overline{EN}$	−5			µA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and Output parameters vary 1:1 with V_{CC}.
3. LVPECL outputs loaded with 50 Ω to V_{CC} − 2 V for proper operation.
4. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
5. V_{th} is applied to the complementary input when operating in single−ended mode.
6. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
7. The common mode voltage is defined as V_{IH}.

Table 6. AC CHARACTERISTICS, V_{CC} = 2.375 V to 3.8 V, T_A = −40°C to +85°C (Note 8)

Symbol	Characteristic			Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency: $V_{OUTpp} \geq 400$ mV	CLK0/$\overline{CLK0}$, $V_{INPPmin} \geq 250$ mV CLK1		700 300			MHz
Φ_N	Phase Noise, f_C = 155.52 MHz	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz	Offset from Carrier		−100.5 −128.2 −138.6 −147.1 −149.7 −154.2 −154.2 −154.2		dBc/Hz
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, @ 50 MHz	Note 9 Note 10	CLK0/$\overline{CLK0}$ to Q/$\overline{Q}$ CLK1 to Q	0.8 0.8	1.0 1.0	1.5 1.5	ns
$t_{j\Phi N}$	Additive Phase Jitter, RMS; f_C = 155.52 MHz, Integration Range: 12 kHz − 20 MHz				0.05		ps
tsk(o)	Output−to−output skew; (Note 11)					30	ps
tsk (pp)	Part−to−Part Skew; (Note 12)					150	ps
V_{INpp}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)			150		1300	mV
t_r/t_f	Output rise and fall times, 20% to 80%,		Q, $\overline{Q}$	200		700	ps
ODC	Output Clock Duty Cycle Input Duty Cycle = 50%	CLK0/$\overline{CLK0}$, f ≤ 700 MHz, $V_{INPPmin} \geq 250$ mV CLK1, f ≤ 250MHz		45 45		55 55	%

All parameters measured at f_{MAX} unless noted otherwise.
The cycle−to−cycle jitter on the input will equal the jitter on the output. The part does not add jitter

8. Measured using a $V_{INPPmin}$ source, Reference Duty Cycle = 50% duty cycle clock source. All output loading with external 50 Ω to V_{CC} − 2 V.
9. Measured from the differential input crossing point to the differential output crossing point.
10. Measured from V_{CC} /2 input crossing point to the differential output crossing point.
11. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
12. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
13. Output voltage swing is a single−ended measurement operating in differential mode.
14. Input voltage swing is a single−ended measurement operating in differential mode.

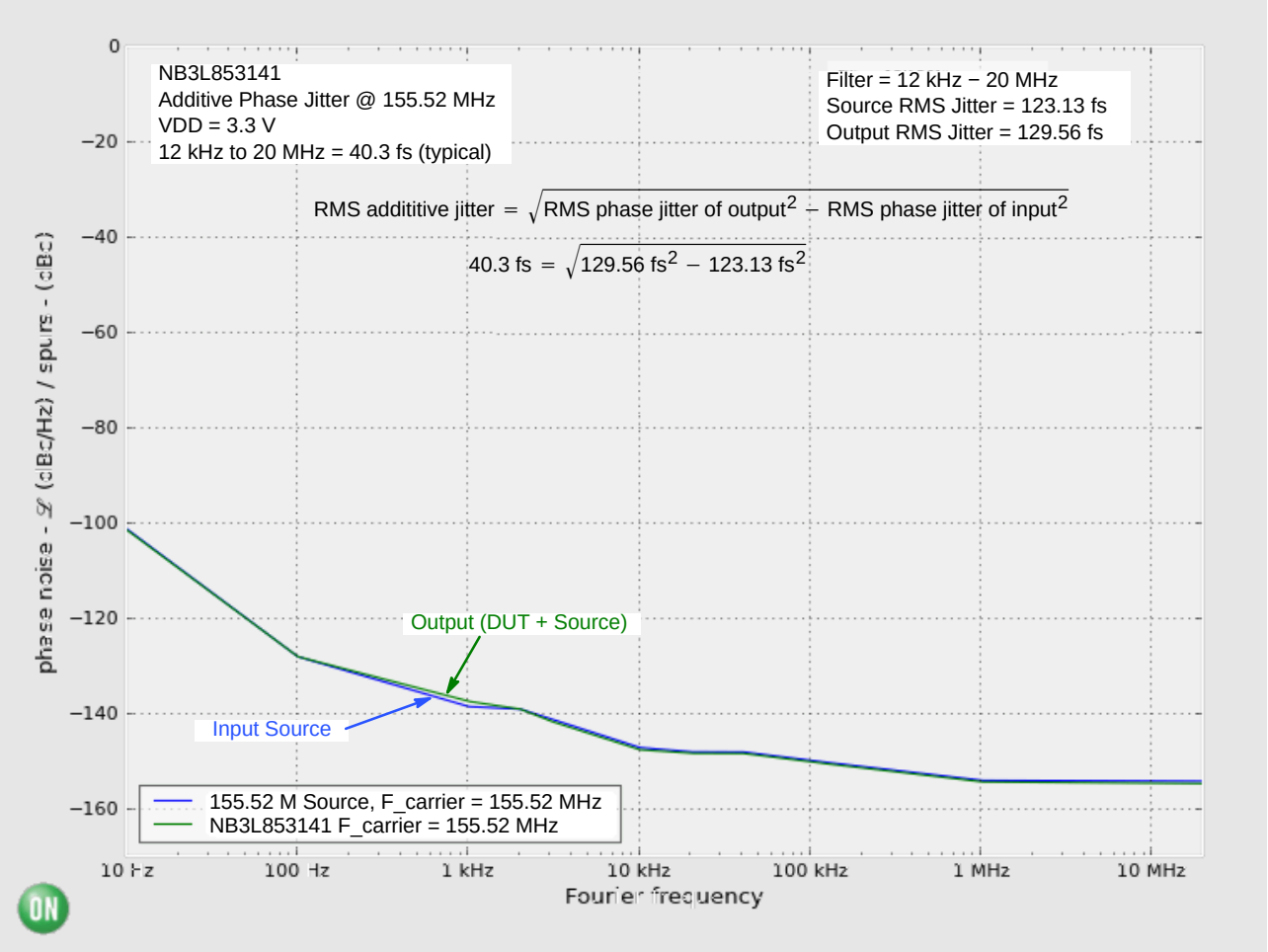


Figure 2. Typical Phase Noise Plot at $f_{carrier}$ = 155.52 MHz at an Operating Voltage of 3.3 V, Room Temperature

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 40.3 fs.

The additive phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most accurate additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the device under test output, the source noise will dominate the additive phase jitter calculation and lead to an artificially low result for the additive phase noise measurement within the integration range. The Figure above is a good example of the NB3L853141 source generator phase noise having a significantly higher floor such that the DUT output results in an additive phase jitter of 40.3 fs.

$$\text{RMS additive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$40.3\ \text{fs} = \sqrt{129.56\ \text{fs}^2 - 123.13\ \text{fs}^2}$$

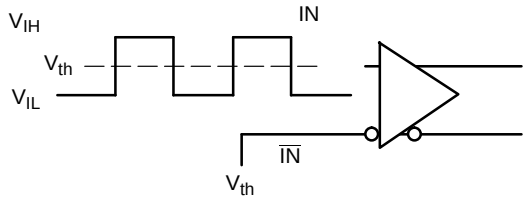


Figure 3. Differential Input Driven Single−Ended

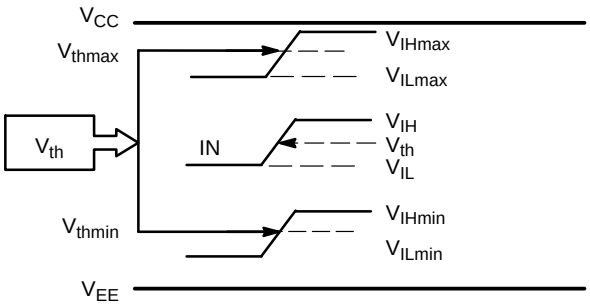


Figure 4. V_{th} Diagram

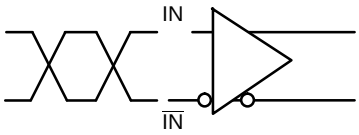


Figure 5. Differential Inputs Driven Differentially

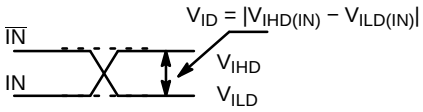


Figure 6. Differential Inputs Driven Differentially

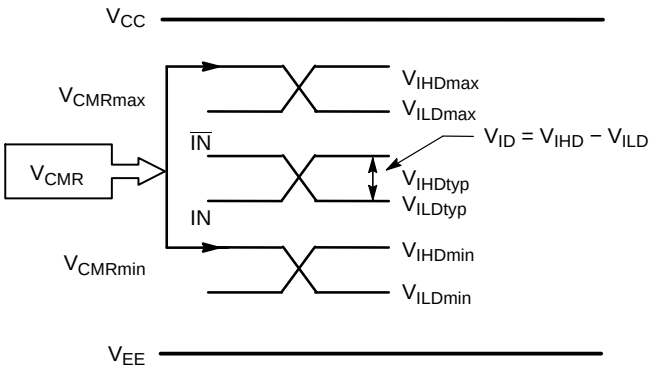


Figure 7. VCMR Diagram

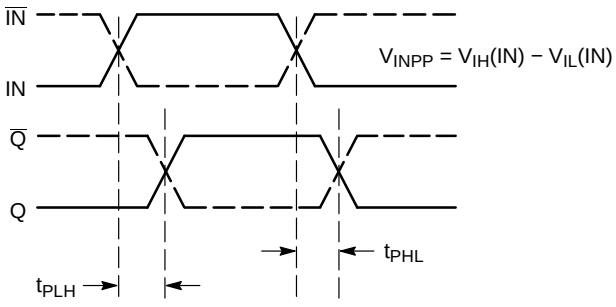


Figure 8. AC Reference Measurement

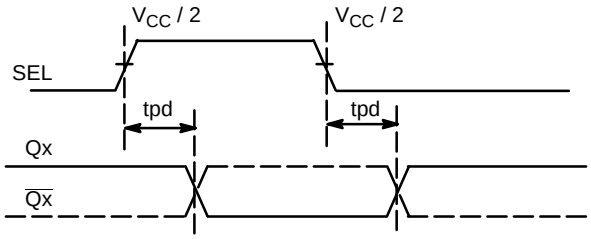


Figure 9. SEL to Qx Timing Diagram

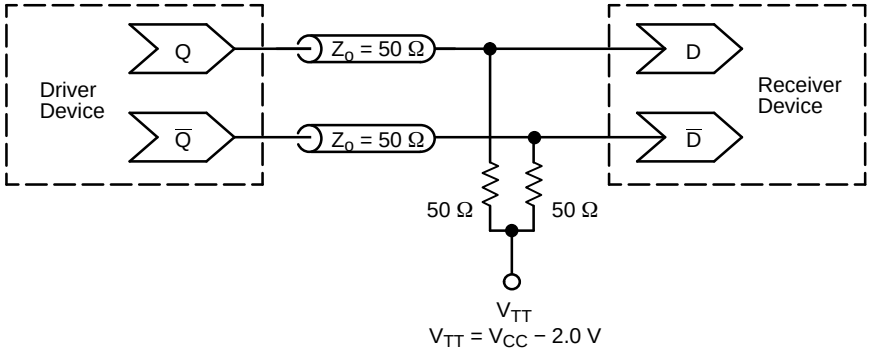


Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

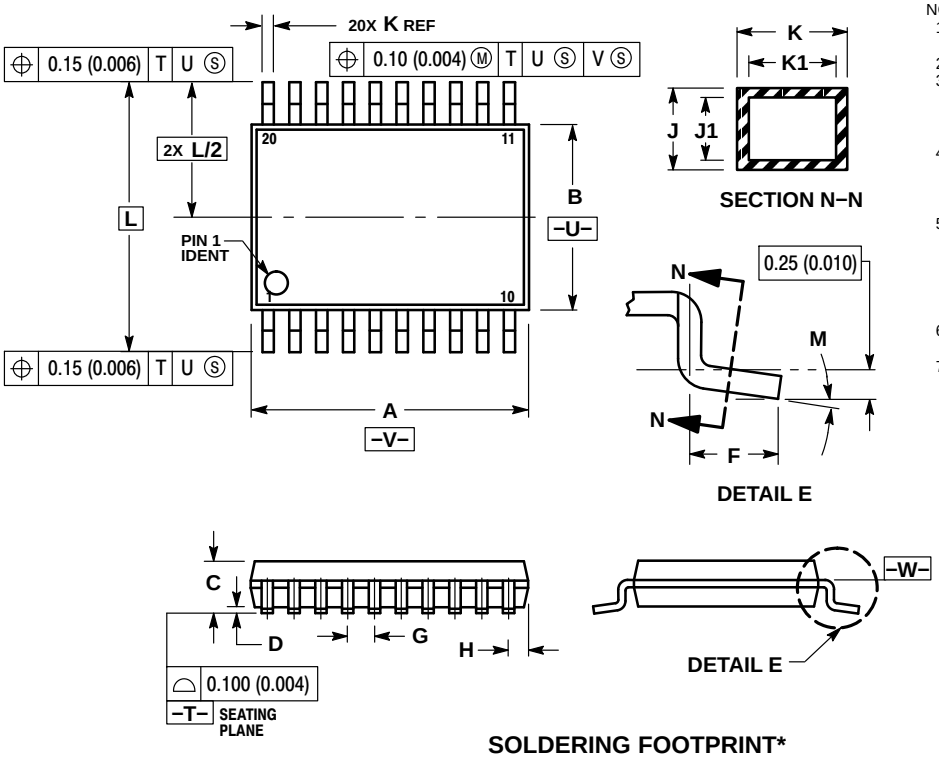
ORDERING INFORMATION

Device	Package	Shipping†
NB3L853141DTG	TSSOP−20 (Pb−Free)	75 Units / Rail
NB3L853141DTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

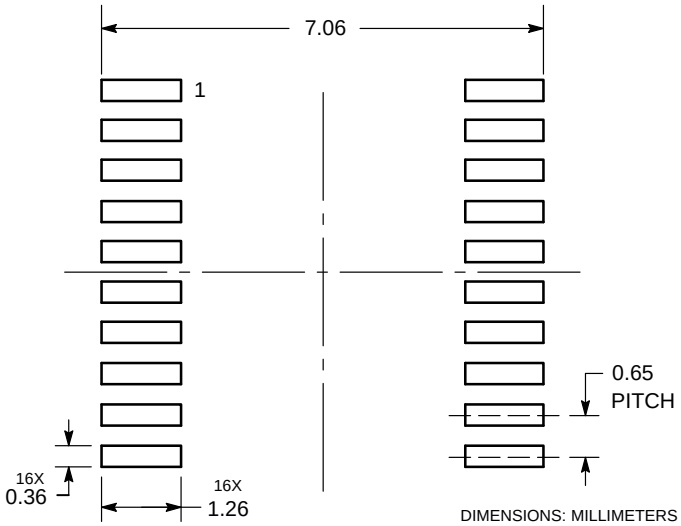
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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