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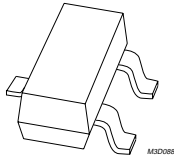
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Kind regards,

Team Nexperia



SI2304DS

N-channel enhancement mode field-effect transistor

Rev. 01 — 17 August 2001

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology

Product availability:

SI2304DS in SOT23.

2. Features

- TrenchMOS™ technology
- Very fast switching
- Subminiature surface mount package.

3. Applications

- Battery management
- High speed switch
- Low power DC to DC converter.

4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MSB003</p> <p>SOT23</p>	<p>MBB076</p>
2	source (s)		
3	drain (d)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



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5. Quick reference data

Table 2: Quick reference data

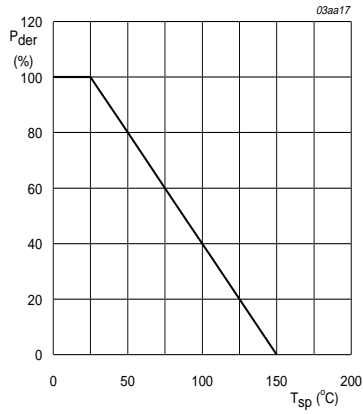
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	–	30	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 5$ V	–	–	1.7	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C	–	–	0.83	W
T_j	junction temperature		–	–	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 500$ mA	–	–	117	mΩ
		$V_{GS} = 4.5$ V; $I_D = 500$ mA	–	–	190	mΩ

6. Limiting values

Table 3: Limiting values

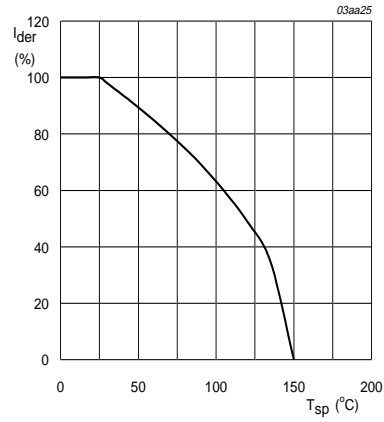
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	30	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 150 °C; $R_{GS} = 20$ kΩ	–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 5$ V; Figure 2 and 3	–	1.7	A
		$T_{sp} = 100$ °C; $V_{GS} = 5$ V; Figure 2 and 3	–	1.1	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	7.5	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Figure 1	–	0.83	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25$ °C	–	0.83	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	3.3	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

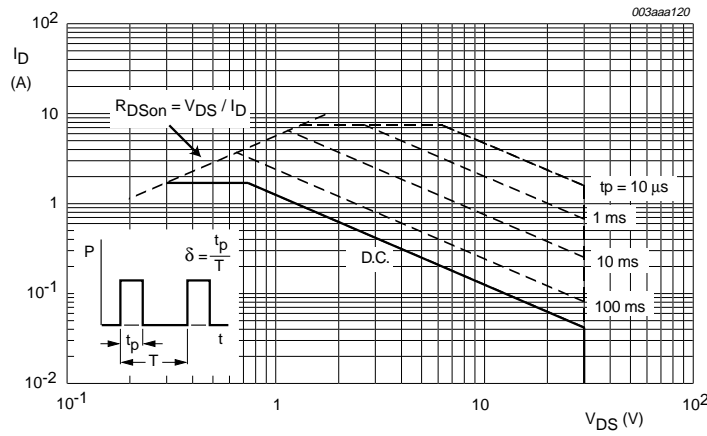
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 10\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 4	100	K/W

7.1 Transient thermal impedance

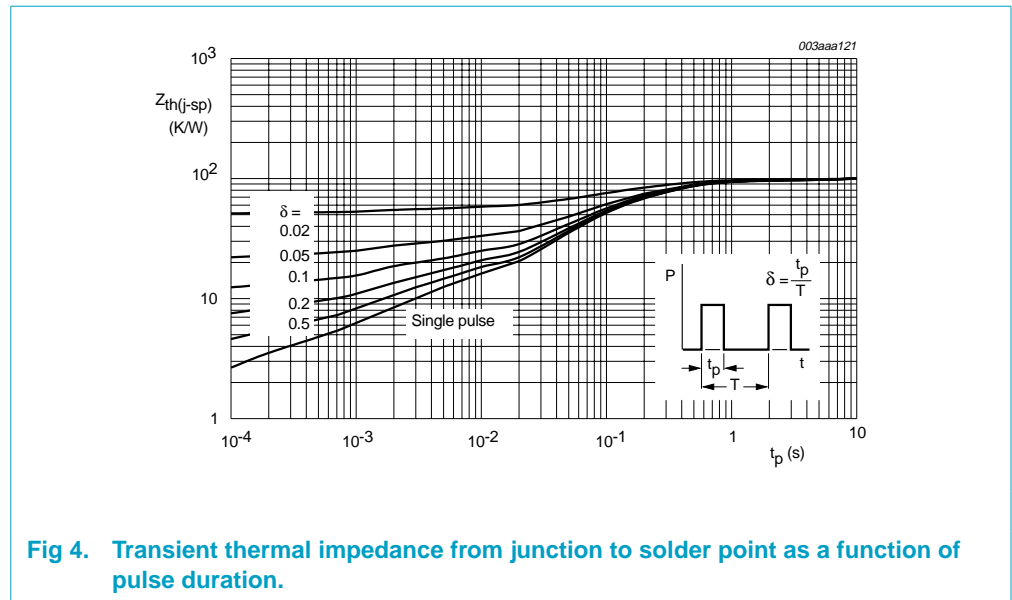
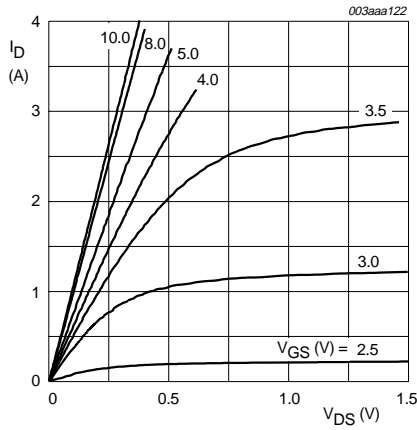


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

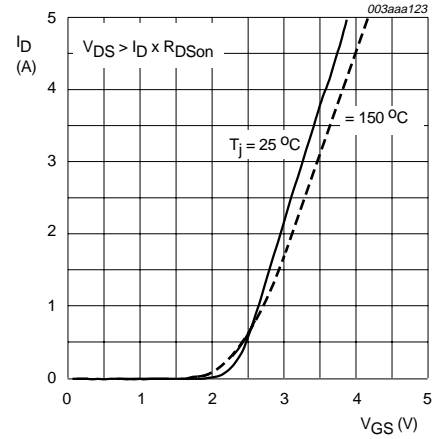
Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	30	40	–	V
		$T_j = -55\text{ }^\circ\text{C}$	27	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ }^\circ\text{C}$	1.5	2	–	V
		$T_j = 150\text{ }^\circ\text{C}$	0.5	–	–	V
		$T_j = -55\text{ }^\circ\text{C}$	–	–	2.7	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	–	0.01	0.5	μA
		$T_j = 150\text{ }^\circ\text{C}$	–	–	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	–	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; Figure 7 and 8 $T_j = 25\text{ }^\circ\text{C}$	–	–	117	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 500\text{ mA}$ $T_j = 25\text{ }^\circ\text{C}$	–	–	190	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	–	–	300	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 1\text{ A}$	1.4	2.5	–	S
$Q_{g(tot)}$	total gate charge	$V_{DD} = 15\text{ V}$; $V_{GS} = 10\text{ V}$; $I_D = 0.5\text{ A}$; Figure 13	–	4.6	–	nC
Q_{gs}	gate-source charge		–	0.6	–	nC
Q_{gd}	gate-drain (Miller) charge		–	1.35	1.83	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; Figure 11	–	147	195	pF
C_{oss}	output capacitance		–	65	78	pF
C_{rss}	reverse transfer capacitance		–	41	56	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$; $R_L = 15\text{ }\Omega$; $V_{GS} = 10\text{ V}$	–	4	6	ns
t_r	rise time		–	7.5	12	ns
$t_{d(off)}$	turn-off delay time		–	18	35	ns
t_f	fall time		–	13	19	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 0.83\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	–	0.7	1.2	V
t_{rr}	reverse recovery time	$I_S = 1\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$	–	69	–	ns



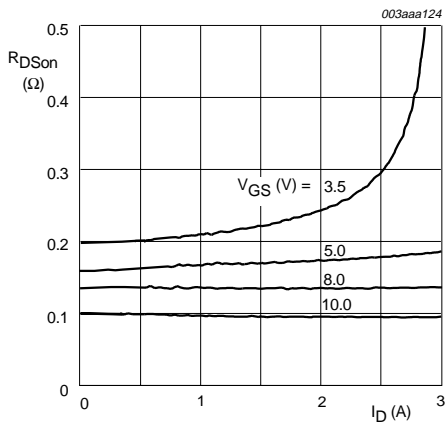
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



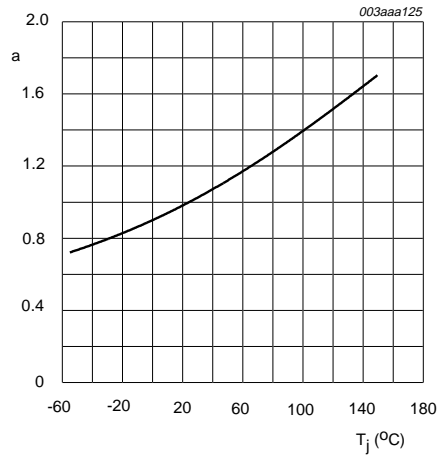
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



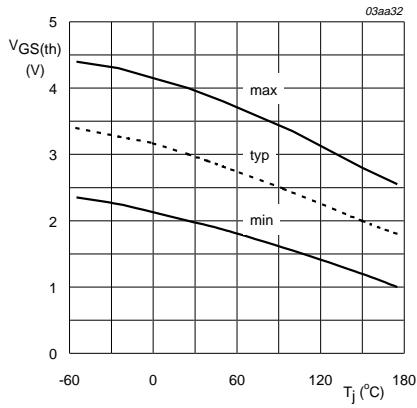
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



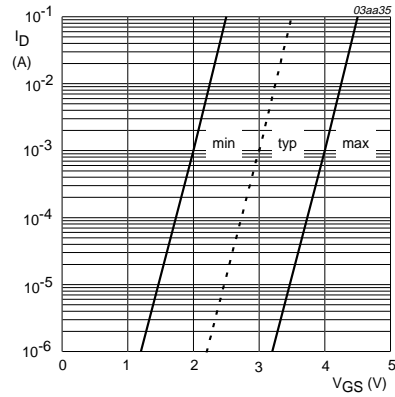
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



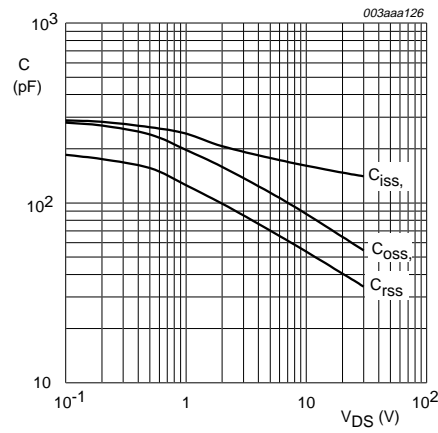
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



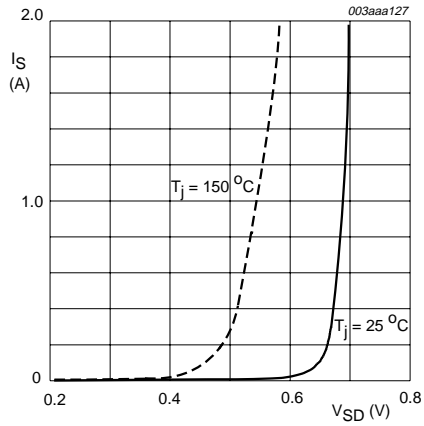
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



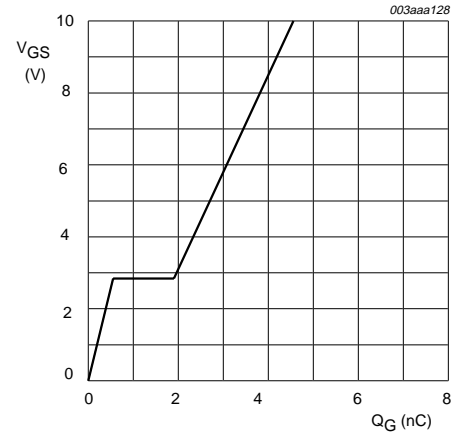
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 0.5\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 3 leads

SOT23

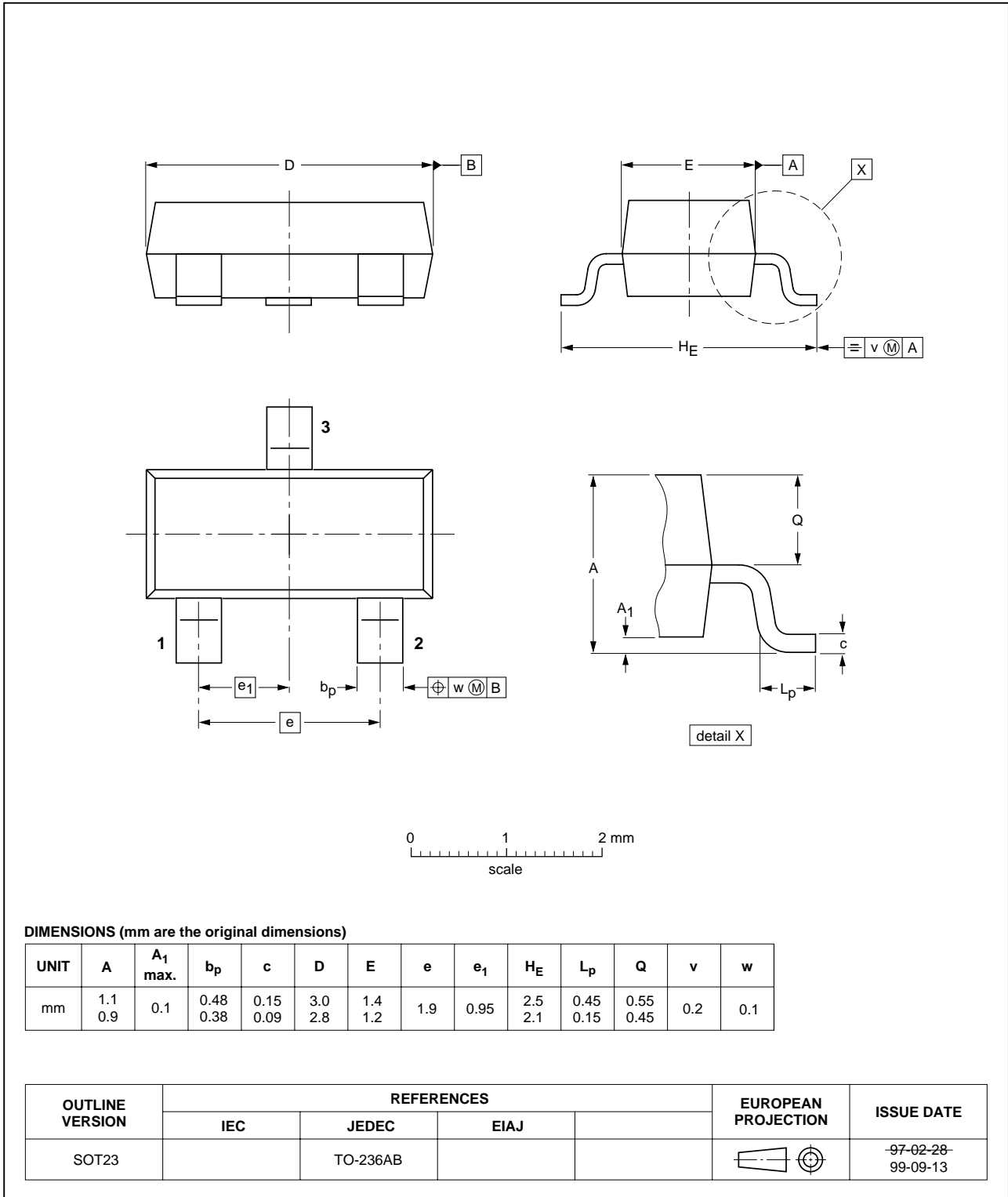


Fig 14. SOT23.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010817	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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