

Features

- Thin small outline package (TSOP) I package configurable as 512K × 16 or 1M × 8 static RAM (SRAM)
- High speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62157DV30
- Ultra low standby power
 - Typical standby current: 2 μA
 - Maximum standby current: 8 μA (Industrial)
- Ultra low active power
 - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA), Pb-free 44-pin thin small outline package (TSOP) II and 48-pin TSOP I packages

Functional Description

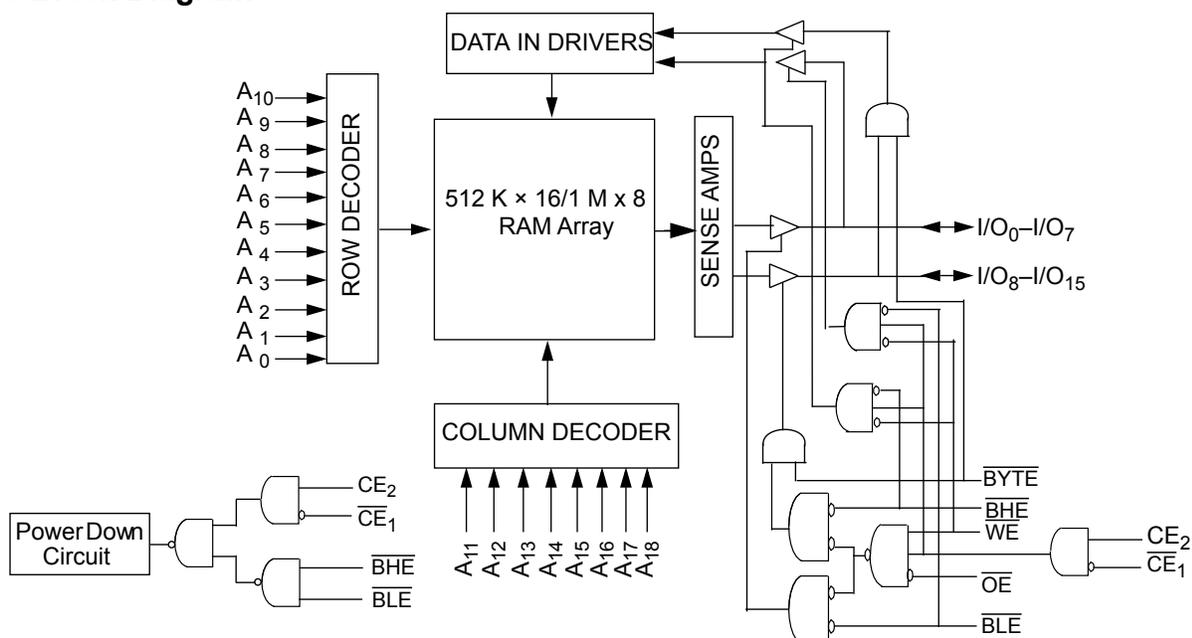
The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input or output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or a write operation is active (CE_1 LOW, CE_2 HIGH and WE LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (WE) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₈). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Truth Table on page 13 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



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Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]

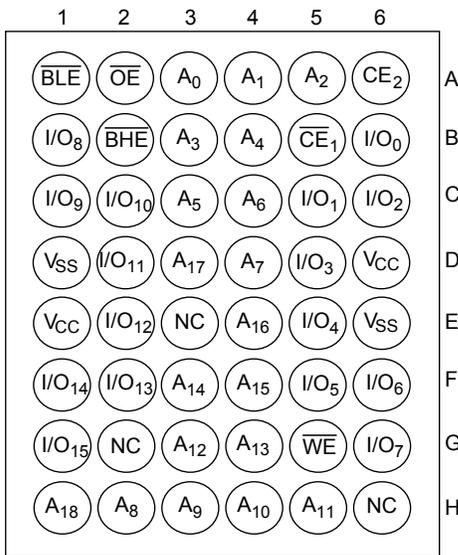


Figure 2. 44-pin TSOP II pinout (Top View) [2]

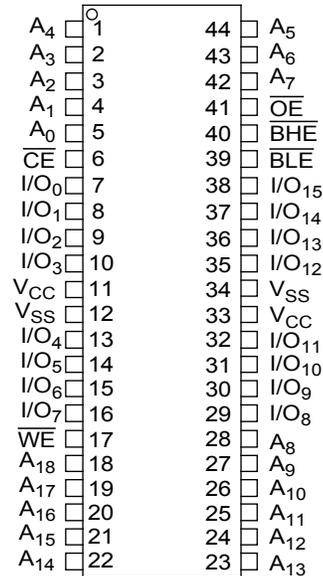


Figure 3. 48-pin TSOP I pinout (Top View) [1, 3]



Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|---------------------------|---------------------------|--------------------|----------------------|--------------------|----------------------------------|-----|--------------------|-----|--------------------------------|----|
| | | | | | | Operating I _{CC} , (mA) | | | | Standby, I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | Typ ^[4] | Max | Typ ^[4] | Max | | |
| Min | Typ ^[4] | Max | Typ ^[4] | Max | Typ ^[4] | | | | | Max | |
| CY62157EV30LL | Industrial / Automotive-A | 2.2 | 3.0 | 3.6 | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |
| | Automotive-E | 2.2 | 3.0 | 3.6 | 55 | 1.8 | 4 | 18 | 35 | 2 | 30 |

Notes

1. NC pins are not connected on the die.
2. The 44-pin TSOP II package has only one chip enable (\overline{CE}) pin.
3. The BYTE pin in the 48-pin TSOP I package must be tied HIGH to use the device as a 512 K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1 M × 8 SRAM by tying the BYTE signal LOW. In the 1 M × 8 configuration, Pin 45 is A19, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature -65 °C to + 150 °C

Ambient Temperature with Power Applied -55 °C to + 125 °C

Supply Voltage to Ground Potential -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC Voltage Applied to Outputs in High Z State ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC Input Voltage ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) > 2001 V

Latch Up Current > 200 mA

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[7] |
|---------------|---------------------------|---------------------|-------------------------|
| CY62157EV30LL | Industrial / Automotive-A | -40 °C to +85 °C | 2.2 V to 3.6 V |
| | Automotive-E | -40 °C to +125 °C | |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns (Industrial/Automotive-A) | | | 55 ns (Automotive-E) | | | Unit |
|--------------------------|---|--|---------------------------------|--------------------|----------------|----------------------|--------------------|----------------|---------|
| | | | Min | Typ ^[8] | Max | Min | Typ ^[8] | Max | |
| V_{OH} | Output HIGH voltage | $I_{OH} = -0.1$ mA | 2.0 | - | - | 2.0 | - | - | V |
| | | $I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V | 2.4 | - | - | 2.4 | - | - | V |
| V_{OL} | Output LOW voltage | $I_{OL} = 0.1$ mA | - | - | 0.4 | - | - | 0.4 | V |
| | | $I_{OL} = 2.1$ mA, $V_{CC} \geq 2.70$ V | - | - | 0.4 | - | - | 0.4 | V |
| V_{IH} | Input HIGH voltage | $V_{CC} = 2.2$ V to 2.7 V | 1.8 | - | $V_{CC} + 0.3$ | 1.8 | - | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.2 | - | $V_{CC} + 0.3$ | 2.2 | - | $V_{CC} + 0.3$ | V |
| V_{IL} | Input LOW voltage | $V_{CC} = 2.2$ V to 2.7 V | -0.3 | - | 0.6 | -0.3 | - | 0.6 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | -0.3 | - | 0.8 | -0.3 | - | 0.8 | V |
| I_{IX} | Input leakage current | $GND \leq V_I \leq V_{CC}$ | -1 | - | +1 | -4 | - | +4 | μ A |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -1 | - | +1 | -4 | - | +4 | μ A |
| I_{CC} | V_{CC} operating supply current | $f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$ | - | 18 | 25 | - | 18 | 35 | mA |
| | | $f = 1$ MHz $I_{OUT} = 0$ mA CMOS levels | - | 1.8 | 3 | - | 1.8 | 4 | |
| I_{SB1} ^[9] | Automatic CE power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V $f = f_{max}$ (Address and Data Only), $f = 0$ (\overline{OE} and \overline{WE}), $V_{CC} = 3.60$ V | - | 2 | 8 | - | 2 | 30 | μ A |
| I_{SB2} ^[9] | Automatic CE power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.60$ V | - | 2 | 8 | - | 2 | 30 | μ A |

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75$ V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μ s ramp time from 0 to $V_{CC(min)}$ and 200 μ s wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
- Chip enables (CE_1 and CE_2), byte enables (BHE and BLE) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

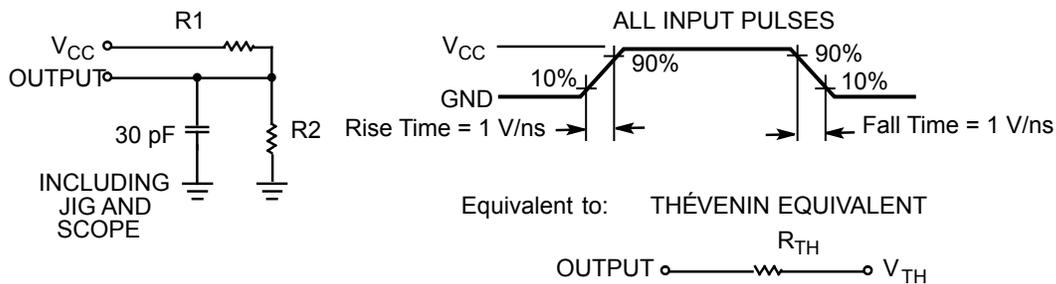
| Parameter ^[10] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter ^[10] | Description | Test Conditions | 48-ball BGA | 48-pin TSOP I | 44-pin TSOP II | Unit |
|---------------------------|--|---|-------------|---------------|----------------|------|
| Θ _{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 48.34 | 55.47 | 55.84 | °C/W |
| Θ _{JC} | Thermal resistance (junction to case) | | 8.78 | 4.08 | 15.79 | °C/W |

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



| Parameters | 2.5 V | 3.0 V | Unit |
|-----------------|-------|-------|------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.20 | 1.75 | V |

Note

10. Tested initially and after any design or process changes that may affect these parameters.

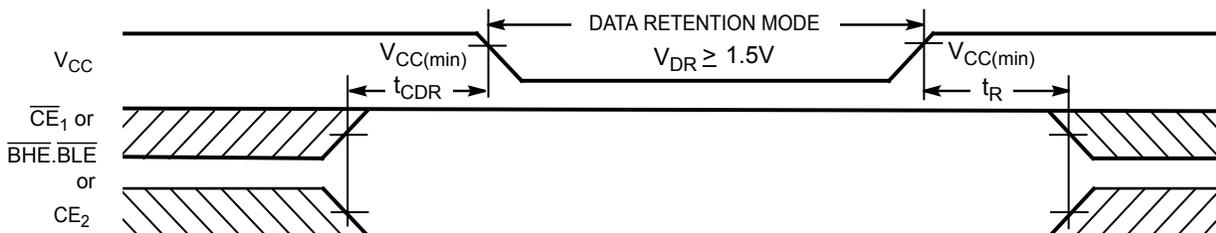
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[11] | Max | Unit |
|----------------------------|--------------------------------------|---|---------------------------|---------------------|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.5 | – | – | V |
| I_{CCDR} ^[12] | Data retention current | $V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$, $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE}\text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 2 | 5 | μA |
| | | | Industrial / Automotive-A | – | – | |
| t_{CDR} ^[13] | Chip deselect to data retention time | | 0 | – | – | ns |
| t_R ^[14] | Operation recovery time | CY62157EV30LL-45 | 45 | – | – | ns |
| | | CY62157EV30LL-55 | 55 | – | – | |

Data Retention Waveform

Figure 5. Data Retention Waveform^[15]



Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
- Chip enables (\overline{CE}_1 and CE_2), byte enables (\overline{BHE} and \overline{BLE}) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.
- $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

| Parameter ^[16, 17] | Description | 45 ns (Industrial / Automotive-A) | | 55 ns (Automotive-E) | | Unit |
|--|---|-----------------------------------|-----|----------------------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read cycle time | 45 | – | 55 | – | ns |
| t_{AA} | Address to data valid | – | 45 | – | 55 | ns |
| t_{OHA} | Data hold from address change | 10 | – | 10 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | – | 45 | – | 55 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | – | 25 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[18] | 5 | – | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[18] | 10 | – | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to power up | 0 | – | 0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to power down | – | 45 | – | 55 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 45 | – | 55 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[18, 20] | 5 | – | 10 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| Write Cycle ^[21, 22] | | | | | | |
| t_{WC} | Write cycle time | 45 | – | 55 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35 | – | 40 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | 40 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35 | – | 40 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35 | – | 40 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[18] | 10 | – | 10 | – | ns |

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 5.
17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
18. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
19. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
20. If both byte enables are toggled together, this value is 10 ns.
21. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [23, 24]

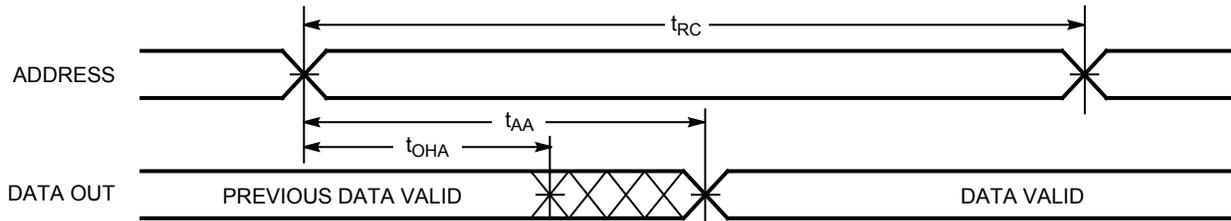
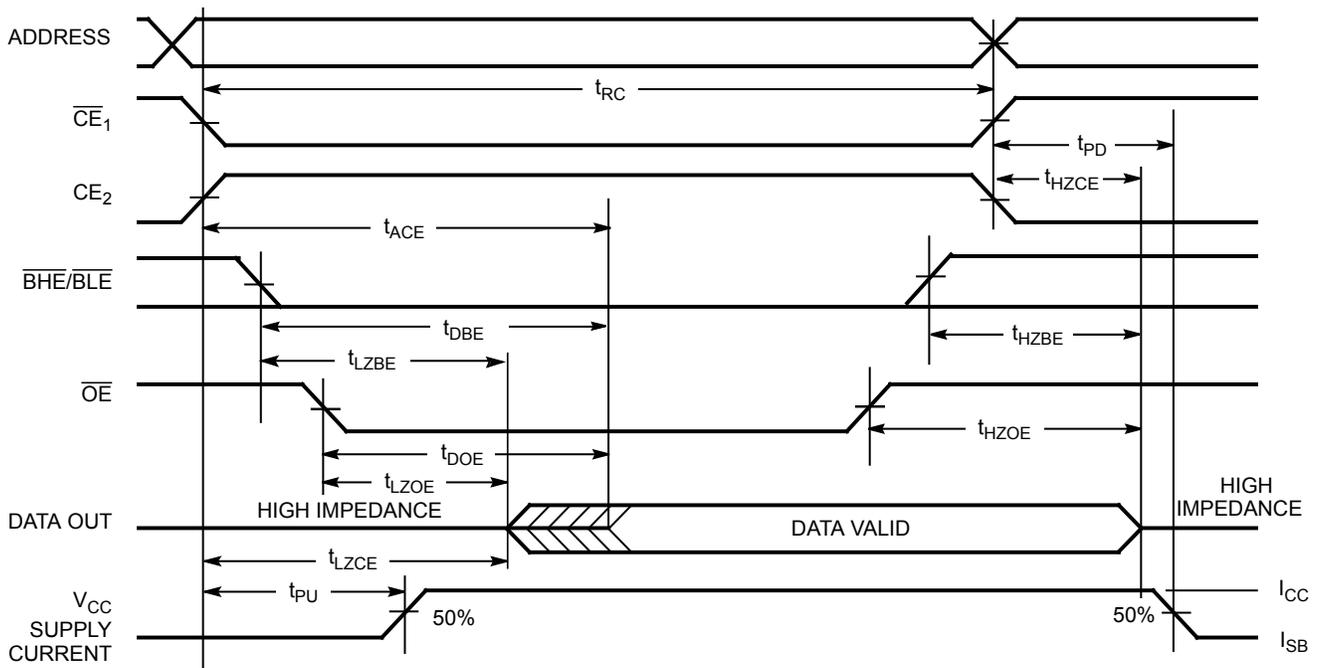


Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [24, 25]

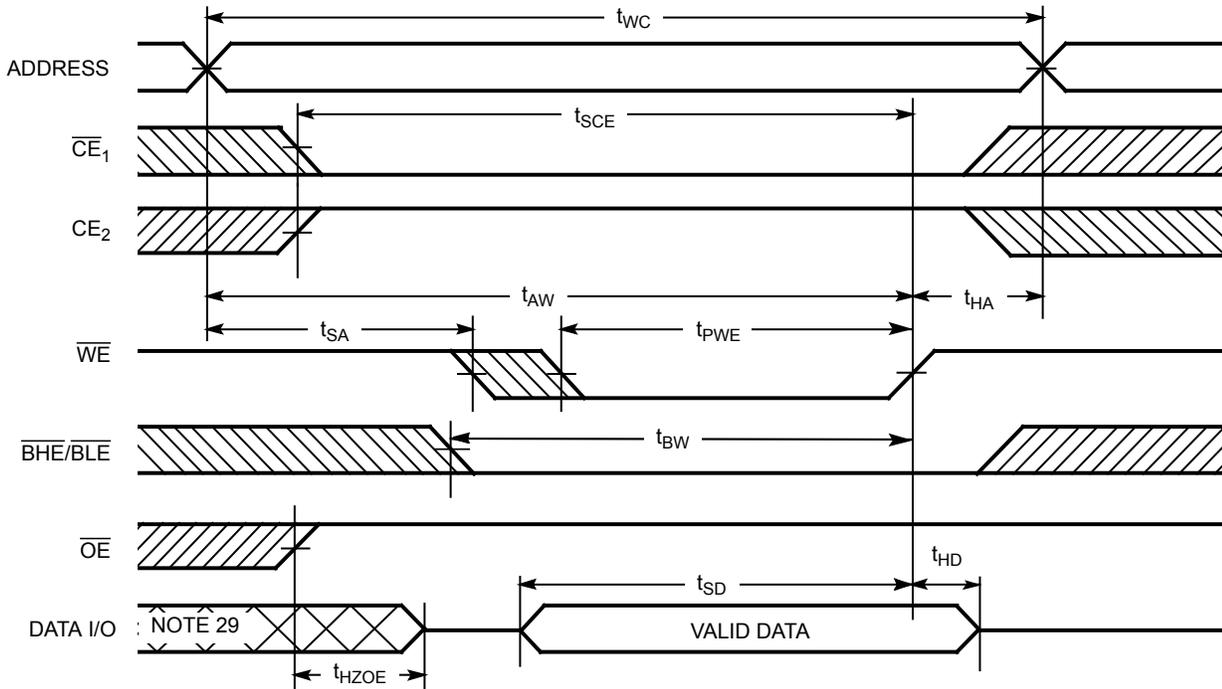


Notes

23. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$.
24. WE is HIGH for read cycle.
25. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (\overline{WE} Controlled) [26, 27, 28]



Notes

26. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

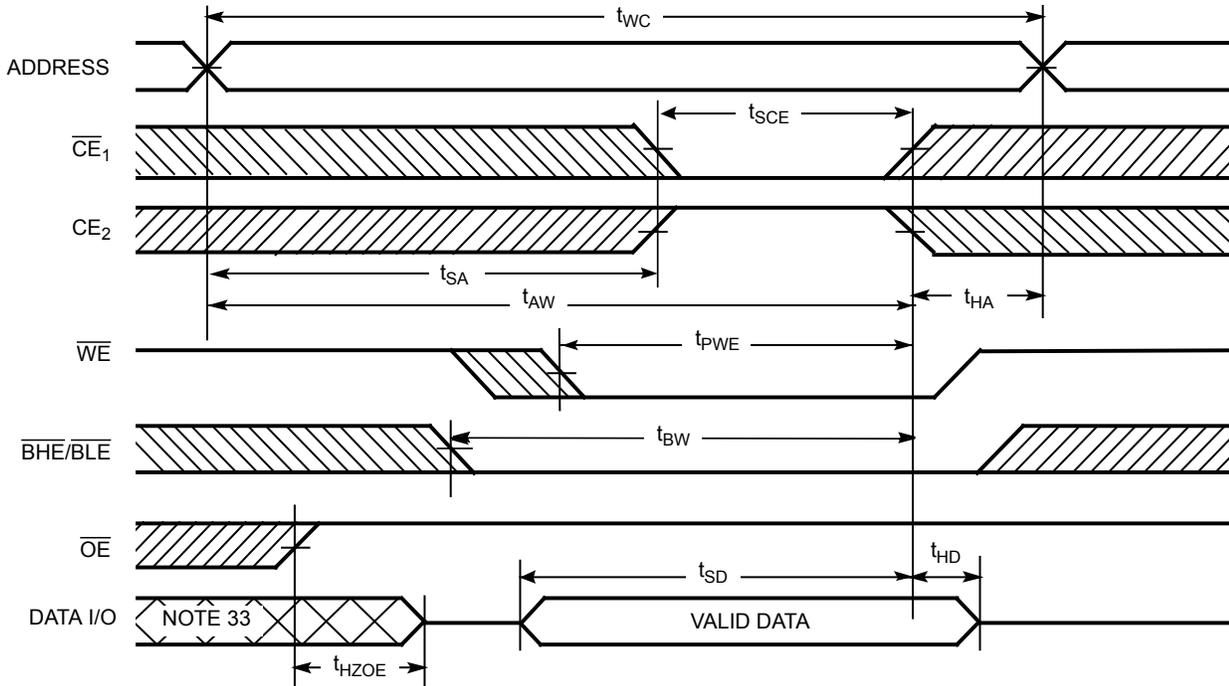
27. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

28. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [30, 31, 32]



Notes

30. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

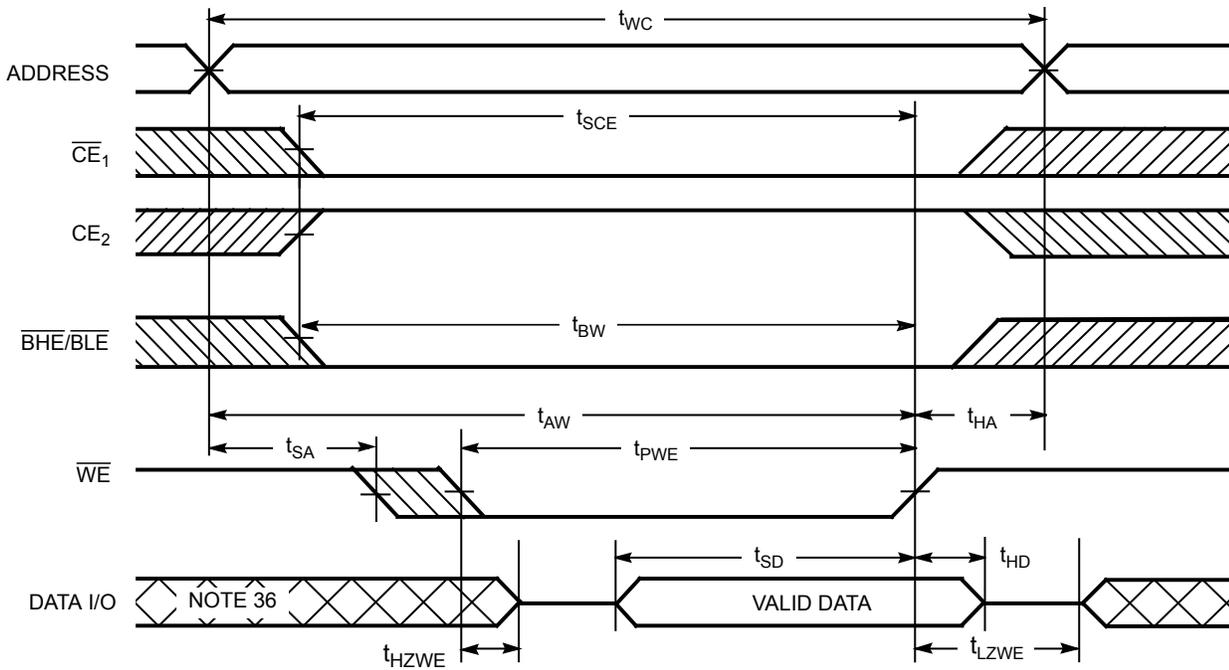
31. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

32. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [34, 35]

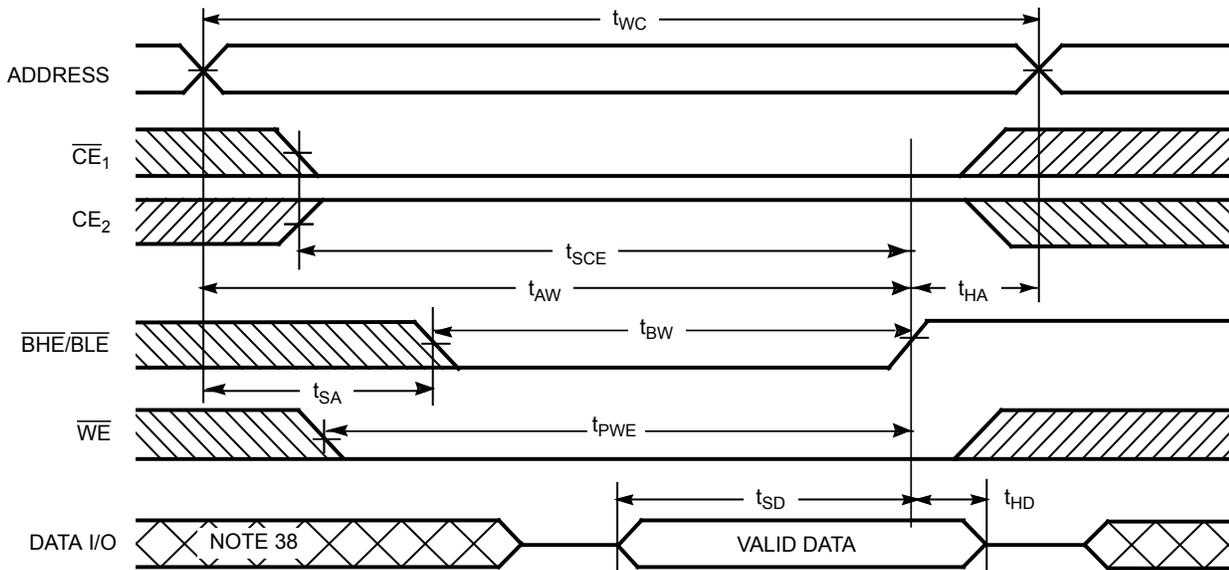


Notes

- 34. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 35. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .
- 36. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) [37]



Notes

- 37. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 38. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

| CE₁ | CE₂ | WE | OE | BHE | BLE | Inputs/Outputs | Mode | Power |
|-----------------------|-----------------------|-----------|-----------|------------|------------|--|---------------------|----------------------------|
| H | X ^[39] | X | X | X | X | High Z | Deselect/power down | Standby (I _{SB}) |
| X ^[39] | L | X | X | X | X | High Z | Deselect/power down | Standby (I _{SB}) |
| X ^[39] | X ^[39] | X | X | H | H | High Z | Deselect/power down | Standby (I _{SB}) |
| L | H | H | L | L | L | Data Out (I/O ₀ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | H | H | L | H | L | Data Out (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | H | H | L | L | H | High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | H | H | H | L | H | High Z | Output disabled | Active (I _{CC}) |
| L | H | H | H | H | L | High Z | Output disabled | Active (I _{CC}) |
| L | H | H | H | L | L | High Z | Output disabled | Active (I _{CC}) |
| L | H | L | X | L | L | Data In (I/O ₀ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | H | L | X | H | L | Data In (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | H | L | X | L | H | High Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅) | Write | Active (I _{CC}) |

Note

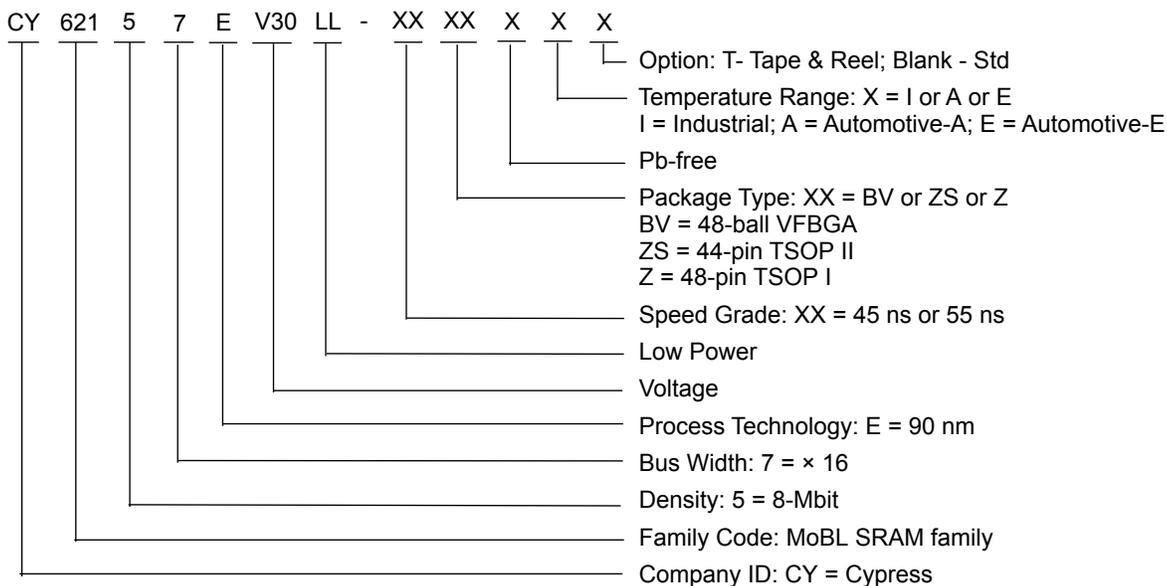
39. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-----------------------|-----------------------|-------------------------------|-------------------------------|
| 45 | CY62157EV30LL-45BVI | 51-85150 | 48-ball VFBGA | Industrial |
| | CY62157EV30LL-45BVIT | 51-85150 | 48-ball VFBGA | |
| | CY62157EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | |
| | CY62157EV30LL-45BVXIT | 51-85150 | 48-ball VFBGA (Pb-free) | |
| | CY62157EV30LL-45ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-45ZSXIT | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-45ZXI | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | CY62157EV30LL-45ZXIT | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | Automotive-A | CY62157EV30LL-45BVXA | 51-85150 | 48-ball VFBGA (Pb-free) |
| | | CY62157EV30LL-45BVXAT | 51-85150 | 48-ball VFBGA (Pb-free) |
| | | CY62157EV30LL-45ZSXA | 51-85087 | 44-pin TSOP Type II (Pb-free) |
| | | CY62157EV30LL-45ZSXAT | 51-85087 | 44-pin TSOP Type II (Pb-free) |
| | | CY62157EV30LL-45ZXA | 51-85183 | 48-pin TSOP Type I (Pb-free) |
| | | CY62157EV30LL-45ZXAT | 51-85183 | 48-pin TSOP Type I (Pb-free) |
| 55 | CY62157EV30LL-55ZSXE | 51-85087 | 44-pin TSOP Type II (Pb-free) | Automotive-E |
| | CY62157EV30LL-55ZSXET | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-55ZXE | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | CY62157EV30LL-55ZXET | 51-85183 | 48-pin TSOP Type I (Pb-free) | |

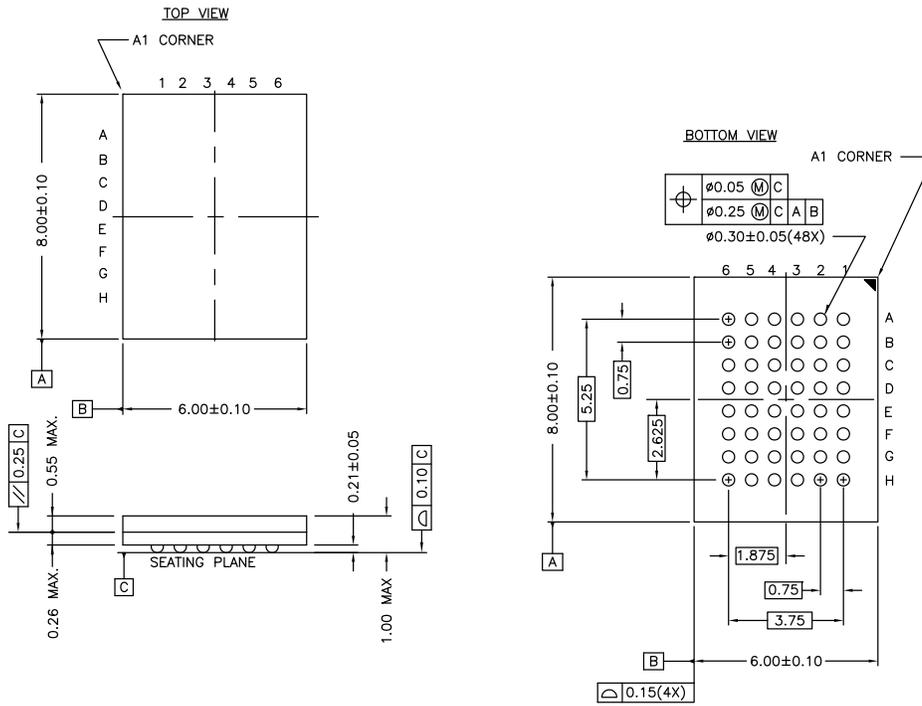
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 12. 48-pin VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150

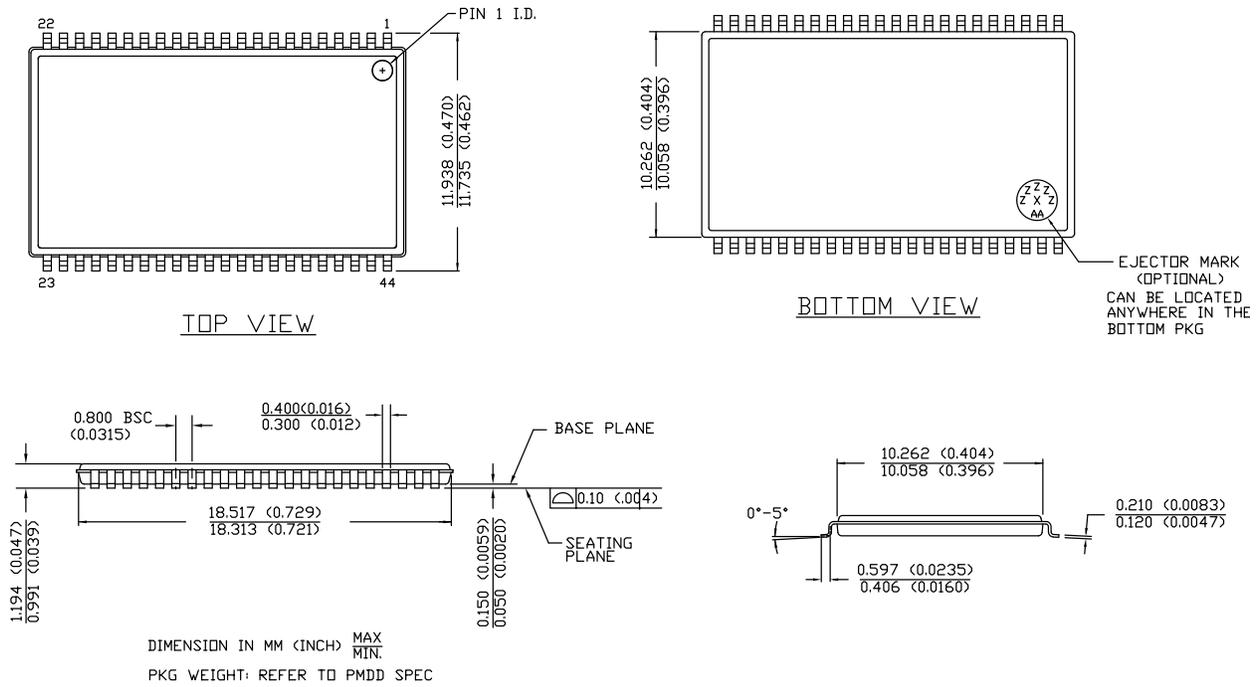


NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
 posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 13. 44-pin TSOP II Package Outline, 51-85087



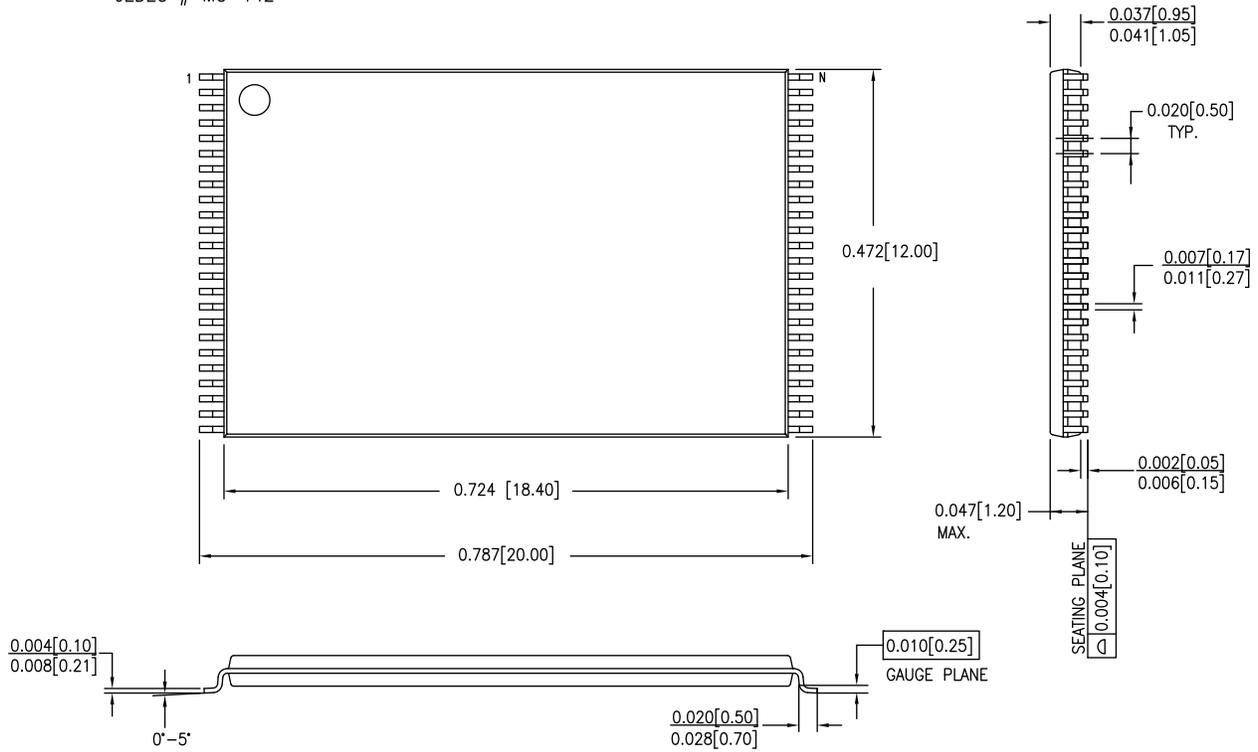
51-85087 *E

Package Diagrams (continued)

Figure 14. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183

DIMENSIONS IN INCHES[MM] MIN. MAX.

JEDEC # MO-142



51-85183 *D

Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| \overline{OE} | Output Enable |
| RAM | Random Access Memory |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| \overline{WE} | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62157EV30 MoBL®, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445 | | | | |
|---|--------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 202940 | AJU | See ECN | New data sheet. |
| *A | 291272 | SYT | See ECN | <p>Changed status from Advance Information to Preliminary. Removed 48-TSOP I Package and the associated footnote Added footnote stating 44 TSOP II Package has only one \overline{CE} on Page # 2 Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 4 to 4.5 μA Changed t_{OHA} from 6 to 10 ns for both 35 and 45 ns Speed Bins Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed t_{HZOE}, t_{HZBE} and t_{HZWE} from 12 and 15 ns to 15 and 18 ns for 35 and 45 ns Speed Bins respectively Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively Changed t_{SCE}, t_{AW} and t_{BW} from 25 and 40 ns to 30 and 35 ns for 35 and 45 ns Speed Bins respectively Changed t_{SD} from 15 and 20 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively Added Lead-Free Package Information</p> |
| *B | 444306 | NXR | See ECN | <p>Changed status from Preliminary to Final. Changed ball E3 from DNU to NC Removed redundant footnote on DNU. Removed 35 ns speed bin Removed "L" bin Added 48 pin TSOP I package Added Automotive product information. Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} Max value from 28 mA to 25 mA for test condition f = fax = 1/t_{RC}. Changed the I_{CC} Max value from 2.3 mA to 3 mA for test condition f = 1MHz. Changed the I_{SB1} and I_{SB2} Max value from 4.5 μA to 8 μA and Typ value from 0.9 μA to 2 μA respectively. Modified ISB_1 test condition to include \overline{BHE}, \overline{BLE} Updated Thermal Resistance table. Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ value for I_{CCDR}. Changed the I_{CCDR} Max value from 4.5 μA to 5 μA Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns. Changed t_{LZOE} from 3 to 5 Changed t_{LZCE} from 6 to 10 Changed t_{HZCE} from 22 to 18 Changed t_{LZBE} from 6 to 5 Changed t_{PWE} from 30 to 35 Changed t_{SD} from 22 to 25 Changed t_{LZWE} from 6 to 10 Added footnote #15 Updated the ordering Information and replaced the Package Name column with Package Diagram.</p> |
| *C | 467052 | NXR | See ECN | <p>Modified Data sheet to include x8 configurability. Updated the Ordering Information table</p> |
| *D | 925501 | VKN | See ECN | <p>Removed Automotive-E information Added Preliminary Automotive-A information Added footnote #10 related to I_{SB2} and I_{CCDR} Added footnote #15 related AC timing parameters</p> |

Document History Page (continued)

| Document Title: CY62157EV30 MoBL®, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445 | | | | |
|---|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *E | 1045801 | VKN | See ECN | Converted Automotive-A specs from preliminary to final Updated footnote #9 |
| *F | 2724889 | NXR / AESA | 06/26/09 | Added Automotive-E information Included -45ZXA/-55ZSX/-55ZXE parts in the Ordering Information table |
| *G | 2927528 | VKN | 05/04/2010 | Renamed “DNU” pins as “NC” for 48 TSOP I package Added footnote #24 related to chip enable Updated Package Diagrams Added Contents Updated links in Sales, Solutions, and Legal Information |
| *H | 3110053 | PRAS | 12/14/2010 | Changed Table Footnotes to Footnotes. Added Ordering Code Definitions. |
| *I | 3269771 | RAME | 05/30/2011 | Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Electrical Characteristics . Updated Data Retention Characteristics . Updated Package Diagrams . Added Acronyms and Units of Measure . Updated to new template. |
| *J | 3578601 | TAVA | 04/11/2012 | Updated Package Diagrams . |
| *K | 4102449 | VINI | 08/22/2013 | Updated Switching Characteristics : Updated Note 17. Updated Package Diagrams : spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template. |
| *L | 4126231 | VINI | 09/18/2013 | Updated Switching Characteristics : Updated Note 17 (Removed last sentence from Note 17 and added the same sentence as a new note namely Note 18). |
| *M | 4214977 | MEMJ | 12/09/2013 | Updated Pin Configurations : Updated Note 3 (Removed ‘NC’ mentioned at the end of the note). |
| *N | 4578508 | MEMJ | 11/24/2014 | Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. Updated Switching Characteristics : Added Note 22 and referred the same note in “Write Cycle”. Updated Switching Waveforms : Added Note 35 and referred the same note in Figure 10 . |
| *O | 4748627 | NILE | 04/30/2015 | Updated Package Diagrams : spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review. |
| *P | 5320972 | NILE | 06/23/2016 | Updated Thermal Resistance : Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated values of Θ_{JA} , Θ_{JC} parameters corresponding to all packages. Updated Ordering Information : Updated part numbers. Updated to new template. |

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