User's Manual

32

RX71M Group

Renesas Starter Kit+ User's Manual

RENESAS MCU
RX Family / RX700 Series

Renesas Electronics
www.renesas.com

Rev. 1.00 Jan 2015

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anticrime systems; and safety equipment etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

CAUTION

With reference to Directive 2014/30/EU Article 2, clause 2 (e) this is a custom built evaluation kit destined for professionals to be used solely at research and development facilities for such purposes. This equipment can cause radio frequency noise when used. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

CAUTION

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

EEDT-ST-004-10

For customers in the European Union only

The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the European Union only. This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner. Renesas Electronics Europe GmbH can take back end of life equipment, register for this service at http://www.renesas.eu/weee

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK+ hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK+ platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK+ and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSK+RX71M. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	RSK+RX71M User's Manual	R20UT3217EG
Tutorial Manual	Provides a guide to setting up RSK+ environment, running sample code and debugging programs.	RSK+RX71M Tutorial Manual	CS+: R20UT3218EG e^{2}studio: R20UT3222EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample, on a single A4 sheet.	RSK+RX71M Quick Start Guide	CS+: R20UT3219EG e^{2}studio: R20UT3223EG
Code Generator Tutorial Manual	Provides a guide to code generation and importing into the IDE (Integrated Development Environment).	RSK+RX71M Code Generator Tutorial Manual	CS+: R20UT3220EG e^{2}studio: R20UT3224EG
Schematics	Full detail circuit schematics of the RSK+.	RSK+RX71M Schematics	R20UT3216EG
User's Manual: Hardware	Provides technical details of the RX71M microcontroller.	RX71M Group User's Manual: Hardware	R01UH0493EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	Bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
E1	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not applicable
n/c (NC)	Not connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
RTC	Realtime Clock
SAU	Serial Array Unit
SCI	Serial Communications Interface
SFR	Special Function Registers
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TAU	Timer Array Unit
TFT	Thin Film Transistor
TPU	Timer Pulse Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog timer

Table of Contents

1. Overview 8
1.1 Purpose 8
1.2 Features 8
1.3 Board specification 9

2. Power Supply 10
2.1 Requirements 10
2.2 Power-Up Behaviour 10

3. Board Layout 11
3.1 Component Layout 11
3.2 Board Dimensions 12
3.3 Component Placement 13

4. Connectivity 15
4.1 Internal RSK+ Connections 15
4.2 Debugger Connections 16

5. User Circuitry 17
5.1 Reset Circuit 17
5.2 Clock Circuit 17
5.3 Switches 17
5.4 LEDs 18
5.5 Potentiometer 18
5.6 Pmod™ 19
5.7 USB Serial Port 20
5.8 Controller Area Network (CAN) 20
5.9 Ethernet 21
5.10 Universal Serial Bus (USB) 23
5.11 LCD Direct Drive Header (TFT) 24
5.12 External Bus 25
5.13 Renesas Serial Peripheral Interface (RSPI) 25
5.14 Quad Serial Peripheral Interface (QSPI) 25
5.15 I^2C Bus (Inter-IC Bus) 25
5.16 SD Host Interface (SDHI) 26
5.17 Parallel Data Capture Unit (PDC) 26
5.18 Serial Sound Interface (SSI) 27

6. Configuration 28
6.1 Modifying the RSK+ 28
6.2 MCU Operating Modes 28
6.3 E1 Debugger Configuration 29
6.4 Power Supply Configuration 30
6.5 Clock Configuration 30
6.6 Analog Power & ADC & DAC Configuration 31
6.7 BUS & SDRAM Configuration 32
6.8 CAN Configuration 36
6.9 LCD Direct Drive (TFT) Configuration 36
6.10 Ethernet Configuration 39
6.11 General IO & LED Configuration 42
6.12 I2C & EEPROM Configuration 44
6.13 MTU & TPU & POE Configuration 45
6.14 IRQ & NMI & Switch Configuration 49
6.15 PDC Configuration 50
6.16 PMOD1 Configuration 51
6.17 PMOD2 Configuration 52
6.18 QSPI Configuration 53

6.19 RSPI Configuration 54
6.20 SDHI Configuration 55
6.21 Serial & USB to Serial Configuration 56
6.22 SSI Configuration 57
6.23 USB Configuration 58

7. Headers 60
7.1 Application Headers 60
7.2 Generic Headers 65

8. Code Development 66
8.1 Overview 66
8.2 Compiler Restrictions 66
8.3 Mode Support 66
8.4 Debugging Support 66
8.5 Address Space 66

9. Additional Information 67

1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK+ hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialization code

The RSK+ board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Item	Specification
Microcontroller	Part No : R5F571MLCDFC
	Package : 176-pin LQFP
	On-Chip Memory : ROM 4MB+64KB, RAM 512KB+32KB+8KB
On-Board Memory	SDRAM : 128Mbit
	I²C EEPROM : 16Kbit
	SPI Serial Flash : 32Mbit x 2
Input Clock	RX71M Main : 24MHz
	RX71M Sub : 32.768kHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for MII) : 25MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC :5V Input, 3.3V Output
Coin Cell Holder	CR2032 Coin Cell Holder for Battery Backup Function
Debug Interface	E1 14-pin box header
DIP Switch	Mode Configuration : 4-pole x 1
	Function Configuration : 10-pole x 5
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	5V Power indicator: green x 1
	3.3V Power Indicator : green x 1
	User : green x 1, orange x 1, red x 2
	Ethernet Status: green x 4, yellow x 2
Ethernet	Connector : RJ45 x 2
	PHY : Dual Channel PHY
SDHI *1	SD Card Slot (4-bit) x 1
CAN	Connector : 2.54mm pitch, 3-pin x 1
	Driver : R2A25416SP (ISO-11898-2 compliance, support for high-speed communication of 1Mbps (max))
USB	USB0-Functiont : USB-MiniB
	USB0-Host : USB-TypeA
	USBA-Function : USB-MiniB
	USBA-Host : USB-TypeA
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 : Straight type, 12-pin Connector
PDC Interface *2	2.54 mm pitch, 20-pin x 1 (J26)
SSI Interface *2	2.54 mm pitch, 12-pin x 1 (J25)
LCD Direct Drive Interface *2	2.54 mm pitch, 50-pin x 1 (TFT)
Application Board Interface *2	2.54mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

Table 1-1: Board specification

*1. The RX71M Group incorporates an SD host interface (SDHI) which is compliant with the SD Specifications. When developing host devices that are compliant with the SD Specifications, the user must enter into the SD Host/Ancillary Product License Agreement (SD HALA).

*2. The connector is not included to a product.

2. Power Supply

2.1 Requirements

An E1 emulator is able to power the RSK+ board with up to 200mA. When the board is connected to another system then that system should supply power to the board. This board have an optional center positive supply connector using a 2.0mm barrel power jack. The default RSK+ power configuration is shown in **bold, blue text.**

This RSK+ board supports one external voltage input shown in **Table 2-1** below. Details of the external power supply connection are shown in **Table 2-2** below.

Connector	Supply voltage
PWR	Input 5VDC

Table 2-1: PWR connector Requirements

There are RSK products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally.

Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

J23Setting	R221	R222	Supply Source	Board_5V	UC_VCC
All open	Don't care	Don't care	**PW Connector**/CON_5V/Unregulated_VCC	**5V**	**3.3V**
	Don't care	Don't care	CON_3V3, E1(3V3)	n/a	3.3V
Pin1-2 shorted	Don't care	Don't care	EXT_BATT	5V	3.3V
Pin2-3 shorted	**Fit**	**DNF**	VBUSA	5V	3.3V
	DNF	Fit	VBUS0	5V	3.3V

Table 2-2: Main Power Supply Requirements

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the 'Release' build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit+ Code Generator Tutorial Manual' for further information of this example..

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

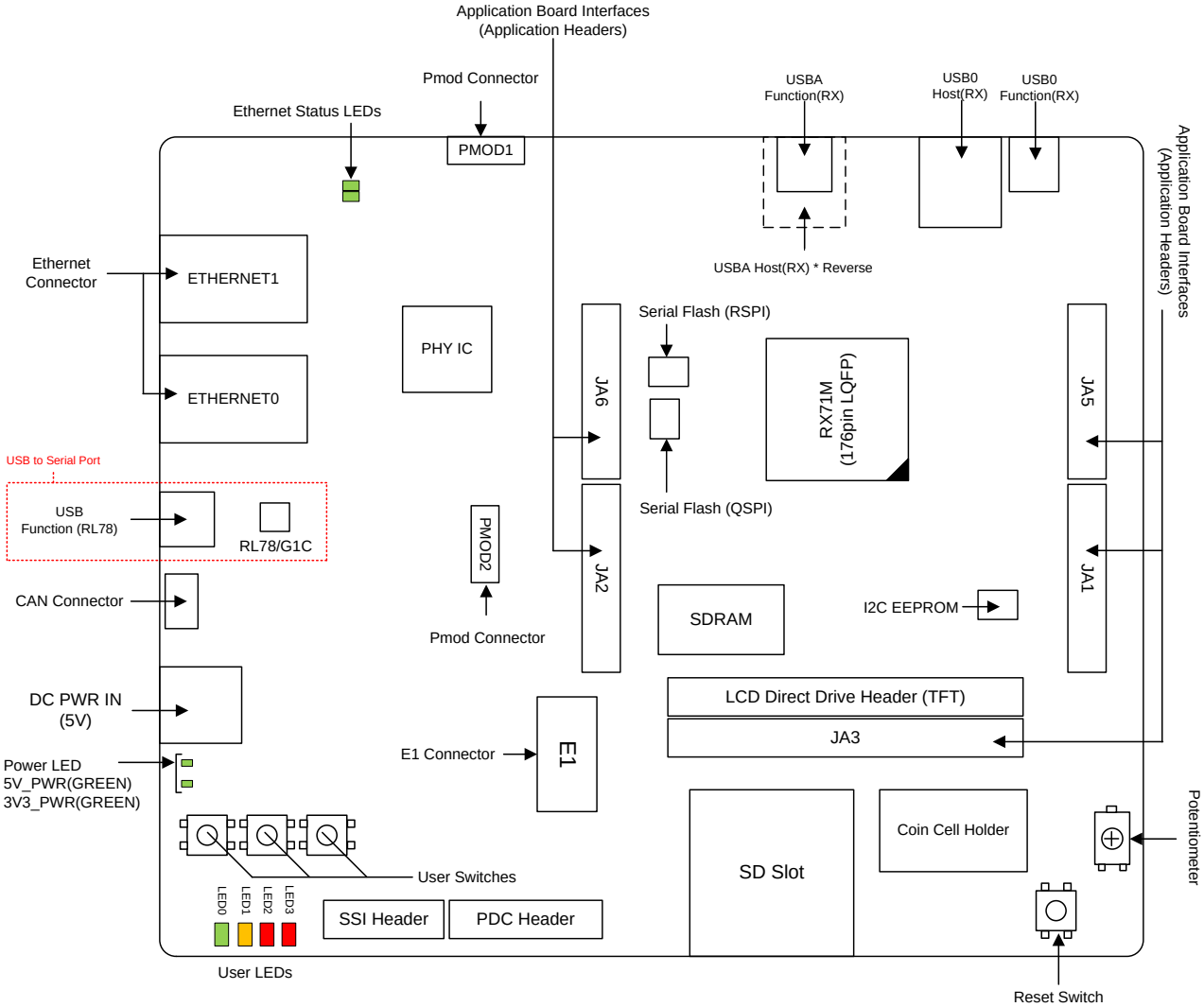

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

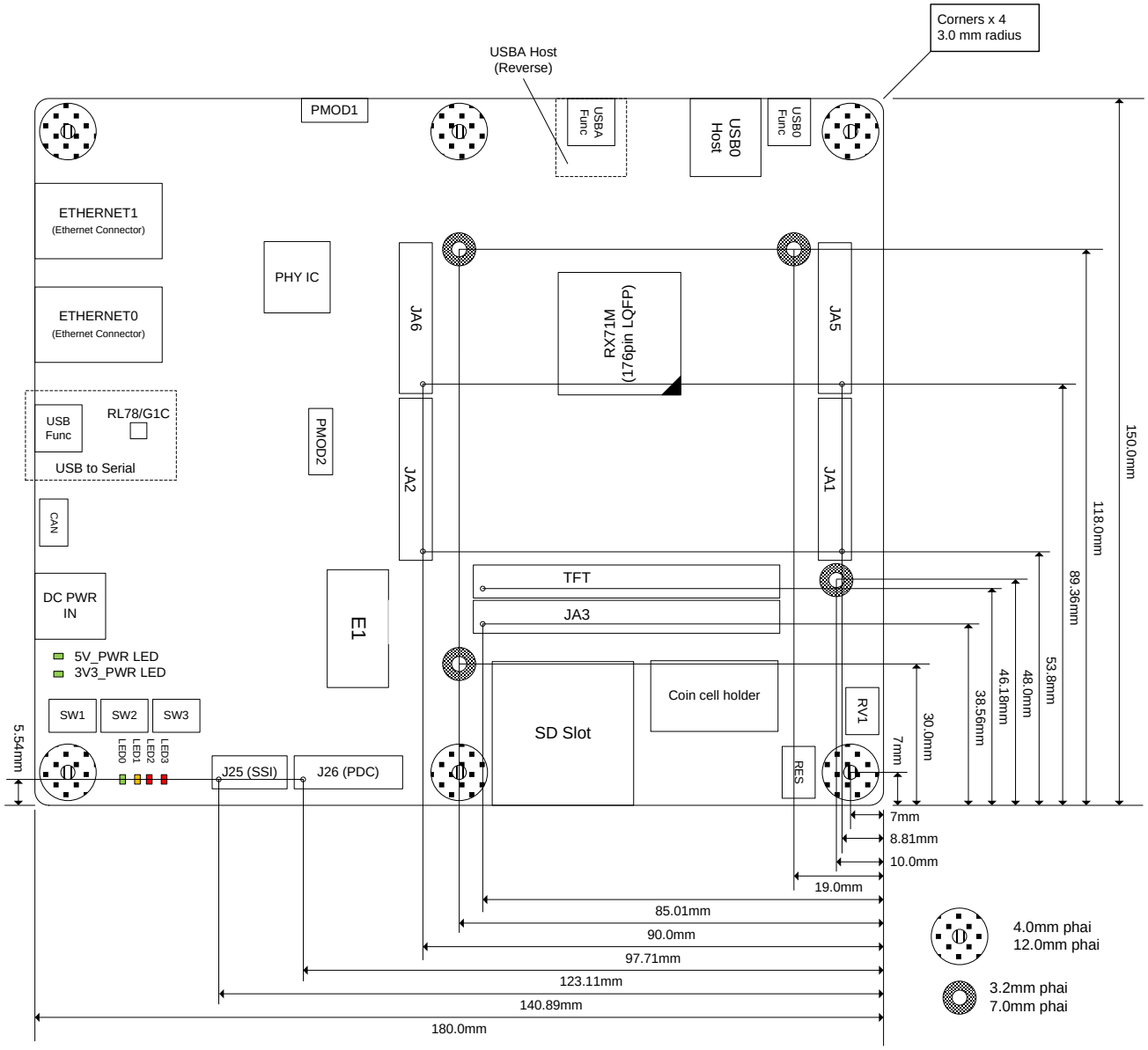

Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values can be looked up using the board schematics.

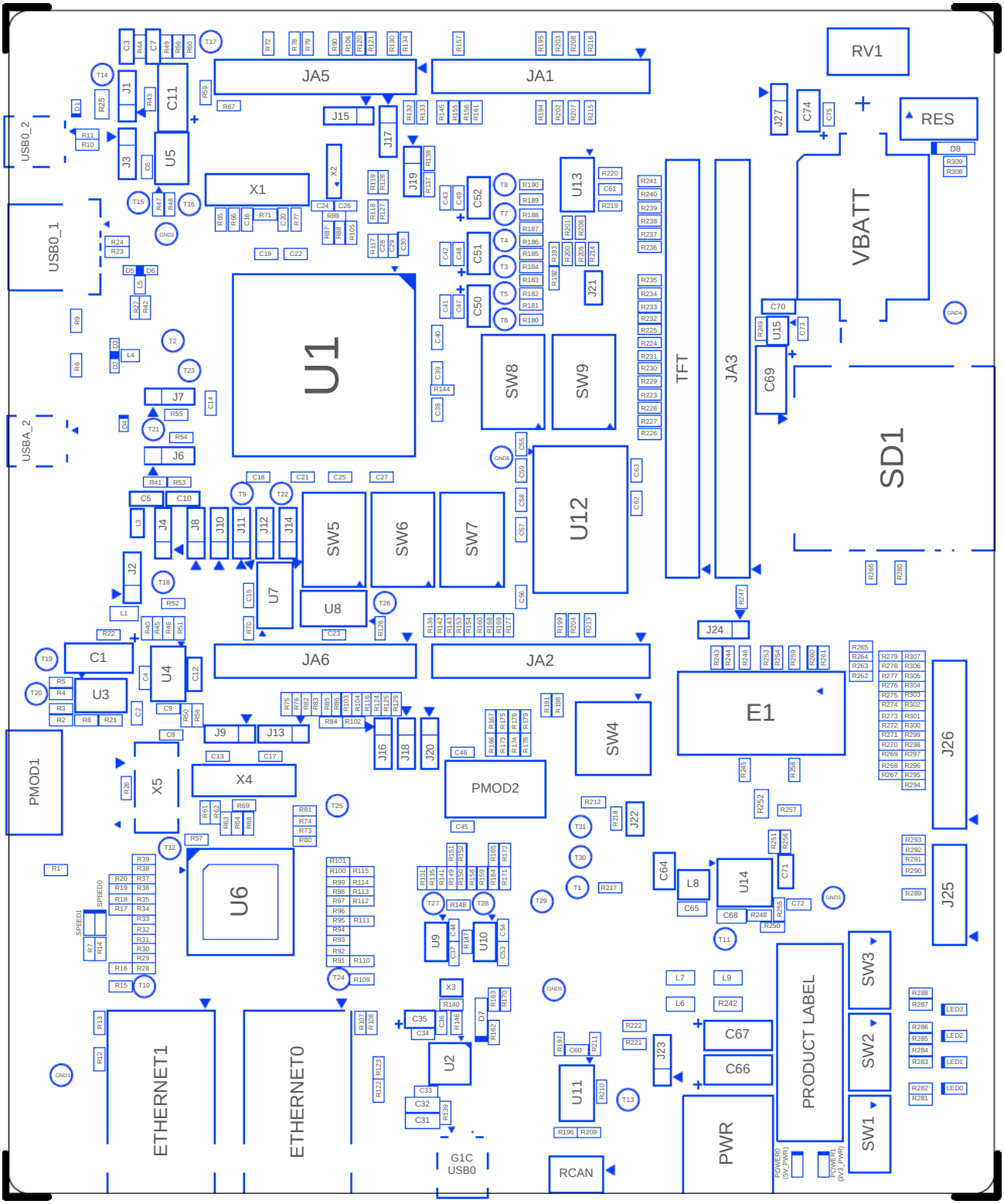

Figure 3-3: Top-Side Component Placement

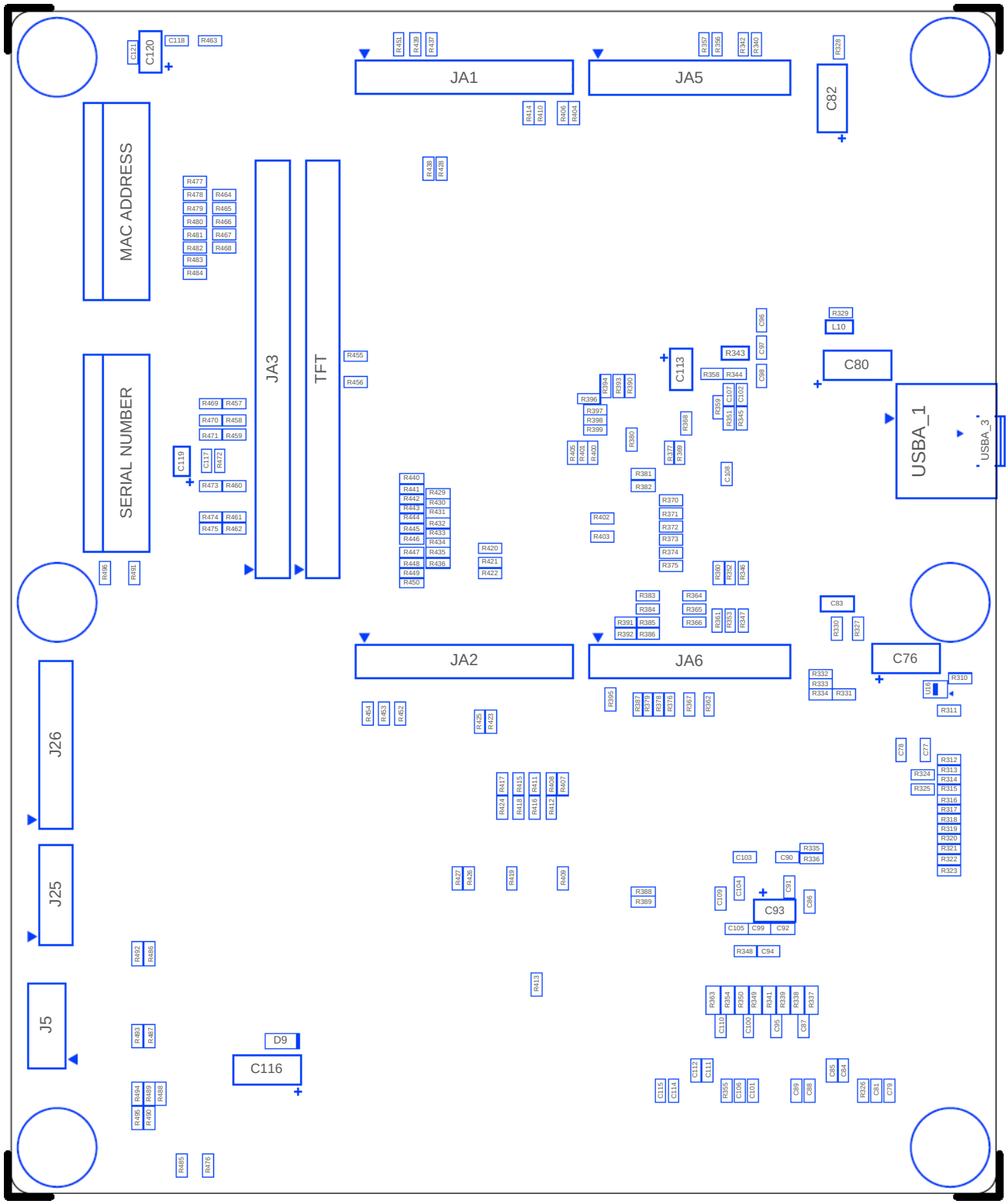

Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal RSK+ Connections

The diagram below shows the RSK+ board components and their connectivity to the MCU.

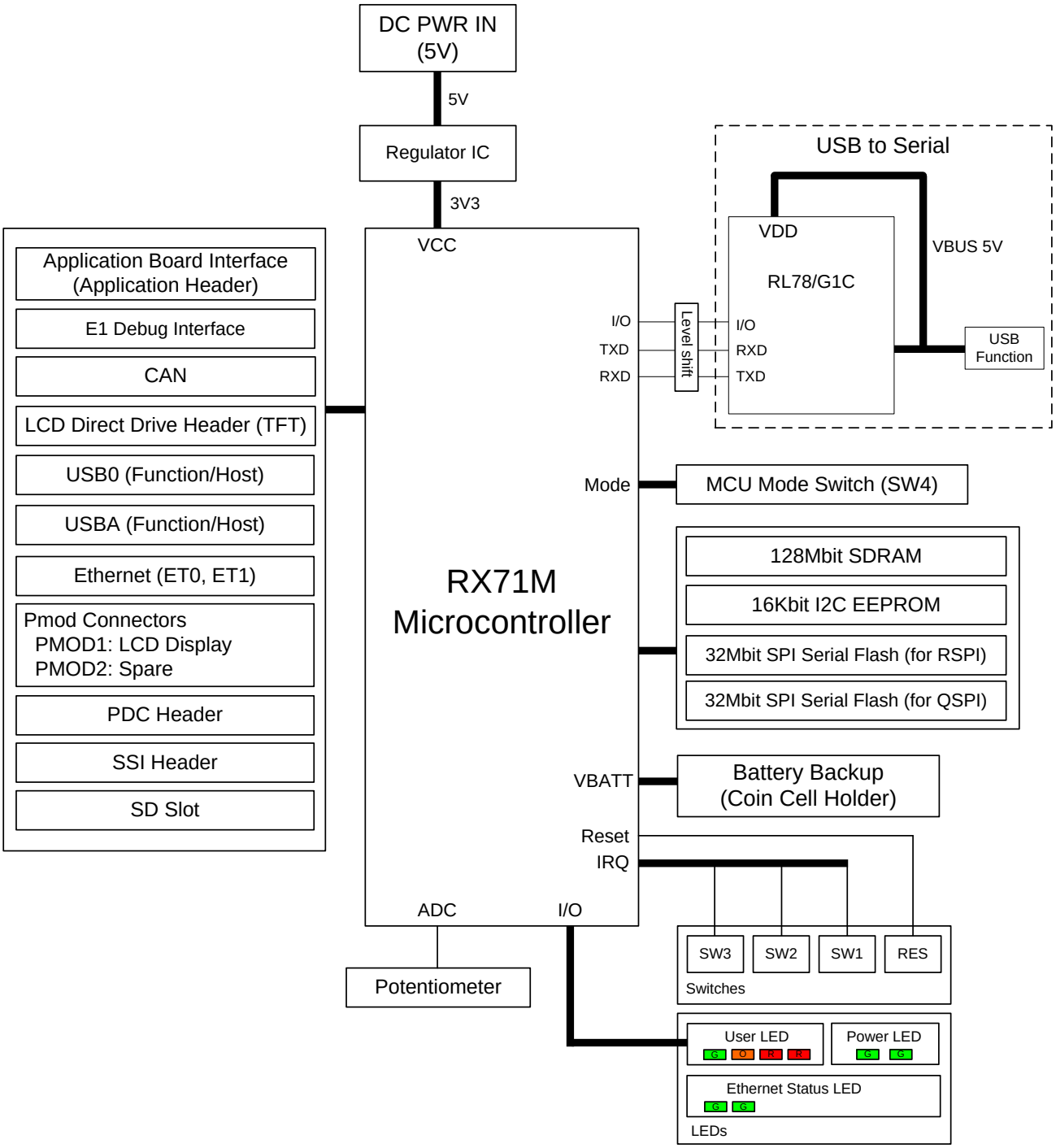

Figure 4-1: Internal RSK+ Block Diagram

4.2 Debugger Connections

The diagram below shows the connections between the RSK+, E1 debugger and the host PC.

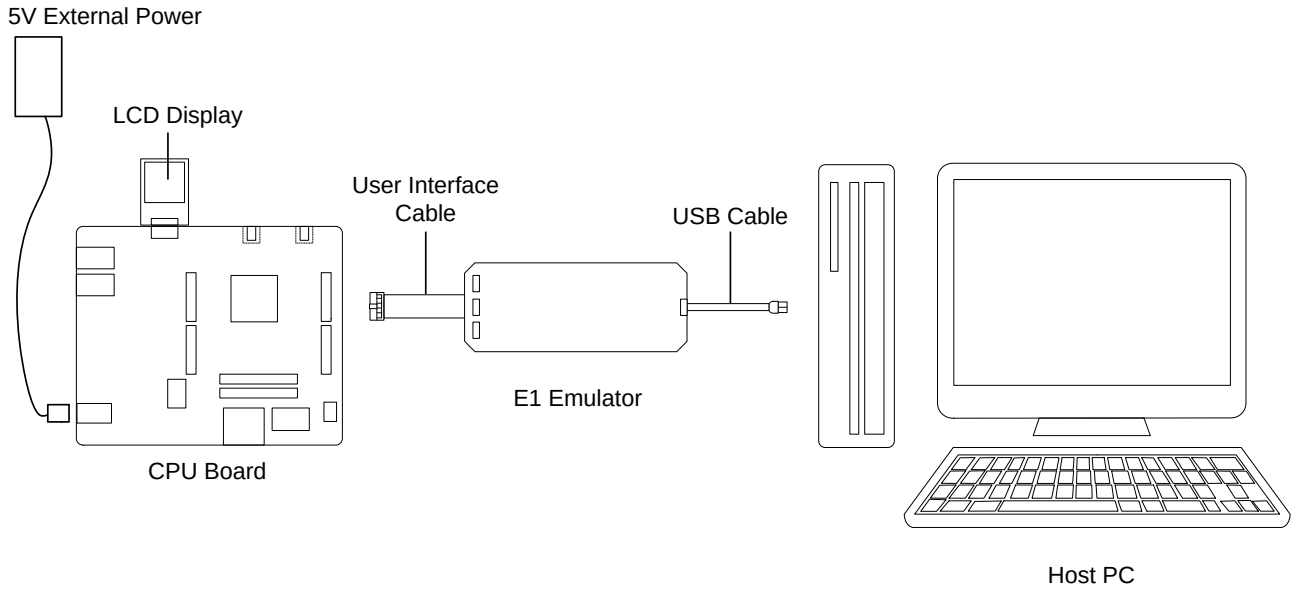

Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the RSK+ to generate a reset signal from the RES switch. Refer to the RX71M Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the RSK+ schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the RSK+ to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX71M Group User's Manual: Hardware and the RL78/G1C Group User's Manual: Hardware for details regarding the clock signal requirements, and the RSK+RX71M board schematics for information regarding the clock circuitry in use on the RSK+. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Crystal Oscillator	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX71M	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX71M	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X4	Crystal for Ethernet (MII)	Fitted	25MHz	Encapsulated, SMT
X5	Oscillator for Ethernet (RMII)	Unfitted	50MHz	Encapsulated, DIP half size

Table 5-1: Oscillators

* When evaluating RMII mode, it is necessary to mount the Oscillator X5. (Manufacture name: Epson, Model-name: SG-8002DC).

5.3 Switches

There are four switches located on the RSK+ board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the RSK+ board schematics.

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	21
SW1	Connects to an IRQ input for user controls.	IRQ5 (P15)	50
SW2	Connects to an IRQ input for user controls.	IRQ2 (P12)	53
SW3	Connects to an ADTRG input for ADC controls. (P07 can be used also as IRQ15)	ADTRG0n (P07)	176

Table 5-2: Switch Connections

5.4 LEDs

There are 12 LEDs on the RSK+ board. The function of each LED, its color, and its connections are shown in **Table 5-3**.

LED	Color	Function	MCU	
			Port	Pin
3V3_PWR	Green	Indicates the status of the Board_3V3 power rail.	NC	NC
5V_PWR	Green	Indicates the status of the Board_5V power rail.	NC	NC
LED0	Green	User operated LED.	P03	4
LED1	Orange	User operated LED.	P05	2
LED2	Red	User operated LED.	P26	37
LED3	Red	User operated LED.	P27	36
SPEED0	Green	Ethernet LED (Speed)	NC	NC
ETHERNET0 Connector	Green	Ethernet LED (Link)	P34	27
ETHERNET0 Connector	Yellow	Ethernet LED (Activity)	NC	NC
SPEED1	Green	Ethernet LED (Speed)	NC	NC
ETHERNET1 Connector	Green	Ethernet LED (Link)	P93	159
ETHERNET1 Connector	Yellow	Ethernet LED (Activity)	NC	NC

Table 5-3: LED Connections

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000 (Port P40, Pin 173). The potentiometer can be used to create a voltage between Board_3V3 and ground.
Refer to the maker site for specification of the potentiometer (PIHER with part number N6 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX71M Group User's Manual: Hardware for further details.

5.6 Pmod™

A Pmod™ Compatible debug LCD module is supplied with the RSK+ board, and should be connected to the PMOD1 header.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4** and **Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK+ designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011

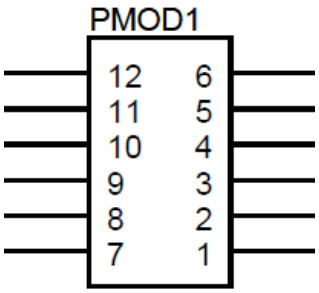

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header (PMOD1) Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	CTS6RTS6	PJ3	13	7	IRQ8	P20	45
	P45	P45	167				
2	TXD6	P00	8	8	IRQ9	P21	44
3	RXD6	P01	7	9	P46	P46	166
4	SCK6	P02	6	10	P47	P47	165
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-4: Pmod™1 Header Connections

Digilent Pmod™ Compatible Header (PMOD2) Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	P-CTS7RTS7	P93	159	7	IRQ10-DS	P42	170
2	P-TXD7	P90	163	8	IRQ11-DS	P43	169
3	P-RXD7	P92	160	9	P96	P96	152
4	P-SCK7	P91	161	10	P97	P97	149
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-5: Pmod™2 Header Connections

5.7 USB Serial Port

A USB serial port implemented in another Renesas low power microcontroller (RL78/G1C) is fitted on the RX71M Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI7 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Signal Name	Function	MCU	
		Port	Pin
TXD1*[1]	SCI1 Transmit Signal.	PF0	35
RXD1*[1]	SCI1 Receive Signal	PF2	31
TXD2*[1]	SCI2 Transmit Signal.	P50	72
RXD2*[1]	SCI2 Receive Signal	P52	70
A-TXD7	SCI7 Transmit Signal.	P90	163
A-RXD7	SCI7 Receive Signal	P92	160
RS232TX*[1]	External SCI Transmit Signal.	-	-
RS232RX*[1]	External SCI Receive Signal.	-	-
RXCTS*[2]	Clear To Send	P41	171
RXRTS*[2]	Request to Send	PJ5	11

Table 5-6: Serial Port Connections

*[1]. This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

*[2]. CTS & RTS control is not supported on this RSK+.

When the RSK+ board is first connected to a PC running Windows with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

Figure 5-2: USB-Serial Windows Installation message

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+ board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX71M Group User's Manual: Hardware.

The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

CAN Signal	Function	MCU	
		Port	Pin
CTX0	CAN Data Transmission.	P32	29
CRX0	CAN Data Reception.	P33	28

Table 5-7: CAN Connections

5.9 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the RSK+RX71M PCB as a sticker, and should be always be used with this device ensured to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

An Ethernet controller IC is fitted to the RSK+ board, and is connected to the Ethernet MCU peripheral. The RX71M MCU supports full duplex 10Mb/s and 100Mb/s transmission and reception. The connections for the Ethernet controller are listed in **Table 5-8** and **Table 5-9** below.

Ethernet signal	Function	MCU	
		Port	Pin
ET0MDIO	Management data serial I/O	P71	102
ET0MDC	Management serial clock	P72	101
ET0TXCLK	Transmit clock	PC4	82
ET0TXEN_RMII0TXDEN	Transmit enable.	P80	81
ET0TXER*	Transmit error.	PC3	83
ET0ETXD0_RMII0TXD0	Transmit data bit 0.	P81	80
ET0ETXD1_RMII0TXD1	Transmit data bit 1.	P82	79
ET0ETXD2	Transmit data bit 2.	PC5	78
ET0ETXD3	Transmit data bit 3.	PC6	77
ET0RXCLK	Receive clock.	P76	85
ET0RXDV	Receive data valid.	PC2	86
ET0RXER_RMII0RXER	Receive data error.	P77	84
ET0ERXD0_RMII0RXD0	Receive data bit 0.	P75	87
ET0ERXD1_RMII0RXD1	Receive data bit 1.	P74	88
ET0ERXD2	Receive data bit 2.	PC1	89
ET0ERXD3	Receive data bit 3.	PC0	91
ET0COL	Collision detects.	PC7	76
ET0LINKSTA	Link status input.	P34	27
ET0CRS_RMII0CRSDV	Carrier sense	P83	74

Table 5-8: Ethernet Connections (ET0)

* It is connected to a testpoint (T26).

Ethernet signal	Function	MCU	
		Port	Pin
ET1MDIO	Management data serial I/O	P30	33
ET1MDC	Management serial clock	P31	32
ET1TXCLK	Transmit clock	PG2	123
ET1TXEN_RMII1TXDEN	Transmit enable.	P60	141
ET1TXER*	Transmit error.	PG7	111
ET1ETXD0_RMII1TXD0	Transmit data bit 0.	PG3	121
ET1ETXD1_RMII1TXD1	Transmit data bit 1.	PG4	119
ET1ETXD2	Transmit data bit 2.	PG5	116
ET1ETXD3	Transmit data bit 3.	PG6	113
ET1RXCLK	Receive clock.	PG0	146
ET1RXDV	Receive data valid.	P90	163
ET1RXER_RMII1RXER	Receive data error.	PG1	144
ET1ERXD0_RMII1RXD0	Receive data bit 0.	P94	157
ET1ERXD1_RMII1RXD1	Receive data bit 1.	P95	155
ET1ERXD2	Receive data bit 2.	P96	152
ET1ERXD3	Receive data bit 3.	P97	149
ET1COL	Collision detects.	P91	161
ET1LINKSTA	Link status input.	P93	159
ET1CRS_RMII1CRSDV	Carrier sense	P92	160

Table 5-9: Ethernet Connections (ET1)

*It is only connected to a testpoint (T22).

5.10 Universal Serial Bus (USB)

This RSK+ board is fitted with a USB host socket (type A) and a function socket (type Mini B). USB module USB0 is connected to the host and function socket, and can operate as either a host or function device. USB module USBA is connected to the host and function socket, and can operate as either a host or function device. The connections for the USB0 module and USBA module are shown in **Table 5-10** and **Table 5-11** below.

USB Signal	Function	MCU	
		Port	Pin
USB0DP	Positive differential data signal.	USB0_DP	56
USB0DM	Negative differential data signal.	USB0_DM	55
USB0VBUS	Cable monitor pin.	P16	48
USB0VBUSEN	VBUS power supply enable.		
USB0OVRCURA	Over-current detection signal A.	P14	51

Table 5-10: USB0 Module Connections

USB Signal	Function	MCU	
		Port	Pin
USBADP	Positive differential data signal.	USBA_DP	64
USBADM	Negative differential data signal.	USBA_DM	63
USBAVBUS	Cable monitor pin.	P11	67
USBAVBUSEN	VBUS power supply enable.		
USBAOVRCURA	Over-current detection signal A.	P10	68
USBAOVRCURB	Over-current detection signal B.	P22	43
USBAEXICEN	Low-power control signal	P21	44
USBAID	ID input signal	P20	45

Table 5-11: USBA Module Connections

Note: This RSK+ board is equipped with the OTG (On The Go™) circuit for USB module USBA.
When evaluating OTG, it is necessary to mount the socket for OTG separately. (Manufacture name: Hirose Electric, Model-name: ZX62 R-AB-5P)

5.11 LCD Direct Drive Header (TFT)

This RSK+ board is fitted with a LCD Direct Drive thru-hole pattern, which allows connection to compatible Renesas LCD application boards.
The pin connections of this header are listed in **Table 5-12** below.

LCD Direct Drive Header (TFT)							
Pin	Header Name	MCU		Pin	Header Name	MCU	
		Port	Pin			Port	Pin
1	5V	-	-	2	5V	-	-
3	3V3	-	-	4	3V3	-	-
5	Reserved	-	-	6	Reserved	-	-
7	Blue	PD0	158	8	Blue	PD1	156
9	Blue	PD2	154	10	Blue	PD3	150
11	Blue	PD4	148	12	Green	PD5	147
13	Green	PD6	145	14	Green	PD7	143
15	Green	PE0	135	16	Green	PE1	134
17	Green	PE2	133	18	Red	PE3	132
19	Red	PE4	131	20	Red	PE5	130
21	Red	PE6	126	22	Red	PE7	125
23	EDACK	P83	74	24	TFT_HSYNC	PJ3	13
25	DOTCLK	P34	27	26	LCDDEN	PC1	89
27	TFT_VSYNC	P26	37	28	EDREQ	P82	79
29	SSCK	P77	84	30	SSI	PC4	82
31	SSO	PC3	83	32	SCS	P76	85
33	RESET	RES#	21	34	GND	-	-
35	BACKLIGHT	P27	36	36	SD_DOTCLK	-	-
37	GND	-	-	38	GND	-	-
39	GND	-	-	40	GND	-	-
41	X_DRIVE	PJ5	11	42	Y_DRIVE	P41	171
43	X_INPUT	P44	168	44	Y_INPUT	P45	167
45	X_INPUT	P46	166	46	Y_INPUT	P47	165
47	Reserved	-	-	48	Reserved	-	-
49	Reserved	-	-	50	Reserved	-	-

Table 5-12: Generic LCD Header Connections

5.12 External Bus

The RX71M features an external data bus, which is connected to various devices on the RSK+ board. Details of the devices connected to the external data bus are listed in **Table 5-13** below. Further details of the devices connected to the external bus can be found in the board schematics.

Chip Select	Device Name	Device Description	Address Space
CS0	JA3	Application Header	FF000000h to FFFFFFFFh (16Mbytes)
SDCS	U12	128MBit SDRAM	08000000h to 0FFFFFFFh (128Mbytes)
	JA3	Application Header	08000000h to 0FFFFFFFh (128Mbytes)
CS1 to CS3	-	Unused	05000000h to 07FFFFFFh (3 x 16Mbytes)
CS4	JA3	Application Header	04000000h to 04FFFFFFh (16Mbytes)
CS5 to CS7	-	Unused	01000000h to 03FFFFFFh (3 x 16Mbytes)

Table 5-13: External Bus Address Space

5.13 Renesas Serial Peripheral Interface (RSPI)

The RX71M features one Renesas Serial Peripheral Interface modules (Renesas SPI or RSPI). **Table 5-14** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
SSLA1-A	U7	SPI Serial Flash, 32Mbits

Table 5-14: RSPI Connections

5.14 Quad Serial Peripheral Interface (QSPI)

The RX71M features one Quad Serial Peripheral Interface modules (QSPI). **Table 5-15** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
QSSL-A (BD_QSSL-A)	U8	SPI Serial Flash, 32Mbits
QSSL-A (TFT_QSSL-A)	TFT	LCD Direct Drive Header

Table 5-15: QSPI Connections

5.15 I^2C Bus (Inter-IC Bus)

The RX71M features two I^2C (Inter-IC Bus) interface modules. RIIC2 is connected to a 16Kbit EEPROM (Electronically-Erasable Programmable Read Only Memory). Specific details of the EEPROM device and the connections can be found in the board schematics.

On board EEPROM only supports single device on bus. To allow external I^2C device, option links have to be modified – refer to §6 for further details.

5.16 SD Host Interface (SDHI)

A SD Card Slot is fitted to the RSK+ board, and connected to the SD Host Interface (SDHI) MCU peripheral. For further details regarding the SDHI operation, please refer to the RX71M Group User's Manual: Hardware. The connections for the SDHI signals are listed in **Table 5-16** below.

SD Card Slot (SD1)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDHID3-B	PD3	150	2	SDHICMD-B	PD4	148
3	GROUND	-	-	4	SDPWREN	PF5	9
5	SDHICLK-B	PD5	147	6	GROUND	-	-
7	SDHID0-B	PD6	145	8	SDHID1-B	PD7	143
9	SDHID2-B	PD2	154	10	SDHICD-B	PE6	126
11	GROUND	-	-	12	SDHIWP-B	PE7	125

Table 5-16: SDHI Connections

5.17 Parallel Data Capture Unit (PDC)

This RSK+ board is fitted with a Parallel Data Capture Unit (PDC) thru-hole pattern.
The connections for the PDC signals are listed in **Table 5-17** below.

PDC Header (J26)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-	-	2	Board_3V3	-	-
3	GROUND	-	-	4	GROUND	-	-
5	PCKO	P33	28	6	RESn	RESn	21
7	GND	-	-	8	PIXCLK	P24	40
9	VSYNC	P32	29	10	HSYNC	P25	38
11	PIXD7	P23	42	12	PIXD6	P22	43
13	PIXD5	P21	44	14	PIXD4	P20	45
15	PIXD3	P17	46	16	PIXD2	P87	47
17	PIXD1	P86	49	18	PIXD0	P15	50
19	PDC_SSDA6	P00	8	20	PDC_SSCL6	P01	7

Table 5-17: PDC Connections

5.18 Serial Sound Interface (SSI)

This RSK+ board is fitted with a Serial Sound Interface (SSI) thru-hole pattern.
The connections for the SSI signals are listed in **Table 5-18** below.

SSI Header (J25)							
Pin	**Circuit Net Name**	**MCU**		**Pin**	**Circuit Net Name**	**MCU**	
		Port	**Pin**			**Port**	**Pin**
1	Board_5V	-	-	2	Board_3V3	-	
3	GROUND	-	-	4	GROUND	-	-
5	AUDIOMCLK	P22	43	6	GROUND	-	-
7	GROUND	-	-	8	NC	-	-
9	SSISCK0	P23	42	10	SSIRXD0	P20	45
11	SSIWS0	P21	44	12	SSITXD0	P17	46

Table 5-18: SSI Connections

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way RSK+ operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to connect or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the RSK+ is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the RSK+ is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX71M Group User's Manual: Hardware and RSK+RX71M schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU operating modes.

Reference	Pin1	Pin2	Pin3	Explanation	Related Ref.
SW4	**OFF**	**OFF**	**OFF**	**Single Chip Mode**	-
	ON	OFF	OFF	User Boot Mode USB Boot Mode (Bus-powered)	-
	OFF	ON	OFF	Single Chip Mode	-
	ON	ON	OFF	SCI Boot Mode	-
	OFF	OFF	ON	Single Chip Mode	-
	ON	OFF	ON	User Boot Mode USB Boot Mode (Self-powered)	-
	OFF	ON	ON	Single Chip Mode	-
	ON	ON	ON	SCI Boot Mode	-

Table 6-1: MCU Mode Switch Settings

6.3 E1 Debugger Configuration

Table 6-2 below details the function of the option links associated with E1 Debugger configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J11.Pin1-2	-	U7.2	-	-
			ET0COL	J11.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.3	-	-
			PC7	J11.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2	-	-
						E1.10	R245	-
TDO_TXD1	35	PF0	TDO	R253	R151	E1.5	-	-
			TXD1	R151	R253	U9.3	R149	R135, R141, R150
						JA6.8	R129	-
TCK_SCK1	34	PF1	TCK	R261	R378	E1.1	-	-
			SCK1	R378	R261	JA6.10	R103	-
TDI_RXD1	31	PF2	TDI	R243	R165	E1.11	-	-
			RXD1	R165	R243	U10.3	R164	R158, R159, R171
						JA6.7	R126	-
EMLE	10	-	EMLE	-	-	J19.2	-	-
						E1.4	R258	-

Table 6-2: E1 Debugger Option Links

Table 6-3 below details the function of the jumpers associated with the E1 Debugger.

Reference	Jumper Position	Explanation	Related Ref.
J19	Shorted Pin1-2	Enables E1 debugging with Hot plug-in function.	-
	Shorted Pin2-3	Enables E1 normal debugging and MCU single operation (without E1).	-
	All open	DO NOT SET	-

Table 6-3: E1 Debugger Jumper Settings

6.4 Power Supply Configuration

Table 6-4 below details the function of the option links associated with power supply configuration.

Reference	MCU Peripheral Selection			Destination Selection
	Function	Fit	DNF	Interface Function
VBUS0, VBUSA	Connects VBUS0 to 5V Power rail.	J1.Pin2-3, J23.Pin2-3, R222	R221	U14
	Connects VBUSA to 5V Power rail.	J4.Pin2-3, J23.Pin2-3, R221	R52, R222	U14
Board_5V	Connects 5V power rail to Board_5V.	R242	-	IIC Pull-up resistors(R262, R414), 5V_PWR, U11.3, U13(R219), J25.1, J26.1, TFT.1, 2
SD_3V3	Connects 3.3V power rail to SD_3V3.	R252	-	U15.1
CON_3V3	Connects CON_3V3 to 3.3V power rail.	R257	-	JA1.3
VCCUSB	Connects 3V3 power rail to VCCUSB.	R217	R212	U1(VCC_USB)
	Connects UC_VCC to VCCUSB.	R212	R217	U1(VCC_USB)
UC_VCC	Connects 3.3V power rail to UC_VCC	R218	-	J22, U1(VCC)

Table 6-4: Power Supply Option Links

Table 6-5 below details the function of the jumpers associated with the power supply.

Reference	Jumper Position	Explanation	Related Ref.
J22	Shorted Pin1-2	Connects 3.3V power rail to UC_VCC.	R218
	All open	Enables current probe for measurement MCU current consumption.	R218
J23	Shorted Pin1-2	Enables external battery input.	-
	Shorted Pin2-3	Enables VBUS input.	R221, R222
	All open	Disables external battery input and VBUS input.	-
J27	Shorted Pin1-2	Connects UC_VCC to VBAT.	-
	Shorted Pin2-3	Connects external coin cell input.	-
	All open	DO NOT SET	-

Table 6-5: Power Supply Jumper Settings

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with clock configuration.

Reference	MCU Peripheral Selection			Destination Selection
	Function	Fit	DNF	Interface Function
XTAL, EXTAL, CON_EXTAL	Connects 24MHz crystal (X1) to RX71M.	R66, R77	R65	U1(EXTAL, XTAL)
	Connects CON_EXTAL to RX71M.	R65	R66, R77	U1(EXTAL)
XCIN, XCOUT	Connects 32.768kHz crystal (X2) to RX71M.	R87, R88	R105	U1(XCIN, XCOUT)
	Disconnects X2 from RX71M.	R105	R87, R88	U1(XCIN, XCOUT)
REF50CK0, REF50CK1	Connects 25MHz crystal (X4) to PHY.	R64, R68	R63	U6(X1, X2)
	Connects 50MHz oscillator (X5) to PHY and REF50CK0 (RX71M).	R62, R63	R26, R64, R68	U6(X1), U1.85
	Connects 50MHz oscillator (X5) to PHY and REF50CK1 (RX71M).	R61, R63	R26, R64, R68	U6(X1), U1.146

Table 6-6: Clock Option Links

6.6 Analog Power & ADC & DAC Configuration

Table 6-7 below details the function of the option links associated with ADC & DAC configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
AN000	173	P40	AN000	-	-	RV1	R463	-
						JA1.9 (Direct Input via JA1.9)	R208	R216, R437
						JA1.9 (Input via Voltage Division Resistor)	R216, R437	R208
AN001_RXCTS_YDRIVE	171	P41	AN001	R207	R237, R419	JA1.10	-	-
			RXCTS	R419	R207, R237	U10.2	-	-
			YDRIVE	R237	R207, R419	TFT.42	-	-
AN002_IRQ10-DS	170	P42	AN002	R203	R179	JA1.11	-	-
			IRQ10-DS	R179	R203	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R202	R176	JA1.12	-	-
			IRQ11-DS	R176	R202	PMOD2.8	-	-
AN004_XINPUT1	168	P44	XINPUT1	R238	R134	TFT.43	-	-
			AN004	R134	R238	JA5.1	-	-
AN005_YINPUT1_P45	167	P45	YINPUT1	R239	R133	TFT.44	-	-
			AN005	R133	R239, R427	JA5.2	-	-
			P45	R427	R133	PMOD1.1	R426	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R240	R130	TFT.45	-	-
			AN006	R130	R240, R315	JA5.3	-	-
			P46	R315	R130	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R241	R132	TFT.46	-	-
			AN007	R132	R241, R313	JA5.4	-	-
			P47	R313	R132	PMOD1.10	-	-
LED0_DA0	4	P03	LED0	R281	R195	LED0	-	-
			DA0	R195	R281	JA1.13	-	-
LED1_DA1	2	P05	LED1	R284	R194	LED1	-	-
			DA1	R194	R284	JA1.14	-	-
ADTRG0n	176	P07	ADTRG0n	-	-	SW3	R492	-
						JA1.8	-	-
VREFH0	174	-	UC_VCC	R181	R182	-	-	-
			CON_VREFH0	R182	R181	JA1.7	-	-
VREFL0	172	-	GROUND	R180	-	-	-	-
AVCC0	175	-	UC_VCC	R184	R183, R185	-	-	-
			CON_AVCC0	R183	R184 R185	JA1.5	-	-
			Board_3V3	R185, R186	R183, R184	-	-	-
AVSS0	1	-	GROUND	R188	R187	-	-	-
			CON_AVSS0	R187	R188	JA1.6	-	-
AVCC1	3	-	UC_VCC	R189	-	-	-	-
AVSS1	5	-	GROUND	R190	-	-	-	-

Table 6-7: Analog Power & ADC & DAC Option Links

6.7 BUS & SDRAM Configuration

Table 6-8 to **Table 6-11** below details the function of the option links associated with BUS & SDRAM configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R362	R76, R480	U3.2	R4	R45
						U4.5	R45	R4
			ALE	R480	R76, R362	JA3.46	R466	R447
			MTIC5W	R76	R362, R480	JA5.14	R357	R75
						JA6.16	R75	R357
WRn_WR0n_TXD2_SSDA2	72	P50	WRn	R116	R104, R124, R125	JA3.26	R387	R431
			WR0n	R124	R104, R116, R125	JA3.48	R464	R429
			TXD2	R104	R116, R124, R125	U9.3	R135	R141, R149, R150
						JA6.9	-	-
			SSDA2	R125	R104, R116, R124	JA1.25	R145	R155
WR1n_WAITn_SCK2	71	P51	WAITn	R483	R478, R484	JA3.45	R468	R467
			WR1n	R478	R483, R484	JA3.47	R465	R444
			SCK2	R484	R483, R478	JA6.11	-	-
RDn_RXD2_SSCL2	70	P52	RDn	R86	R84, R85	JA3.25	-	-
			RXD2	R85	R84, R86	U10.3	R159	R158, R164, R171
						JA6.12	-	-
			SSCL2	R84	R85, R86	JA1.26	R156	R161
BCLK	69	P53	BCLK	R344	-	JA3.44	R358	R445
ET1TXEN_RMII1TXDEN_CS0n	141	P60	ET1TXEN_RMII1TXDEN	R111	R397	U6.49	R95	-
			CS0n	R397	R111	JA3.45	R467	R468
SDCSn	139	P61	BD_SDCSn	R435	R398	U12.19	-	-
			CON_SDCSn	R398	R435	JA3.28	-	-
RASn	138	P62	RASn	-	-	U12.18	-	-
						JA3.50	-	-
CASn	137	P63	CASn	-	-	U12.17	-	-
						JA3.49	-	-
WEn	136	P64	WEn	-	-	U12.16	-	-
						JA3.26	R431	R387
CKE	124	P65	CKE	-	-	U12.37	-	-
						JA3.46	R447	R466
DQM0_MTIOC7D	122	P66	DQM0	R430	R59	U12.15	-	-
						JA3.48	R429	R464
			MTIOC7D	R59	R430	JA5.24	-	-
DQM1_MTIOC7C	120	P67	DQM1	R443	R67	U12.39	-	-
						JA3.47	R444	R465
			MTIOC7C	R67	R443	JA5.22	-	-

Table 6-8: BUS & SDRAM Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
SDCLK	128	P70	SDCLK	R380	-	U12.38	R446	-
						JA3.44	R445	R358
ET0ERXD1_RMII0RXD1_CS4n	88	P74	ET0ERXD1_RMII 0RXD1	SW6.7.ON	SW6.8.OFF	U6.5	R36	-
			CS4n	SW6.8.ON	SW6.7.OFF	JA3.27	-	-
A0_MTIOC6D	118	PA0	A0	R247	R340	JA3.1	-	-
			MTIOC6D	R340	R247	JA5.20	-	-
A1_MTIOC7B	114	PA1	A1	R421	R377	U12.23, JA3.2	-	-
			MTIOC7B	R377	R421	JA5.23	-	-
A2_MTIOC7A	112	PA2	A2	R422	R369	U12.24, JA3.3	-	-
			MTIOC7A	R369	R422	JA5.21	-	-
A3	110	PA3	A3	-	-	U12.25, JA3.4	-	-
A4	109	PA4	A4	-	-	U12.26, JA3.5	-	-
A5_MTIOC6B	108	PA5	A5	R450	R368	U12.29, JA3.6	-	-
			MTIOC6B	R368	R450	JA5.19	-	-
A6	107	PA6	A6	-	-	U12.30, JA3.7	-	-
A7	106	PA7	A7	-	-	U12.31, JA3.8	-	-
A8	104	PB0	A8	-	-	U12.32, JA3.9	-	-
A9	100	PB1	A9	-	-	U12.33, JA3.10	-	-
A10	99	PB2	A10	-	-	U12.34, JA3.11	-	-
A11	98	PB3	A11	-	-	U12.22, JA3.12	-	-
A12	97	PB4	A12	-	-	U12.35, JA3.13	-	-
A13_POE4n	96	PB5	A13	R351, R420	R359	U12.20, JA3.14	-	-
			POE4n	R351, R359	R420	JA5.16	-	-
A14	95	PB6	A14	-	-	U12.21, JA3.15	-	-
A15	94	PB7	A15	-	-	JA3.16	-	-
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J10.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J10.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J10.Pin2-3, SW5.1.ON	-	JA3.37, U6.9	R34	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_ MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.8	R35	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTIOC4B	86	PC2	A18_ET0RXDV_ MTIOC4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.80	-	-
			MTIOC4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-

Table 6-9: BUS & SDRAM Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
A19_ET0TXER_QIO0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIO0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, T26	-	-
			BD_QIO0-A	SW5.7.ON, R375	SW5.6.OFF, SW5.8.OFF, R374	JA3.40, U8.5	-	-
			TFT_QIO0-A	SW5.7.ON, R374	SW5.6.OFF, SW5.8.OFF, R375	JA3.40, TFT.31	R234	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIO1-A_POE0n	82	PC4	A20_ET0TXCLK_QIO1-A_POE0n	R345	-	JA3.41	-	-
			ET0TXCLK	R345, SW5.9.ON	SW5.10.OFF	JA3.41, U6.12	R33	-
			BD_QIO1-A	R345, SW5.10.ON, R371	SW5.9.OFF, R370, R372	JA3.41, U8.2	-	-
			TFT_QIO1-A	R345, SW5.10.ON, R370	SW5.9.OFF, R371, R372	JA3.41, TFT.30	R225	-
			POE0n	R345, SW5.10.ON, R372	SW5.9.OFF, R370, R371	JA3.41, JA2.24	-	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J12.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J12.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J12.Pin2-3, SW6.1.ON	-	JA3.42, U6.16	R29	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.17	R28	-
D0	158	PD0	D0	-	-	U12.2, JA3.17, TFT.7	-	-
D1	156	PD1	D1	-	-	U12.4, JA3.18, TFT.8	-	-
D2_SDHID2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U12.5, JA3.19, TFT.9	-	-
			SDHID2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDHID3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U12.7, JA3.20, TFT.10	-	-
			SDHID3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDHICMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U12.8, JA3.21, TFT.11	-	-
			SDHICMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDHICLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U12.10, JA3.22, TFT.12	-	-
			SDHICLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-

Table 6-10: BUS Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D6_SDHID0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U12.11, JA3.23, TFT.13	-	-
			SDHID0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDHID1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U12.13, JA3.24, TFT.14	-	-
			SDHID1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D8_IO0	135	PE0	D8	R442	R405	U12.42, JA3.29, TFT.15	-	-
			IO0	R405	R442	JA1.15	-	-
D9_IO1	134	PE1	D9	R441	R401	U12.44, JA3.30, TFT.16	-	-
			IO1	R401	R441	JA1.16	-	-
D10_IO2	133	PE2	D10	R440	R400	U12.45, JA3.31, TFT.17	-	-
			IO2	R400	R440	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R394	U12.47, JA3.32, TFT.18	-	-
			IO3	R394	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R393	U12.48, JA3.33, TFT.19	-	-
			IO4	R393	R227	JA1.19	-	-
D13_IO5	130	PE5	D13	R228	R390	U12.50, JA3.34, TFT.20	-	-
			IO5	R390	R228	JA1.20	-	-
D14_SDHICD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U12.51, JA3.35, TFT.21	-	-
			SDHICD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDHIWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U12.53, JA3.36, TFT.22	-	-
			SDHIWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-

Table 6-11: BUS Option Links (4)

6.8 CAN Configuration

Table 6-12 below details the function of the option links associated with CAN configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
CTX0_VSYNC_MTIOC0C_IRQ2-DS	29	P32	VSYNC	R269	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R269	U11.1	R211	-
						JA5.5	-	-
			MTIOC0C_IRQ2-DS	J15.Pin2-3	R269	JA2.23	R154	R90, R153
						JA5.10	R90	R154
CRX0_PCKO_MTIOC0D	28	P33	PCKO	R294	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R294	U11.4	R197	-
						JA5.6	-	-
			MTIOC0D	J17.Pin2-3	R294	JA2.21	-	-

Table 6-12: CAN Option Links

6.9 LCD Direct Drive (TFT) Configuration

Table 6-13 to **Table 6-16** below details the function of the option links associated with LCD Direct Drive (TFT) configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
LED2_MTIOC2A	37	P26	LED2	R285	R121	LED2	-	-
			MTIOC2A	R121	R285	JA5.9	R120	R106
						TFT.27	-	-
LED3_MTIOC2B_BACKLIGHT	36	P27	LED3	J24.Pin1-2	-	LED3	-	-
			MTIOC2B	J24.Pin2-3, R177	R235	JA2.19	-	-
			BACKLIGHT	J24.Pin2-3, R235	R177	TFT.35	-	-
ET0LINKSTA_MTIOC0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.19, ETHERNET0.11	-	-
			MTIOC0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R157	R213, R494
						JA2.7	R213	R157
						TFT.25	-	-
AN001_RXCTS_YDRIVE	171	P41	AN001	R207	R237, R419	JA1.10	-	-
			RXCTS	R419	R207, R237	U10.2	-	-
			YDRIVE	R237	R207, R419	TFT.42	-	-
AN004_XINPUT1	168	P44	XINPUT1	R238	R134	TFT.43	-	-
			AN004	R134	R238	JA5.1	-	-

Table 6-13: Direct LCD Drive (TFT) Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
AN005_YINPUT1_P45	167	P45	YINPUT1	R239	R133	TFT.44	-	-
			AN005	R133	R239, R427	JA5.2	-	-
			P45	R427	R133	PMOD1.1	R426	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R240	R130	TFT.45	-	-
			AN006	R130	R240, R315	JA5.3	-	-
			P46	R315	R130	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R241	R132	TFT.46	-	-
			AN007	R132	R241, R313	JA5.4	-	-
			P47	R313	R132	PMOD1.10	-	-
ET0RXCLK_REF50CK0_QSSL-A	85	P76	REF50CK0	J8.Pin1-2, R58	R50	U6.70, X5.3	R62, R63	R26, R64, R68
			ET0RXCLK	J8.Pin1-2, R50	R58	U6.79	R57	-
			BD_QSSL-A	J8.Pin2-3, R386	R392	U8.1	-	-
			TFT_QSSL-A	J8.Pin2-3, R392	R386	TFT.32	-	-
ET0RXER_RMII0RXER_QSPCLK-A	84	P77	ET0RXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.2	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R381	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R381	SW6.9.OFF, R382	TFT.29	R232	-
ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.15	R30	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R455	JA6.1, TFT28	-	-
			MTIOC4A	SW7.8.ON, R455	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.1	-	-
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R456	JA6.2, TFT23	-	-
			MTIOC4C	SW7.10.ON, R456	SW7.9.OFF, R229	JA2.16	-	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.8	R35	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A19_ET0TXER_QIO0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIO0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, T26	-	-
			BD_QIO0-A	SW5.7.ON, R375	SW5.6.OFF, SW5.8.OFF, R374	JA3.40, U8.5	-	-
			TFT_QIO0-A	SW5.7.ON, R374	SW5.6.OFF, SW5.8.OFF, R375	JA3.40, TFT.31	R234	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIO1-A_POE0n	82	PC4	A20_ET0TXCLK_QIO1-A_POE0n	R345	-	JA3.41	-	-
			ET0TXCLK	R345, SW5.9.ON	SW5.10.OFF	JA3.41, U6.12	R33	-
			BD_QIO1-A	R345, SW5.10.ON, R371	SW5.9.OFF, R370, R372	JA3.41, U8.2	-	-
			TFT_QIO1-A	R345, SW5.10.ON, R370	SW5.9.OFF, R371, R372	JA3.41, TFT.30	R225	-
			POE0n	R345, SW5.10.ON, R372	SW5.9.OFF, R370, R371	JA3.41, JA2.24	-	-

Table 6-14: Direct LCD Drive (TFT) Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D0	158	PD0	D0	-	-	U12.2, JA3.17, TFT.7	-	-
D1	156	PD1	D1	-	-	U12.4, JA3.18, TFT.8	-	-
D2_SDHID2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U12.5, JA3.19, TFT.9	-	-
			SDHID2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDHID3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U12.7, JA3.20, TFT.10	-	-
			SDHID3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDHICMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U12.8, JA3.21, TFT.11	-	-
			SDHICMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDHICLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U12.10, JA3.22, TFT.12	-	-
			SDHICLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-
D6_SDHID0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U12.11, JA3.23, TFT.13	-	-
			SDHID0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDHID1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U12.13, JA3.24, TFT.14	-	-
			SDHID1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D8_IO0	135	PE0	D8	R442	R405	U12.42, JA3.29, TFT.15	-	-
			IO0	R405	R442	JA1.15	-	-
D9_IO1	134	PE1	D9	R441	R401	U12.44, JA3.30, TFT.16	-	-
			IO1	R401	R441	JA1.16	-	-
D10_IO2	133	PE2	D10	R440	R400	U12.45, JA3.31, TFT.17	-	-
			IO2	R400	R440	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R394	U12.47, JA3.32, TFT.18	-	-
			IO3	R394	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R393	U12.48, JA3.33, TFT.19	-	-
			IO4	R393	R227	JA1.19	-	-

Table 6-15: Direct LCD Drive (TFT) Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D13_IO5	130	PE5	D13	R228	R390	U12.50, JA3.34, TFT.20	-	-
			IO5	R390	R228	JA1.20	-	-
D14_SDHICD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U12.51, JA3.35, TFT.21	-	-
			SDHICD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDHIWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U12.53, JA3.36, TFT.22	-	-
			SDHIWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
CTS6RTS6_MTIOC3C	13	PJ3	CTS6RTS6	R323	R230	PMOD1.1	R1	R426
			MTIOC3C	R230	R323	JA2.11, TFT.24	-	-
RXRTS_XDRIVE	11	PJ5	RXRTS	R409	R236	U9.2	-	-
			XDRIVE	R236	R409	TFT.41	-	-

Table 6-16: Direct Drive LCD (TFT) Option Links (4)

6.10 Ethernet Configuration

Table 6-17 to **Table 6-21** below details the function of the option links associated with Ethernet configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET0LINKSTA_MTIOC0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.19, ETHERNET0.11	-	-
			MTIOC0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R157	R213, R494
						JA2.7	R213	R157
						TFT.25	-	-
ET0MDIO	102	P71	ET0MDIO	-	-	U6.66	J13.Pin1-2	-
ET0MDC	101	P72	ET0MDC	-	-	U6.67	J9.Pin1-2	-
ET0ERXD1_RMII0RXD1_CS4n	88	P74	ET0ERXD1_RMII0RXD1	SW6.7.ON	SW6.8.OFF	U6.5	R36	-
			CS4n	SW6.8.ON	SW6.7.OFF	JA3.27	-	-
ET0ERXD0_RMII0RXD0	87	P75	ET0ERXD0_RMII0RXD0	-	-	U6.4	R37	-
ET0RXCLK_REF50CK0_QSSL-A	85	P76	REF50CK0	J8.Pin1-2, R58	R50	U6.70, X5.3	R62, R63	R26, R64, R68
			ET0RXCLK	J8.Pin1-2, R50	R58	U6.79	R57	-
			BD_QSSL-A	J8.Pin2-3, R386	R392	U8.1	-	-
			TFT_QSSL-A	J8.Pin2-3, R392	R386	TFT.32	-	-
ET0RXER_RMII0RXER_QSPCLK-A	84	P77	ET0RXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.2	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R381	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R381	SW6.9.OFF, R382	TFT.29	R232	-

Table 6-17: Ethernet Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET0TXEN_RMII0TXDEN_QIO2-A_MTIOC3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.13	R32	-
			QIO2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTIOC3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIO3-A_MTIOC3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.14	R31	-
			QIO3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTIOC3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-
ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.15	R30	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R455	JA6.1, TFT28	-	-
			MTIOC4A	SW7.8.ON, R455	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.1	-	-
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R456	JA6.2, TFT23	-	-
			MTIOC4C	SW7.10.ON, R456	SW7.9.OFF, R229	JA2.16	-	-
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J10.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J10.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J10.Pin2-3, SW5.1.ON	-	JA3.37, U6.9	R34	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.8	R35	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTIOC4B	86	PC2	A18_ET0RXDV_MTIOC4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.80	-	-
			MTIOC4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-
A19_ET0TXER_QIO0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIO0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, T26	-	-
			BD_QIO0-A	SW5.7.ON, R375	SW5.6.OFF, SW5.8.OFF, R374	JA3.40, U8.5	-	-
			TFT_QIO0-A	SW5.7.ON, R374	SW5.6.OFF, SW5.8.OFF, R375	JA3.40, TFT.31	R234	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-

Table 6-18: Ethernet Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
A20_ET0TXCLK_QIO1-A_POE0n	82	PC4	A20_ET0TXCLK_QIO1-A_POE0n	R345	-	JA3.41	-	-
			ET0TXCLK	R345, SW5.9.ON	SW5.10.OFF	JA3.41, U6.12	R33	-
			BD_QIO1-A	R345, SW5.10.ON, R371	SW5.9.OFF, R370, R372	JA3.41, U8.2	-	-
			TFT_QIO1-A	R345, SW5.10.ON, R370	SW5.9.OFF, R371, R372	JA3.41, TFT.30	R225	-
			POE0n	R345, SW5.10.ON, R372	SW5.9.OFF, R370, R371	JA3.41, JA2.24	-	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J12.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J12.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J12.Pin2-3, SW6.1.ON	-	JA3.42, U6.16	R29	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.17	R28	-
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J11.Pin1-2	-	U7.2	-	-
			ET0COL	J11.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.3	-	-
			PC7	J11.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2	-	-
						E1.10	R245	-

Table 6-19: Ethernet Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Connection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET1MDIO	33	P30	ET1MDIO	-	-	U6.66	J13.Pin2-3	-
ET1MDC	32	P31	ET1MDC	-	-	U6.67	J9.Pin2-3	-
ET1TXEN_RMII1TXDEN_CS0n	141	P60	ET1TXEN_RMII1TXDEN	R111	R397	U6.49	R95	-
			CS0n	R397	R111	JA3.45	R467	R468
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.62	-	-
			A-TXD7	J16.Pin2-3, R152	R411	U9.3	R150	R135, R141, R149
						JA2.6	-	-
			P-TXD7	J16.Pin2-3, R411	R152	PMOD2.2	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.59	-	-
			A-SCK7	J20.Pin2-3, R198	R417	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R417	R198	PMOD2.4	-	-

Table 6-20: Ethernet Option Links (4)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET1CRS_RMII1CRSDV_A-RXD7_P-RXD7	160	P92	ET1CRS_RMII1CRSDV	J18.Pin1-2	-	U6.61	-	-
			A-RXD7	J18.Pin2-3, R172	R415	U10.3	R171	R158, R159, R164
						JA2.8	-	-
			P-RXD7	J18.Pin2-3, R415	R172	PMOD2.3	-	-
ET1LINKSTA_A-CTS7RTS7_P-CTS7RTS7	159	P93	ET1LINKSTA	R407	R191, R408	U6.43, ETHERNET1.11	-	-
			A-CTS7RTS7	R191	R407, R408	JA2.12	-	-
			P-CTS7RTS7	R408	R191, R407	PMOD2.1	-	-
ET1ERXD0_RMII1RXD0	157	P94	ET1ERXD0_RMII1RXD0	-	-	U6.58	R100	-
ET1ERXD1_RMII1RXD1	155	P95	ET1ERXD1_RMII1RXD1	-	-	U6.57	R99	-
ET1ERXD2_P96	152	P96	ET1ERXD2	R388	R175	U6.56	R98	-
			P96	R175	R388	PMOD2.9	-	-
ET1ERXD3_P97	149	P97	ET1ERXD3	R389	R167	U6.53	R97	-
			P97	R167	R389	PMOD2.10	-	-
ET1RXCLK_REF50CK1	146	PG0	ET1RXCLK	R396	R144	U6.63	R74	-
			REF50CK1	R144	R396	U6.70, X5.3	R61, R63	R26, R64, R68
ET1RXER_RMII1RXER	144	PG1	ET1RXER_RMII1RXER	-	-	U6.60	-	-
ET1TXCLK	123	PG2	ET1TXCLK	-	-	U6.50	R96	-
ET1ETXD0_RMII1TXD0	121	PG3	ET1ETXD0_RMII1TXD0	-	-	U6.48	R94	-
ET1ETXD1_RMII1TXD1	119	PG4	ET1ETXD1_RMII1TXD1	-	-	U6.47	R93	-
ET1ETXD2	116	PG5	ET1ETXD2	-	-	U6.46	R92	-
ET1ETXD3	113	PG6	ET1ETXD3	-	-	U6.45	R91	-
ET1TXER	111	PG7	ET1TXER	-	-	T22	-	-

Table 6-21: Ethernet Option Links (5)

6.11 General IO & LED Configuration

Table 6-22 and Table 6-23 below details the function of the option links associated with General IO & LED configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D8_IO0	135	PE0	D8	R442	R405	U12.42, JA3.29, TFT.15	-	-
			IO0	R405	R442	JA1.15	-	-
D9_IO1	134	PE1	D9	R441	R401	U12.44, JA3.30, TFT.16	-	-
			IO1	R401	R441	JA1.16	-	-
D10_IO2	133	PE2	D10	R440	R400	U12.45, JA3.31, TFT.17	-	-
			IO2	R400	R440	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R394	U12.47, JA3.32, TFT.18	-	-
			IO3	R394	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R393	U12.48, JA3.33, TFT.19	-	-
			IO4	R393	R227	JA1.19	-	-
D13_IO5	130	PE5	D13	R228	R390	U12.50, JA3.34, TFT.20	-	-
			IO5	R390	R228	JA1.20	-	-

Table 6-22: General IO & LED Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D14_SDHICD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U12.51, JA3.35, TFT.21	-	-
			SDHICD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDHIWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U12.53, JA3.36, TFT.22	-	-
			SDHIWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
LED0_DA0	4	P03	LED0	R281	R195	LED0	-	-
			DA0	R195	R281	JA1.13	-	-
LED1_DA1	2	P05	LED1	R284	R194	LED1	-	-
			DA1	R194	R284	JA1.14	-	-
LED2_MTIOC2A	37	P26	LED2	R285	R121	LED2	-	-
			MTIOC2A	R121	R285	JA5.9	R120	R106
						TFT.27	-	-
LED3_MTIOC2B_BACKLIGHT	36	P27	LED3	J24.Pin1-2	-	LED3	-	-
			MTIOC2B	J24.Pin2-3, R177	R235	JA2.19	-	-
			BACKLIGHT	J24.Pin2-3, R235	R177	TFT.35	-	-

Table 6-23: General IO & LED Option Links (2)

6.12 I2C & EEPROM Configuration

Table 6-24 and **Table 6-25** below detail the function of the option links associated with I2C & EEPROM configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
TXD6_SSDA6	8	P00	TXD6	R119	-	PMOD1.2	-	-
			SSDA6	R118	-	J26.19	R307	-
RXD6_SSCL6	7	P01	RXD6	R128	-	PMOD1.3	-	-
			SSCL6	R127	-	J26.20	R306	-
USB0VBUS_USB0VBUSEN_SCL2-DS	48	P16	SCL2-DS	J21.Pin1-2	J3.Open	U13.6	R206	-
						JA1.26	R161	R156
			USB0VBUS	J3.Pin1-2	J21.Open	USB0 Function Bus-Powered	R60	R56
						USB0 Function Self-Powered	R56	R60
			USB0VBUSEN	J3.Pin2-3	J21.Open	U5.1	-	-
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R292	R192, R275	J25.12	-	-
			PIXD3	R275	R192, R292	J26.15	-	-
			SDA2-DS	R192	R275, R292	U13.5	R201	-
						JA1.25	R155	R145
WRn_WR0n_TXD2_SSDA2	72	P50	WRn	R116	R104, R124, R125	JA3.26	R387	R431
			WR0n	R124	R104, R116, R125	JA3.48	R464	R429
			TXD2	R104	R116, R124, R125	U9.3	R135	R141, R149, R150
						JA6.9	-	-
			SSDA2	R125	R104, R116, R124	JA1.25	R145	R155
RDn_RXD2_SSCL2	70	P52	RDn	R86	R84, R85	JA3.25	-	-
			RXD2	R85	R84, R86	U10.3	R159	R158, R164, R171
						JA6.12	-	-
			SSCL2	R84	R85, R86	JA1.26	R156	R161

Table 6-24: I2C & EEPROM Option Links (1)

Reference	MCU Peripheral Selection			Destination Selection
	Function	Fit	DNF	Interface Function
SSDA2, SSCL2	Connects pull-up resistor to Board_3V3.	R404	R414	SSDA2, SSCL2
	Connects pull-up resistor to Board_5V.	R414	R404	SSDA2, SSCL2
SSDA6, SSCL6	Connects pull-up resistor to Board_3V3.	R265	R262	SSDA6, SSCL6
	Connects pull-up resistor to Board_5V.	R262	R265	SSDA6, SSCL6
SDA2-DS, SCL2-DS	Connects pull-up resistor and EEPROM power pin to Board_3V3.	R220	R219	SDA2-DS, SCL2-DS, U13
	Connects pull-up resistor and EEPROM power pin to Board_5V.	R219	R220	SDA2-DS, SCL2-DS, U13

Table 6-25: I2C & EEPROM Option Links (2)

6.13 MTU & TPU & POE Configuration

Table 6-26 to **Table 6-29** below details the function of the option links associated with MTU & TPU & POE configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R362	R76, R480	U3.2	R4	R45
						U4.5	R45	R4
			ALE	R480	R76, R362	JA3.46	R466	R447
			MTIC5W	R76	R362, R480	JA5.14	R357	R75
						JA6.16	R75	R357
USBAVBUS_USBAVBUSEN_MTIC5V	67	P11	MTIC5V	R55	J7.Open	JA5.13	R78	R70
						JA6.15	R70	R78
			USBAVBUS	J7.Pin1-2	R55	J6.1	J6.Pin1-2	-
						J6.3	J6.Pin2-3	-
			USBAVBUSEN	J7.Pin2-3	R55	U3.1	R5	R46
						U4.4	R46	R5
MTIC5U_IRQ2	53	P12	MTIC5U	R83	R367	JA5.12	R79	R82
						JA6.14	R82	R79
			IRQ2	R367	R83	SW2	R493	-
MTIOC0B_IRQ3	52	P13	MTIOC0B_IRQ3	-	-	JA2.9	R204	R106
						JA5.9	R106	R120, R204
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154

Table 6-26: MTU & TPU & POE Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
USBAOVRCURB_AUDIOMCLK_PIXD6_MTCLKC	43	P22	AUDIOMCLK	R289	R72, R270, R327	J25.5	-	-
			USBAOVRCURB	R327	R72, R270, R289	U4.6	-	-
			PIXD6	R270	R72, R289, R327	J26.12	-	-
			MTCLKC	R72	R270, R289, R327	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R291	R271, R342	J25.9	-	-
			PIXD7	R271	R291, R342	J26.11	-	-
			MTCLKD	R342	R271, R291	JA5.18	-	-
PIXCLK_MTCLKA	40	P24	PIXCLK	R267	R142	J26.8	-	-
			MTCLKA	R142	R267	JA2.25	-	-
HSYNC_MTCLKB	38	P25	HSYNC	R268	R136	J26.10	-	-
			MTCLKB	R136	R268	JA2.26	-	-
LED2_MTIOC2A	37	P26	LED2	R285	R121	LED2	-	-
			MTIOC2A	R121	R285	JA5.9	R120	R106
						TFT.27	-	-
LED3_MTIOC2B_BACKLIGHT	36	P27	LED3	J24.Pin1-2	-	LED3	-	-
			MTIOC2B	J24.Pin2-3, R177	R235	JA2.19	-	-
			BACKLIGHT	J24.Pin2-3, R235	R177	TFT.35	-	-
CTX0_VSYNC_MTIOC0C_IRQ2-DS	29	P32	VSYNC	R269	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R269	U11.1	R211	-
						JA5.5	-	-
			MTIOC0C_IRQ2-DS	J15.Pin2-3	R269	JA2.23	R154	R90, R153
						JA5.10	R90	R154
CRX0_PCKO_MTIOC0D	28	P33	PCKO	R294	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R294	U11.4	R197	-
						JA5.6	-	-
			MTIOC0D	J17.Pin2-3	R294	JA2.21	-	-
ET0LINKSTA_MTIOC0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.19, ETHERNET0.11	-	-
			MTIOC0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R157	R213, R494
						JA2.7	R213	R157
						TFT.25	-	-
DQM0_MTIOC7D	122	P66	DQM0	R430	R59	U12.15	-	-
						JA3.48	R429	R464
			MTIOC7D	R59	R430	JA5.24	-	-
DQM1_MTIOC7C	120	P67	DQM1	R443	R67	U12.39	-	-
						JA3.47	R444	R465
			MTIOC7C	R67	R443	JA5.22	-	-
ET0TXEN_RMII0TXDEN_QIO2-A_MTIOC3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.13	R32	-
			QIO2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTIOC3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIO3-A_MTIOC3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.14	R31	-
			QIO3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTIOC3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-

Table 6-27: MTU & TPU & POE Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.15	R30	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R455	JA6.1, TFT28	-	-
			MTIOC4A	SW7.8.ON, R455	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.1	-	-
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R456	JA6.2, TFT23	-	-
			MTIOC4C	SW7.10.ON, R456	SW7.9.OFF, R229	JA2.16	-	-
PIXD1_TIOCA0	49	P86	PIXD1	R277	R168	J26.17	-	-
			TIOCA0	R168	R277	JA2.22	-	-
PIXD2_TIOCA2	47	P87	PIXD2	R274	R169	J26.16	-	-
			TIOCA2	R169	R274	JA2.20	-	-
A0_MTIOC6D	118	PA0	A0	R247	R340	JA3.1	-	-
			MTIOC6D	R340	R247	JA5.20	-	-
A1_MTIOC7B	114	PA1	A1	R421	R377	U12.23, JA3.2	-	-
			MTIOC7B	R377	R421	JA5.23	-	-
A2_MTIOC7A	112	PA2	A2	R422	R369	U12.24, JA3.3	-	-
			MTIOC7A	R369	R422	JA5.21	-	-
A5_MTIOC6B	108	PA5	A5	R450	R368	U12.29, JA3.6	-	-
			MTIOC6B	R368	R450	JA5.19	-	-
A13_POE4n	96	PB5	A13	R351, R420	R359	U12.20, JA3.14	-	-
			POE4n	R351, R359	R420	JA5.16	-	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.8	R35	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTIOC4B	86	PC2	A18_ET0RXDV_MTIOC4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.80	-	-
			MTIOC4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-
A19_ET0TXER_QIO0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIO0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, T26	-	-
			BD_QIO0-A	SW5.7.ON, R375	SW5.6.OFF, SW5.8.OFF, R374	JA3.40, U8.5	-	-
			TFT_QIO0-A	SW5.7.ON, R374	SW5.6.OFF, SW5.8.OFF, R375	JA3.40, TFT.31	R234	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-

Table 6-28: MTU & TPU & POE Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
A20_ET0TXCLK_QIO1-A_POE0n	82	PC4	A20_ET0TXCLK_QIO1-A_POE0n	R345	-	JA3.41	-	-
			ET0TXCLK	R345, SW5.9.ON	SW5.10.OFF	JA3.41, U6.12	R33	-
			BD_QIO1-A	R345, SW5.10.ON, R371	SW5.9.OFF, R370, R372	JA3.41, U8.2	-	-
			TFT_QIO1-A	R345, SW5.10.ON, R370	SW5.9.OFF, R371, R372	JA3.41, TFT.30	R225	-
			POE0n	R345, SW5.10.ON, R372	SW5.9.OFF, R370, R371	JA3.41, JA2.24	-	-
D14_SDHICD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U12.51, JA3.35, TFT.21	-	-
			SDHICD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDHIWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U12.53, JA3.36, TFT.22	-	-
			SDHIWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
CTS6RTS6_MTIOC3C	13	PJ3	CTS6RTS6	R323	R230	PMOD1.1	R1	R426
			MTIOC3C	R230	R323	JA2.11, TFT.24	-	-

Table 6-29: MTU & TPU & POE Option Links (4)

6.14 IRQ & NMI & Switch Configuration

Table 6-30 below details the function of the option links associated with IRQ & NMI & Switch configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ADTRG0n	176	P07	ADTRG0n	-	-	SW3	R492	-
						JA1.8	-	-
MTIC5U_IRQ2	53	P12	MTIC5U	R83	R367	JA5.12	R79	R82
						JA6.14	R82	R79
			IRQ2	R367	R83	SW2	R493	-
MTIOC0B_IRQ3	52	P13	MTIOC0B_IRQ3	-	-	JA2.9	R204	R106
						JA5.9	R106	R120, R204
PIXD0_IRQ5	50	P15	IRQ5	R488	R276	SW1	R495	-
						JA1.23	R494	R157
			PIXD0	R276	R488	J26.18	-	-
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R334	R273, R293, R333	PMOD1.8	-	-
			USBAEXICEN	R333	R273, R293, R334	U4.11	-	-
			SSIWS0	R293	R273, R333, R334	J25.11	-	-
			PIXD5	R273	R293, R333, R334	J26.13	-	-
CTX0_VSYNC_MTIOC0C_IRQ2-DS	29	P32	VSYNC	R269	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R269	U11.1	R211	-
						JA5.5	-	-
			MTIOC0C_IRQ2-DS	J15.Pin2-3	R269	JA2.23	R154	R90, R153
						JA5.10	R90	R154
ET0LINKSTA_MTIOC0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.19, ETHERNET0.11	-	-
			MTIOC0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R157	R213, R494
						JA2.7	R213	R157
						TFT.25	-	-
NMI	26	P35	NMI	-	-	JA2.3	-	-
						SW4.3	-	-
AN002_IRQ10-DS	170	P42	AN002	R203	R179	JA1.11	-	-
			IRQ10-DS	R179	R203	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R202	R176	JA1.12	-	-
			IRQ11-DS	R176	R202	PMOD2.8	-	-

Table 6-30: IRQ & Switch Option Links

6.15 PDC Configuration

Table 6-31 and **Table 6-32** below details the function of the option links associated with PDC configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
TXD6_SSDA6	8	P00	TXD6	R119	-	PMOD1.2	-	-
			SSDA6	R118	-	J26.19	R307	-
RXD6_SSCL6	7	P01	RXD6	R128	-	PMOD1.3	-	-
			SSCL6	R127	-	J26.20	R306	-
PIXD0_IRQ5	50	P15	IRQ5	R488	R276	SW1	R495	-
						JA1.23	R494	R157
			PIXD0	R276	R488	J26.18	-	-
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R292	R192, R275	J25.12	-	-
			PIXD3	R275	R192, R292	J26.15	-	-
			SDA2-DS	R192	R275, R292	U13.5	R201	-
						JA1.25	R155	R145
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R334	R273, R293, R333	PMOD1.8	-	-
			USBAEXICEN	R333	R273, R293, R334	U4.11	-	-
			SSIWS0	R293	R273, R333, R334	J25.11	-	-
			PIXD5	R273	R293, R333, R334	J26.13	-	-
USBAOVRCURB_AUDIOMCLK_PIXD6_MTCLKC	43	P22	AUDIOMCLK	R289	R72, R270, R327	J25.5	-	-
			USBAOVRCURB	R327	R72, R270, R289	U4.6	-	-
			PIXD6	R270	R72, R289, R327	J26.12	-	-
			MTCLKC	R72	R270, R289, R327	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R291	R271, R342	J25.9	-	-
			PIXD7	R271	R291, R342	J26.11	-	-
			MTCLKD	R342	R271, R291	JA5.18	-	-
PIXCLK_MTCLKA	40	P24	PIXCLK	R267	R142	J26.8	-	-
			MTCLKA	R142	R267	JA2.25	-	-
HSYNC_MTCLKB	38	P25	HSYNC	R268	R136	J26.10	-	-
			MTCLKB	R136	R268	JA2.26	-	-
CTX0_VSYNC_MTIOC0C_IRQ2-DS	29	P32	VSYNC	R269	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R269	U11.1	R211	-
						JA5.5	-	-
			MTIOC0C_IRQ2-DS	J15.Pin2-3	R269	JA2.23	R154	R90, R153
						JA5.10	R90	R154
CRX0_PCKO_MTIOC0D	28	P33	PCKO	R294	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R294	U11.4	R197	-
						JA5.6	-	-
			MTIOC0D	J17.Pin2-3	R294	JA2.21	-	-
PIXD1_TIOCA0	49	P86	PIXD1	R277	R168	J26.17	-	-
			TIOCA0	R168	R277	JA2.22	-	-
PIXD2_TIOCA2	47	P87	PIXD2	R274	R169	J26.16	-	-
			TIOCA2	R169	R274	JA2.20	-	-

Table 6-31: PDC Interface Option Links (1)

Reference	MCU Peripheral Selection			Destination Selection
	Function	Fit	DNF	Interface / Function
SSDA6, SSCL6	Connects pull-up resistor to Board_3V3.	R265	R262	SSDA6, SSCL6
	Connects pull-up resistor to Board_5V.	R262	R265	SSDA6, SSCL6

Table 6-32: PDC Interface Option Links (2)

6.16 PMOD1 Configuration

Table 6-33 below details the function of the option links associated with PMOD1 Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
TXD6_SSDA6	8	P00	TXD6	R119	-	PMOD1.2	-	-
			SSDA6	R118	-	J26.19	R307	-
RXD6_SSCL6	7	P01	RXD6	R128	-	PMOD1.3	-	-
			SSCL6	R127	-	J26.20	R306	-
SCK6	6	P02	SCK6	-	-	PMOD1.4	-	-
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R334	R273, R293, R333	PMOD1.8	-	-
			USBAEXICEN	R333	R273, R293, R334	U4.11	-	-
			SSIWS0	R293	R273, R333, R334	J25.11	-	-
			PIXD5	R273	R293, R333, R334	J26.13	-	-
AN005_YINPUT1_P45	167	P45	YINPUT1	R239	R133	TFT.44	-	-
			AN005	R133	R239, R427	JA5.2	-	-
			P45	R427	R133	PMOD1.1	R426	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R240	R130	TFT.45	-	-
			AN006	R130	R240, R315	JA5.3	-	-
			P46	R315	R130	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R241	R132	TFT.46	-	-
			AN007	R132	R241, R313	JA5.4	-	-
			P47	R313	R132	PMOD1.10	-	-
CTS6RTS6_MTIOC3C	13	PJ3	CTS6RTS6	R323	R230	PMOD1.1	R1	R426
			MTIOC3C	R230	R323	JA2.11, TFT.24	-	-

Table 6-33: PMOD1 Interface Option Links

6.17 PMOD2 Configuration

Table 6-34 below details the function of the option links associated with PMOD2 Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
AN002_IRQ10-DS	170	P42	AN002	R203	R179	JA1.11	-	-
			IRQ10-DS	R179	R203	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R202	R176	JA1.12	-	-
			IRQ11-DS	R176	R202	PMOD2.8	-	-
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.62	-	-
			A-TXD7	J16.Pin2-3, R152	R411	U9.3	R150	R135, R141, R149
						JA2.6	-	-
			P-TXD7	J16.Pin2-3, R411	R152	PMOD2.2	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.59	-	-
			A-SCK7	J20.Pin2-3, R198	R417	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R417	R198	PMOD2.4	-	-
ET1CRS_RMII1CRSDV_A-RXD7_P-RXD7	160	P92	ET1CRS_RMII1CRSDV	J18.Pin1-2	-	U6.61	-	-
			A-RXD7	J18.Pin2-3, R172	R415	U10.3	R171	R158, R159, R164
						JA2.8	-	-
			P-RXD7	J18.Pin2-3, R415	R172	PMOD2.3	-	-
ET1LINKSTA_A-CTS7RTS7_P-CTS7RTS7	159	P93	ET1LINKSTA	R407	R191, R408	U6.43, ETHERNET1.11	-	-
			A-CTS7RTS7	R191	R407, R408	JA2.12	-	-
			P-CTS7RTS7	R408	R191, R407	PMOD2.1	-	-
ET1ERXD2_P96	152	P96	ET1ERXD2	R388	R175	U6.56	R98	-
			P96	R175	R388	PMOD2.9	-	-
ET1ERXD3_P97	149	P97	ET1ERXD3	R389	R167	U6.53	R97	-
			P97	R167	R389	PMOD2.10	-	-

Table 6-34: PMOD2 Interface Option Links

6.18 QSPI Configuration

Table 6-35 below details the function of the option links associated with QSPI configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
ET0RXCLK_REF50CK0_QSSL-A	85	P76	REF50CK0	J8.Pin1-2, R58	R50	U6.70, X5.3	R62, R63	R26, R64, R68
			ET0RXCLK	J8.Pin1-2, R50	R58	U6.79	R57	-
			BD_QSSL-A	J8.Pin2-3, R386	R392	U8.1	-	-
			TFT_QSSL-A	J8.Pin2-3, R392	R386	TFT.32	-	-
ET0RXER_RMII0RXER_QSPCLK-A	84	P77	ET0RXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.2	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R381	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R381	SW6.9.OFF, R382	TFT.29	R232	-
ET0TXEN_RMII0TXDEN_QIO2-A_MTIOC3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.13	R32	-
			QIO2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTIOC3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIO3-A_MTIOC3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.14	R31	-
			QIO3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTIOC3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-
A19_ET0TXER_QIO0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIO0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, T26	-	-
			BD_QIO0-A	SW5.7.ON, R375	SW5.6.OFF, SW5.8.OFF, R374	JA3.40, U8.5	-	-
			TFT_QIO0-A	SW5.7.ON, R374	SW5.6.OFF, SW5.8.OFF, R375	JA3.40, TFT.31	R234	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIO1-A_POE0n	82	PC4	A20_ET0TXCLK_QIO1-A_POE0n	R345	-	JA3.41	-	-
			ET0TXCLK	R345, SW5.9.ON	SW5.10.OFF	JA3.41, U6.12	R33	-
			BD_QIO1-A	R345, SW5.10.ON, R371	SW5.9.OFF, R370, R372	JA3.41, U8.2	-	-
			TFT_QIO1-A	R345, SW5.10.ON, R370	SW5.9.OFF, R371, R372	JA3.41, TFT.30	R225	-
			POE0n	R345, SW5.10.ON, R372	SW5.9.OFF, R370, R371	JA3.41, JA2.24	-	-

Table 6-35: QSPI Option Links

6.19 RSPI Configuration

Table 6-36 below details the function of the option links associated with RSPI configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J10.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J10.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J10.Pin2-3, SW5.1.ON	-	JA3.37, U6.9	R34	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J12.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J12.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J12.Pin2-3, SW6.1.ON	-	JA3.42, U6.16	R29	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.17	R28	-
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J11.Pin1-2	-	U7.2	-	-
			ET0COL	J11.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.3	-	-
			PC7	J11.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2	-	-
						E1.10	R245	-

Table 6-36: RSPI Option Links

6.20 SDHI Configuration

Table 6-37 below details the function of the option links associated with SD Host Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
D2_SDHID2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U12.5, JA3.19, TFT.9	-	-
			SDHID2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDHID3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U12.7, JA3.20, TFT.10	-	-
			SDHID3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDHICMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U12.8, JA3.21, TFT.11	-	-
			SDHICMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDHICLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U12.10, JA3.22, TFT.12	-	-
			SDHICLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-
D6_SDHID0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U12.11, JA3.23, TFT.13	-	-
			SDHID0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDHID1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U12.13, JA3.24, TFT.14	-	-
			SDHID1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D14_SDHICD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U12.51, JA3.35, TFT.21	-	-
			SDHICD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDHIWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U12.53, JA3.36, TFT.22	-	-
			SDHIWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-

Table 6-37: SD Host Interface Option Links

6.21 Serial & USB to Serial Configuration

Table 6-38 below details the function of the option links associated with Serial & USB to Serial configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
AN001_RXCTS_YDRIVE	171	P41	AN001	R207	R237, R419	JA1.10	-	-
			RXCTS	R419	R207, R237	U10.2	-	-
			YDRIVE	R237	R207, R419	TFT.42	-	-
WRn_WR0n_TXD2_SSDA2	72	P50	WRn	R116	R104, R124, R125	JA3.26	R387	R431
			WR0n	R124	R104, R116, R125	JA3.48	R464	R429
			TXD2	R104	R116, R124, R125	U9.3	R135	R141, R149, R150
						JA6.9	-	-
			SSDA2	R125	R104, R116, R124	JA1.25	R145	R155
WR1n_WAITn_SCK2	71	P51	WAITn	R483	R478, R484	JA3.45	R468	R467
			WR1n	R478	R483, R484	JA3.47	R465	R444
			SCK2	R484	R483, R478	JA6.11	-	-
RDn_RXD2_SSCL2	70	P52	RDn	R86	R84, R85	JA3.25	-	-
			RXD2	R85	R84, R86	U10.3	R159	R158, R164, R171
						JA6.12	-	-
			SSCL2	R84	R85, R86	JA1.26	R156	R161
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.62	-	-
			A-TXD7	J16.Pin2-3, R152	R411	U9.3	R150	R135, R141, R149
						JA2.6	-	-
			P-TXD7	J16.Pin2-3, R411	R152	PMOD2.2	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.59	-	-
			A-SCK7	J20.Pin2-3, R198	R417	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R417	R198	PMOD2.4	-	-
ET1CRS_RMII1CRSDV_A-RXD7_P-RXD7	160	P92	ET1CRS_RMII1 CRSDV	J18.Pin1-2	-	U6.61	-	-
			A-RXD7	J18.Pin2-3, R172	R415	U10.3	R171	R158, R159, R164
						JA2.8	-	-
			P-RXD7	J18.Pin2-3, R415	R172	PMOD2.3	-	-
ET1LINKSTA_A-CTS7RTS7_P-CTS7RTS7	159	P93	ET1LINKSTA	R407	R191, R408	U6.43, ETHERNET1.11	-	-
			A-CTS7RTS7	R191	R407, R408	JA2.12	-	-
			P-CTS7RTS7	R408	R191, R407	PMOD2.1	-	-
TDO_TXD1	35	PF0	TDO	R253	R151	E1.5	-	-
			TXD1	R151	R253	U9.3	R149	R135, R141, R150
						JA6.8	R129	-
TCK_SCK1	34	PF1	TCK	R261	R378	E1.1	-	-
			SCK1	R378	R261	JA6.10	R103	-
TDI_RXD1	31	PF2	TDI	R243	R165	E1.11	-	-
			RXD1	R165	R243	U10.3	R164	R158, R159, R171
						JA6.7	R126	-
RXRTS_XDRIVE	11	PJ5	RXRTS	R409	R236	U9.2	-	-
			XDRIVE	R236	R409	TFT.41	-	-
RS232TX	-	-	RS232TX	-	-	U9.3	R141	R135, R149, R150
RS232RX	-	-	RS232RX	-	-	U10.3	R158	R159, R164, R171

Table 6-38: Serial & USB to Serial Option Links

6.22 SSI Configuration

Table 6-39 below details the function of the option links associated with Serial Sound Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R292	R192, R275	J25.12	-	-
			PIXD3	R275	R192, R292	J26.15	-	-
			SDA2-DS	R192	R275, R292	U13.5	R201	-
						JA1.25	R155	R145
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R334	R273, R293, R333	PMOD1.8	-	-
			USBAEXICEN	R333	R273, R293, R334	U4.11	-	-
			SSIWS0	R293	R273, R333, R334	J25.11	-	-
			PIXD5	R273	R293, R333, R334	J26.13	-	-
USBAOVRCURB_AUDIOMCLK_PIXD6_MTCLKC	43	P22	AUDIOMCLK	R289	R72, R270, R327	J25.5	-	-
			USBAOVRCURB	R327	R72, R270, R289	U4.6	-	-
			PIXD6	R270	R72, R289, R327	J26.12	-	-
			MTCLKC	R72	R270, R289, R327	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R291	R271, R342	J25.9	-	-
			PIXD7	R271	R291, R342	J26.11	-	-
			MTCLKD	R342	R271, R291	JA5.18	-	-

Table 6-39: Serial Sound Interface Option Links

6.23 USB Configuration

Table 6-40 and **Table 6-41** below details the function of the option links associated with the USB Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface Function	Fit	DNF
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R362	R76, R480	U3.2	R4	R45
						U4.5	R45	R4
			ALE	R480	R76, R362	JA3.46	R466	R447
			MTIC5W	R76	R362, R480	JA5.14	R357	R75
						JA6.16	R75	R357
USBAVBUS_USBAVBUSEN_MTIC5V	67	P11	MTIC5V	R55	J7.Open	JA5.13	R78	R70
						JA6.15	R70	R78
			USBAVBUS	J7.Pin1-2	R55	J6.1	J6.Pin1-2	-
						J6.3	J6.Pin2-3	-
			USBAVBUSEN	J7.Pin2-3	R55	U3.1	R5	R46
						U4.4	R46	R5
USB0OVRCURA	51	P14	USB0OVRCURA	-	-	U5.2	-	-
USB0VBUS_USB0VBUSEN_SCL2-DS	48	P16	SCL2-DS	J21.Pin1-2	J3.Open	U13.6	R206	-
						JA1.26	R161	R156
			USB0VBUS	J3.Pin1-2	J21.Open	USB0 Function Bus-Powered	R60	R56
						USB0 Function Self-Powered	R56	R60
			USB0VBUSEN	J3.Pin2-3	J21.Open	U5.1	-	-
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R322	R51, R143, R272, R290	PMOD1.7	-	-
			USBAID	R51	R143, R272, R290, R322	U4.3	-	-
			SSIRXD0	R290	R51, R143, R272, R322	J25.10	-	-
			PIXD4	R272	R51, R143, R290, R322	J26.14	-	-
			MTIOC1A	R143	R51, R272, R290, R322	JA2.23	R153	R154
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R334	R273, R293, R333	PMOD1.8	-	-
			USBAEXICEN	R333	R273, R293, R334	U4.11	-	-
			SSIWS0	R293	R273, R333, R334	J25.11	-	-
			PIXD5	R273	R293, R333, R334	J26.13	-	-
USBAOVRCURB_AUDIOMCLK_PIXD6_MTCLKC	43	P22	AUDIOMCLK	R289	R72, R270, R327	J25.5	-	-
			USBAOVRCURB	R327	R72, R270, R289	U4.6	-	-
			PIXD6	R270	R72, R289, R327	J26.12	-	-
			MTCLKC	R72	R270, R289, R327	JA5.17	-	-

Table 6-40: USB Option Links (1)

Reference	MCU Peripheral Selection			Destination Selection
	Function	Fit	DNF	Interface Function
USB0VBUS	Enables Self-powered.	R56	R60	J1
	Enables Bus-powered.	R60	R56	J1
ILIM	Sets current limit as 0.7A.	R3	R21	U3.4
	Sets current limit as 1.95A.	R21	R3	U3.4
VBUSA	Enables USBA OTG mode.	R52	J4.Open	U4.1
VBUS0, VBUSA	Connects VBUSA to J23.3	R221	R222	J23.3
	Connects VBUS0 to J23.3	R222	R221	J23.3

Table 6-41: USB Option Links (2)

Table 6-42 below details the function of the option links associated with the USB Configuration.

Reference	Jumper Position	Explanation	Related Ref.
J1	Shorted Pin1-2	Enables USB0 Host mode.	-
	Shorted Pin2-3	Enables USB0 Function mode.	R56, R60
	All open	DO NOT SET	-
J2	Shorted Pin1-2	Connects USBA VBUS to EXT_CHG.	-
	Shorted Pin2-3	Connects USBA VBUS to EXT_VBUS.	-
	All open	Disconnects USBA VBUS from EXT_CHG and EXT_VBUS.	-
J4	Shorted Pin1-2	Enables USBA Host mode.	-
	Shorted Pin2-3	Enables USBA Function mode.	J6
	All open	Enables USBA OTG mode.	R52
J6	Shorted Pin1-2	Enables Bus-powered.	J4
	Shorted Pin2-3	Enables Self-powered.	J4
	All open	DO NOT SET	-
J23	Shorted Pin1-2	Enables external battery input.	-
	Shorted Pin2-3	Enables VBUS input.	R221, R222
	All open	Disables external battery input and VBUS input.	-

Table 6-42: USB Option Settings

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Application Header JA1					
Pin	**Function** **Circuit Net Name**	**MCU Pin**	**Pin**	**Function** **Circuit Net Name**	**MCU Pin**
1	5V CON_5V	-	2	0V GROUND	-
3	3V3 CON_3V3	-	4	0V GROUND	-
5	AVCC CON_AVCC0	175	6	AVSS CON_AVSS0	1
7	AVREF CON_VREFH0	174	8	ADTRG ADTRG0n	176
9	ADC0 AN000	173	10	ADC1 AN001	171
11	ADC2 AN002	170	12	ADC3 AN003	169
13	DAC0 DA0	4	14	DAC1 DA1	2
15	IO_0 IO0	135	16	IO_1 IO1	134
17	IO_2 IO2	133	18	IO_3 IO3	132
19	IO_4 IO4	131	20	IO_5 IO5	130
21	IO_6 IO6	126	22	IO_7 IO7	125
23	IRQ3 / IRQAEC / M2_HSIN0 IRQ5 / MTIOC0A_IRQ4	50 / NC / 27	24	IIC_EX NC	NC
25	IIC_SDA SDA2-DS / SSDA2	46 / 72	26	IIC_SCL SCL2-DS / SSCL2	48 / 70

Table 7-1: Application Header JA1 Connections

Table 7-2 below lists the connections of the application header, JA2.

Application Header JA2					
Pin	**Function** **Circuit Net Name**	**MCU Pin**	**Pin**	**Function** **Circuit Net Name**	**MCU Pin**
1	RESET RESn	21	2	EXTAL CON_EXTAL	24
3	NMI NMI	26	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX A-TXD7	163
7	IRQ0 / WKUP / M1_HSIN0 MTIOC0A_IRQ4	27 / NC / 27	8	SCIaRX A-RXD7	160
9	IRQ1 / M1_HSIN1 MTIOC0B_IRQ3	52 / 52	10	SCIaCK A-SCK7	161
11	M1_UD MTIOC3C	13	12	CTSRTS A-CTS7RTS7	159
13	M1_UP MTIOC3B	81	14	M1_UN MTIOC3D	80
15	M1_VP MTIOC4A	79	16	M1_VN MTIOC4C	74
17	M1_WP MTIOC4B	86	18	M1_WN MTIOC4D	83
19	TimerOut MTIOC2B	36	20	TimerOut TIOCA2	47
21	TimerIn MTIOC0D	28	22	TimerIn TIOCA0	49
23	IRQ2 / M1_EncZ / M1_HSIN2 MTIOC0C_IRQ2-DS / MTIOC1A	29 / 45 / 29	24	M1_POE POE0n	82
25	M1_TRCCLK MTCLKA	40	26	M1_TRDCLK MTCLKB	38

Table 7-2: Application Header JA2 Connections

Table 7-3 below lists the connections of the BUS application header, JA3.

Application Header JA3 (Bus)					
Pin	Function Circuit Net Name	MCU Pin	Pin	Function Circuit Net Name	MCU Pin
1	A0 A0	118	2	A1 A1	114
3	A2 A2	112	4	A3 A3	110
5	A4 A4	109	6	A5 A5	108
7	A6 A6	107	8	A7 A7	106
9	A8 A8	104	10	A9 A9	100
11	A10 A10	99	12	A11 A11	98
13	A12 A12	97	14	A13 A13	96
15	A14 A14	95	16	A15 A15	94
17	D0 D0	158	18	D1 D1	156
19	D2 D2	154	20	D3 D3	150
21	D4 D4	148	22	D5 D5	147
23	D6 D6	145	24	D7 D7	143
25	RDn RDn	70	26	WR / SDWE WRn / WEn	72 / 136
27	CSa CS4n	88	28	CSb CON_SDCSn	139
29	D8 D8	135	30	D9 D9	134
31	D10 D10	133	32	D11 D11	132
33	D12 D12	131	34	D13 D13	130
35	D14 D14	126	36	D15 D15	125
37	A16 A16_ET0ERXD3	91	38	A17 A17_ET0ERXD2_MTIOC3A	89
39	A18 A18_ET0RXDV_MTIOC4B	86	40	A19 A19_ET0TXER_QIO0-A_MTIOC4D	83
41	A20 A20_ET0TXCLK_QIO1-A_POE0n	82	42	A21 A21_ET0ETXD2	78
43	A22 A22_ET0ETXD3	77	44	SDCLK SDCLK / BCLK	128 / 69
45	CSc / Wait CS0n / WAITn	141 / 71	46	ALE / SDCKE ALE / CKE	68 / 124
47	HWRn / DQM1 WR1n / DQM1	71 / 120	48	LWRn / DQM0 WR0n / DQM0	72 / 122
49	CAS CASn	137	50	RAS RASn	138

Table 7-3: Application Header JA3 Connections

Table 7-4 below lists the connections of the application header, JA5.

Application Header JA5					
Pin	**Function** **Circuit Net Name**	**MCU Pin**	**Pin**	**Function** **Circuit Net Name**	**MCU Pin**
1	ADC4 AN004	168	2	ADC5 AN005	167
3	ADC6 AN006	166	4	ADC7 AN007	165
5	CAN1TX CTX0	29	6	CAN1RX CRX0	28
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQ4 / M2_EncZ / M2HSIN1 MTIOC0B_IRQ3 / MTIOC2A	52 / 37 / 52	10	IRQ5 / M2_HSIN2 MTIOC0C_IRQ2-DS	29 / 29
11	M2_UD MTIOC6C	126	12	M2_Uin MTIC5U	53
13	M2_Vin MTIC5V	67	14	M2_Win MTIC5W	68
15	M2_Toggle MTIOC6A	125	16	M2_POE POE4n	96
17	M2_TRCCLK MTCLKC	43	18	M2_TRDCLK MTCLKD	42
19	M2_UP MTIOC6B	108	20	M2_Un MTIOC6D	118
21	M2_VP MTIOC7A	112	22	M2_Vn MTIOC7C	120
23	M2_WP MTIOC7B	114	24	M2_Wn MTIOC7D	122

Table 7-4: Application Header JA5 Connections

Table 7-5 below lists the connections of the application header, JA6.

Application Header JA6					
Pin	**Function**	**MCU Pin**	**Pin**	**Function**	**MCU Pin**
	Circuit Net Name			**Circuit Net Name**	
1	DREQ EDREQ1	79	2	DACK EDACK1	74
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX RS232TX	NC	6	RS232RX RS232RX	NC
7	SCIbRX RXD1	31	8	SCIbTX TXD1	35
9	SCIcTX TXD2	72	10	SCIbCK SCK1	34
11	SCIcCK SCK2	71	12	SCIcRX RXD2	70
13	M1_Toggle MTIOC3A	89	14	M1_Uin MTIC5U	53
15	M1_Vin MTIC5V	67	16	M1_Win MTIC5W	68
17	EXT_USB_VBUS EXT_VBUS	-	18	Reserved NC	NC
19	EXT_USB_BATT EXT_BATT	-	20	Reserved NC	NC
21	EXT_USB_CHG EXT_CHG	-	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

Table 7-5: Application Header JA6 Connections

7.2 Generic Headers

Generic headers, used to provide easy connections to various pins from devices fitted to the RSK+.
Table 7-6 below lists the connections of the LCD Direct Drive (TFT) Header.

LCD Direct Drive Header (TFT)					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V Board_5V	-	2	5V Board_5V	-
3	3V3 Board_3V3	-	4	3V3 Board_3V3	-
5	Reserved NC	NC	6	Reserved NC	NC
7	B1 D0	158	8	B2 D1	156
9	B3 D2	154	10	B4 D3	150
11	B5 D4	148	12	G0 D5	147
13	G1 D6	145	14	G2 D7	143
15	G3 D8	135	16	G4 D9	134
17	G5 D10	133	18	R1 D11	132
19	R2 D12	131	20	R3 D13	130
21	R4 D14	126	22	R5 D15	125
23	EDACK EDACK1	74	24	HSYNC MTIOC3C	13
25	DOTCLK MTIOC0A_IRQ4	27	26	LCDDEN MTIOC3A	89
27	VSYNC MTIOC2A	37	28	EDREQ EDREQ1	79
29	SSCK TFT_QSPCLK-A	84	30	SSI TFT_QIO1-A	82
31	SSO TFT_QIO0-A	83	32	SCS TFT_QSSLA-A	85
33	RESET RESn	21	34	GND GROUND	-
35	BACKLIGHT BACKLIGHT	36	36	SD_DOTCLK NC	NC
37	GND GROUND	-	38	GND GROUND	-
39	GND GROUND	-	40	GND GROUND	-
41	X_DRIVE XDRIVE	11	42	Y_DRIVE YDRIVE	171
43	X_INPUT1 XINPUT1	168	44	Y_INPUT1 YINPUT1	167
45	X_INPUT2 XINPUT2	166	46	Y_INPUT2 YINPUT2	165
47	Reserved NC	NC	48	Reserved NC	NC
49	Reserved NC	NC	50	Reserved NC	NC

Table 7-6: TFT Connector Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E1/E20 debugger. An E1 debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E1/E20 debuggers, refer to E1/E20 Emulator Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK+ is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot modes (SCI and USB), which are configured on the RSK+ board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX71M group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 emulator (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer RX Family E1/E20 Emulator User's Manual.

8.5 Address Space

For the MCU address space details, refer to the 'Address Space' of RX71M Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX71M Group microcontrollers refer to the RX71M Group User's Manual: Hardware.

For information about the RX assembly language, refer to the RX Family Software Manual.

Technical Contact Details

***Please refer to the contact details listed in section 8 of the* "Quick Start Guide"**

General information on Renesas microcontrollers can be found on the Renesas website at:
http://www.renesas.com/

Trademarks
All brand or product names used in this manual are trademarks or registered trademarks of their respective companies or organisations.

Copyright

REVISION HISTORY	RSK+RX71M User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Jan 23, 2015	—	First Edition issued

Renesas Starter Kit+ Manual: User’s Manual

Publication Date: Rev. 1.00 Jan 23, 2015

Published by: Renesas Electronics Corporation

Renesas Electronics Corporation

SALES OFFICES http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130
Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004
Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900
Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327
Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679
Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999
Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022
Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670
Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300
Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510
Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777
Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 4.0

RX71M Group

Renesas Electronics Corporation

R20UT3217EG0100