LVCMOS Dual-Frequency Programmable VCXO

IDT8N0DV85

DATA SHEET

General Description

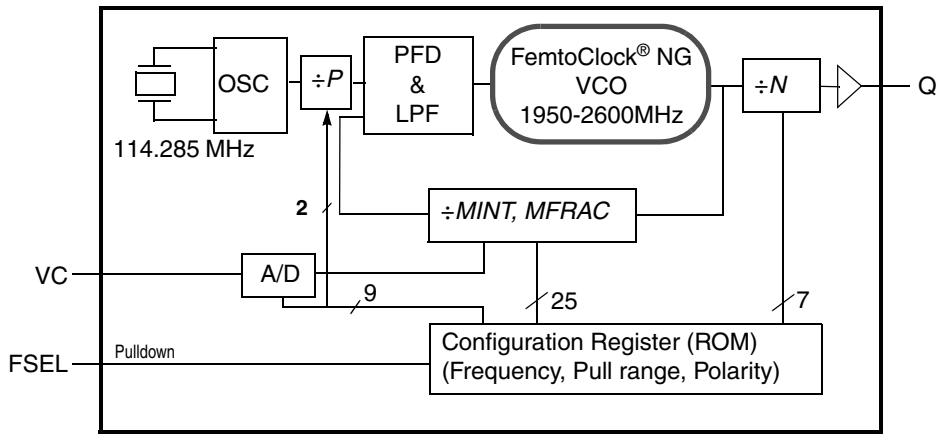
The IDT8N0DV85 is a LVCMOS Dual-Frequency Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory-programmed to any two frequencies in the range of 15.476MHz to 260MHz to the very high degree of frequency precision of 218Hz or better. The output frequency is selected by the FSEL pin. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

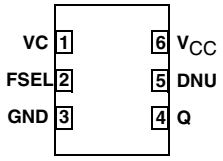
Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 260MHz
- Two factory-programmed output frequencies
- Frequency programming resolution is 218Hz and better
- Absolute pull-range (APR) programmable from ±4.5 to ±754.5ppm
- One 2.5V or 3.3V LVCMOS clock output
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.65ps (typical)
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): 0.94ps (typical)
- 2.5V or 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package

Block Diagram



Pin Assignment



IDT8N0DV85
6-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	VC	Input		VCXO Control Voltage input.
2	FSEL	Input	Pulldown[NOTE 1]	Frequency select pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
3	GND	Power		Power supply pin.
4	Q	Output		Clock output. LVCMOS interface levels.
5	DNU			Do not use.
6	V_{CC}	Power		Power supply pin.

NOTE 1. *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	FSEL			5.5		pF
		VC			10		pF
C_{PD}	Power Dissipation Capacitance		V_{CC} = 3.465V or 2.625V		8		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{OUT}	Output Impedance	Q	V_{CC} = 3.3V		14		Ω
			V_{CC} = 2.5V		17		Ω

Function Tables

Table 3A. Output Frequency

15.476MHz to 260MHz

NOTE. Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz.

Principles of Operation

The block diagram consists of the internal 3RD overtone crystal and oscillator which provide the reference clock f_{XTAL} of 114.285MHz. The PLL includes the FemtoClock NG VCO along with the Pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the f_{XTAL} reference. The feedback divider is fractional supporting a huge number of output frequencies. Internal registers are used to hold up to two different factory pre-set configuration settings. The configuration is selected via the FSEL pin. Changing the FSEL control results in an immediate change of the output frequency to the selected register values. The *P*, *M*, and *N* frequency configurations support an output frequency range 15.476MHz to 260MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator. The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right] \quad (1)$$

Frequency Configuration

An order code is assigned to each frequency configuration and the VCXO pull-range programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information Section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information on programming capabilities of the device for custom frequency and pull-range configurations, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide.*

Table 3B. Frequency Selection

Input FSEL	Selects
0 (default)	Frequency 0
1	Frequency 1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	49.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			135	163	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current			124	148	mA

Table 4C. LVCMOS/LVTTL DC Characteristic, V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = V_{IN} = 3.465V	-0.3		0.8	V
			V_{CC} = V_{IN} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	FSEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	FSEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Q	V_{CC} = 3.465V	2.6			V
			V_{CC} = 2.625V	1.8			V
V_{OL}	Output Low Voltage	Q	V_{CC} = 3.465V or 2.625V			0.6	V

AC Electrical Characteristics

Table 5A. VCXO Control Voltage Input (V_C) Characterisitics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
K_V	Oscillator Gain, NOTE 1, 2, 3 V_{CC} = 3.3V	ADC_GAIN[5:0] = 000001		7.57		ppm/V
		ADC_GAIN[5:0] = 000010		15.15		ppm/V
		ADC_GAIN[5:0] = XXXXXX		25 · ADC_GAIN ÷ V_{CC}		ppm/V
		ADC_GAIN[5:0] = 111110		469.69		ppm/V
		ADC_GAIN[5:0] = 111111		477.27		ppm/V
	Oscillator Gain, NOTE 1, 2, 3 V_{CC} = 2.5V	ADC_GAIN[5:0] = 000001		10		ppm/V
		ADC_GAIN[5:0] = 000010		20		ppm/V
		ADC_GAIN[5:0] = XXXXXX		25 · ADC_GAIN ÷ V_{CC}		ppm/V
		ADC_GAIN[5:0] = 111110		620		ppm/V
		ADC_GAIN[5:0] = 111111		630		ppm/V
L_{VC}	Control Voltage Linearity	BSL Variation; NOTE 4	-1	±0.1	+1	%
BW	Modulation Bandwidth			100		kHz
R_{VC}	VC Input Resistance		500			kΩ
VC_{NOM}	Nominal Control Voltage			V_{CC}÷2		V
V_C	Control Voltage Tuning Range; NOTE 4		0		V_{CC}	V

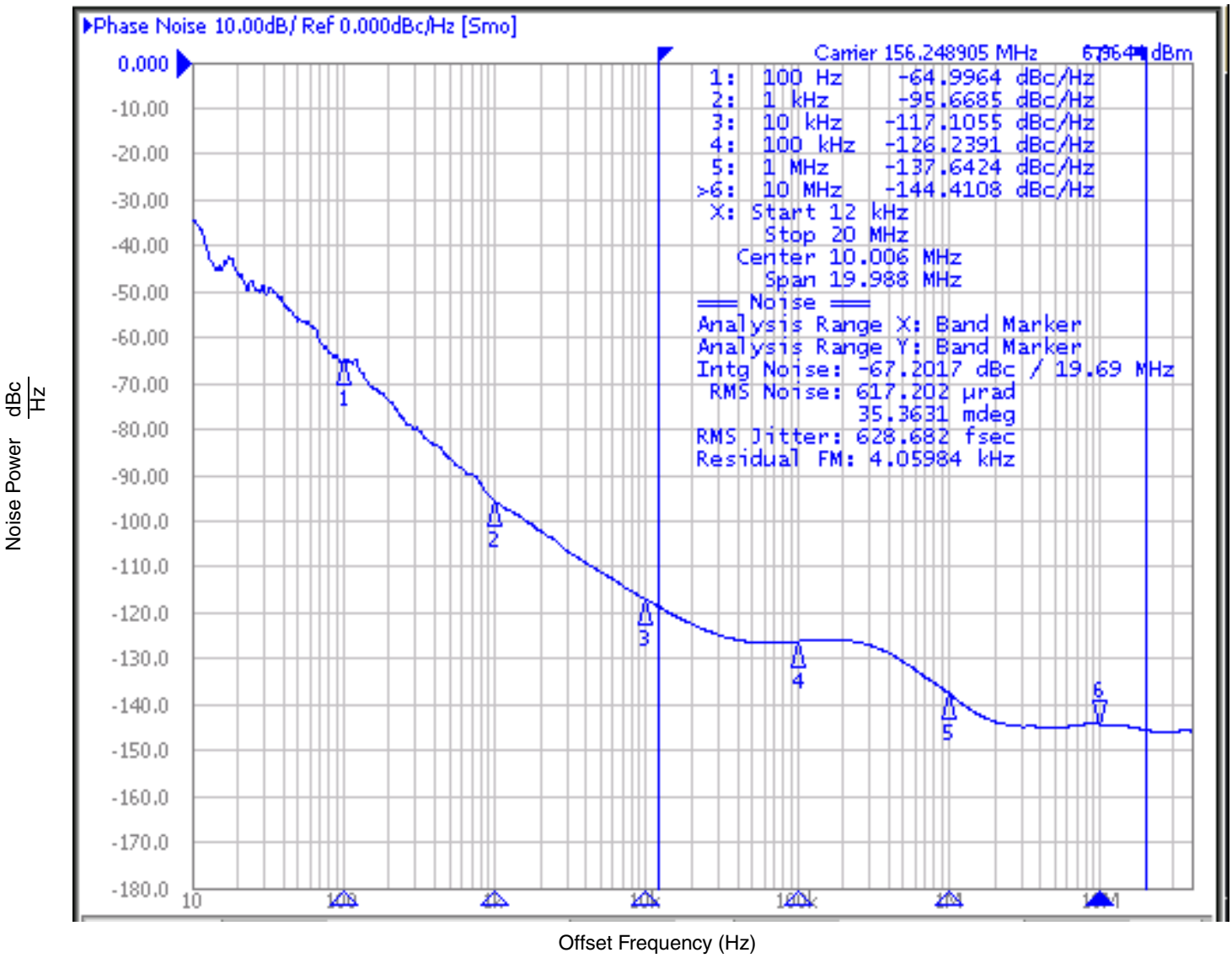
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: V_C = 10% to 90% of V_{CC}.
NOTE 2: Nominal oscillator gain: Pull range divided by the control voltage tuning range of 3.3V.
E.g. for ADC_GAIN[6:0] = 000001 the pull range is ±12.5ppm, resulting in an oscillator gain of 25ppm ÷ 3.3V = 7.57ppm/V.
NOTE 3: For best phase noise performance, use the lowest K_V that meets the requirements of the application.
NOTE 4: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage V_C, in percent. V_C ranges from 10% to 90% V_{CC}.

Table 5B. AC Characterisitics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

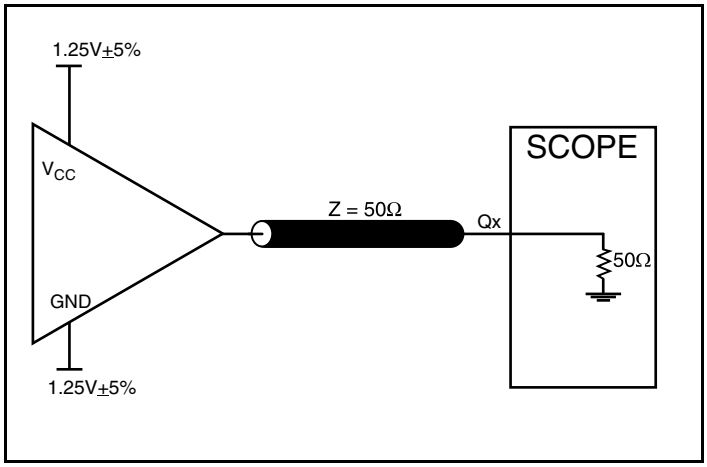
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q		15.476		260	MHz
f_I	Initial Accuracy	Measured at 25°C			±10	ppm
f_S	Temperature Stability	Option Code = A or B			±100	ppm
		Option Code = E or F			±50	ppm
		Option Code = K or L			±20	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Option Code A or B (10 year life time)			±113	ppm
		Option Code E or F (10 year life time)			±63	ppm
		Option Code K or L (10 year life time)			±33	ppm
tjit(cc)	Cycle-to-Cycle Jitter NOTE 1, 2, 3			20		ps
tjit(per)	Period Jitter, RMS; NOTE 1, 2, 3			3.3		ps
tjit(Ø)	RMS Phase Jitter (Random) NOTE 4	f_{OUT} = 156.25MHz, Integration Range: 12kHz - 20MHz		0.65	0.90	ps
		f_{OUT} = 156.25MHz, Integration Range: 1kHz - 40MHz		0.94		ps
tjit(Ø)	RMS Phase Jitter (Random) NOTE 4, 5	Integration Range: 12kHz - 20MHz		0.65	1.05	ps
Φ_N(100)	Single-side Band Phase Noise	f_{OUT} = 156.25MHz, 100Hz from Carrier		-65		dBc/Hz
Φ_N(1k)	Single-side band phase noise	f_{OUT} = 156.25MHz, 1kHz from Carrier		-96		dBc/Hz
Φ_N(10k)	Single-side band phase noise	f_{OUT} = 156.25MHz, 10kHz from Carrier		-117		dBc/Hz
Φ_N(100k)	Single-side band phase noise	f_{OUT} = 156.25MHz, 100kHz from Carrier		-126		dBc/Hz
Φ_N(1M)	Single-side band phase noise,	f_{OUT} = 156.25MHz, 1MHz from Carrier		-138		dBc/Hz
Φ_N(10M)	Single-side band phase noise,	f_{OUT} = 156.25MHz, 10MHz from Carrier		-144		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		715	ps
odc	Output Duty Cycle		45		55	%
$t_{STARTUP}$	Device Start-up Time After Power-up				20	ms
t_{SET}	Output Frequency Settling Time After FSEL0 and FSEL1 Values are Changed				1	ms

NOTE: Characterized with VC in linear range.
NOTE: XTAL parameters (Initial Accuracy, temperature Stability, Aging and Total Stability) are guaranteed by manufacturing.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Tested at supply voltage V_{CC} = 3.3V ± 5%.
NOTE 3: Applies to output frequencies: 15.476, 19.44, 25, 33.33, 74.174, 74.25, 100, 106.25, 122.88, 125, 150, 155.52, 156.25, 161.132, 176.8328, 187.5, 200, 212.5, 250 and 260MHz.
NOTE 4: Refer to phase noise plot.
NOTE 5: Applies to output frequencies: 25, 33.33, 100, 106.25, 122.88, 125, 148.5, 150, 155.52, 156.25, 161.132, 164.3555, 166.62875, 176.8328, 187.5, 212.5 and 250MHz.

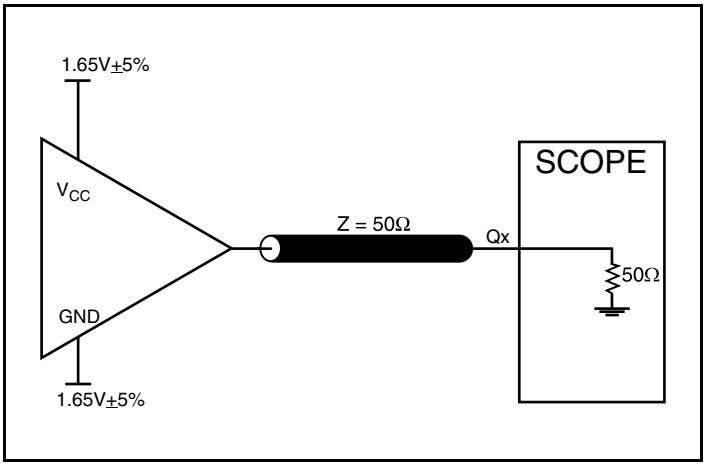
Typical Phase Noise at 156.25MHz (12kHz - 20MHz)



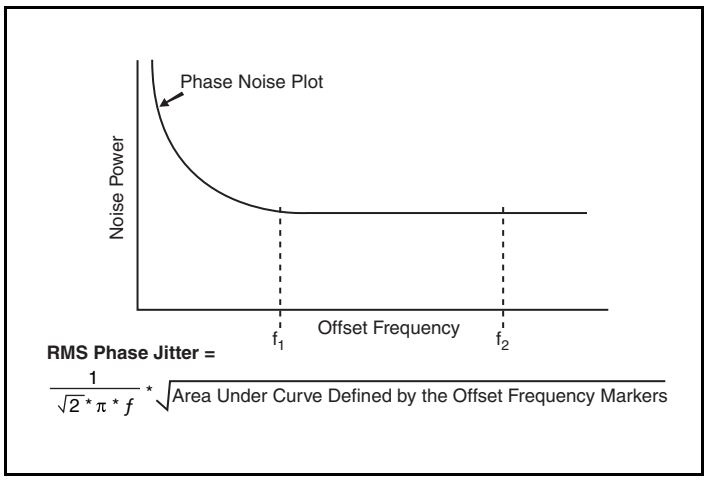
Parameter Measurement Information



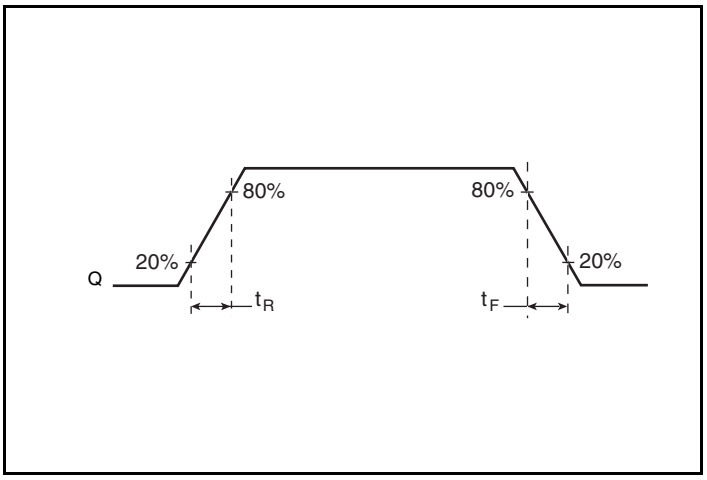
2.5V LVCMOS/LVTTL Output Load AC Test Circuit



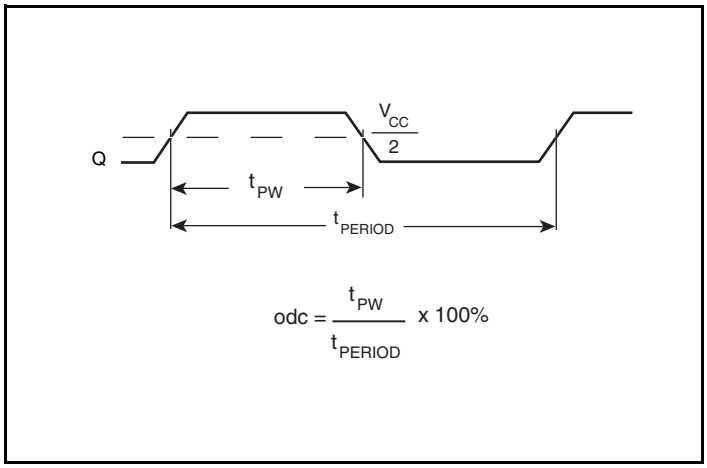
3.3V LVCMOS/LVTTL Output Load AC Test Circuit



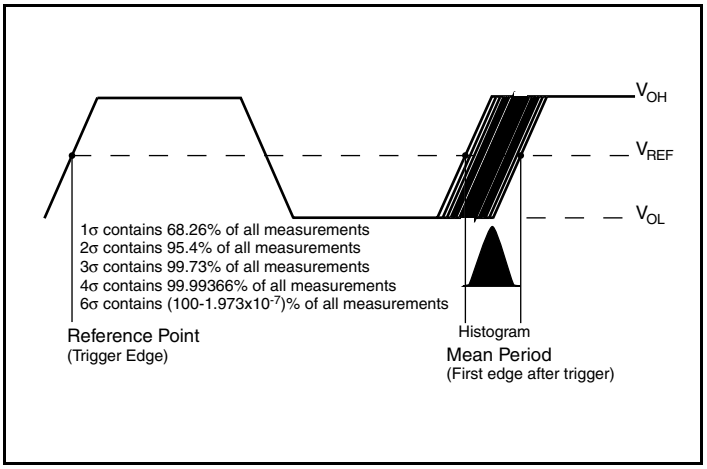
RMS Phase Jitter



Output Rise and Fall Time



Output Duty Cycle/Pulse Width/Period



RMS Period Jitter

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Pins

The control pin has an internal pulldown; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Schematic Layout

Figure 1 shows an example of IDT8N0DV85 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example FSEL can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

The typical application of the IDT8N0DV85 is a voltage-controlled oscillator as part of a PLL. The two connections necessary to be made to the PLL are VC, the analog control voltage that sets the center frequency of the VCXO, and Q, which is the oscillator output. VC is the analog output of the PLL low pass loop filter that serves to remove noise from the phase detector error output.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{CC} pin from the power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor on the V_{CC} pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

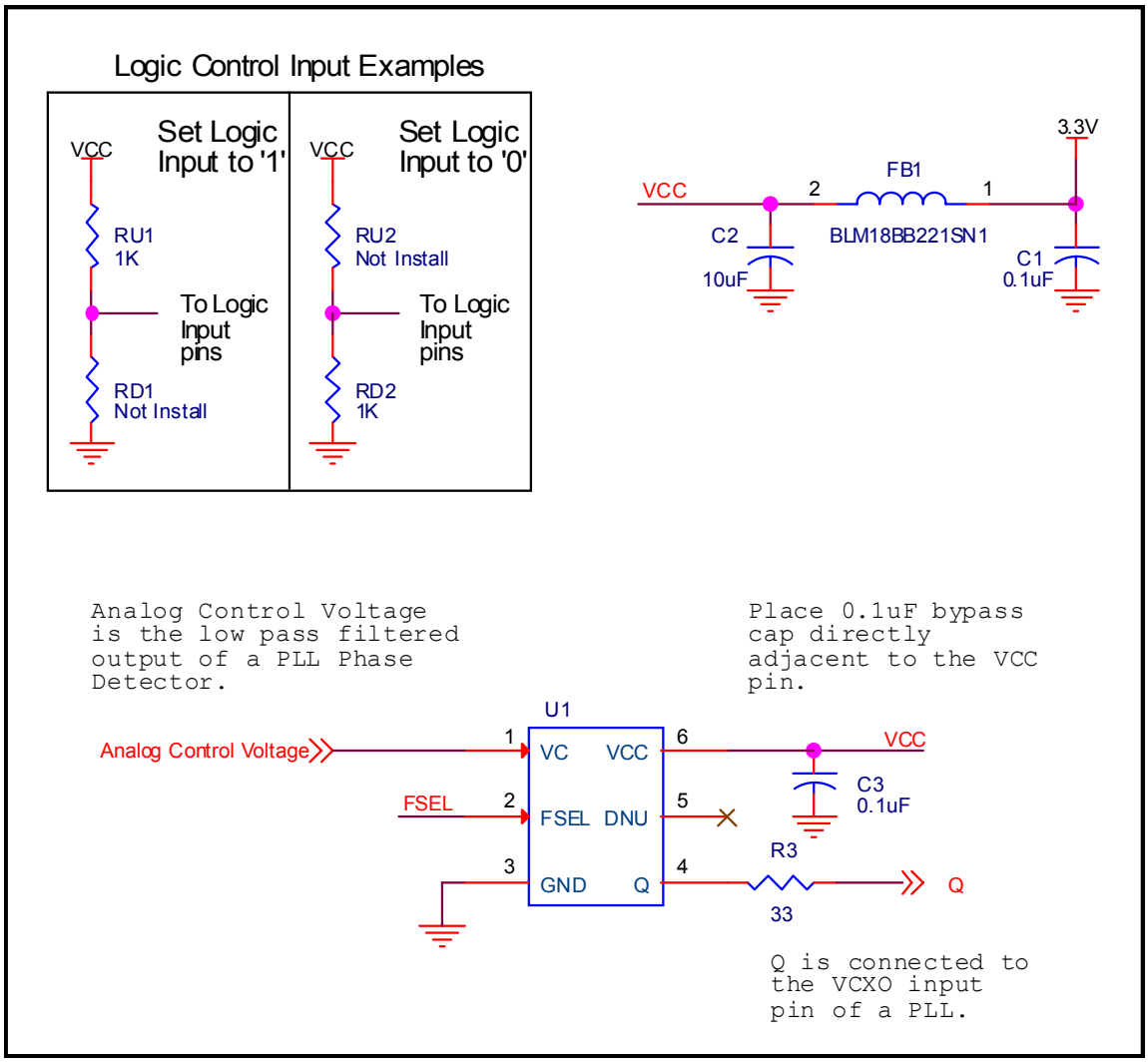


Figure 1. IDT8N0DV85 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N0DV85.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N0DV85 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for V_{CC} = 3.3V +5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{CC}= 3.465V * 163mA = **564.8mW**

Total Static Power:

= Power (core)$_{MAX}$ = **564.8mW**

Dynamic Power Dissipation at F_{OUT} (max)

Total Power (F_{OUT_MAX}) = [(C_{PD} * N) * Frequency * (V_{CC})^2**]** = [(8pF *1) * 260MHz * (3.465V)^2] = **25mW**

Total Power

Total Power
= Static Power + Dynamic Power Dissipation
= 564.8mW + 25mW
= 589.8mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.590W * 49.4°C/W = 114.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for a 6-lead Ceramic 5mm x 7mm Package, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Reliability Information

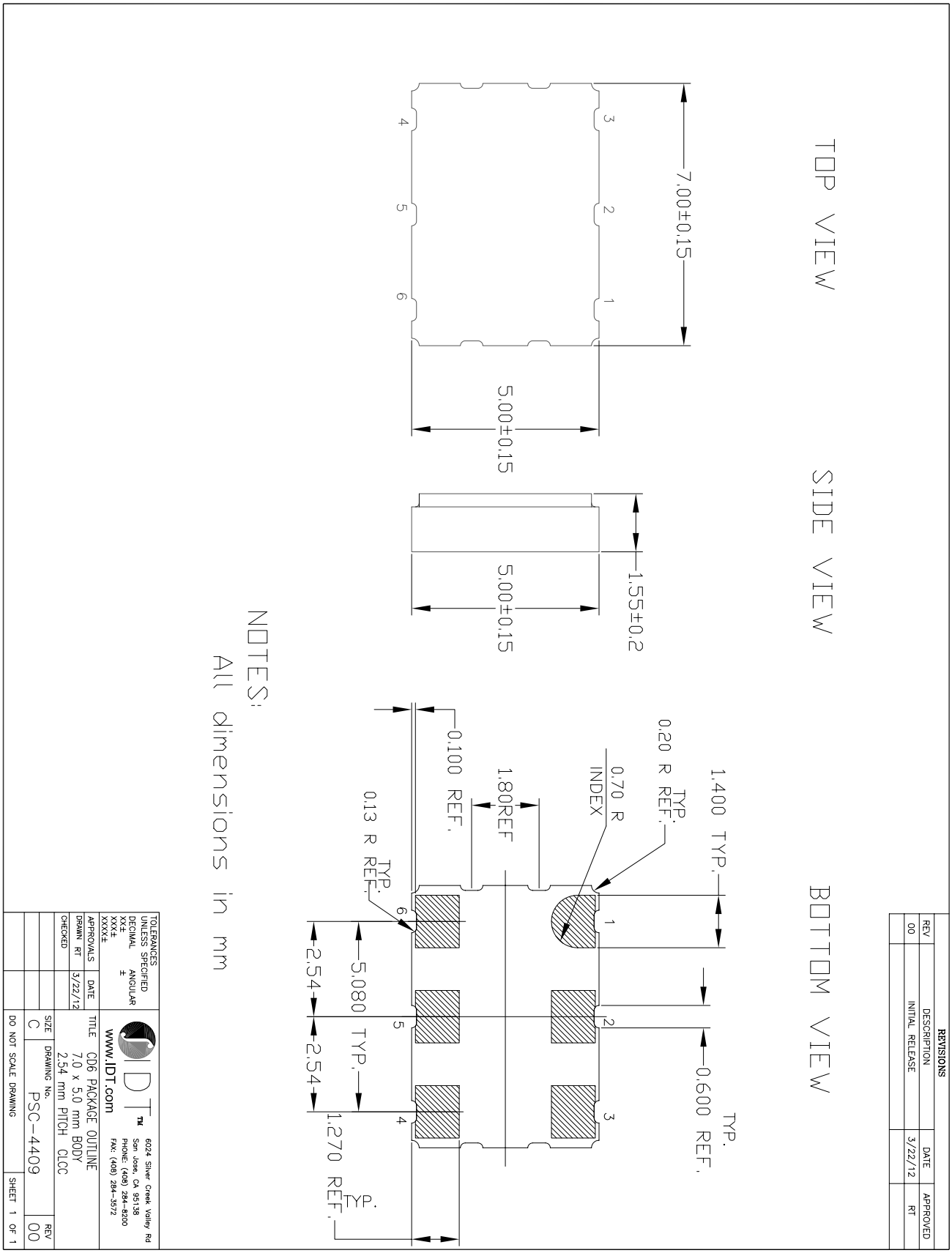
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Transistor Count

The transistor count for IDT8N0DV85 is: 47,414

Package Outline and Package Dimensions



Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. The table below specifies the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N3QV01FG-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ±50ppm crystal frequency accuracy, contains a 114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of min. ±100ppm.

Other default frequencies and order codes are available from IDT on request. For more information on available default frequencies, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

Part/Order Numbers

8N X X XXX X X - dddd XX X X

FemtoClock NG

I/O Identifier
0: LVCMOS
3: LVPECL
4: LVDS

Number of Default Frequencies
S: 1: Single
D: 2: Dual
Q: 4: Quad

Part Number

	Function	#pins	OE fct. at pin
001	XO	10	OE@2
003	XO	10	OE@1
V01	VCXO	10	OE@2
V03	VCXO	10	OE@1
V75	VCXO	6	OE@2
V76	VCXO	6	nOE@2
V85	VCXO	6	—
085	XO	6	OE@1
270	XO	6	OE@1
271	XO	6	OE@2
272	XO	6	nOE@2
273	XO	6	nOE@1

Option Code (Supply Voltage and Frequency-Stability)
A: V_{CC} = 3.3V±5%, ±100ppm
B: V_{CC} = 2.5V±5%, ±100ppm
E: V_{CC} = 3.3V±5%, ±50ppm
F: V_{CC} = 2.5V±5%, ±50ppm
K: V_{CC} = 3.3V±5%, ±20ppm
L: V_{CC} = 2.5V±5%, ±20ppm

Die Revision
A

Default-Frequency and VCXO Pull Range
See document *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information.*

dddd	f_{XTAL} (MHz)	PLL feedback	Use for
0000 to **0999**	114.285	Fractional	VCXO, XO
1000 to **1999**	100.000	Integer	XO
2000 to **2999**		Fractional	XO

Last digit = **L**: configuration pre-programmed and not

Package Code
CD: Lead-Free, 6/10-lead ceramic 5mm x 7mm x 1.55mm

Ambient Temperature Range
"**I**": Industrial: (T_A = -40°C to 85°C)
(no letter) : (T_A = 0°C to 70°C)

Shipping Package
8: Tape & Reel
(no letter): Tray

NOTE: For order information, also see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

Table 8. Device Marking

	Industrial Temperature Range (T_A = -40°C to 85°C)	Commercial Temperature Range (T_A = 0°C to 70°C)
Marking	IDT8N0DV85**y**A- **dddd**CDI	IDT8N0DV85**y**A- **dddd**CD
	y = Option Code, **dddd**=Default-Frequency and VCXO Pull Range	

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