128Mx8, 64Mx16 1Gb DDR3 SDRAM

ADVANCED INFORMATION
DECEMBER 2011

FEATURES

- Standard Voltage: V_{DD} and V_{DDQ} = 1.5V ± 0.075V
  Low Voltage (L): V_{DD} and V_{DDQ} = 1.35V + 0.1V, -0.067V
- High speed data transfer rates with system frequency up to 933 MHz
- 8 internal banks for concurrent operation
- 8Bits pre-fetch architecture
- Programmable CAS Latency: 5, 6, 7, 8, 9, 10 and 11
- Programmable Additive Latency: 0, CL-1,CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)
- Refresh Interval:
  7.8 us (8192 cycles/64 ms) Tc= -40°C to 85°C
  3.9 us (8192 cycles/32 ms) Tc= 85°C to 105°C
- Partial Array Self Refresh
- Asynchronous RESET pin
- TDQS (Termination Data Strobe) supported (x8 only)
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Operating temperature:
  Commercial (T_C = 0°C to +95°C)
  Industrial (T_C = -40°C to +95°C)
  Automotive, A1 (T_C = -40°C to +95°C)
  Automotive, A2 (T_C = -40°C to +105°C)

OPTIONS

- Configuration:
  128Mx8
  64Mx16
- Package:
  96-ball FBGA (9mm x 13mm) for x16
  78-ball FBGA (8mm x 10.5mm) for x8

ADDRESS TABLE

Parameter	128Mx8	64Mx16
Row Addressing	A0-A13	A0-A12
Column Addressing	A0-A9	A0-A9
Bank Addressing	BA0-2	BA0-2
Page size	1KB	2KB
Auto Precharge Addressing	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#

SPEED BIN

Speed Option	187F	15G	15H	125J	125K	107K	107L	Units
JEDEC Speed Grade	DDR3-1066F	DDR3-1333G	DDR3-1333H	DDR3-1600J	DDR3-1600K	DDR3-1866K	DDR3-1866L	
CL-nRCD-nRP	7-7-7	8-8-8	9-9-9	10-10-10	11-11-11	11-11-11	12-12-12	tCK
tRCD,tRP(min)	13.125	12.0	13.5	12.5	13.75	11.77	12.84	ns

Note: Faster speed options are backward compatible to slower speed options.

1. DDR3 PACKAGE BALLOUT

1.1 DDR3 SDRAM package ballout 78-ball FBGA – x8

	1	2	3	4	5	6	7	8	9
A	VSS	VDD	NC				NU/TDQS#	VSS	VDD
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ
D	VSSQ	DQ6	DQS#				VDD	VSS	VSSQ
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ
F	NC[1]	VSS	RAS#				CK	VSS	NC
G	ODT	VDD	CAS#				CK#	VDD	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	VSS	BA0	BA2				A15	VREFCA	VSS
K	VDD	A3	A0				A12/BC#	BA1	VDD
L	VSS	A5	A2				A1	A4	VSS
M	VDD	A7	A9				A11	A6	VDD
N	VSS	RESET#	A13				NC/A14	A8	VSS

Note:
NC balls have no internal connection. NC/14 and NC/15 are one of NC pins and reserved for higher densities.

1.2 DDR3 SDRAM package ballout 96-ball FBGA – x16

	1	2	3	4	5	6	7	8	9
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS
B	VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ
G	VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ
J	NC	VSS	RAS#				CK	VSS	NC
K	ODT	VDD	CAS#				CK#	VDD	CKE
L	NC	CS#	WE#				A10/AP	ZQ	NC
M	VSS	BA0	BA2				NC/A15	VREFCA	VSS
N	VDD	A3	A0				A12/BC#	BA1	VDD
P	VSS	A5	A2				A1	A4	VSS
R	VDD	A7	A9				A11	A6	VDD
T	VSS	RESET#	NC/A13				NC/A14	A8	VSS

Note:
NC balls have no internal connection. NC/13, NC/14 and NC/15 are one of NC pins and reserved for higher densities.

1.3 Pinout Description - JEDEC Standard

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A13	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail- to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage
VSSQ	Supply	DQ Ground

VDD	Supply	Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage
VSS	Supply	Ground
VREFDQ	Supply	Reference voltage for DQ
VREFCA	Supply	Reference voltage for CA
ZQ, (ZQ0), (ZQ1), (ZQ2), (ZQ3)	Supply	Reference Pin for ZQ calibration Input only pins (BA0-BA2, A0-A13, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

ORDERING INFORMATION

64Mx16 - Commercial Range: (0°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS43TR16640A -187FBL	96-ball FBGA,Lead-free
1333MT/s	8-8-8	IS43TR16640A -15GBL	96-ball FBGA,Lead-free
1333MT/s	9-9-9	IS43TR16640A -15HBL	96-ball FBGA,Lead-free
1600MT/s	10-10-10	IS43TR16640A -125JBL	96-ball FBGA,Lead-free
1600MT/s	11-11-11	IS43TR16640A -125KBL	96-ball FBGA,Lead-free

64Mx16 - Industrial Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS43TR16640A -187FBLI	96-ball FBGA,Lead-free
1333MT/s	8-8-8	IS43TR16640A -15GBLI	96-ball FBGA,Lead-free
1333MT/s	9-9-9	IS43TR16640A -15HBLI	96-ball FBGA,Lead-free
1600MT/s	10-10-10	IS43TR16640A -125JBLI	96-ball FBGA,Lead-free
1600MT/s	11-11-11	IS43TR16640A -125KBLI	96-ball FBGA,Lead-free

64Mx16 – Automotive, A1 Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS46TR16640A -187FBLA1	96-ball FBGA,Lead-free
1333MT/s	8-8-8	IS46TR16640A -15GBLA1	96-ball FBGA,Lead-free
1333MT/s	9-9-9	IS46TR16640A -15HBLA1	96-ball FBGA,Lead-free
1600MT/s	10-10-10	IS46TR16640A -125JBLA1	96-ball FBGA,Lead-free
1600MT/s	11-11-11	IS46TR16640A -125KBLA1	96-ball FBGA,Lead-free

64Mx16 – Automotive, A2 Range: (–40°C ≤ T_C ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS46TR16640A -187FBLA2	96-ball FBGA,Lead-free
1333MT/s	8-8-8	IS46TR16640A -15GBLA2	96-ball FBGA,Lead-free
1333MT/s	9-9-9	IS46TR16640A -15HBLA2	96-ball FBGA,Lead-free
1600MT/s	10-10-10	IS46TR16640A -125JBLA2	96-ball FBGA,Lead-free
1600MT/s	11-11-11	IS46TR16640A -125KBLA2	96-ball FBGA,Lead-free

Note: Contact ISSI for availability of options.

ORDERING INFORMATION

128Mx8 - Commercial Range: (0°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS43TR81280A -187FBL	78-ball FBGA,Lead-free
1333MT/s	8-8-8	IS43TR81280A -15GBL	78-ball FBGA,Lead-free
1333MT/s	9-9-9	IS43TR81280A -15HBL	78-ball FBGA,Lead-free
1600MT/s	10-10-10	IS43TR81280A -125JBL	78-ball FBGA,Lead-free
1600MT/s	11-11-11	IS43TR81280A -125KBL	78-ball FBGA,Lead-free

128Mx8 - Industrial Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS43TR81280A -187FBLI	78-ball FBGA,Lead-free
1333MT/s	8-8-8	IS43TR81280A -15GBLI	78-ball FBGA,Lead-free
1333MT/s	9-9-9	IS43TR81280A -15HBLI	78-ball FBGA,Lead-free
1600MT/s	10-10-10	IS43TR81280A -125JBLI	78-ball FBGA,Lead-free
1600MT/s	11-11-11	IS43TR81280A -125KBLI	78-ball FBGA,Lead-free

128Mx8 – Automotive, A1 Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS46TR81280A -187FBLA1	78-ball FBGA,Lead-free
1333MT/s	8-8-8	IS46TR81280A -15GBLA1	78-ball FBGA,Lead-free
1333MT/s	9-9-9	IS46TR81280A -15HBLA1	78-ball FBGA,Lead-free
1600MT/s	10-10-10	IS46TR81280A -125JBLA1	78-ball FBGA,Lead-free
1600MT/s	11-11-11	IS46TR81280A -125KBLA1	78-ball FBGA,Lead-free

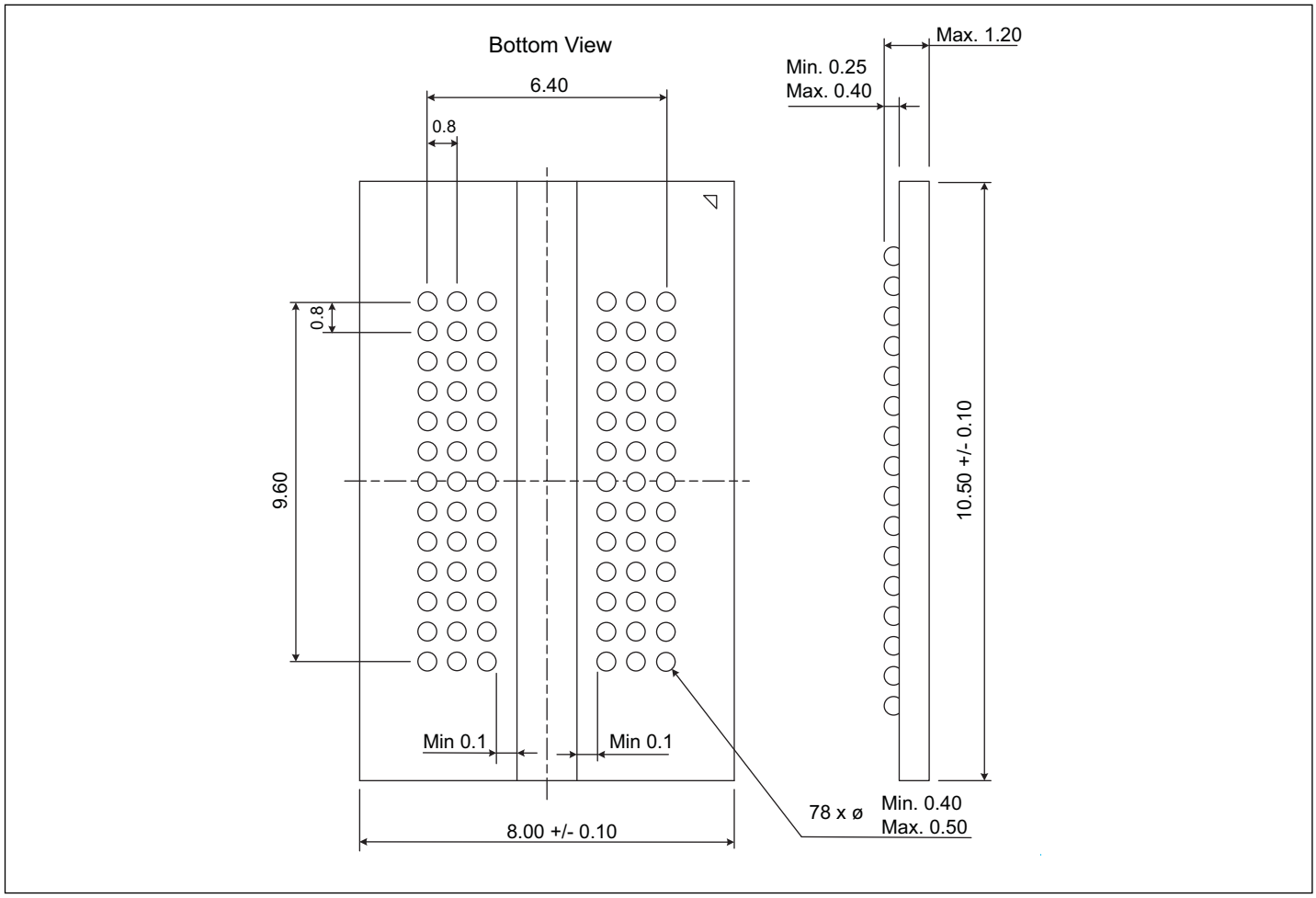
128Mx8 – Automotive, A2 Range: (–40°C ≤ T_C ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1066MT/s	7-7-7	IS46TR81280A -187FBLA2	78-ball FBGA,Lead-free
1333MT/s	8-8-8	IS46TR81280A -15GBLA2	78-ball FBGA,Lead-free
1333MT/s	9-9-9	IS46TR81280A -15HBLA2	78-ball FBGA,Lead-free
1600MT/s	10-10-10	IS46TR81280A -125JBLA2	78-ball FBGA,Lead-free
1600MT/s	11-11-11	IS46TR81280A -125KBLA2	78-ball FBGA,Lead-free

Note: Contact ISSI for availability of options.

PACKAGE OUTLINE DRAWING

78-ball BGA (8mm x 10.5mm): 0.8mm x 0.8mm Pitch (x8)



PACKAGE OUTLINE DRAWING

96-ball BGA (9mm x 13mm): 0.8mm x 0.8mm Pitch (x16)