

## FEATURES

- **16-Bit Monotonic Over Temperature**
- **Low Glitch Impulse: 2nV-s**
- **Low Noise: 30nV/√Hz**
- **Buffered Rail-to-Rail Voltage Output**
- Low Power: 50mW from  $\pm 5V$  Supplies
- Unipolar or Bipolar Output ( $0V$  to  $V_{REF}$  or  $\pm V_{REF}$ )
- 4-Quadrant Multiplying Capability
- Asynchronous Clear to User-Defined Voltage
- Power-On Reset
- Three-Wire SPI and MICROWIRE™ Compatible Serial Interface
- Schmitt Trigger On CLK Input Allows Direct Optocoupler Interface
- 16-Pin Narrow SO Package

## APPLICATIONS

- Industrial Process Control
- Precision Industrial Equipment
- Waveform Generation
- Automatic Test Equipment
- High Resolution Offset and Gain Adjustment

## DESCRIPTION

The LTC<sup>®</sup>1650 is a deglitched rail-to-rail voltage output 16-bit digital-to-analog converter (DAC) available in a 16-pin narrow SO package. It has 16-bit monotonicity over temperature and includes a rail-to-rail output buffer amplifier and an easy to use three-wire cascadable serial interface. The LTC1650 operates with dual  $\pm 5V$  supplies.

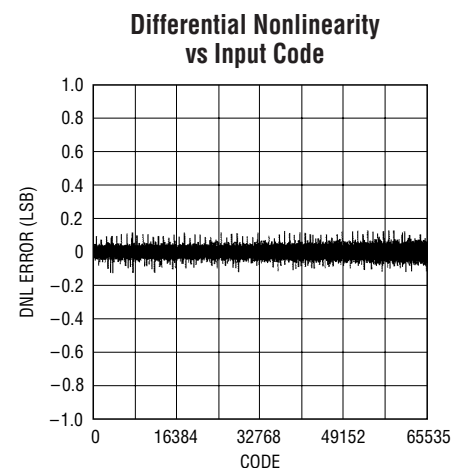
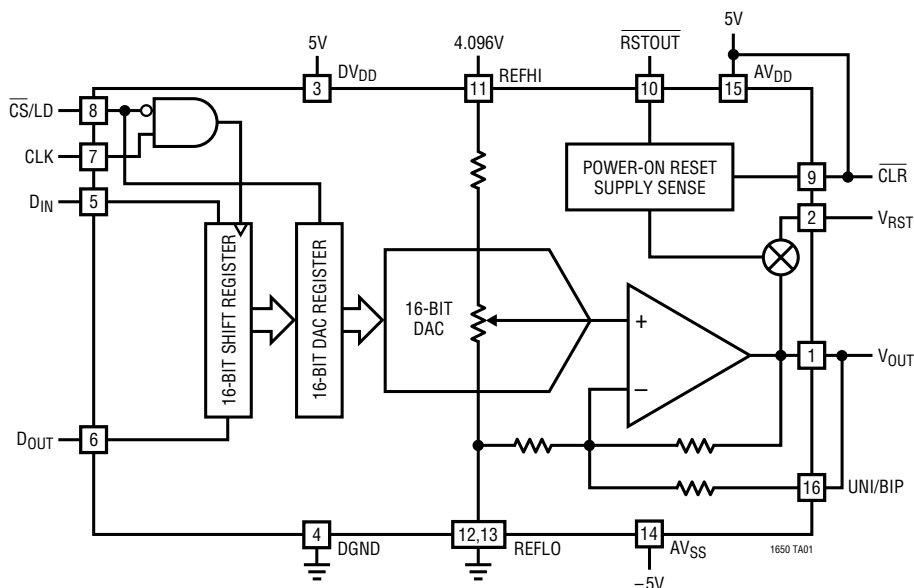
With  $REFLO = 0V$  and  $REFHI = V_{REF}$ , the output will swing from  $0V$  to  $V_{REF}$  in unipolar mode or  $\pm V_{REF}$  in bipolar mode.

The LTC1650 has excellent accuracy over its full operating temperature range along with very low power dissipation of 50mW with dual  $\pm 5V$  supplies. This, along with the small outline package, makes it the most flexible high resolution digital-to-analog converter available today.

The LTC1650 has a fast settling time of  $4\mu s$  to 16 bits and a low midscale glitch of under 2nV-s. This makes the LTC1650 ideal for waveform generation or other applications where output dynamic performance is important.

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## TYPICAL APPLICATION

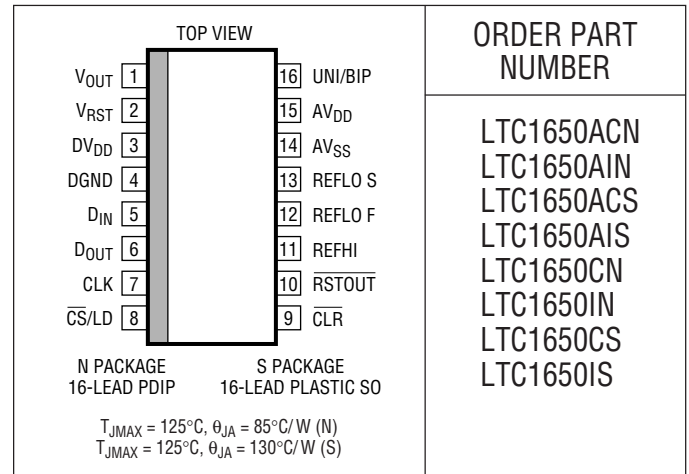


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$AV_{DD}$ , $DV_{DD}$ to DGND .....	-0.5V to 7.5V
TTL Input Voltage .....	-0.5V to 7.5V
$V_{OUT}$ , $V_{RST}$ .....	-0.5V to ( $AV_{DD} + 0.5V$ )
$AV_{SS}$ .....	0.5V to -7.5V
Operating Temperature Range	
LTC1650C .....	0°C to 70°C
LTC1650I .....	-40°C to 85°C
Maximum Junction Temperature .....	125°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION



Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $AV_{DD} = 4.75V$  to  $5.25V$ ,  $AV_{SS} = -4.75V$  to  $-5.25V$ ,  $DV_{DD} = 4.75V$  to  $5.25V$ , REFLO = 0V, REFHI = 4.096V,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1650CS/CN LTC1650IS/IN			LTC1650ACS/ACN LTC1650AIS/AIN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>DAC Characteristics, Unipolar/Bipolar Output Unless Otherwise Noted</b>									
	Resolution		●	16		16			Bits
	Monotonicity		●	16		16			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●		$\pm 0.15$	$\pm 0.9$	$\pm 0.15$	$\pm 0.5$	LSB
INL	Integral Nonlinearity	Integral Nonlinearity (Note 2)	●		$\pm 4$	$\pm 16$	$\pm 4$	$\pm 8$	LSB
	Bipolar Zero Error	$T_A = 25^{\circ}C$			$\pm 5$	$\pm 12$	$\pm 5$	$\pm 12$	LSB
	Bipolar Zero Error	$T_A = T_{MIN}$ to $T_{MAX}$	●			$\pm 18$		$\pm 18$	LSB
$V_{OS}$	Unipolar Offset Error	$T_A = T_{MIN}$ to $T_{MAX}$	●		$\pm 0.5$	$\pm 12$	$\pm 0.5$	$\pm 12$	LSB
$V_{OSTC}$	Offset Error Temperature Coefficient				$\pm 0.5$		$\pm 0.5$		$\mu V/^{\circ}C$
	Gain Error	$T_A = T_{MIN}$ to $T_{MAX}$	●		$\pm 4$	$\pm 18$	$\pm 4$	$\pm 12$	LSB
	Gain Error Temperature Coefficient				$\pm 0.5$		$\pm 0.5$		ppm/ $^{\circ}C$
	Bipolar Negative Full-Scale Error	$T_A = T_{MIN}$ to $T_{MAX}$ See Definitions Section	●		$\pm 1$	$\pm 16$	$\pm 1$	$\pm 12$	LSB
	Bipolar Negative Full-Scale Error Tempco	See Definitions Section			$\pm 0.75$		$\pm 0.75$		ppm/ $^{\circ}C$

**ELECTRICAL CHARACTERISTICS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $AV_{DD} = 4.75\text{V}$  to  $5.25\text{V}$ ,  $AV_{SS} = -4.75\text{V}$  to  $-5.25\text{V}$ ,  $DV_{DD} = 4.75\text{V}$  to  $5.25\text{V}$ ,  $REFLO = 0\text{V}$ ,  $REFHI = 4.096\text{V}$ ,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Power Supply Characteristics</b>							
$AV_{DD}$	Positive Supply Voltage		●	4.75	5.0	5.25	V
$DV_{DD}$	Positive Supply Voltage		●	4.75	5.0	5.25	V
$AV_{SS}$	Negative Supply Voltage		●	-4.75	-5.0	-5.25	V
$I_{AVDD}$	$AV_{DD}$ Supply Current	$4.75\text{V} \leq AV_{DD} \leq 5.25\text{V}$ (Note 5)	●		5	7.5	mA
$I_{AVSS}$	$AV_{SS}$ Supply Current	$-5.25\text{V} \leq AV_{SS} \leq -4.75\text{V}$ (Note 5)	●	-7.5	-5		mA
$I_{DVDD}$	$DV_{DD}$ Supply Current	$4.75\text{V} \leq DV_{DD} \leq 5.25\text{V}$ (Note 5)	●		0.1	0.25	mA
PSRR	$AV_{DD}$ , $DV_{DD}$ Supply Rejection	$4.75\text{V} \leq AV_{DD}$ , $DV_{DD} \leq 5.25\text{V}$	●		0.5	1.5	LSB/V
	$AV_{SS}$ Supply Rejection	$-5.25\text{V} \leq AV_{SS} \leq -4.75\text{V}$	●		0.5	1.5	LSB/V
<b>Reference Input</b>							
$R_{IN}$	Reference Input Resistance		●	2.5	5	7.5	k $\Omega$
	REFHI Range		●	-4.0	4.0	4.5	V
	REFLO Range		●	-1.0	0	1.0	V
<b>Op Amp DC Performance</b>							
	Short-Circuit Current Low	$V_{OUT}$ Shorted to GND	●		25	50	mA
	Short-Circuit Current High	$V_{OUT}$ Shorted to $V_{CC}$	●		25	50	mA
	Output Impedance	Measured at Midscale			0.15		$\Omega$
	DAC Output Range	Unipolar Mode (Note 9) Bipolar Mode (Note 9)			0V to $V_{REF}$ $\pm V_{REF}$		V V
<b>AC Performance</b>							
	Voltage Output Slew Rate		●	0.8	2.0		V/ $\mu\text{s}$
	Voltage Output Settling Time	Unloaded (Note 4)			4		$\mu\text{s}$
	Midscale Glitch Impulse				1.8		nV-s
	Digital Feedthrough				0.05		nV-s
	Output Noise Voltage Density	1kHz to 100kHz (Note 6)			30		nV/ $\sqrt{\text{Hz}}$
SINAD	Signal-to-Noise + Distortion Ratio	REFHI = 1kHz $4V_{P-P}$			96		dB

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Digital I/O Characteristics</b>							
$V_{IH}$	Digital Input High Voltage		●	2.4			V
$V_{IL}$	Digital Input Low Voltage		●			0.8	V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1\text{mA}$ , $D_{OUT}$ Only	●	$V_{CC} - 1.0$			V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1\text{mA}$ , $D_{OUT}$ Only	●			0.4	V
$I_{LK}$	Digital Input Leakage	$V_{IN} = \text{GND to } V_{CC}$	●			$\pm 10$	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance	(Note 3)				10	pF
<b>Reset Characteristics</b>							
$R_{ON}$	$V_{OUT}$ and $V_{RST}$ Switch Resistance	$V_{RST} = 0.5\text{V}$ (Note 7)	●		200	500	$\Omega$
	Threshold Voltage for Reset	$AV_{DD}$ or $DV_{DD}$ (Note 8) $ AV_{SS} $ (Note 8)	●	1.5	2.5	3.2	V
			●	1.5	2.5	3.2	V
<b>Switching Characteristics</b>							
$t_1$	$D_{IN}$ Valid to CLK Setup		●	40			ns
$t_2$	$D_{IN}$ Valid to CLK Hold		●	0			ns
$t_3$	CLK High Time	(Note 3)	●	40			ns
$t_4$	CLK Low Time	(Note 3)	●	40			ns
$t_5$	$\overline{CS}/LD$ Pulse Width	(Note 3)	●	50			ns
$t_6$	LSB CLK to $\overline{CS}/LD$	(Note 3)	●	40			ns
$t_7$	$\overline{CS}/LD$ Low to CLK	(Note 3)	●	20			ns
$t_8$	$D_{OUT}$ Output Delay	$C_{LOAD} = 100\text{pF}$	●	5	45	150	ns
$t_9$	CLK Low to $\overline{CS}/LD$ Low	(Note 3)	●	20			ns
$t_{10}$	CLR Pulse Width		●	50			ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Nonlinearity is defined from code 0 to code 65535 (full scale) (end point INL, see Definitions section).

**Note 3:** Guaranteed by design. Not subject to test.

**Note 4:** To  $\pm 1\text{LSB}$ . Unipolar mode. DAC switched between all 1s and all 0s.

**Note 5:** Digital Inputs at 0V or  $DV_{DD}$ .

**Note 6:** Measured at  $V_{OUT}$ .  $REFHI = REFLO = 0\text{V}$ , unipolar mode.

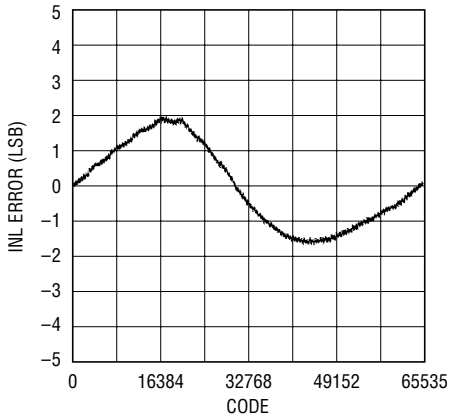
**Note 7:** When part powers up or when it is reset, the output is connected to  $V_{RST}$  through this switch.

**Note 8:** Reset is active when any supply goes below this threshold.

**Note 9:**  $REFLO = 0\text{V}$ ,  $REFHI = V_{REF}$ . For  $REFLO \neq 0\text{V}$  see Operation section.

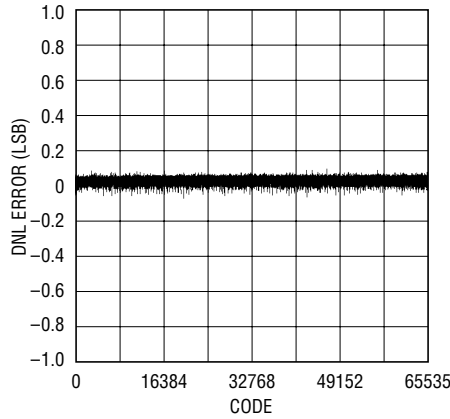
# TYPICAL PERFORMANCE CHARACTERISTICS

**Integral Nonlinearity (INL) vs Input Code**



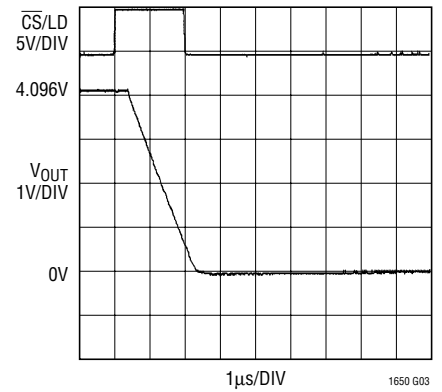
1650 G01

**Differential Nonlinearity (DNL) vs Input Code**



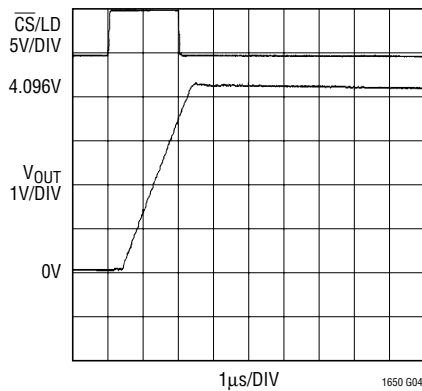
1650 G02

**Large Signal Settling Time**



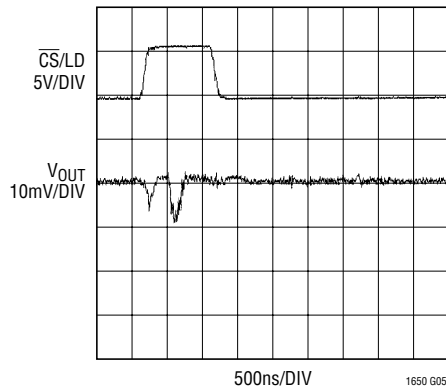
1650 G03

**Large Signal Settling Time**



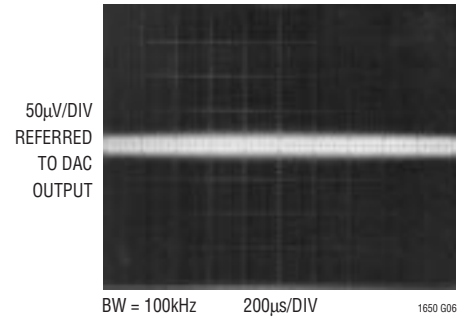
1650 G04

**Mid-Scale Glitch**



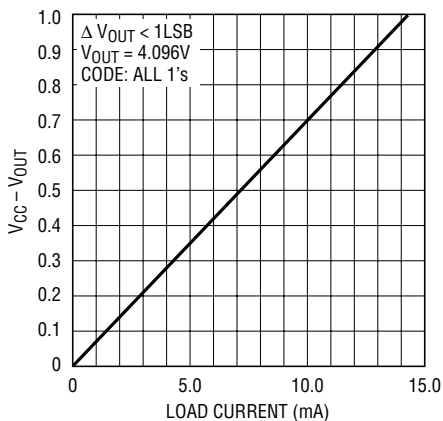
1650 G05

**Broadband Noise**



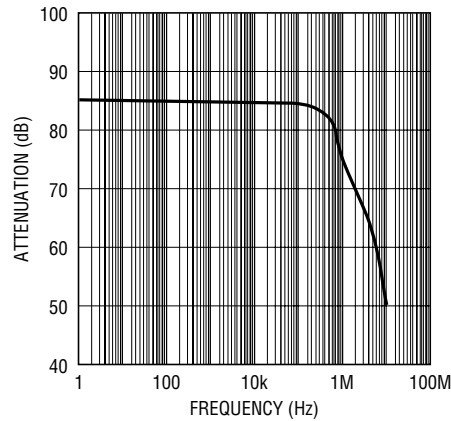
1650 G06

**Minimum Supply Headroom for Full Output Swing vs Load Current**



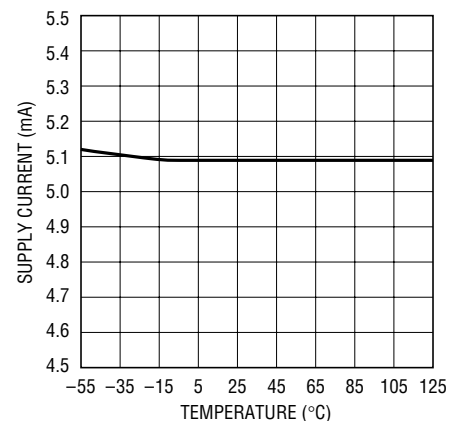
1650 G07

**Reference Feedthrough**



1650 G08

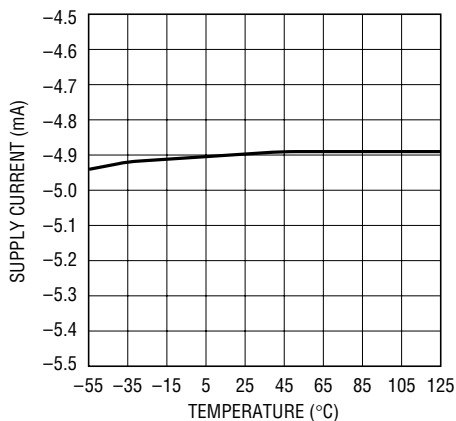
**AVDD Supply Current vs Temperature**



1650 G09

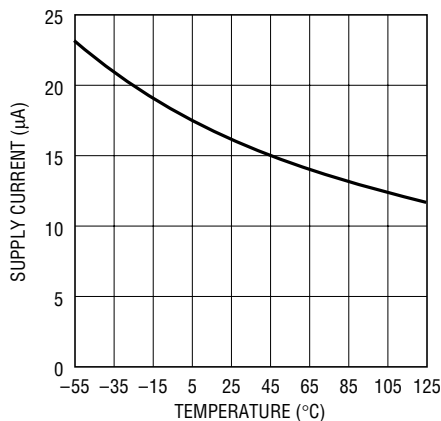
## TYPICAL PERFORMANCE CHARACTERISTICS

**AV<sub>SS</sub> Supply Current vs Temperature**



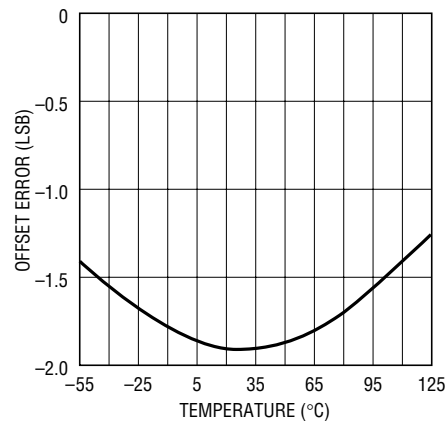
1650 G10

**DV<sub>DD</sub> Supply Current vs Temperature**



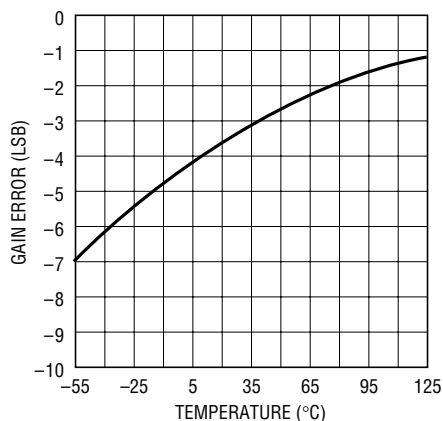
1650 G11

**Offset Error vs Temperature**



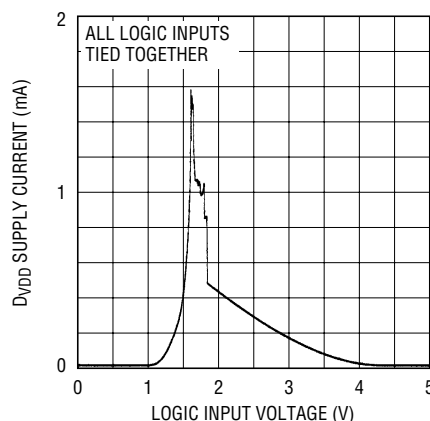
1650 G12

**Gain Error vs Temperature**



1650 G13

**Supply Current vs Logic Input Voltage**



1650 G14

## PIN FUNCTIONS

**V<sub>OUT</sub> (Pin 1):** The DAC Output. The output will swing from REFLO to REFHI in unipolar mode and from (2 • REFLO – REFHI) to REFHI in bipolar mode.

**V<sub>RST</sub> (Pin 2):** The user-defined voltage to which the output gets reset when CLR is active, when any of the supplies drop below 2.5V or when the part powers-up. The output will stay at this voltage until a new code is loaded into the DAC register.

**DV<sub>DD</sub> (Pin 3):** The Digital Positive Supply Input.  $4.75V \leq DV_{DD} \leq 5.25V$ .

**DGND (Pin 4):** Digital Ground.

**D<sub>IN</sub> (Pin 5):** The TTL Level Input for the Serial Interface Data. Data on the D<sub>IN</sub> pin is latched into the shift register on the rising edge of the serial clock. Data is loaded as one 16-bit word, MSB first.

**D<sub>OUT</sub> (Pin 6):** The output of the shift register that becomes valid on the rising edge of the serial clock.

**CLK (Pin 7):** The TTL Level Input for the Serial Interface Clock.

## PIN FUNCTIONS

**$\overline{\text{CS/LD}}$  (Pin 8):** The TTL Level Input for the Serial Interface Enable and Load Control. When  $\overline{\text{CS/LD}}$  is low, the CLK signal is enabled so the data can be clocked in. When  $\overline{\text{CS/LD}}$  is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

**$\overline{\text{CLR}}$  (Pin 9):** The DAC is cleared to  $V_{\text{RST}}$  when this pin is pulled low. It should be logic high for normal operation.

**$\overline{\text{RSTOUT}}$  (Pin 10):** The logic output pin that goes active when any of the supplies drop below 2.5V. This pin is active low.

**REFHI (Pin 11):** The Reference Input Pin. The DAC is capable of 4-quadrant multiplying; this pin can swing from 4.5V to -4V.

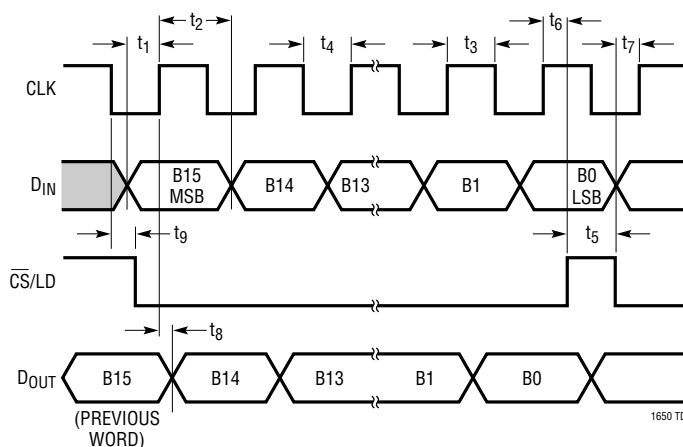
**REFLO F/REFLO S (Pins 12, 13):** The Force and Sense Pin for the Lower Reference Input. This should nominally be tied to ground. This pin can swing from -1V to 1V.

**$\text{AV}_{\text{SS}}$  (Pin 14):** The Analog Negative Supply Input.  $-5.25\text{V} \leq \text{AV}_{\text{SS}} \leq -4.75\text{V}$ . Requires a bypass capacitor to ground.

**$\text{AV}_{\text{DD}}$  (Pin 15):** The Analog Positive Supply Input.  $4.75\text{V} \leq \text{AV}_{\text{DD}} \leq 5.25\text{V}$ . Requires a bypass capacitor to ground.

**UNI/BIP (Pin 16):** The Unipolar/Bipolar Selection Pin. For unipolar operation, tie this pin to  $V_{\text{OUT}}$  and for bipolar operation, tie this pin the REFHI.

## TIMING DIAGRAM



## DEFINITIONS

### Resolution (n)

Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. The resolution does not imply linearity.

### Full-Scale Voltage ( $V_{FS}$ )

This is the output of the DAC when all bits are set to 1. The output will swing from REFLO to REFHI in unipolar mode and from ( $2 \cdot \text{REFLO} - \text{REFHI}$ ) to REFHI when in bipolar mode.

### Voltage Offset Error ( $V_{OS}$ )

This is the voltage at the output when the DAC is loaded with all zeros.

### Least Significant Bit (LSB)

One LSB is the ideal voltage difference between two successive codes.

$$\text{LSB} = (V_{FS} - V_{OS}) / (2^n - 1) = (V_{FS} - V_{OS}) / 65535$$

### Integral Nonlinearity (INL)

Endpoint INL is the maximum deviation from a straight line passing through the endpoints of the DAC transfer curve. It is measured after adjusting out gain and offset error for the DAC.

### Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$\text{DNL} = (\Delta V_{OUT} - \text{LSB}) / \text{LSB}$$

$\Delta V_{OUT}$  = The measured voltage difference between two adjacent codes.

### Gain Error (GE)

Gain error is the difference between the full-scale output of a DAC from its ideal full-scale value after offset error has been adjusted for.

### Bipolar Zero Error

When configured for bipolar output and with REFLO tied to 0V, the LTC1650 output should be 0V with (100...00) loaded in. Any deviation from 0V at this code is called bipolar zero error.

### Bipolar Negative Full-Scale Error

This is the offset error of the LTC1650 in bipolar mode.



## OPERATION

### Serial Interface

The data on the  $D_{IN}$  input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 16-bit word, MSB first. The DAC register loads the data from the shift register when  $\overline{CS/LD}$  is pulled high. The clock is disabled internally when  $\overline{CS/LD}$  is high. Note: CLK must be low before  $\overline{CS/LD}$  is pulled low to avoid an extra internal clock pulse.

The buffered output of the 16-bit shift register is available on the  $D_{OUT}$  pin which swings from DGND to  $DV_{DD}$ .

Multiple LTC1650s may be daisy-chained together by connecting the  $D_{OUT}$  pin to the  $D_{IN}$  pin of the next chip while the clock and  $\overline{CS/LD}$  signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the  $\overline{CS/LD}$  signal is pulled high to update all of them simultaneously.

When  $\overline{CLR}$  is pulled low or when the part powers up, the output connects through an internal pass gate to  $V_{RST}$  and will go to whatever voltage is on  $V_{RST}$ . When any of three supplies ( $DV_{DD}$ ,  $AV_{DD}$ ,  $|AV_{SS}|$ ) goes below 2.5V, the  $\overline{RSTOUT}$  pin goes low and stays low as long as the supply is below 2.5V. The power-on reset is also activated when one of the supplies drops below 2.5V and the output is then connected to  $V_{RST}$ . The output connects to  $V_{RST}$  when any of three conditions occur:  $\overline{CLR}$  goes low, the part powers up or one of the supplies drops below 2.5V. This

condition exists as long as  $\overline{CS/LD}$  is low. As soon as  $\overline{CS/LD}$  goes high, the DAC register is loaded with the data in the shift register and the output will settle to its new value.

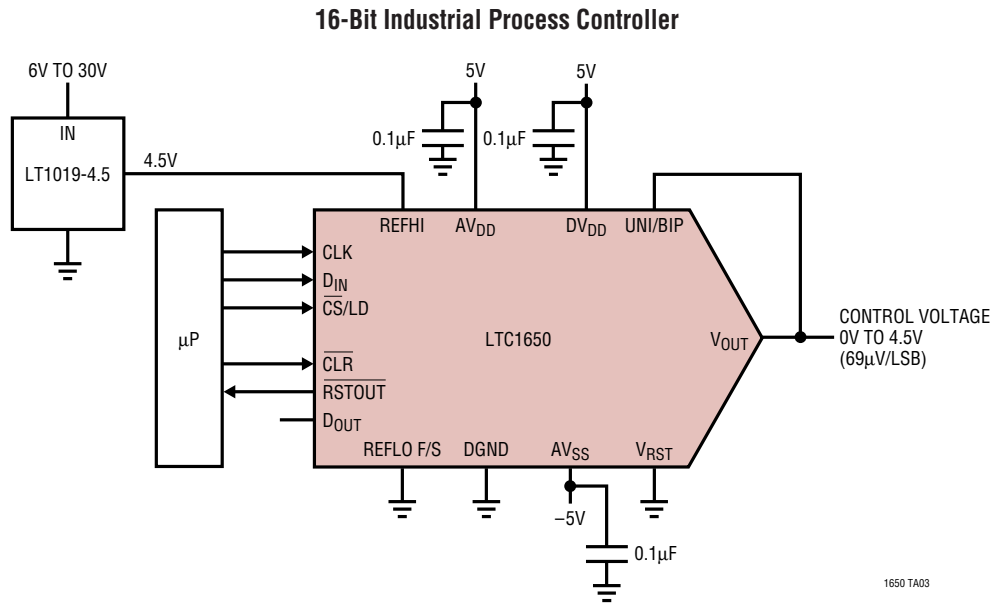
### Voltage Output

The LTC1650 rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range. The output is specified to swing up to  $\pm 4.5V$  on  $\pm 4.75V$  supplies with  $V_{OUT}$  unloaded. (For typical output swing at various load currents, refer to the typical curve "Minimum Supply Headroom for Full Output Swing vs Load Current.") The buffer amplifier can drive 1000pF without going into oscillation. The LTC1650 has a deglitched voltage output. The midscale glitch is less than 2nV-s. The digital feedthrough is about 0.05nV-s.

### Output Ranges

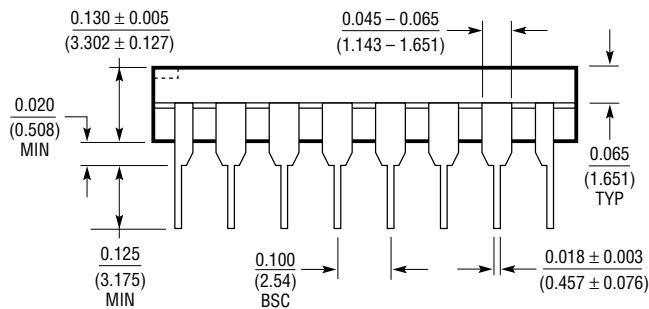
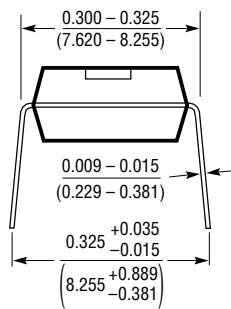
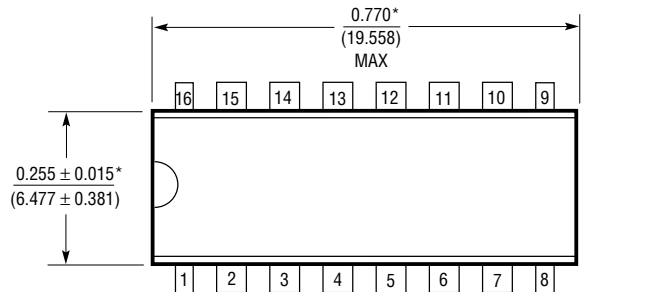
The LTC1650 is capable of unipolar or bipolar output swing. When the UNI/BIP pin is connected to  $V_{OUT}$  the part is configured for unipolar operation and the output will swing from REFLO to REFHI. When UNI/BIP is connected to REFHI the part is configured in bipolar mode and the output will swing from  $(2 \cdot \text{REFLO} - \text{REFHI})$  to REFHI and will be at REFLO at midscale. With REFLO = 0V the output swing is  $\pm \text{REFHI}$  in bipolar mode and 0V to REFHI in unipolar mode.

# TYPICAL APPLICATION



# PACKAGE DESCRIPTION

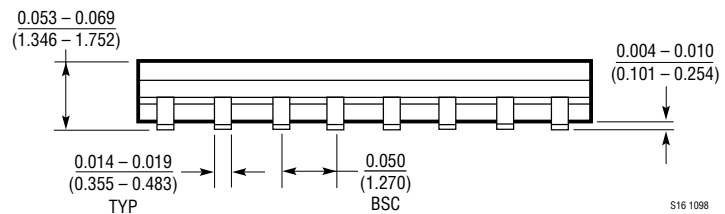
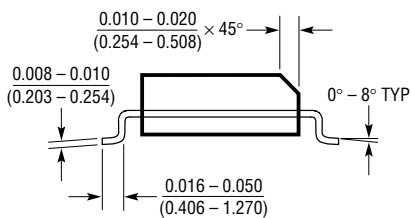
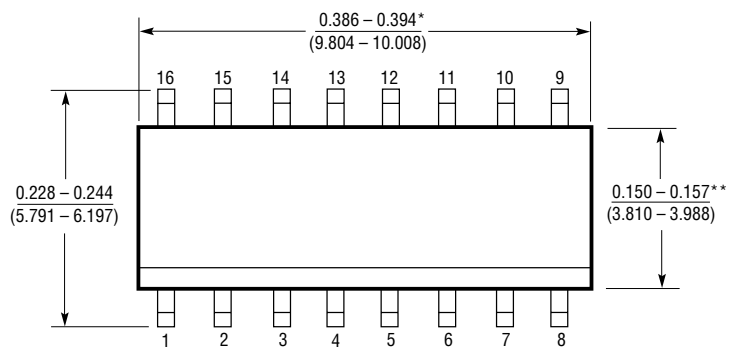
## N Package 16-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1098

## S Package 16-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

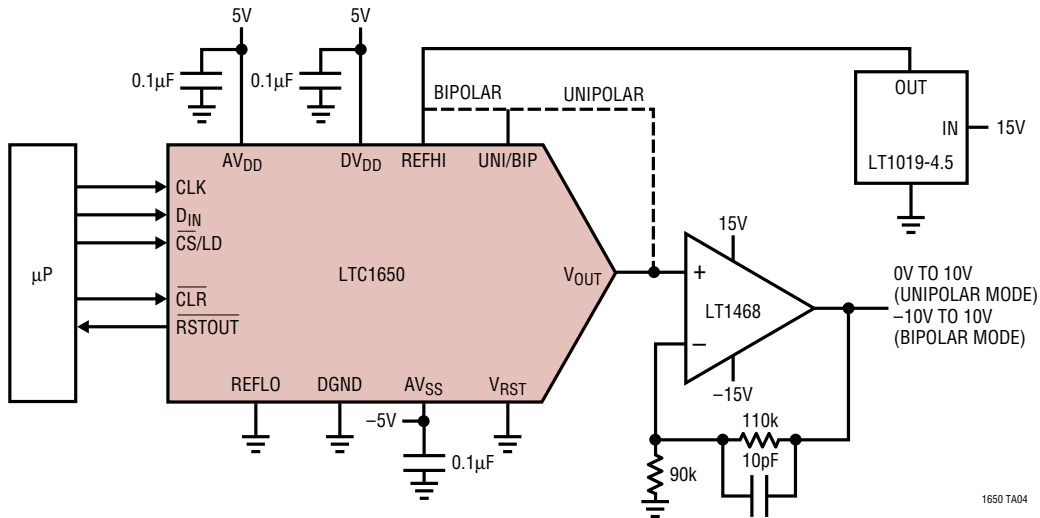


\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 1098

**TYPICAL APPLICATION**

**A ±10V Bipolar Output 16-Bit DAC**



1650 TA04

**RELATED PARTS**

PART NUMBER	DESCRIPTION	COMMENTS
<b>DACs</b>		
LTC1257	Single 12-Bit $V_{OUT}$ DAC, Full Scale: 2.048V, $V_{CC}$ : 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., $FS_{MAX} = 12V$	5V to 15V Single Supply, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit $V_{OUT}$ DACs in SO-8 Package	LTC1446: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1446L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1448	Dual 12-Bit $V_{OUT}$ DAC, $V_{CC}$ : 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to $V_{CC}$
LTC1450/LTC1450L	Single 12-Bit $V_{OUT}$ DACs with Parallel Interface	LTC1450: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1450L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1451/LTC1452/ LTC1453	Single 12-Bit $V_{OUT}$ DACs with Serial Interface	LTC1451: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1452: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to $2 \cdot V_{REF}$ LTC1453: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V	Low Power, Complete $V_{OUT}$ DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1458L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1595/LTC1596	16-Bit Serial I/O Multiplying $I_{OUT}$ DACs	$\pm 1$ LSB Max INL/DNL, Low Glitch, SO-8 Package (LTC1595), Clear Pin (LTC1596)
LTC1659	Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC in MSOP-8 Package, $V_{CC}$ : 2.7V TO 5.5V	Low Power Multiplying $V_{OUT}$ DAC in MSOP-8 Package. Output Swings from GND to REF. REF Input Can be Tied to $V_{CC}$
<b>References</b>		
LT1019	Precision Voltage Reference	Ultralow Drift 5ppm/ $^{\circ}C$ , Initial Accuracy: 0.05%
LT1634	Micropower Precision Reference	Low Drift 10ppm/ $^{\circ}C$ , Initial Accuracy: 0.05%