NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL9021A

...50mA Single LDO with Low I_Q, Low Noise and High PSRR LDO

The ISL9021 is a single LDO providing high performance low input voltage, high PSRR. It delivers guaranteed continuous 250mA load current and is stable with 1µF to 4.7µF of output capacitance (±30%) with an ESR range of 5mΩ to 400mΩ.

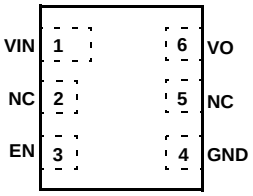
The input voltage range for the ISL9021 is between 1.5V to 5.5V and the output voltage comes in many fixed voltage options with ±1.8% accuracy over temperature, line and load ranges. Other output voltage within the range of 0.9V to 3.3V may be available upon request. The ISL9021 has typical PSRR of 75dB @ 10kHz and 50dB @ 1MHz.

The reverse current protection feature prevents current from flowing back to the power source when the output voltage is pulled higher than the input.

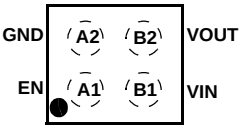
The ISL9021 is offered in tiny 4-bump 1.155mmx0.975mm WLCSP and 1.6mmx1.6mm 6 Ld µTDFN packages.

Pinouts

ISL9021
(6 LD 1.6x1.6 µTDFN)
TOP VIEW



ISL9021
(4 BALL 1.155x0.975 WLCSP)
TOP VIEW



Features

- High Performance LDO with 250mA guaranteed continuous output current
- Input Voltage Range: 1.5V to 5.5V
- Output Voltage Range: 0.9V to 3.3V
- High PSRR: 75dB @ 10kHz, 50dB @ 1MHz
- Low Quiescent Current: 35µA
- Dropout Voltage: <150mV @ 250mA
- Stable with 1µF to 4.7µF Output Capacitance (±30%) with an ESR range of 5mΩ to 400mΩ
- ±1.8% Output Accuracy Over-Temperature/Load/Line
- Soft-start Limits Input Current Surge During Enable
- Current Limit and Overheat Protection
- -40°C to +85°C Operating Temperature Range
- Available in 1.155mmx0.975mm 4-bump WLCSP Package and 1.6mmx1.6mm 6 Ld µTDFN
- Pb-free (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handhelds

Ordering Information

PART NUMBER	PART MARKING	V_O Voltage (Note 2)	TEMP RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PACKAGE DWG. #
ISL9021II1Z-T (Notes 1, 3)	0211	1.1	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021II2Z-T (Notes 1, 3)	0212	2.1	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021II3Z-T (Notes 1, 3)	0213	1.3	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021II4Z-T (Notes 1, 3)	0214	1.0	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIBZ-T (Notes 1, 3)	021B	1.5	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IICZ-T (Notes 1, 3)	021C	1.8	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIFZ-T (Notes 1, 3)	021F	2.5	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIGZ-T (Notes 1, 3)	021G	2.7	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIJZ-T (Notes 1, 3)	021J	2.8	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIKZ-T (Notes 1, 3)	021K	2.85	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIMZ-T (Notes 1, 3)	021M	3.0	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IINZ-T (Notes 1, 3)	021N	3.3	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIPZ-T (Notes 1, 3)	021P	1.85	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIRZ-T (Notes 1, 3)	021R	2.6	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IISZ-T (Notes 1, 3)	021S	1.6	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IITZ-T (Notes 1, 3)	021T	1.9	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIWZ-T (Notes 1, 3)	021W	1.2	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IIYZ-T (Notes 1, 3)	021Y	0.9	-40 to +85	4 Ball WLCSP	W2x2.4
ISL9021IRU1Z-T (Notes 1, 4)	S1	1.1	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRU2Z-T (Notes 1, 4)	S9	2.1	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRU3Z-T (Notes 1, 4)	S3	1.3	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRU4Z-T (Notes 1, 4)	S0	1.0	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUBZ-T (Notes 1, 4)	S4	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUCZ-T (Notes 1, 4)	S6	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUFZ-T (Notes 1, 4)	T0	2.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUGZ-T (Notes 1, 4)	T2	2.7	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUJZ-T (Notes 1, 4)	T3	2.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUKZ-T (Notes 1, 4)	T4	2.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUMZ-T (Notes 1, 4)	T5	3.0	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUNZ-T (Notes 1, 4)	R8	3.3	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUPZ-T (Notes 1, 4)	S7	1.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRURZ-T (Notes 1, 4)	T1	2.6	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUSZ-T (Notes 1, 4)	S5	1.6	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUTZ-T (Notes 1, 4)	S8	1.9	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUWZ-T (Notes 1, 4)	S2	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6
ISL9021IRUYZ-T (Notes 1, 4)	R9	0.9	-40 to +85	6 Ld µTDFN	L6.1.6x1.6

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . +6.5V
All Other Pins . . . . . -0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) . . . . . 1.5 to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
4 Ball WLCSP	135.64
6 Lead µTDFN	140

Junction Temperature Range . . . . . -40°C to +125°C
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications

T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 5.5V with a minimum V_{IN} of 1.5V; C_{IN} = 1µF; C_O = 1µF; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		1.5		5.5	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO+}	V_{IN} Rising		1.425	1.5	V
	V_{UVLO-}	V_{IN} Falling	1.3	1.375		V
Ground Current	I_{DD}	Output Enabled; I_O = 0; V_{IN} = 1.5V to 5.5V		35	50	µA
Shutdown Current	I_{DDS}	V_{IN} = 5.5V, EN = Low, I_O = 0		0.1	1.0	µA
Output Voltage Accuracy		V_{IN} = V_O + 0.5V to 5.5V, I_O = 1mA to 150mA, T_J = +25°C	-0.8		+0.8	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 1mA to 150mA, T_J = -40°C to +125°C	-1.8		+1.8	
Maximum Output Current	I_{MAX}	Continuous	250			mA
Internal Current Limit	I_{LIM}		260			mA
Dropout Voltage (Notes 6, 7)	V_{DO}	I_O = 250mA; V_O > 1.8V		150	250	mV
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis				20		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 6)		V_{IN} = 4.5V, V_O = 3.3V @ 1kHz		60		dB
		V_{IN} = 4.5V, V_O = 3.3V @ 10kHz		75		dB
		V_{IN} = 4.5V, V_O = 3.3V @ 1MHz		50		dB
Output Noise Voltage (Note 6)		V_{IN} = 4.2V, T_A = +25°C, BW = 10Hz to 100kHz, I_O = 10mA		8.5*V_O		μV_{RMS}
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the EN pin to when the output voltage reaches 95% of the V_O (nom)		250	600	µs
LDO Soft-start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V
EN LOGIC CHARACTERISTICS						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.1			V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA

NOTES:

6. Limits established by characterization and are not production tested.
7. Dropout voltage is measured as V_{IN} - V_O, when V_O is 4% lower than the value of V_O; when V_{IN} = V_O + 0.5V.

Typical Operating Performance

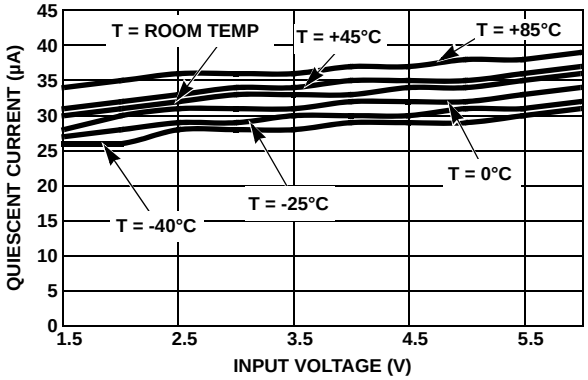


FIGURE 1. QUIESCENT CURRENT vs INPUT VOLTAGE (V_{OUT} = 0.9V)

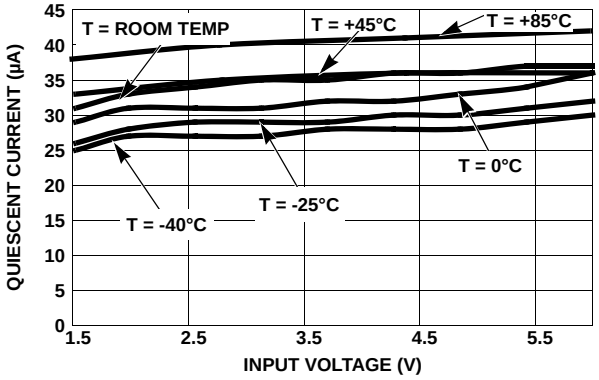


FIGURE 2. QUIESCENT CURRENT vs INPUT VOLTAGE (V_{OUT} = 1.85V)

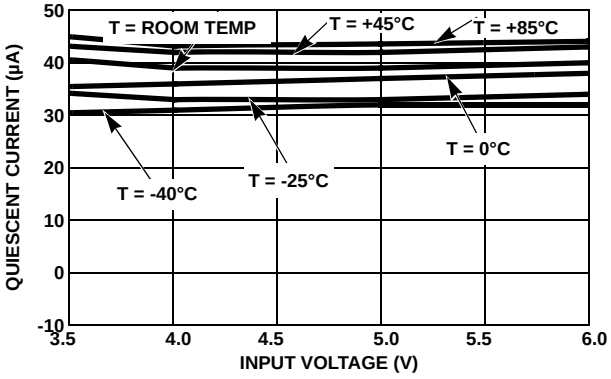


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V)

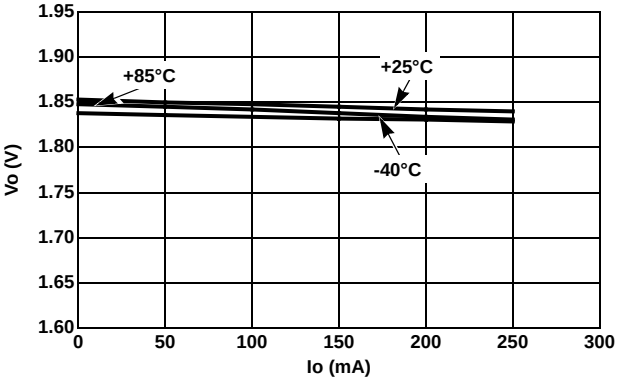


FIGURE 4. LOAD REGULATION vs TEMPERATURE (V_{OUT} = 1.85V)

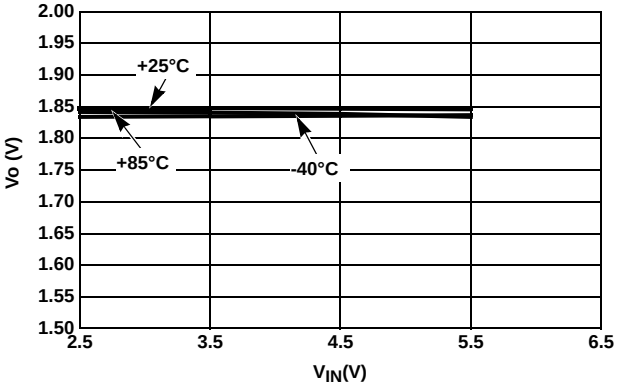


FIGURE 5. LINE REGULATION vs TEMPERATURE (V_{OUT} = 1.85V)

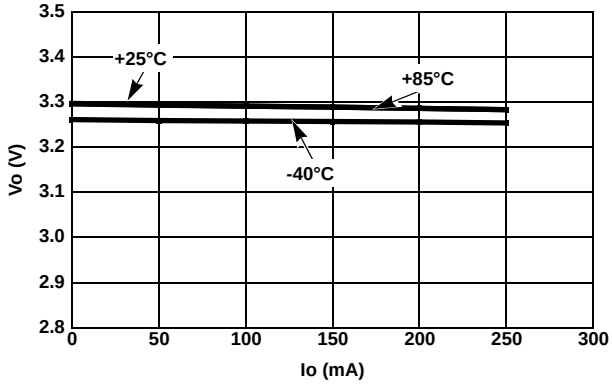


FIGURE 6. LOAD REGULATION vs TEMPERATURE (V_{OUT} = 3.3V)

Typical Operating Performance (Continued)

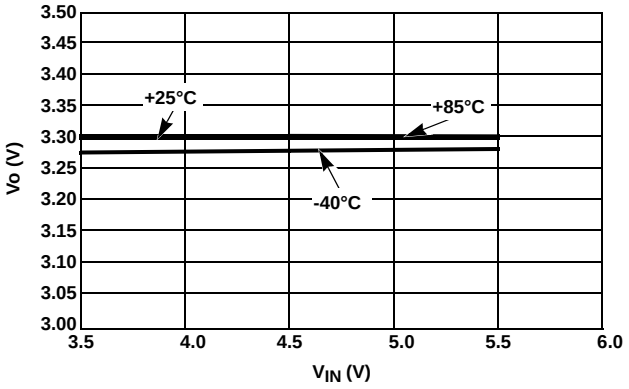


FIGURE 7. LINE REGULATION vs TEMPERATURE (V_{OUT} = 3.3V)

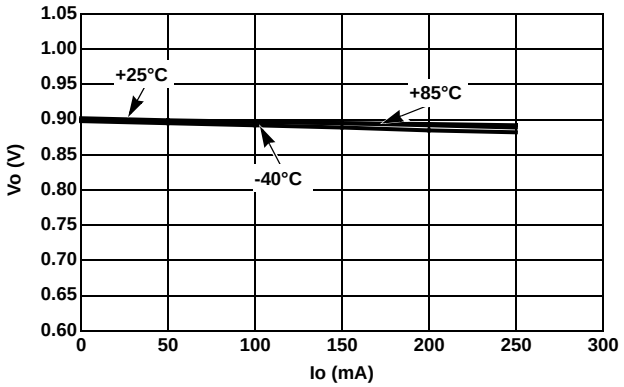


FIGURE 8. LOAD REGULATION vs TEMPERATURE (V_{OUT} = 0.9V)

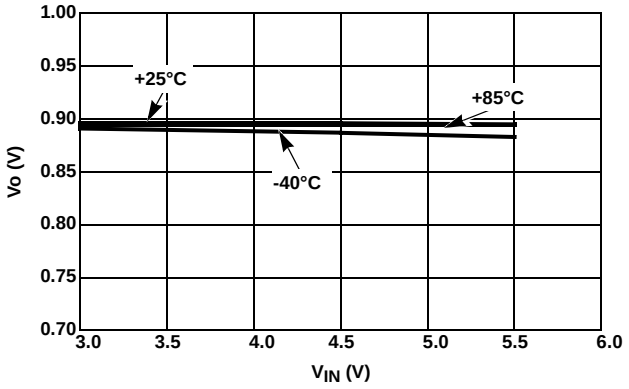


FIGURE 9. LINE REGULATION vs TEMPERATURE (V_{OUT} = 0.9V)

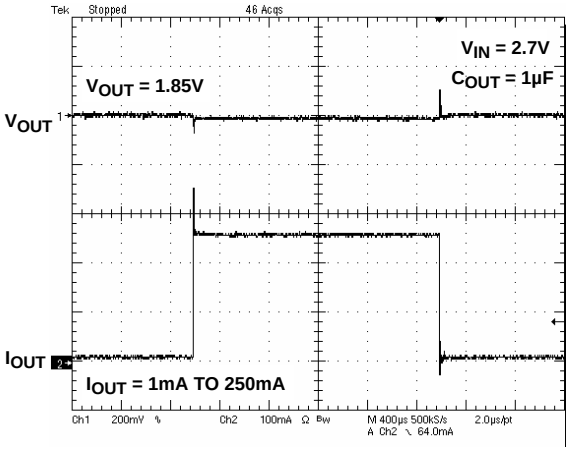


FIGURE 10. LOAD TRANSIENT RESPONSE

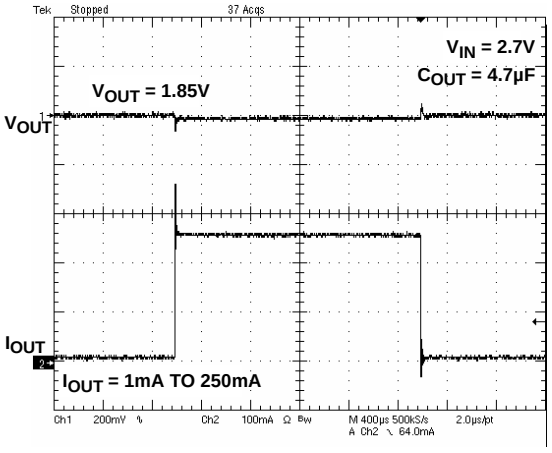


FIGURE 11. LOAD TRANSIENT RESPONSE

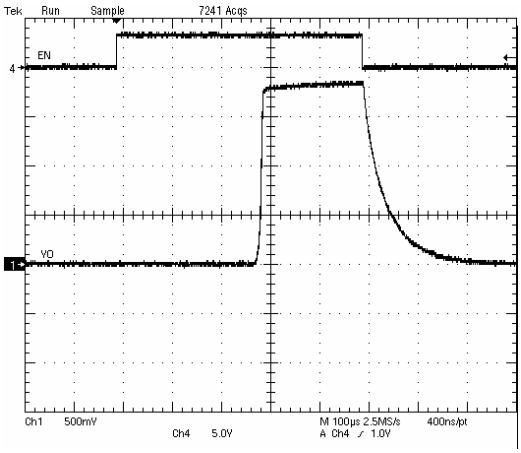


FIGURE 12. ENABLE FUNCTION (V_{IN} = 3.6V, V_{OUT} = 1.85V, C_{OUT} 1µF)

Typical Operating Performance (Continued)

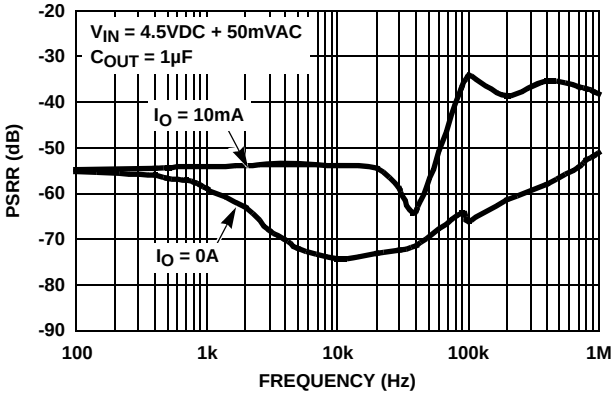
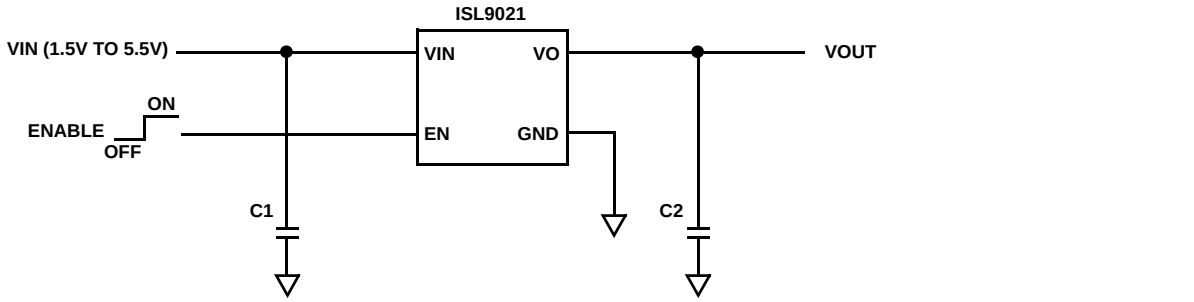


FIGURE 13. POWER SUPPLY REJECTION vs FREQUENCY

Pin Descriptions

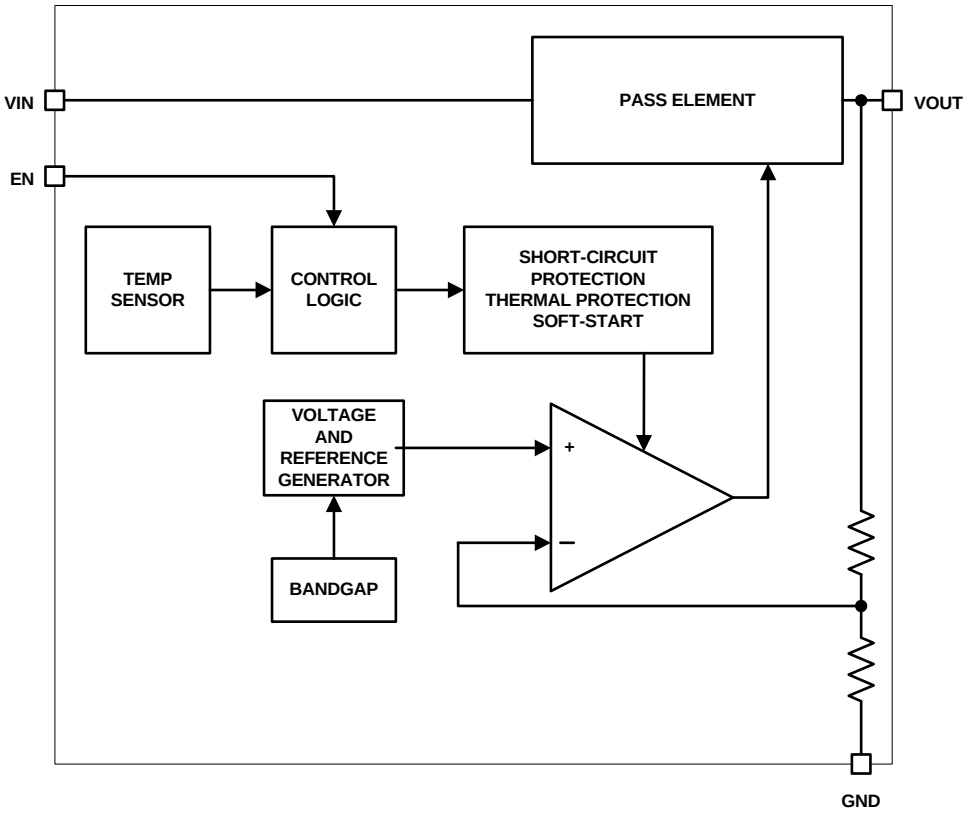
PIN NAME	DESCRIPTION
VIN	IC Supply/LDO Input. Connect a 1µF capacitor to GND.
GND	System ground pin.
EN	LDO Enable. When this signal goes high, the LDO is turned on.
VO	LDO Output. Connect a 1µF to 4.7µF capacitor to GND.
E-Pad	For µTDFN package option only. Connect it to the system ground.

Typical Application



C1, C2: 1µF X5R CERAMIC CAPACITOR

Block Diagram



Functional Description

The ISL9021 is a high performance low-dropout regulator (LDO) with 250mA sourcing capability. The extra low ground current makes this part a good choice for handheld product applications. The device also incorporates overcurrent, thermal shutdown, reverse current protections, and soft-start features.

Thermal shutdown protects the device against overheating. Soft-start limits the start-up input current surges. In some applications, the output voltage may be externally pulled higher than input, or the input voltage could be connected to ground, or connected to some voltage lower than the output side. The ISL9021 features reverse current protection; that can block the reverse current from output to input.

Enable Control

The ISL9021 has an enable pin. When EN is low, the IC is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1µA(typ). Driving this pin high will turn on the device.

LDO Protections

The ISL9021 offers several protection functions, making it ideal for use in battery-powered applications.The ISL9021 provides short-circuit protection by limiting the output current at current limit of 260mA(min). If the short circuit lasts long enough, the die temperature increases, and the over-temperature protection circuit will shut down the output. When the die temperature reaches about +145°C, thermal protection starts to work with output being loaded with at least 50mA. Once the die temperature drops to about +110°C, the LDO will resume operation beginning with a soft-start.

The ISL9021's reverse current protection is intended to block reverse conduction if output voltage is higher than input voltage.

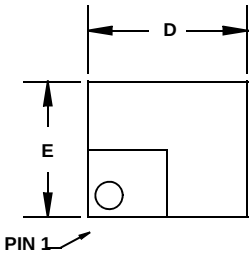
Input and Output Capacitors

The ISL9021 provides a linear regulator that has low quiescent current, fast transient response, and overall stable operation across the recommended operating conditions. A ceramic capacitor (X5R or X7R) with a capacitance of 1µF to 4.7µF with an ESR up to 400mΩ is suitable for the ISL9021 to maintain its output stability. The ground connection of the output capacitor should be routed directly to the GND pin of the device, and also placed close to the IC. Similarly for the input capacitor, usually a 1µF ceramic capacitor (X5R or 7R) is suitable for most cases, but if a large, fast rising load transient condition is expected, a higher value input capacitor may be necessary to achieve satisfactory performance.

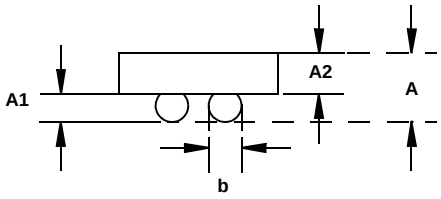
Board Layout Recommendations

A good PCB layout is an important step to achieve good performance. It is recommended to design the board with separate ground planes for input and output, and connect both ground planes at the GND pin of the IC. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance, and keep the parasitic inductance low. Usually the input/output capacitors should be placed as close to the IC as possible with a good ground connection.

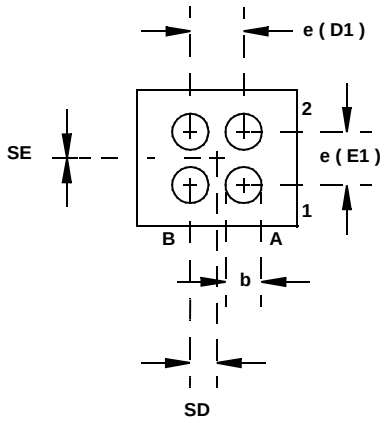
Wafer Level Chip Scale Package (WLCSP 0.4mm Ball Pitch)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

W2x2.4

2x2 ARRAY 4 BALL WAFER LEVEL CHIP SCALE PACKAGE

SYMBOL	MILLIMETERS
A	0.44 Min, 0.495 Nom, 0.55 Max
A1	0.190 ±0.030
A2	0.305 ±0.025
b	0.270 ±0.030
D	1.155 ±0.020
D1	0.400 BASIC
E	0.975 ±0.020
E1	0.400 BASIC
e	0.400 BASIC
SD	0.200 BASIC
SE	0.00 BASIC
NUMBER OF BUMPS: 4	

Rev. 2 6/08

NOTES:

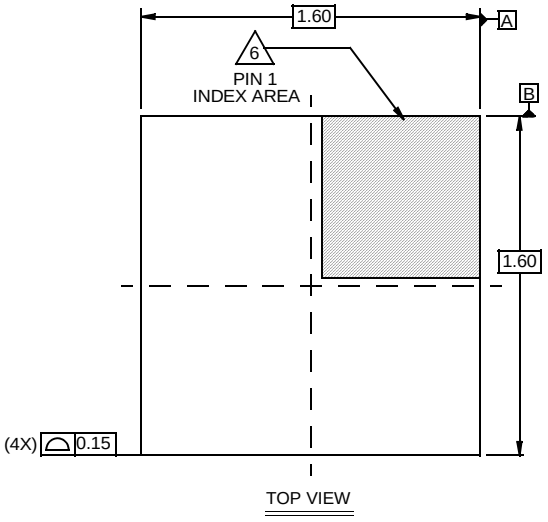
1. All dimensions are in millimeters.

Package Outline Drawing

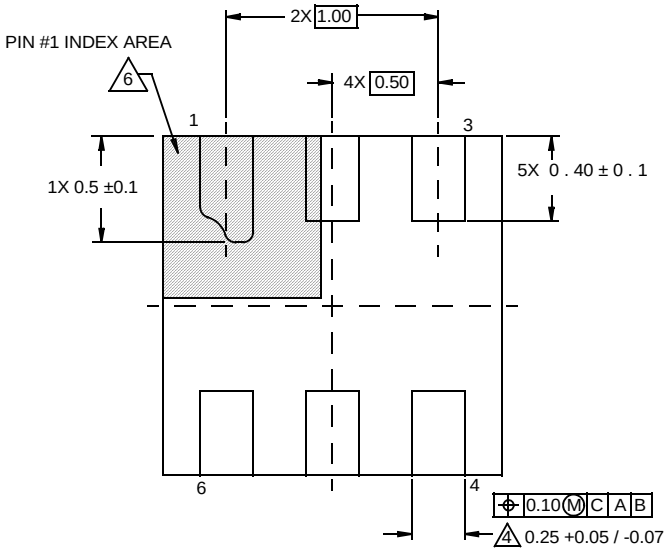
L6.1.6x1.6

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD COL PLASTIC PACKAGE (UTDFN COL)

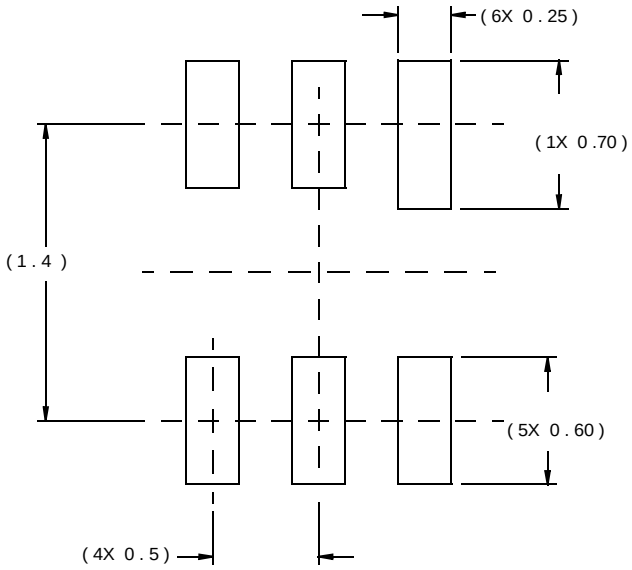
Rev 1, 11/07



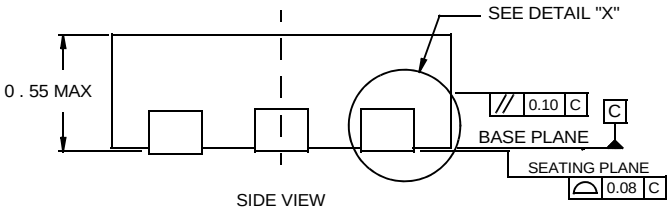
TOP VIEW



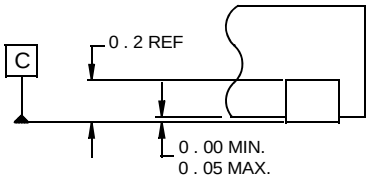
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.