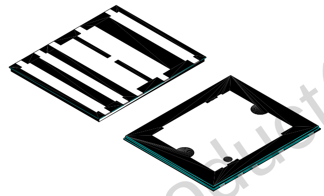
STK800

N-channel 30V - 0.006Ω - 20A - PolarPAK®
STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	$R_{DS(on)}$*Q_g	P_{TOT}
STK800	30V	<0.0078Ω	100.5nC*mΩ	5.2W

- Ultra low top and bottom junction to case thermal resistance
- Very low capacitances
- 100% Rg tested
- Fully encapsulated die
- 100% Matte tin finish (in compliance with the 2002/95/EC european directive)
- PolarPAK® is a trademark of VISHAY



PolarPAK®

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, moreover the double sides cooling package with ultra low junction to case thermal resistance allows to handle higher levels of current.

Figure 1. Internal schematic diagram

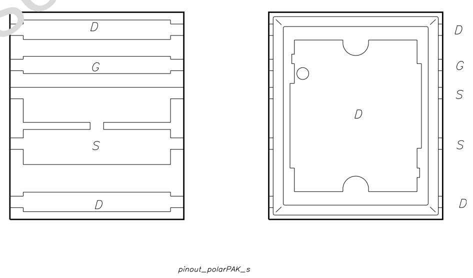


Table 1. Device summary

Order code	Marking	Package	Packaging
STK800	K800	PolarPAK®	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS} (1)	Gate-source voltage	± 16	V
V_{GS}(2)	Gate-source voltage	± 18	V
I_D (4)	Drain current (continuous) at T_C = 25°C	20	A
I_D	Drain current (continuous) at T_C = 100°C	12.5	A
I_{DM} (3)	Drain current (pulsed)	80	A
P_{TOT} (4)	Total dissipation at T_C = 25°C	5.2	W
	Derating factor	0.0416	W/°C
E_{AS} (5)	Single pulse avalanche energy	1	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time ≤15ms
3. Pulse width limited by package
4. When mounted on FR-4 board of 1inch^2, 2 oz Cu and ≤10sec
5. Starting T_J = 25°C, I_D = 10A, V_{DD} = 25V

Table 3. Thermal data

Symbol	Parameter	Typ.	Max.	Unit
Rthj-amb(1)	Thermal resistance junction-amb	20	24	°C/W
Rthj-c(2)	Thermal resistance junction-case (top drain)	1	1.2	°C/W
Rthj-c(3)	Thermal resistance junction-case (source)	2.8	3.4	°C/W

1. When mounted on FR-4 board of 1inch^2, 2 oz Cu and ≤10sec
2. Steady state
3. Measured at source pin when the device is mounted on FR-4 board in steady state

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 10A V_{GS}= 4.5V, I_D= 10A		0.006 0.0075	0.0078 0.0098	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		1380 450 75		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15V, I_D = 20A V_{GS} =4.5V *(see Figure 16)*		13.4 3.4 4.5		nC nC nC
Q_{gs1} Q_{gs2}	Pre V_{th} gate-to-source charge Post V_{th} gate-to-source charge	V_{DD}=15V, I_D = 12A V_{GS} =4.5V *(see Figure 21)*		1 2.4		nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain		1		Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 15V, I_D= 10A, R_G=4.7Ω, V_{GS}=4.5V *(see Figure 15)*		15 50		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=15V, I_D= 10A, R_G=4.7Ω, V_{GS}=4.5V *(see Figure 15)*		45 15		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				20 80	A A
V_{SD}(2)	Forward on Voltage	I_{SD}= 20A, V_{GS}=0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 20A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C *(see Figure 20)*		32 28.8 1.8		ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

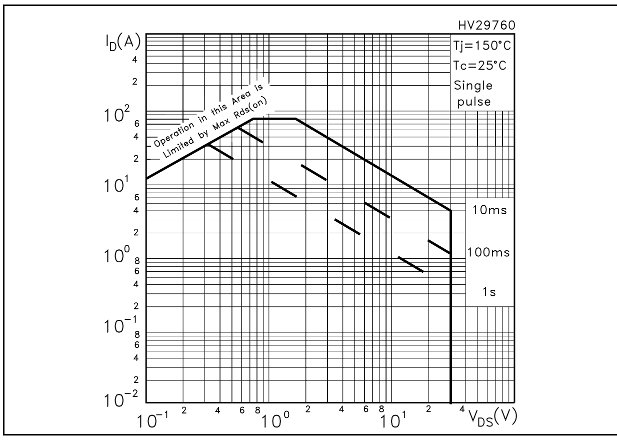


Figure 3. Thermal impedance

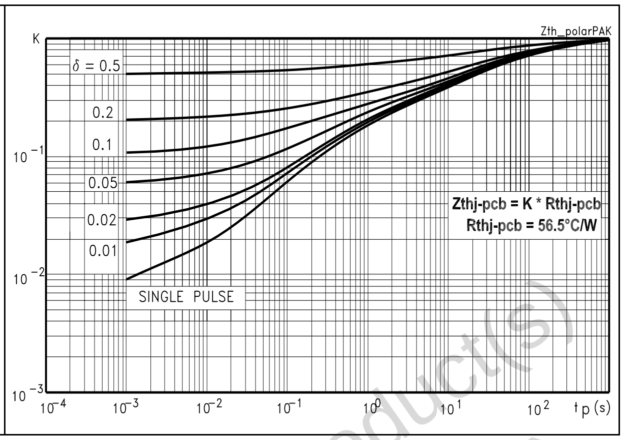


Figure 4. Output characteristics

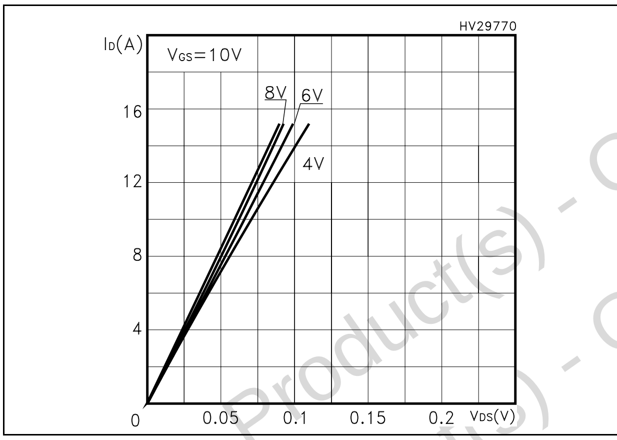


Figure 5. Transfer characteristics

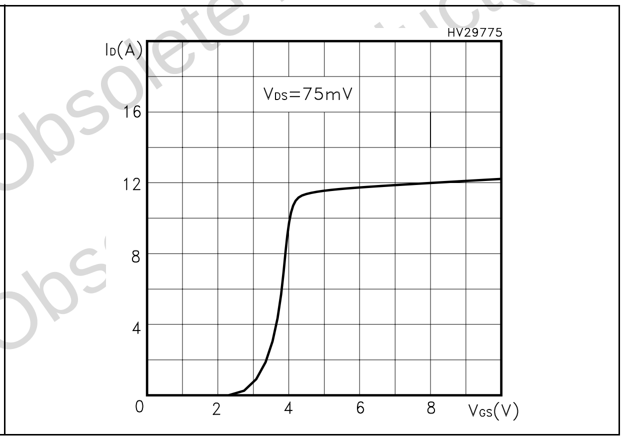


Figure 6. Transconductance

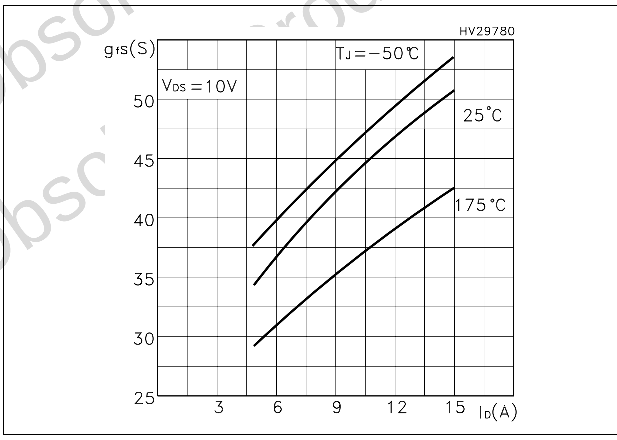


Figure 7. Static drain-source on resistance

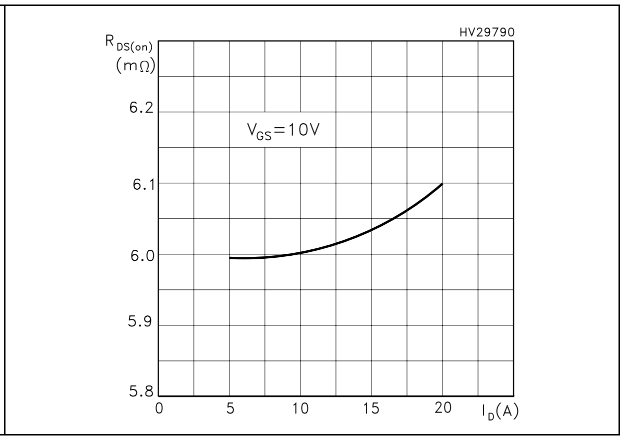


Figure 8. Gate charge vs gate-source voltage

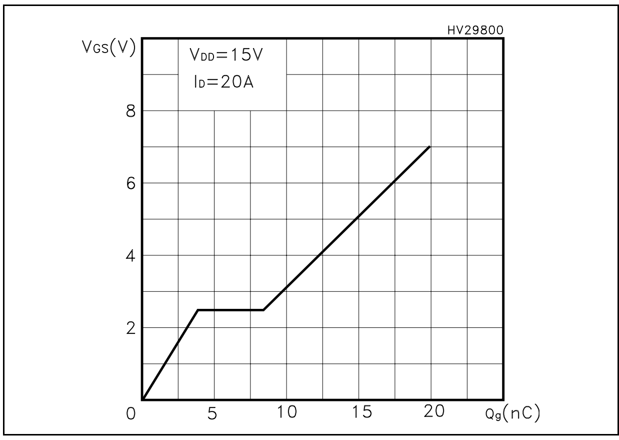


Figure 9. Capacitance variations

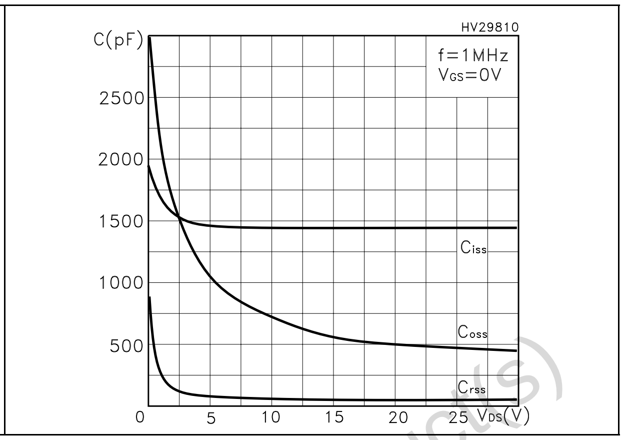


Figure 10. Normalized gate threshold voltage vs temperature

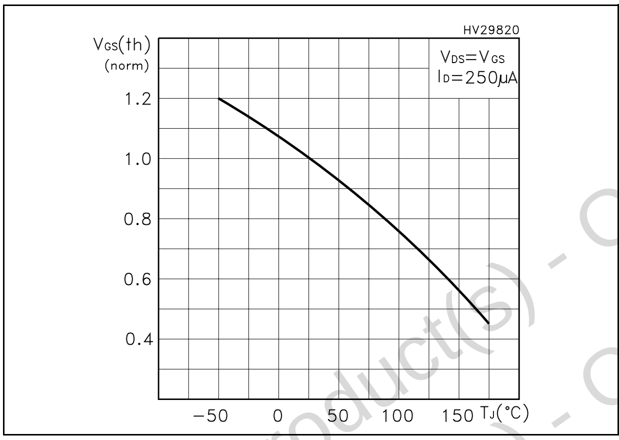


Figure 11. Normalized on resistance vs temperature

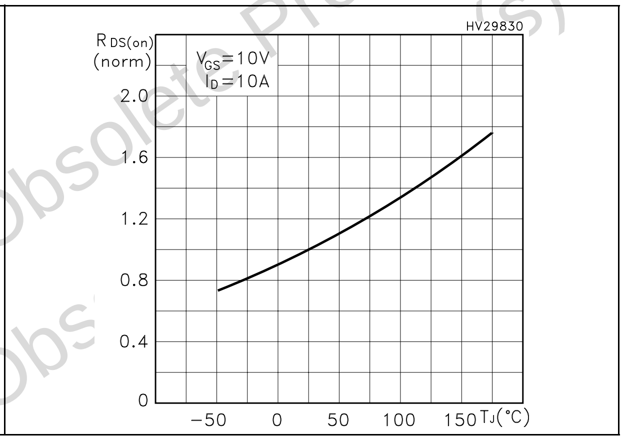


Figure 12. Source-drain diode forward characteristics

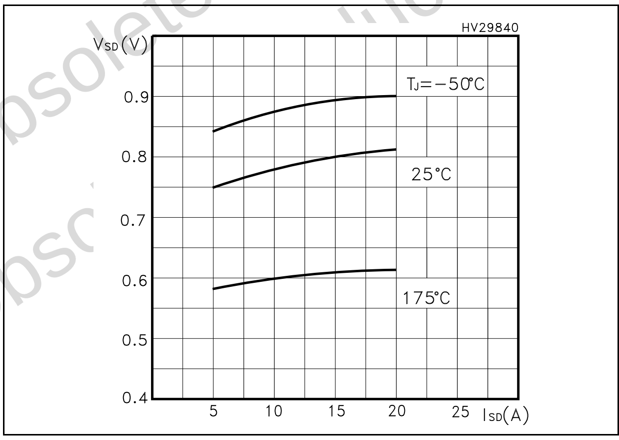


Figure 13. Normalized B_{VDSS} vs temperature

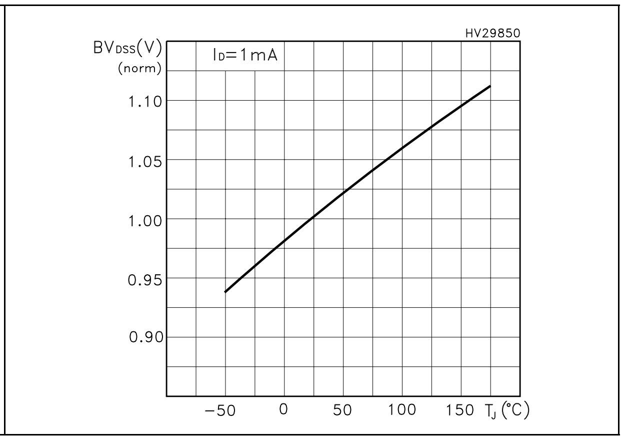
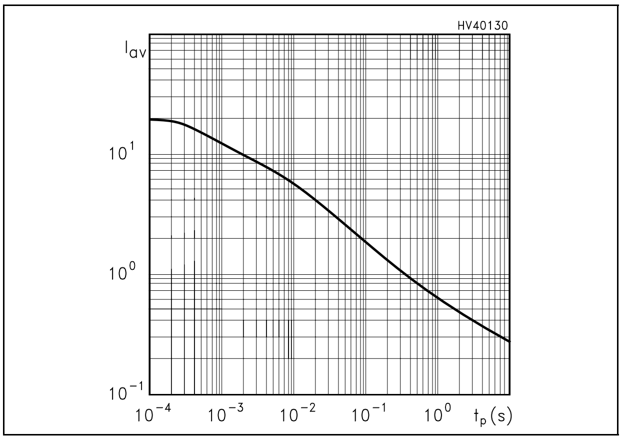


Figure 14. Allowable I_{AV} vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*B_{VDSS} *I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} *t_{AV}$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

3 Test circuit

Figure 15. Switching times test circuit for resistive load

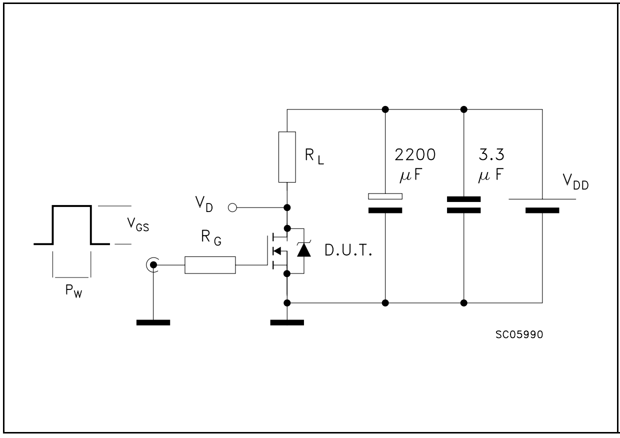


Figure 16. Gate charge test circuit

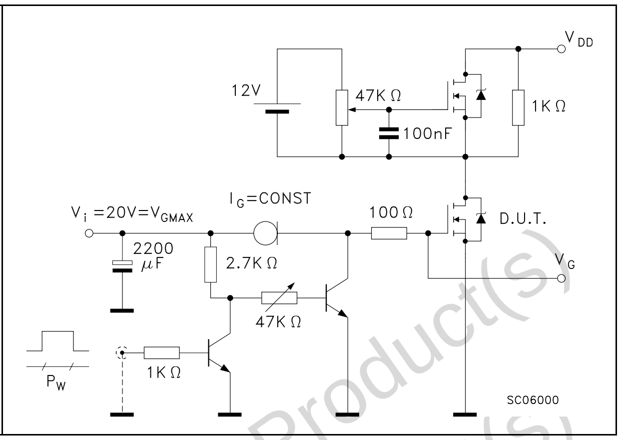


Figure 17. Test circuit for inductive load switching and diode recovery times

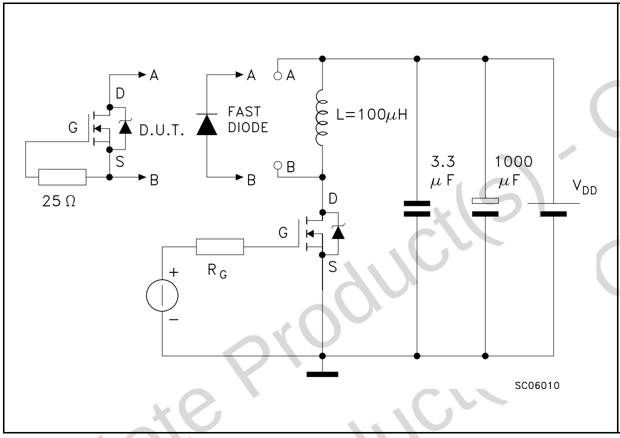


Figure 18. Unclamped inductive load test circuit

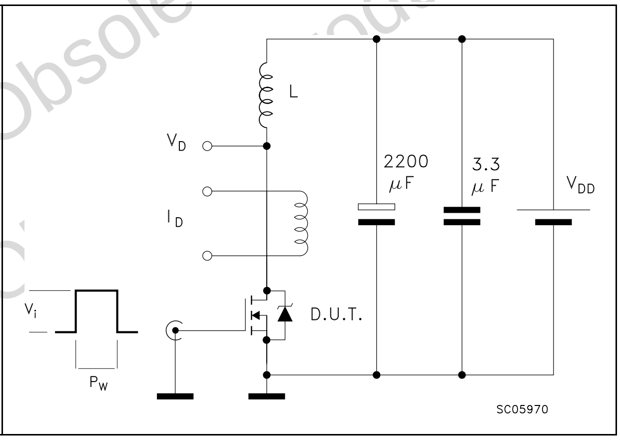


Figure 19. Unclamped inductive waveform

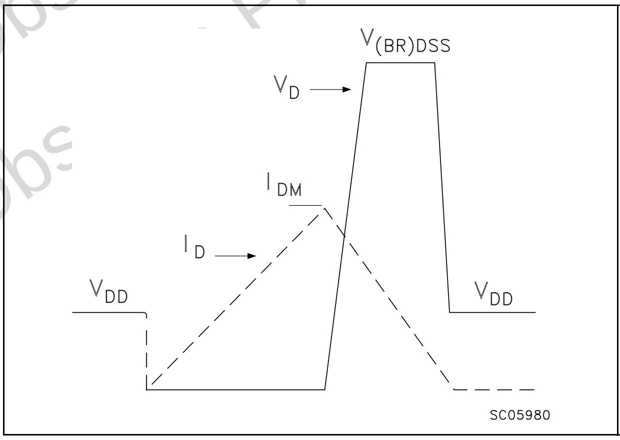


Figure 20. Switching time waveform

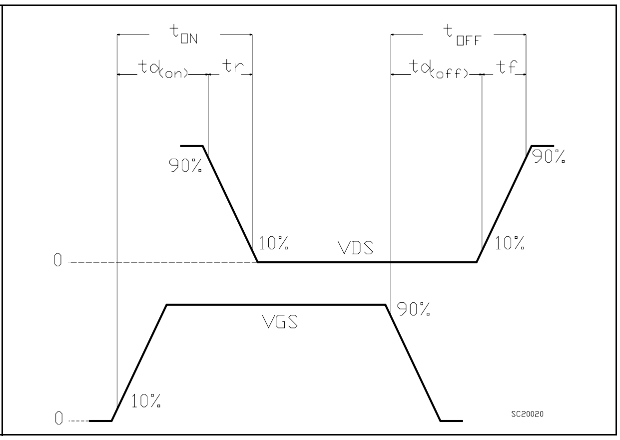
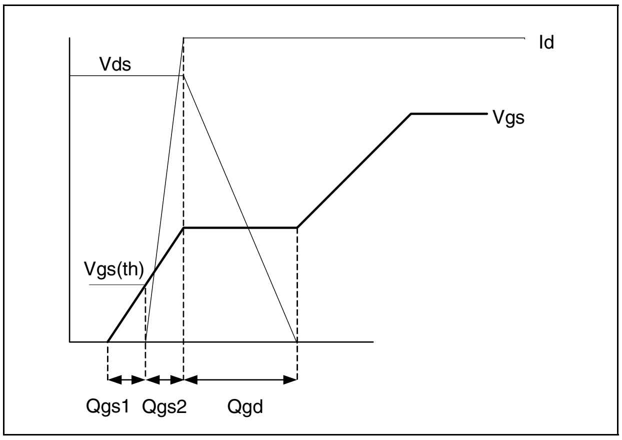


Figure 21. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

Table 8. PolarPAK® (option "S") mechanical data

Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.018		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.018		0.022
I1	1.92	1.97	2.02	0.075	0.077	0.079
J1	0.38	0.43	0.48	0.014	0.016	0.018
K1	4.22	4.37	4.52	0.166	0.172	0.178
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.047		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Figure 22. PolarPAK® (option "S") drawings

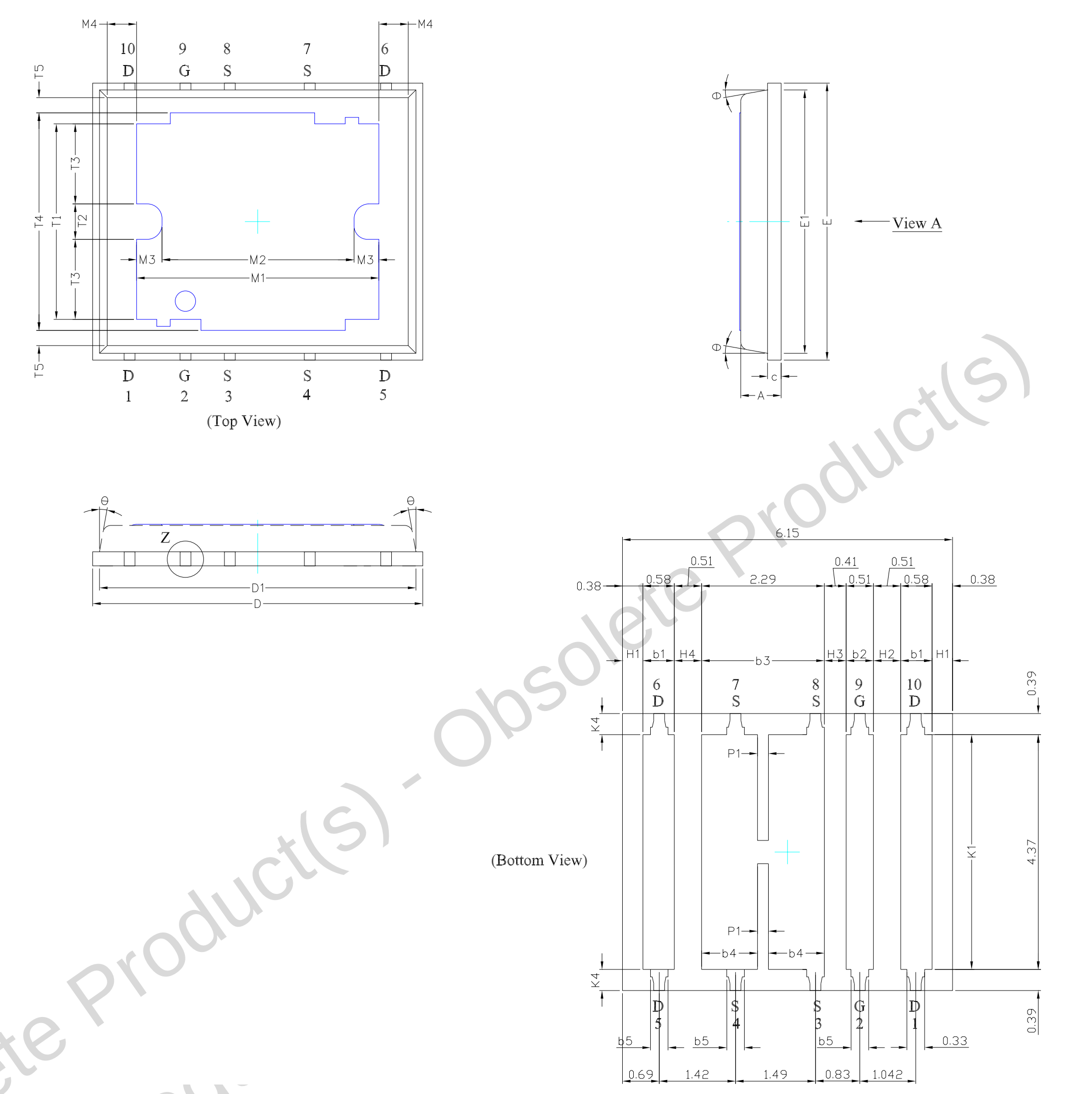
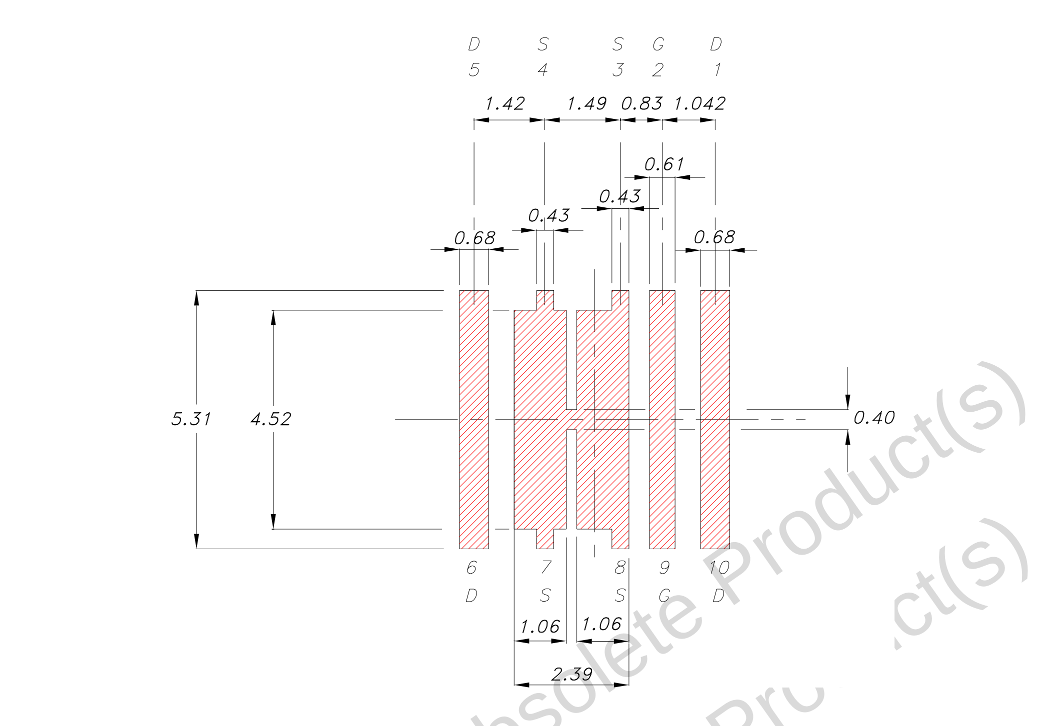


Figure 23. Recommended PAD layout



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Nov-2005	1	First version
02-Feb-2006	2	Complete version
21-Mar-2006	3	The document has been reformatted
25-May-2006	4	New note on page 1
14-Nov-2006	5	Modified *: Features*
14-May-2007	6	New data on *Table 5* and new *Figure 21*
11-Jun-2007	7	Updated *Figure 2*, *Figure 3*
03-Sep-2007	8	Updated mechancal data
05-Oct-2007	9	Inserted new *Figure 23: Recommended PAD layout*