

1A, Low-Voltage, Low Quiescent Current LDO Regulator

Features:

- 1A Output Current Capability
- Input Operating Voltage Range: 2.3V to 6.0V
- Adjustable Output Voltage Range: 0.8V to 5.0V
- Standard Fixed Output Voltages:
 - 0.8V, 1.2V, 1.8V, 2.5V, 3.0V, 3.3V, 5.0V
- Low Dropout Voltage: 220 mV typical at 1A
- Typical Output Voltage Tolerance: $\pm 0.5\%$
- Stable with 1.0 μF Ceramic Output Capacitor
- Fast Response to Load Transients
- Low Supply Current: 140 μA (typical)
- Low Shutdown Supply Current: 0.1 μA (typical)
- Adjustable Delay on Power Good Output
- Short-Circuit Current Limiting and Overtemperature Protection
- 3x3 DFN-8 and SOIC-8 Package Options

Applications:

- High-Speed Driver Chipset Power
- Networking Backplane Cards
- Notebook Computers
- Network Interface Cards
- Palmtop Computers
- 2.5V to 1.XV Regulators

Description:

The MCP1726 is a 1A Low Dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. The MCP1726 comes in fixed or adjustable output voltage versions, with an output voltage range of 0.8V to 5.0V. The 1A output current capability and low output voltage capability make the MCP1726 a good choice for new sub-1.8V output voltage LDO applications that have high current demands.

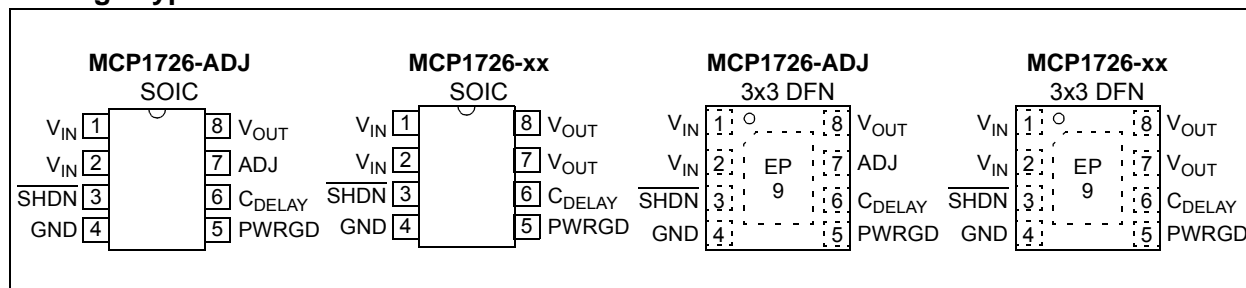
The MCP1726 is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 μF of output capacitance is needed to stabilize the LDO.

Using CMOS construction, the quiescent current consumed by the MCP1726 is typically less than 140 μA over the entire input voltage range, making it attractive for portable computing applications that demand high output current. When the MCP1726 is shut down, the quiescent current is reduced to less than 0.1 μA .

The scaled-down output voltage is internally monitored and a Power Good (PWRGD) output is provided when the output is within 92% of regulation (typical). An external capacitor can be used on the C_{DELAY} pin to adjust the delay from 1 ms to 300 ms.

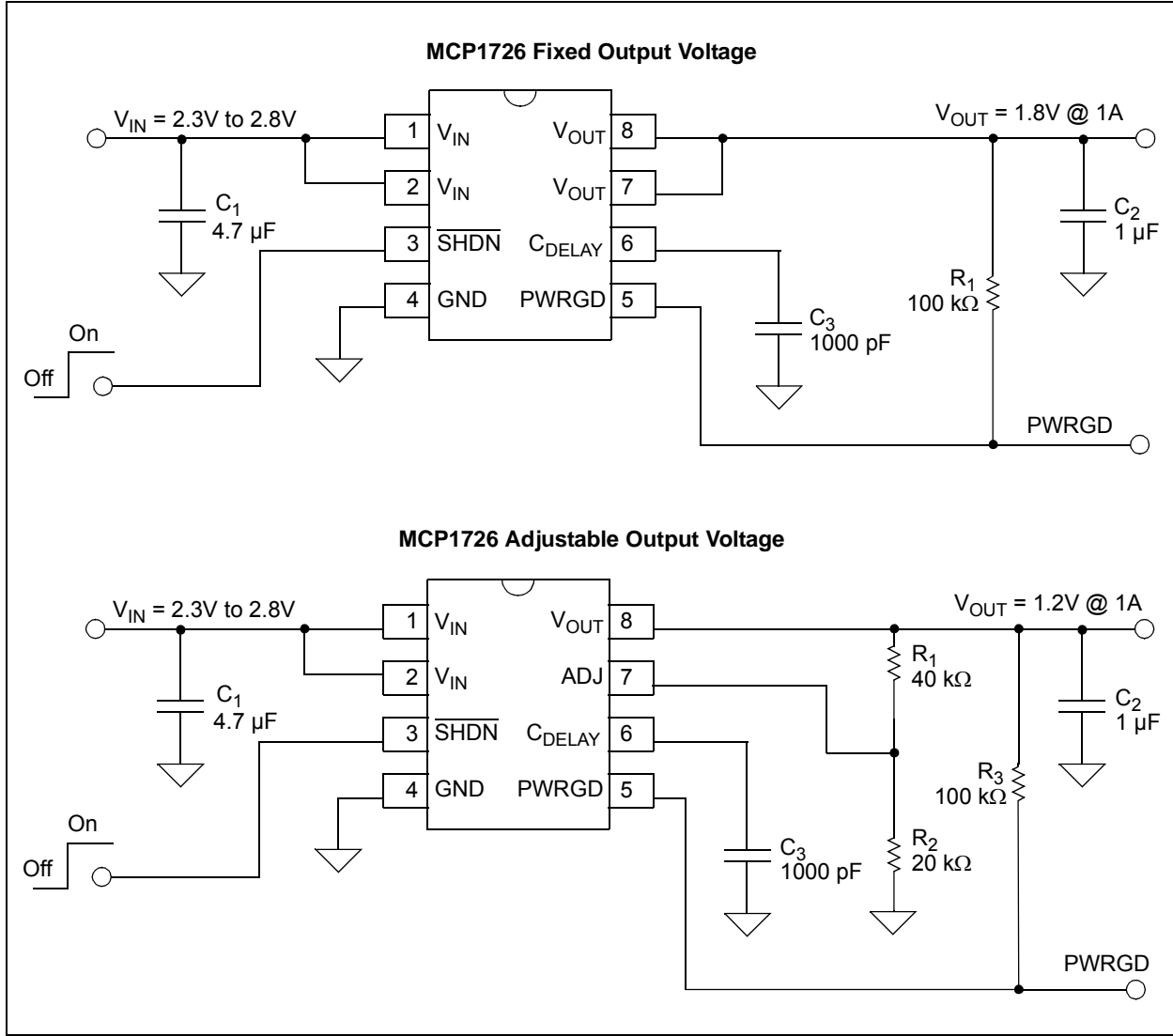
The overtemperature and short-circuit current limiting provide additional protection for the LDO during system fault conditions.

Package Types

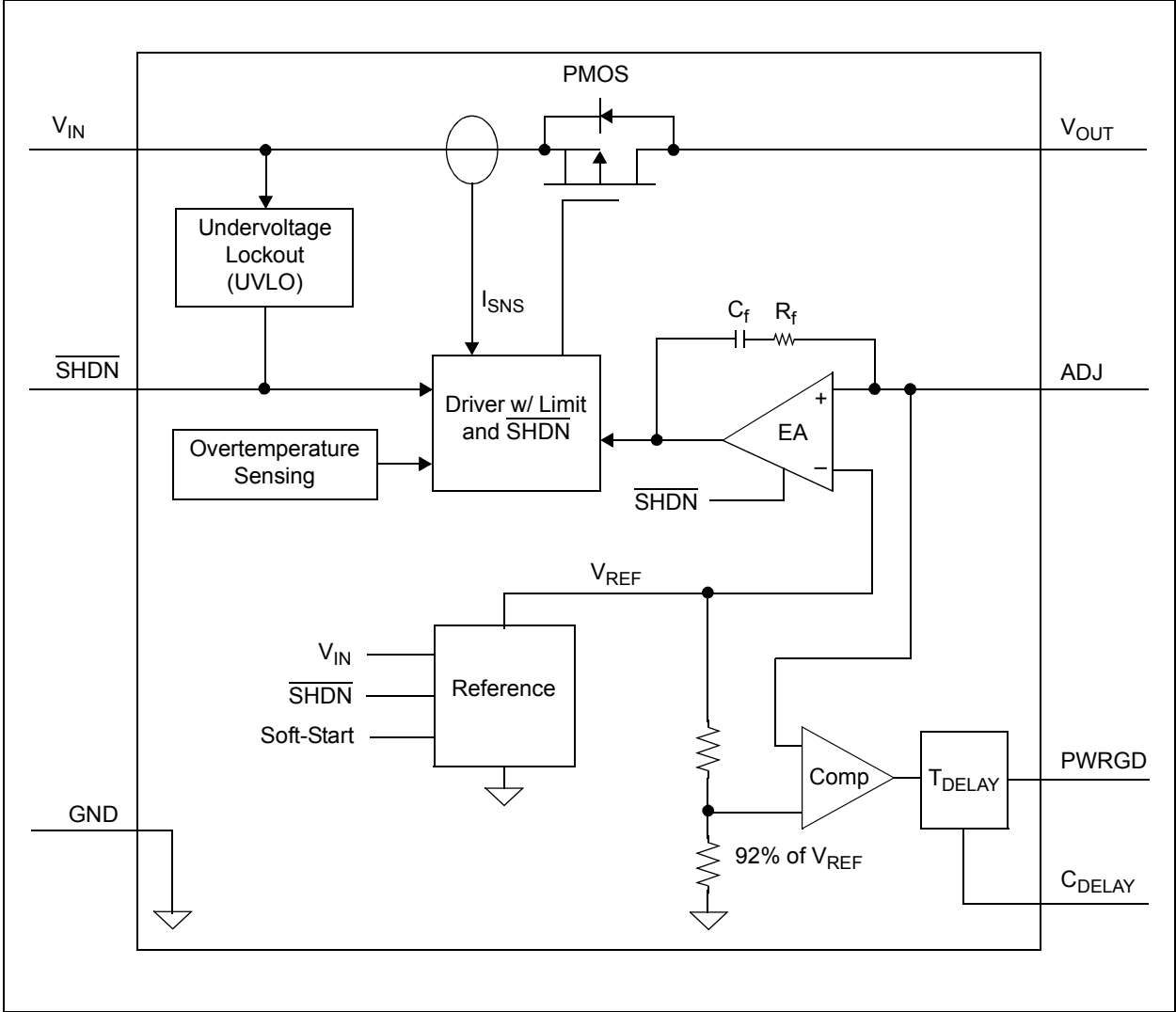


MCP1726

Typical Application



Functional Block Diagram



MCP1726

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|---|-----------------------------|
| V_{IN} | 6.5V |
| Maximum Voltage on Any Pin ..(GND – 0.3V) to (V_{DD} + 0.3)V | |
| Maximum Junction Temperature, T_J | +150°C |
| Maximum Power Dissipation | Internally-Limited (Note 6) |
| Storage Temperature..... | -65°C to +150°C |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

| Electrical Specifications: Unless otherwise noted, $V_{IN} = (V_R + 0.5V)$ or 2.3V, whichever is greater, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7$ μ F (X7R Ceramic), $T_A = +25^\circ$ C. Boldface type applies for junction temperatures, T_J (Note 7), of -40°C to +125°C . | | | | | | |
|---|---|---------------------------------|-----------------|---------------------------------|---------|---|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Input Operating Voltage | V_{IN} | 2.3 | | 6.0 | V | Note 1 |
| Input Quiescent Current | I_q | — | 140 | 220 | μ A | $I_L = 0$ mA, $V_{IN} = V_R + 0.5V$, $V_{OUT} = 0.8V$ to 5.0V |
| Input Quiescent Current for SHDN Mode | I_{SHDN} | — | 0.1 | 3 | μ A | SHDN = GND |
| Maximum Output Current | I_{OUT} | 1 | — | — | A | $V_{IN} = 2.3V$ to 6.0V (Note 1) |
| Line Regulation | $\frac{\Delta V_{OUT}}{(V_{OUT} \times \Delta V_{IN})}$ | — | 0.05 | 0.3 | %/V | $(V_R + 0.5)V \leq V_{IN} \leq 6V$ |
| Load Regulation | $\Delta V_{OUT}/V_{OUT}$ | -1.5 | ± 0.5 | 1.5 | % | $I_{OUT} = 1$ mA to 1A, $V_{IN} = (V_R + 0.6)V$ (Note 4) |
| Output Short-Circuit Current | I_{OUT_SC} | — | 1.7 | — | A | $V_{IN} = (V_R + 0.5)V$, $R_{LOAD} < 0.1\Omega$, Peak Current |
| Adjust Pin Characteristics | | | | | | |
| Adjust Pin Reference Voltage | V_{ADJ} | 0.402 | 0.410 | 0.418 | V | $V_{IN} = 2.3V$ to $V_{IN} = 6.0V$, $I_{OUT} = 1$ mA |
| Adjust Pin Leakage Current | I_{ADJ} | -10 | ± 0.01 | +10 | nA | $V_{IN} = 6.0V$, $V_{ADJ} = 0V$ to 6V |
| Adjust Temperature Coefficient | TCV_{OUT} | — | 40 | — | ppm/°C | Note 3 |
| Fixed-Output Characteristics | | | | | | |
| Voltage Regulation | V_{OUT} | $V_R - 2.5\%$ | $V_R \pm 0.5\%$ | $V_R + 2.5\%$ | V | Note 2 |
| Dropout Characteristics | | | | | | |
| Dropout Voltage | $V_{IN} - V_{OUT}$ | — | 220 | 500 | mV | $I_{OUT} = 1A$, $V_{IN(MIN)} = 2.3V$ (Note 5) |

- Note 1:** The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.
- Note 2:** V_R is the nominal regulator output voltage for the fixed cases. $V_R = 1.2V, 1.8V$, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} \times ((R_1/R_2) + 1)$. See Figure 4-1.
- Note 3:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \times 10^6 / (V_R \times \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.
- Note 4:** Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
- Note 5:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 0.5V$.
- Note 6:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 125°C can impact device reliability.
- Note 7:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

DC CHARACTERISTICS (CONTINUED)

| Electrical Specifications: Unless otherwise noted, $V_{IN} = (V_R + 0.5V)$ or 2.3V, whichever is greater, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 4.7\text{ }\mu\text{F}$ (X7R Ceramic), $T_A = +25^\circ\text{C}$. Boldface type applies for junction temperatures, T_J (Note 7), of -40°C to $+125^\circ\text{C}$. | | | | | | |
|---|-------------------------|-------------|-------------|-------------|--------------------------------|---|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Power Good Characteristics | | | | | | |
| Input Voltage Operating Range for Valid PWRGD | V_{PWRGD_VIN} | 1.0 | — | 6.0 | V | $T_A = +25^\circ\text{C}$ |
| | | 1.2 | — | 6.0 | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ |
| | | | | | | $I_{SINK} = 100\text{ }\mu\text{A}$ |
| PWRGD Threshold Voltage (Referenced to V_{OUT}) | PWRGD_THF | 88 | 92 | 96 | % | $V_{OUT} < 2.5V$, Falling Edge |
| | | 89 | 92 | 95 | % | $V_{OUT} > 2.5V$, Falling Edge |
| | PWRGD_THR | 89 | 94 | 98 | % | $V_{OUT} < 2.5V$, Rising Edge |
| | | 90 | 93 | 96 | % | $V_{OUT} > 2.5V$, Rising Edge |
| PWRGD Output Voltage Low | V_{PWRGD_L} | — | 0.2 | 0.4 | V | $I_{PWRGD\ SINK} = 1.2\text{ mA}$ |
| PWRGD Leakage | P_{PWRGD_LK} | — | 0.1 | — | μA | $V_{PWRGD} = V_{IN} = 6.0V$ |
| PWRGD Time Delay | T_{PG} | — | 200 | — | μs | $C_{DELAY} = \text{OPEN}$ |
| | | 10 | 30 | 55 | ms | $C_{DELAY} = 0.01\text{ }\mu\text{F}$ |
| | | — | 300 | — | ms | $C_{DELAY} = 0.1\text{ }\mu\text{F}$ |
| Detect Threshold to PWRGD Active Time Delay | $T_{VDET-PWRGD}$ | — | 170 | — | μs | |
| Shutdown Input | | | | | | |
| Logic-High Input | $V_{SHDN-HIGH}$ | 45 | — | — | $\%V_{IN}$ | $V_{IN} = 2.3V$ to $6.0V$ |
| Logic-Low Input | $V_{SHDN-LOW}$ | — | — | 15 | $\%V_{IN}$ | $V_{IN} = 2.3V$ to $6.0V$ |
| SHDN Input Leakage Current | \overline{SHDN}_{ILK} | -0.1 | ± 0.001 | +0.1 | μA | $V_{IN} = 6V$, $\overline{SHDN} = V_{IN}$, $SHDN = GND$ |
| AC Performance | | | | | | |
| Output Delay from \overline{SHDN} | T_{OR} | — | 100 | — | μs | $\overline{SHDN} = GND$ to V_{IN} , $V_{OUT} = GND$ to $95\% V_R$ |
| Output Noise | e_N | — | 2.0 | — | $\mu\text{V}/\sqrt{\text{Hz}}$ | $I_{OUT} = 200\text{ mA}$, $f = 1\text{ kHz}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (X7R Ceramic), $V_{OUT} = 2.5V$ |
| Power Supply Ripple Rejection Ratio | PSRR | — | 54 | — | dB | $f = 100\text{ Hz}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 100\text{ mA}$, $V_{INAC} = 30\text{ mV pk-pk}$, $C_{IN} = 0\text{ }\mu\text{F}$ |
| Thermal Shutdown Temperature | T_{SD} | — | 150 | — | $^\circ\text{C}$ | $I_{OUT} = 100\text{ }\mu\text{A}$, $V_{OUT} = 1.8V$, $V_{IN} = 2.8V$ |
| Thermal Shutdown Hysteresis | ΔT_{SD} | — | 10 | — | $^\circ\text{C}$ | $I_{OUT} = 100\text{ }\mu\text{A}$, $V_{OUT} = 1.8V$, $V_{IN} = 2.8V$ |

- Note 1:** The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.
- Note 2:** V_R is the nominal regulator output voltage for the fixed cases. $V_R = 1.2V$, $1.8V$, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} \times ((R_1/R_2) + 1)$. See Figure 4-1.
- Note 3:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \times 10^6 / (V_R \times \Delta\text{Temperature})$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.
- Note 4:** Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
- Note 5:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 0.5V$.
- Note 6:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 125°C can impact device reliability.
- Note 7:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

MCP1726

TEMPERATURE SPECIFICATIONS

| Electrical Specifications: Unless otherwise indicated, all limits apply for $V_{IN} = 2.3V$ to $6.0V$. | | | | | | |
|--|---------------|------|------|------|-------|---|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Temperature Ranges | | | | | | |
| Operating Junction Temperature Range | T_J | -40 | — | +125 | °C | Steady State |
| Maximum Junction Temperature | T_J | — | — | +150 | °C | Transient |
| Storage Temperature Range | T_A | -65 | — | +150 | °C | |
| Thermal Package Resistances | | | | | | |
| Thermal Resistance, 8L 3x3 DFN | θ_{JA} | — | 64 | — | °C/W | 4-Layer JC51-5 Standard Board with Vias |
| | θ_{JC} | — | 12 | — | | |
| Thermal Resistance, 8L SOIC | θ_{JA} | — | 163 | — | °C/W | 4-Layer JC51-7 Standard Board |
| | θ_{JC} | — | 42 | — | | |

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

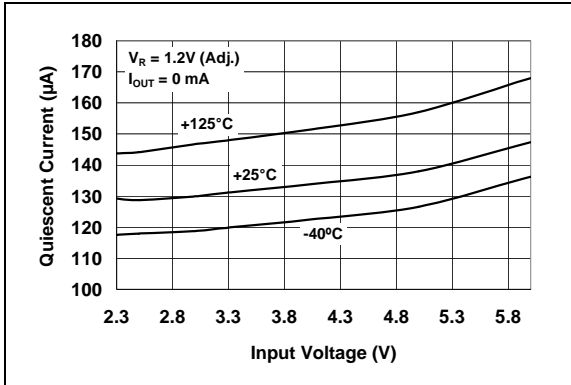


FIGURE 2-1: Quiescent Current vs. Input Voltage (1.2V Adjustable).

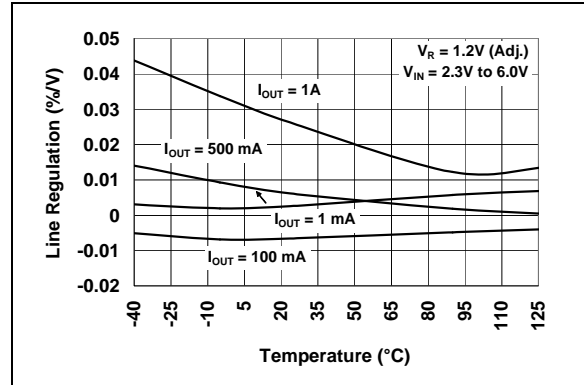


FIGURE 2-4: Line Regulation vs. Temperature (1.2V Adjustable).

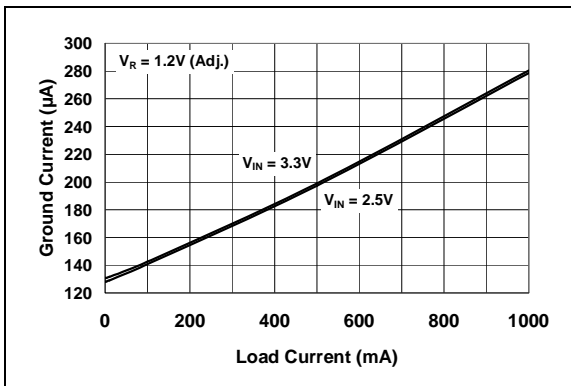


FIGURE 2-2: Ground Current vs. Load Current (1.2V Adjustable).

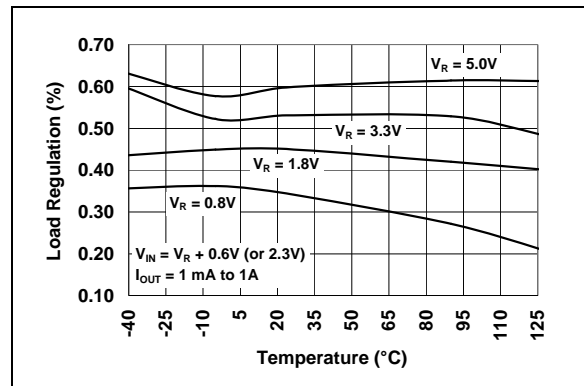


FIGURE 2-5: Load Regulation vs. Temperature.

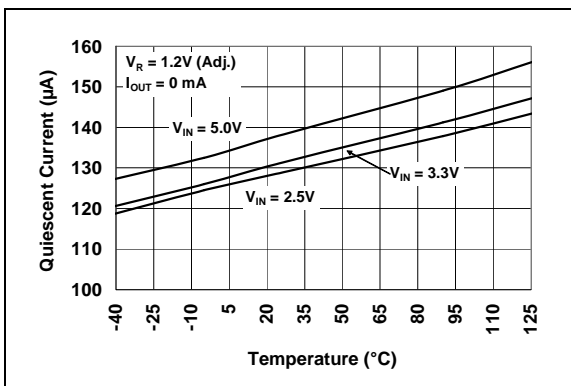


FIGURE 2-3: Quiescent Current vs. Junction Temperature (1.2V Adjustable).

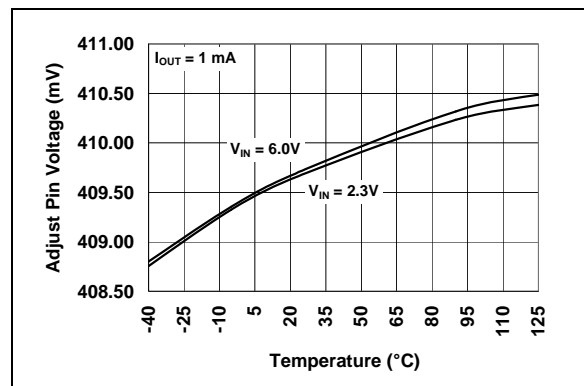


FIGURE 2-6: Adjust Pin Voltage vs. Temperature.

MCP1726

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

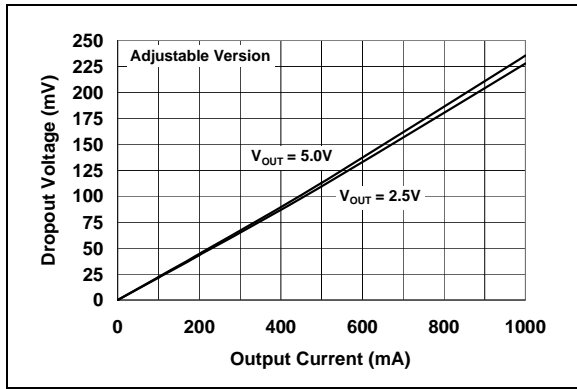


FIGURE 2-7: Dropout Voltage vs. Output Current (Adjustable Version).

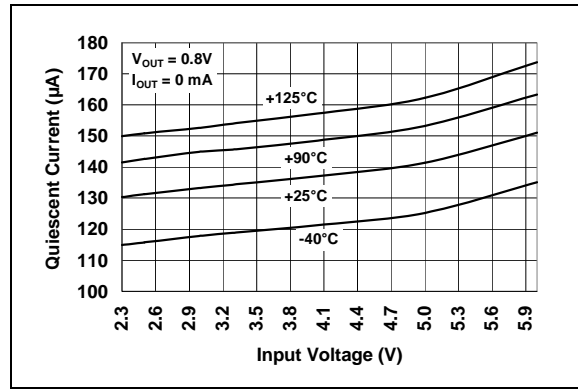


FIGURE 2-10: Quiescent Current vs. Input Voltage (0.8V Fixed).

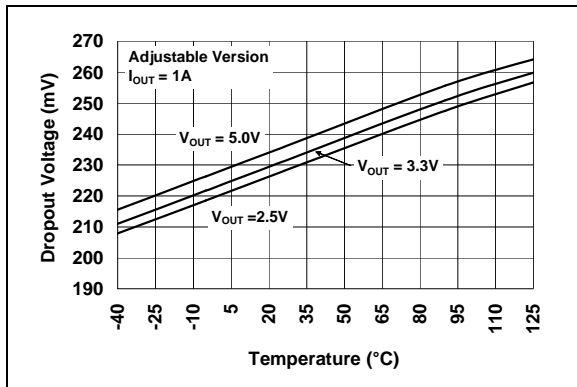


FIGURE 2-8: Dropout Voltage vs. Temperature (Adjustable Version).

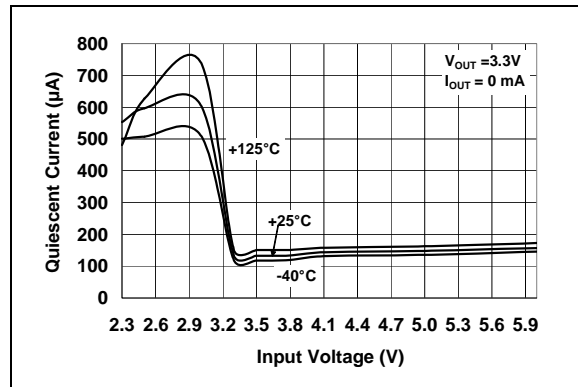


FIGURE 2-11: Quiescent Current vs. Input Voltage (3.3V Fixed).

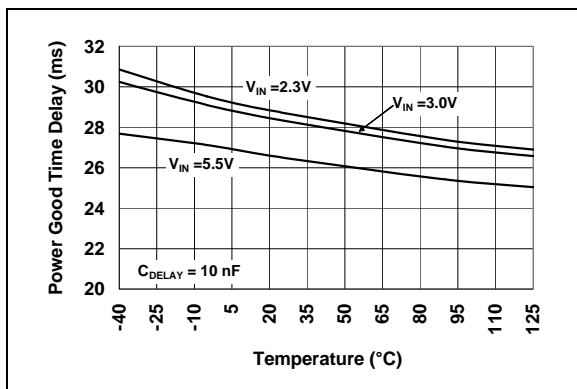


FIGURE 2-9: Power Good (PWRGD) Time Delay vs. Temperature.

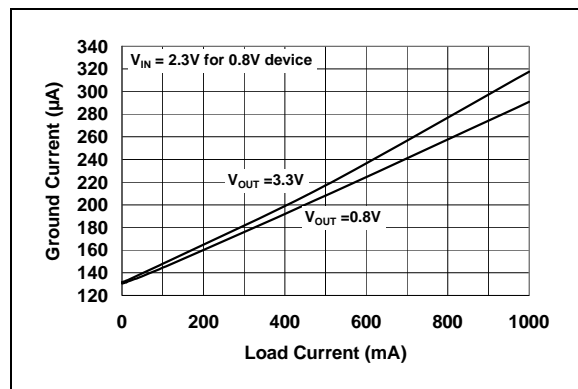


FIGURE 2-12: Ground Current vs. Load Current.

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

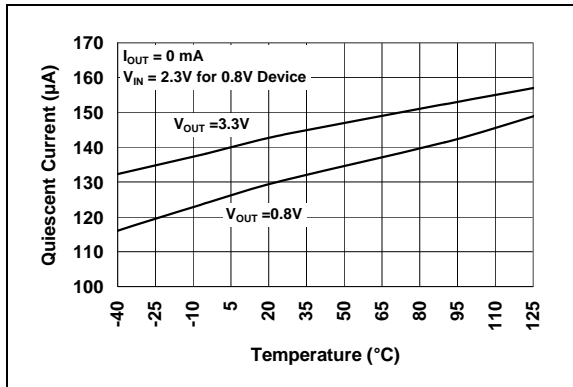


FIGURE 2-13: Quiescent Current vs. Temperature.

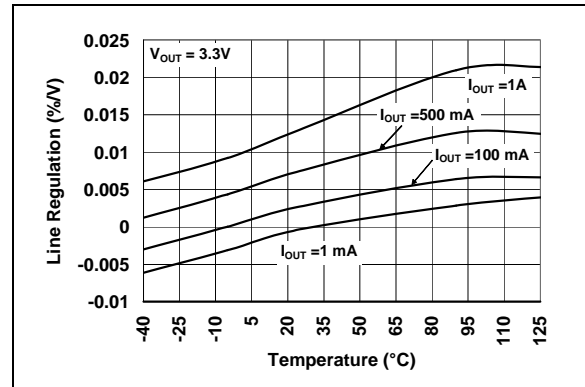


FIGURE 2-16: Line Regulation vs. Temperature (3.3V Fixed).

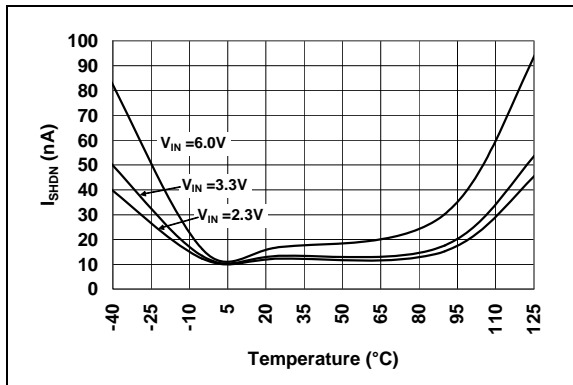


FIGURE 2-14: $\overline{I_{SHDN}}$ vs. Temperature.

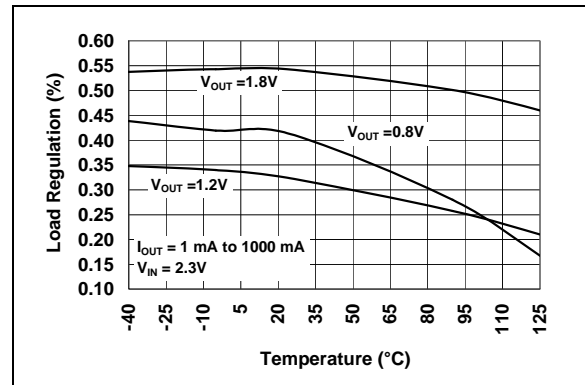


FIGURE 2-17: Load Regulation vs. Temperature ($V_{OUT} < 2.5V$ Fixed).

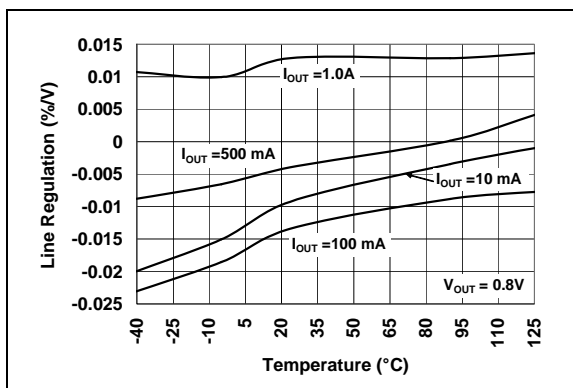


FIGURE 2-15: Line Regulation vs. Temperature (0.8V Fixed).

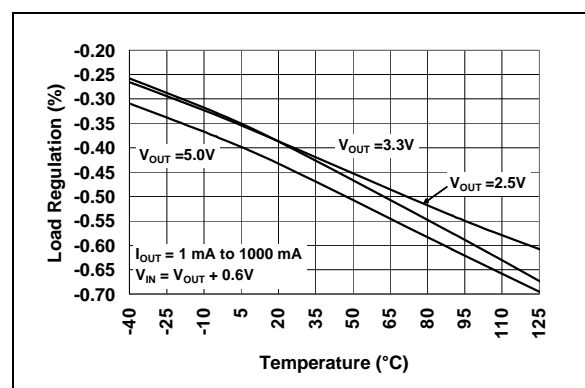


FIGURE 2-18: Load Regulation vs. Temperature ($V_{OUT} \geq 2.5V$ Fixed).

MCP1726

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

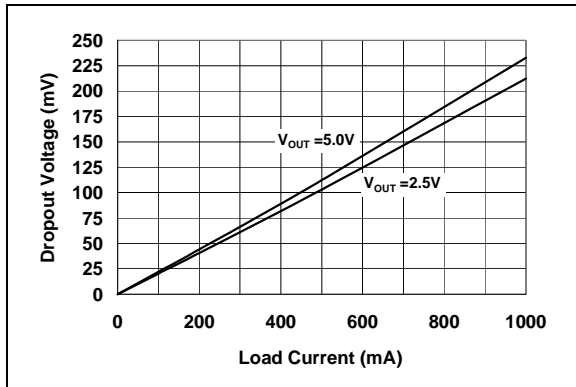


FIGURE 2-19: Dropout Voltage vs. Load Current.

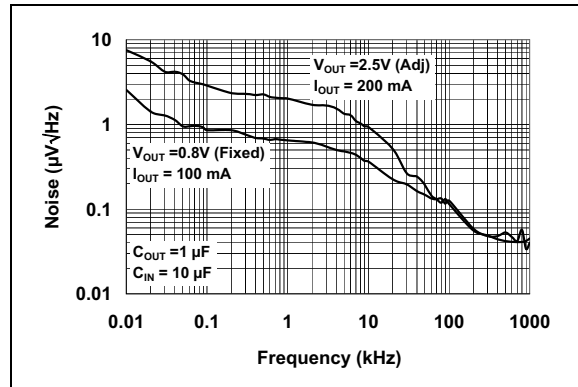


FIGURE 2-22: Output Noise Voltage Density vs. Frequency.

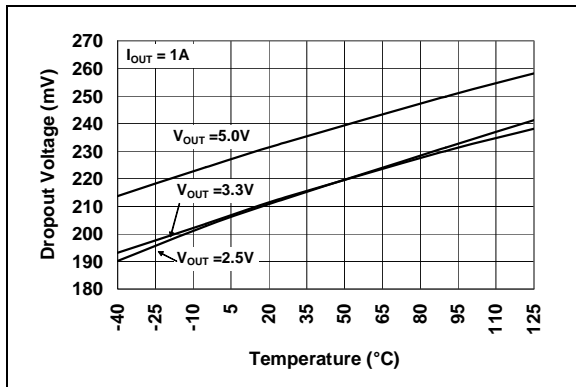


FIGURE 2-20: Dropout Voltage vs. Temperature.

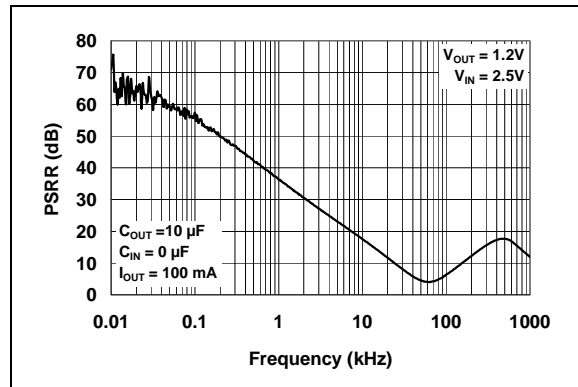


FIGURE 2-23: Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT} = 1.2V$ Adjustable).

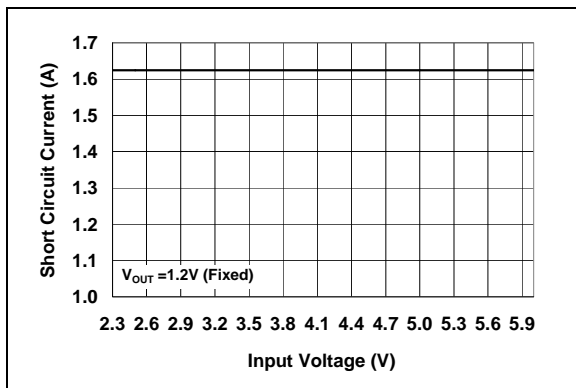


FIGURE 2-21: Short-Circuit Current vs. Input Voltage.

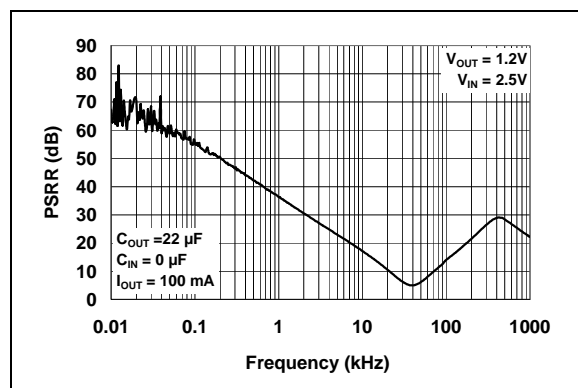


FIGURE 2-24: Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT} = 1.2V$ Adjustable).

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

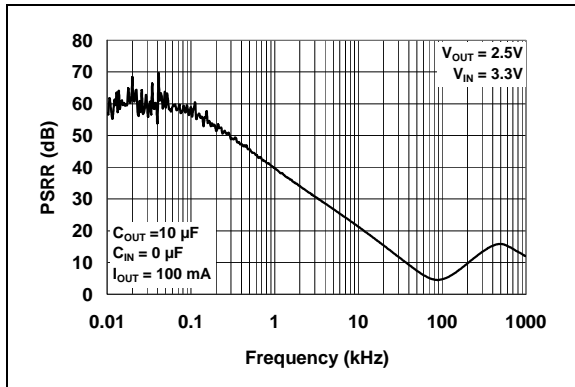


FIGURE 2-25: Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT} = 2.5V$ Fixed).

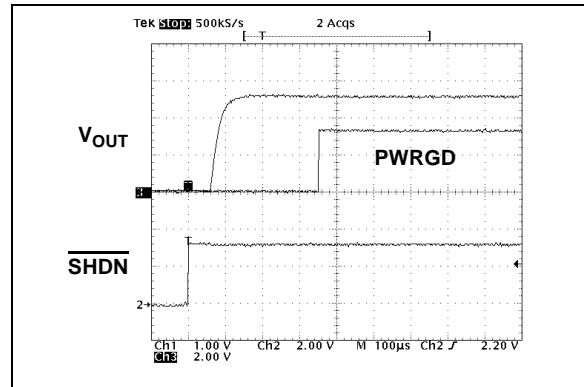


FIGURE 2-28: 2.5V (Adjustable) Start-Up from Shutdown.

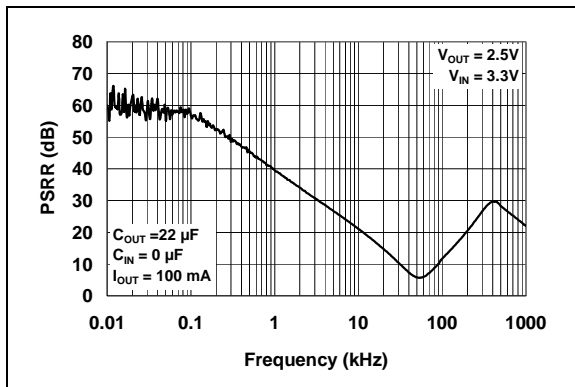


FIGURE 2-26: Power Supply Ripple Rejection (PSRR) vs. Frequency ($V_{OUT} = 2.5V$ Fixed).

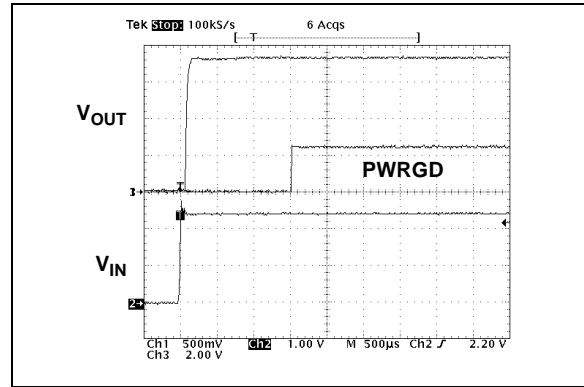


FIGURE 2-29: Power Good (PWRGD) Timing with C_{BYPASS} of 1000 pF.

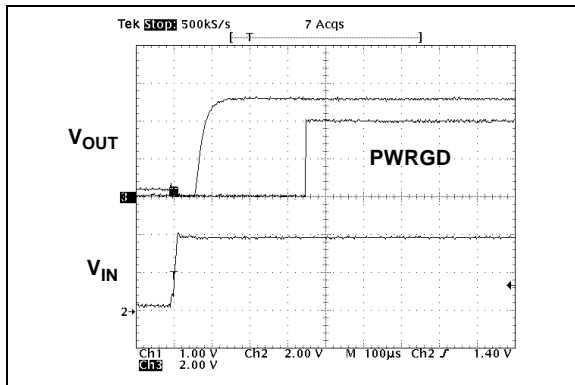


FIGURE 2-27: 2.5V (Adjustable) Start-Up from V_{IN} .

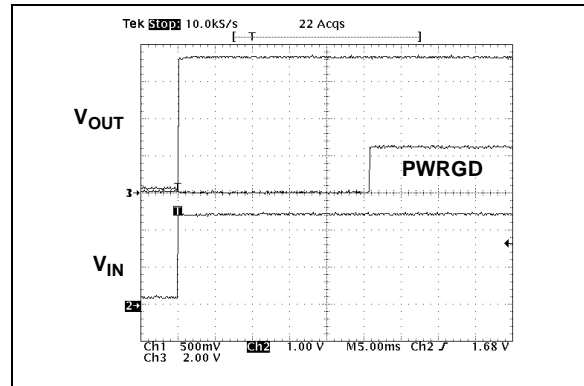


FIGURE 2-30: Power Good (PWRGD) Timing with C_{BYPASS} of 0.01 μF .

MCP1726

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1\text{ mA}$ and $T_A = +25^\circ\text{C}$.

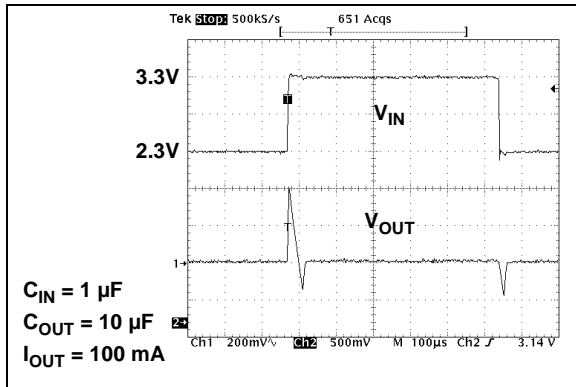


FIGURE 2-31: Dynamic Line Response (1.2V Fixed).

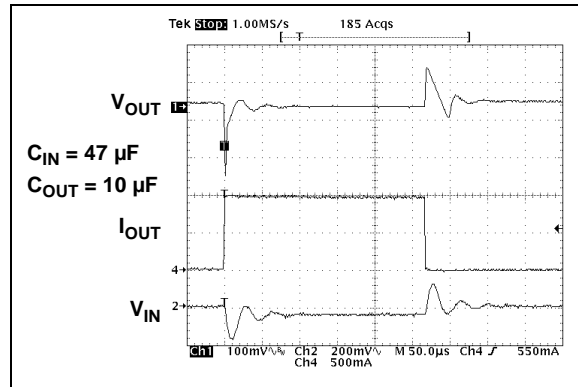


FIGURE 2-33: Dynamic Load Response (2.5V Fixed, 10 mA to 1000 mA).

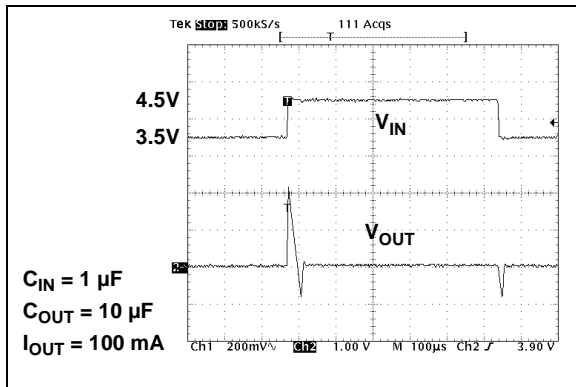


FIGURE 2-32: Dynamic Line Response (2.5V Fixed).

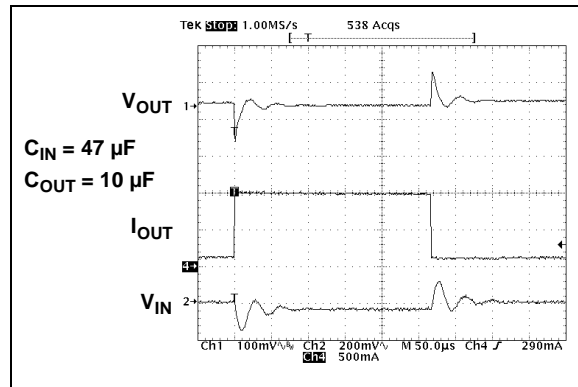


FIGURE 2-34: Dynamic Load Response (2.5V Fixed, 100 mA to 1000 mA).

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

| Fixed Output | | Adjustable Output | | Name | Description |
|--------------|------|-------------------|------|-------------------|---|
| 3x3 DFN | SOIC | 3x3 DFN | SOIC | | |
| 1 | 1 | 1 | 1 | V_{IN} | Input Voltage Supply |
| 2 | 2 | 2 | 2 | V_{IN} | Input Voltage Supply |
| 3 | 3 | 3 | 3 | \overline{SHDN} | Shutdown Control Input (active-low) |
| 4 | 4 | 4 | 4 | GND | Ground |
| 5 | 5 | 5 | 5 | PWRGD | Power Good Output |
| 6 | 6 | 6 | 6 | C_{DELAY} | Power Good Delay Set-Point Input |
| — | — | 7 | 7 | ADJ | Output Voltage Sense Input (adjustable version) |
| 7 | 7 | — | — | V_{OUT} | Regulated Output Voltage |
| 8 | 8 | 8 | 8 | V_{OUT} | Regulated Output Voltage |
| 9 | — | 9 | — | EP | Exposed Pad |

3.1 Input Voltage Supply (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN} . If the input voltage source is located several inches away from the LDO or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 μF to 10 μF should be sufficient for most applications.

3.2 Shutdown Control Input (\overline{SHDN})

The \overline{SHDN} input is used to turn the LDO output voltage on and off. When the \overline{SHDN} input is at a logic-high level, the LDO output voltage is enabled. When the \overline{SHDN} input is pulled to a logic-low level, the LDO output voltage is disabled. When the \overline{SHDN} input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.1 μA .

3.3 Ground (GND)

Connect the GND pin of the LDO to a quiet circuit ground. This will help the LDO power supply rejection ratio and noise performance. The ground pin of the LDO only conducts the quiescent current of the LDO (typically 140 μA), so a heavy trace is not required.

3.4 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD output has a typical hysteresis value of 2% for the adjustable voltage version and for voltage outputs less than 2.5V. For fixed output voltage versions greater than 2.5V, the hysteresis is 0.7%. The PWRGD output is delayed on power-up by 200 μs (typical, no capacitance on the C_{DELAY} pin). This delay time is controlled by the C_{DELAY} pin.

3.5 Power Good Delay Set-Point Input (C_{DELAY})

The C_{DELAY} input sets the power-up delay time for the PWRGD output. By connecting an external capacitor from the C_{DELAY} pin to ground, the delay times for the PWRGD output can be adjusted from 200 μs (no capacitance) to 300 ms (0.1 μF capacitor). This allows for the optimal setting of the system reset time.

3.6 Output Voltage Sense Input (ADJ)

The output voltage adjust pin (ADJ) for the adjustable output voltage version of the MCP1726 allows the user to set the output voltage of the LDO by using two external resistors. The adjust pin voltage is 0.41V (typical).

3.7 Regulated Output Voltage (V_{OUT})

The V_{OUT} pin(s) is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 μF is required for LDO stability. The MCP1726 is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See [Section 4.3 “Output Capacitor”](#) for output capacitor selection guidance.

3.8 Exposed Pad (EP)

The 3x3 DFN package has an exposed pad on the bottom of the package. This pad should be soldered to the Printed Circuit Board (PCB) to aid in the removal of heat from the package during operation. The exposed pad is at the ground potential of the LDO.

MCP1726

4.0 DEVICE OVERVIEW

The MCP1726 is a high output current, Low Dropout (LDO) voltage regulator with an adjustable delay power-good output and shutdown control input. The low dropout voltage of 220 mV at 1A of current makes it ideal for battery-powered applications. Unlike other high output current LDOs, the MCP1726 only draws 220 μ A of quiescent current at full load.

4.1 LDO Output Voltage

The MCP1726 LDO is available with either a fixed output voltage or an adjustable output voltage. The allowable output voltage range is 0.8V to 5.5V for both versions.

4.1.1 ADJUSTABLE INPUT

The adjustable version of the MCP1726 uses the ADJ pin (pin 7) to get the output voltage feedback for output voltage regulation. This allows the user to set the output voltage of the device with two external resistors. The nominal voltage for ADJ is 0.41V.

Figure 4-1 shows the adjustable version of the MCP1726. Resistors R_1 and R_2 form the resistor divider network necessary to set the output voltage. With this configuration, the equation for setting V_{OUT} is:

EQUATION 4-1:

$$V_{OUT} = V_{ADJ} \left(\frac{R_1 + R_2}{R_2} \right)$$

V_{OUT} = LDO Output Voltage

V_{ADJ} = ADJ Pin Voltage (typically 0.41V)

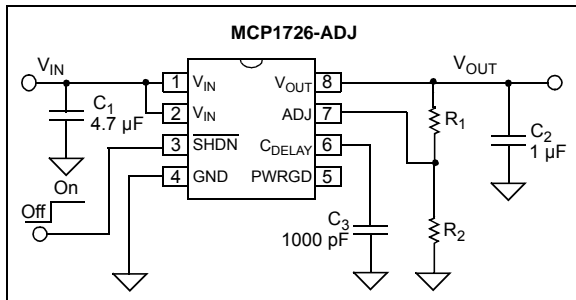


FIGURE 4-1: Typical Adjustable Output Voltage Application Circuit.

The range of allowable resistance values for resistor R_2 is 10 k Ω to 200 k Ω . Solving the equation for R_1 yields the following equation:

EQUATION 4-2:

$$R_1 = R_2 \left(\frac{V_{OUT} - V_{ADJ}}{V_{ADJ}} \right)$$

V_{OUT} = LDO Output Voltage

V_{ADJ} = ADJ Pin Voltage (typically 0.41V)

4.2 Output Current and Current Limiting

The MCP1726 LDO is tested and ensured to supply a minimum of 1A of output current. The MCP1726 has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1726 also incorporates an output current limit. If the output voltage falls below 0.7V due to an overload condition (usually represents a shorted load condition), the output current is limited to 1.7A (typical). If the overload condition is a soft overload, the MCP1726 will supply higher load currents of up to 3A. The MCP1726 should not be operated in this condition continuously as it may result in failure of the device. However, this does allow for device usage in applications that have higher pulsed load currents having an average output current value of 1A or less.

Output overload conditions may also result in an overtemperature shutdown of the device. If the junction temperature rises above 150°C, the LDO will shut down the output voltage. See [Section 4.9 "Overtemperature Protection"](#) for more information on overtemperature shutdown.

4.3 Output Capacitor

The MCP1726 requires a minimum output capacitance of 1 μ F for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor must be no greater than 2 Ω . The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 μ F X7R 0805 capacitor has an ESR of 50 m Ω .

Larger LDO output capacitors can be used with the MCP1726 to improve dynamic performance and power supply ripple rejection performance. A maximum of 22 μ F is recommended. Aluminum-electrolytic capacitors are not recommended for low-temperature applications of < -25°C.

4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 μF to 4.7 μF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent (or higher) value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.5 Power Good Output (PWRGD)

The PWRGD output is used to indicate when the output voltage of the LDO is within 92% (typical value, see the [DC Characteristics](#) table for Min/Max specs) of its nominal regulation value.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as T_{PG} in the [DC Characteristics](#) table). The power good time delay is adjustable via the C_{DELAY} pin of the LDO (see [Section 4.6 "C_{DELAY} Input"](#)). By placing a capacitor from the C_{DELAY} pin to ground, the power good time delay can be adjusted from 200 μs (no capacitance) to 300 ms (0.1 μF capacitor). After the time delay period, the PWRGD output will go high, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 170 μs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See [Figure 4-2](#) for power good timing characteristics.

When the LDO is put into Shutdown mode using the SHDN input, the power good output is pulled low immediately, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in [Figure 4-3](#).

The power good output is an open-drain output that can be pulled up to any voltage that is equal to or less than the LDO input voltage. This output is capable of sinking 1.2 mA ($V_{PWRGD} < 0.4\text{V}$ maximum).

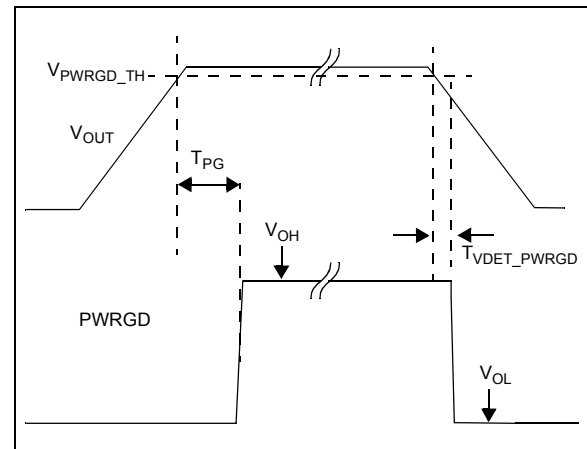


FIGURE 4-2: Power Good Timing.

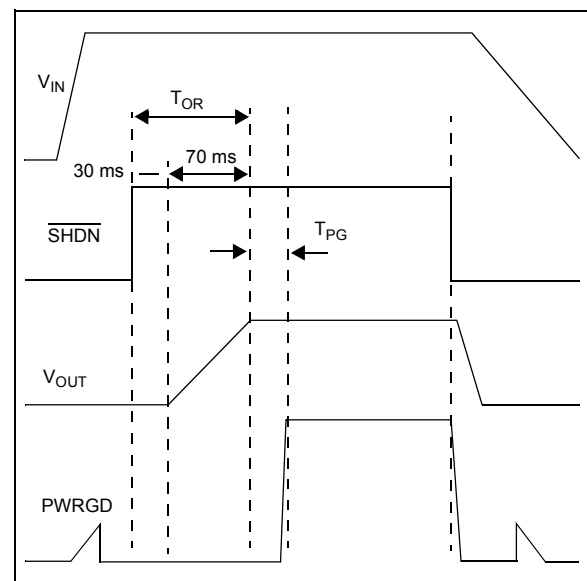


FIGURE 4-3: Power Good Timing from Shutdown.

4.6 C_{DELAY} Input

The C_{DELAY} input is used to provide the power-up delay timing for the power good output, as discussed in the previous section. By adding a capacitor from the C_{DELAY} pin to ground, the PWRGD power-up time delay can be adjusted from 200 μs (no capacitance on C_{DELAY}) to 300 ms (0.1 μF of capacitance on C_{DELAY}). See the [DC Characteristics](#) table for C_{DELAY} timing tolerances.

MCP1726

Once the power good threshold (rising) has been reached, the C_{DELAY} pin charges the external capacitor to 1.5V (typical; this level can vary between 1.4V and 1.75V across the input voltage range of the part). The PWRGD output will transition high when the C_{DELAY} pin voltage has charged to 0.42V. If the output falls below the power good threshold limit during the charging time between 0.0V and 0.42V on the C_{DELAY} pin, the C_{DELAY} pin voltage will be pulled to ground, thus resetting the timer. The C_{DELAY} pin will be held low until the output voltage of the LDO has once again risen above the power good rising threshold. A timing diagram showing C_{DELAY} , PWRGD and V_{OUT} is shown in Figure 4-4.

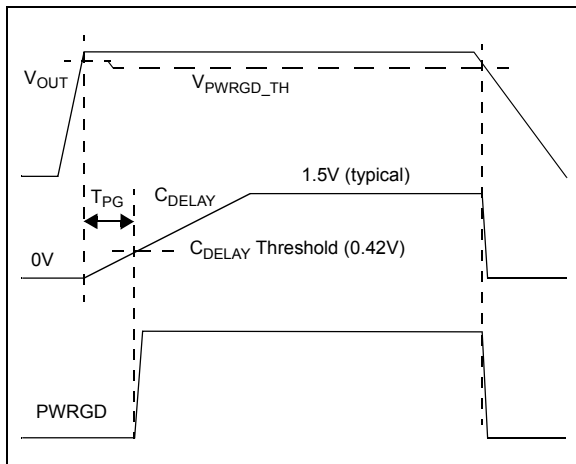


FIGURE 4-4: C_{DELAY} and PWRGD Timing Diagram.

4.7 Shutdown Input (SHDN)

The \overline{SHDN} input is an active-low input signal that turns the LDO on and off. The \overline{SHDN} threshold is a percentage of the input voltage. The typical value of this shutdown threshold is 30% of V_{IN} , with minimum and maximum limits over the entire operating temperature range of 45% and 15%, respectively.

The SHDN input will ignore low-going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO will enter Shutdown mode. This small bit of filtering helps reject any system noise spikes on the shutdown input signal.

On the rising edge of the \overline{SHDN} input, the shutdown circuitry has a 30 μ s delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the SHDN input signal. After the 30 μ s delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the \overline{SHDN} input signal is pulled low during the 30 μ s delay period, the timer will be reset and the delay time will start over again on the next rising edge of the SHDN input. The total time from the \overline{SHDN} input going high (turn-on) to the LDO output being in regulation is typically 100 μ s. See Figure 4-5 for a timing diagram of the SHDN input.

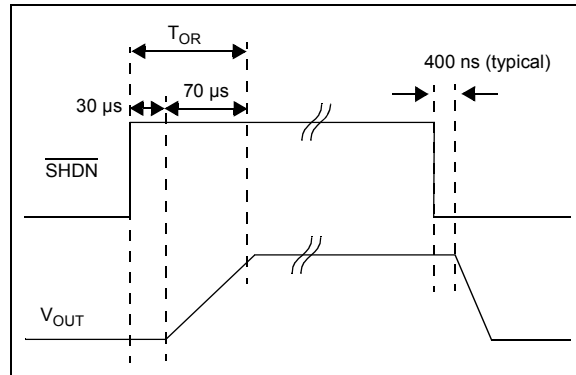


FIGURE 4-5: Shutdown Input Timing Diagram.

4.8 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a $V_R + 0.5V$ differential applied. The MCP1726 LDO has a very low dropout voltage specification of 220 mV (typical) at 1A of output current. See the DC Characteristics table for maximum dropout voltage specifications.

The MCP1726 LDO operates across an input voltage range of 2.3V to 6.0V and incorporates input Undervoltage Lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 2.18V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output will remain on until the input voltage level reaches 2.04V (typical).

Since the MCP1726 LDO Undervoltage Lockout activates at 2.04V as the input voltage is falling, the dropout voltage specification does not apply for output voltages that are less than 1.9V.

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 2.3V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

4.9 Overtemperature Protection

The MCP1726 LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately 150°C. If the LDO junction temperature does reach 150°C, the LDO output will be turned off until the junction temperature cools to approximately 140°C, at which point the LDO output will automatically resume normal operation. If the internal power dissipation continues to be excessive, the device will shut off again. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See [Section 5.0 “Application Circuits/Issues”](#) for more information on LDO power dissipation and junction temperature.

MCP1726

5.0 APPLICATION CIRCUITS/ISSUES

5.1 Typical Application

The MCP1726 is used for applications that require high LDO output current and a power good output.

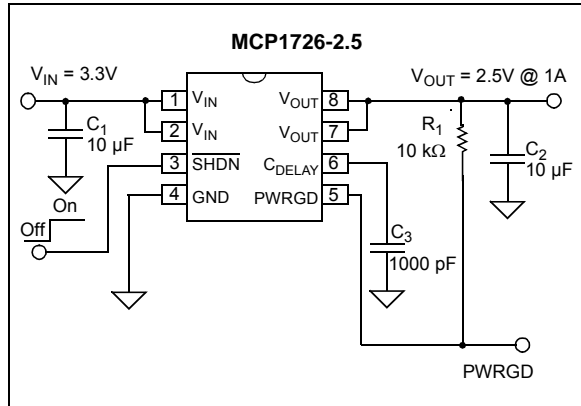


FIGURE 5-1: Typical Application Circuit.

5.1.1 APPLICATION CONDITIONS

| | |
|--------------------------|------------------|
| Package Type | = 8-Lead 3x3 DFN |
| Input Voltage Range | = 3.3V ± 10% |
| V _{IN} maximum | = 3.63V |
| V _{IN} minimum | = 2.97V |
| V _{OUT} typical | = 2.5V |
| I _{OUT} | = 1.0A maximum |

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1726 is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

P_{LDO} = LDO Pass device internal power dissipation

V_{IN(MAX)} = Maximum input voltage

V_{OUT(MIN)} = LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1726 as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

P_{I(GND)} = Power dissipation due to the quiescent current of the LDO

V_{IN(MAX)} = Maximum input voltage

I_{VIN} = Current flowing in the V_{IN} pin with no LDO output current (LDO quiescent current)

The total power dissipated within the MCP1726 is the sum of the power dissipated in the LDO pass device and the P_{I(GND)} term. Because of the CMOS construction, the typical I_{GND} for the MCP1726 is 140 µA. Operating at a maximum of 3.63V results in a power dissipation of 0.51 mW. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1726 is +125°C. To estimate the internal junction temperature of the MCP1726, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient (R_{θJA}) of the device. The thermal resistance from junction to ambient for the 3x3 DFN package is estimated at 64°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{TOTAL} \times R_{\theta JA} + T_{A(MAX)}$$

T_{J(MAX)} = Maximum continuous junction temperature

P_{TOTAL} = Total device power dissipation

R_{θJA} = Thermal resistance from junction-to-ambient

T_{A(MAX)} = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
 $T_{J(MAX)}$ = Maximum continuous junction temperature
 $T_{A(MAX)}$ = Maximum ambient temperature
 $R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
 $P_{D(MAX)}$ = Maximum device power dissipation
 $R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction temperature
 $T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
 T_A = Ambient temperature

5.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 3x3 DFN

Input Voltage

V_{IN} = 3.3V ± 10%

LDO Output Voltage and Current

V_{OUT} = 2.5V

I_{OUT} = 1.0A

Maximum Ambient Temperature

$T_{A(MAX)}$ = 70°C

Internal Power Dissipation

$P_{LDO(MAX)} = [V_{IN(MAX)} - V_{OUT(MIN)}] \times I_{OUT(MAX)}$

$P_{LDO} = [(3.3V \times 1.1) - (0.975 \times 2.5V)]$
 $\times 1.0A$

$P_{LDO} = 1.192W$

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7 "High Effective Thermal Conductivity Test Board for Leaded Surface-Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$

$T_{J(RISE)} = 1.192W \times 64.0^\circ C/W$

$T_{J(RISE)} = 76.3^\circ C$

MCP1726

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$$T_J = T_{JRISE} + T_{A(MAX)}$$

$$T_J = 76.3^{\circ}\text{C} + 70.0^{\circ}\text{C}$$

$$T_J = 146.3^{\circ}\text{C}$$

As can be seen from the result, this application will be operating above the maximum operating junction temperature of 125°C. The PCB layout for this application is very important, as it has a significant impact on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the 3x3 DFN package, which is very important in this application.

Maximum Package Power Dissipation at 70°C Ambient Temperature

3x3 DFN (64°C/W $R_{\theta JA}$)

$$P_{D(MAX)} = (125^{\circ}\text{C} - 70^{\circ}\text{C})/64^{\circ}\text{C/W}$$

$$P_{D(MAX)} = 0.86\text{W}$$

8LD SOIC (163°C/W $R_{\theta JA}$)

$$P_{D(MAX)} = (125^{\circ}\text{C} - 70^{\circ}\text{C})/163^{\circ}\text{C/W}$$

$$P_{D(MAX)} = 0.337\text{W}$$

From this table you can see the difference in maximum allowable power dissipation between the 3x3 DFN package and the 8-pin SOIC package. This difference is due to the exposed metal tab on the bottom of the DFN package. The exposed tab of the DFN package provides a very good thermal path from the die of the LDO to the PCB. The PCB then acts like a heat sink, providing more area to distribute the heat generated by the LDO. When the PCB heat sink area is used, the $R_{\theta JA}$ should be replaced by $R_{\theta JC}$ plus $R_{\theta HS}$, where $R_{\theta HS}$ is the PCB copper area heat sink thermal resistance. This will allow for higher maximum power dissipation compared to the free-air power dissipation calculated using $R_{\theta JA}$.

6.0 PACKAGING INFORMATION

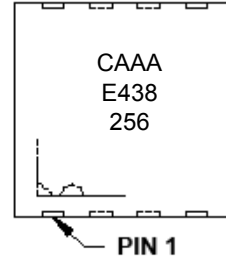
6.1 Package Marking Information

8-Lead DFN (3x3x0.9 mm)

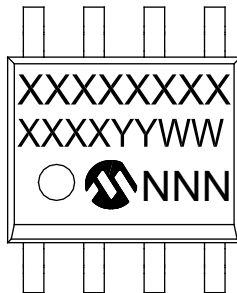


| Voltage Option | Code |
|----------------|------|
| 0.8V | CAAA |
| 1.2V | CAAB |
| 1.8V | CAAC |
| 2.5V | CAAD |
| 3.0V | CAAE |
| 3.3V | CAAF |
| 5.0V | CAAG |
| Adj | AADJ |

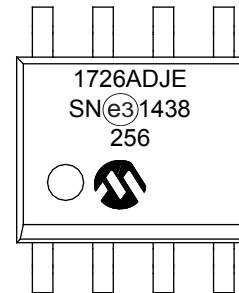
Example



8-Lead SOIC (3.90 mm)



Example



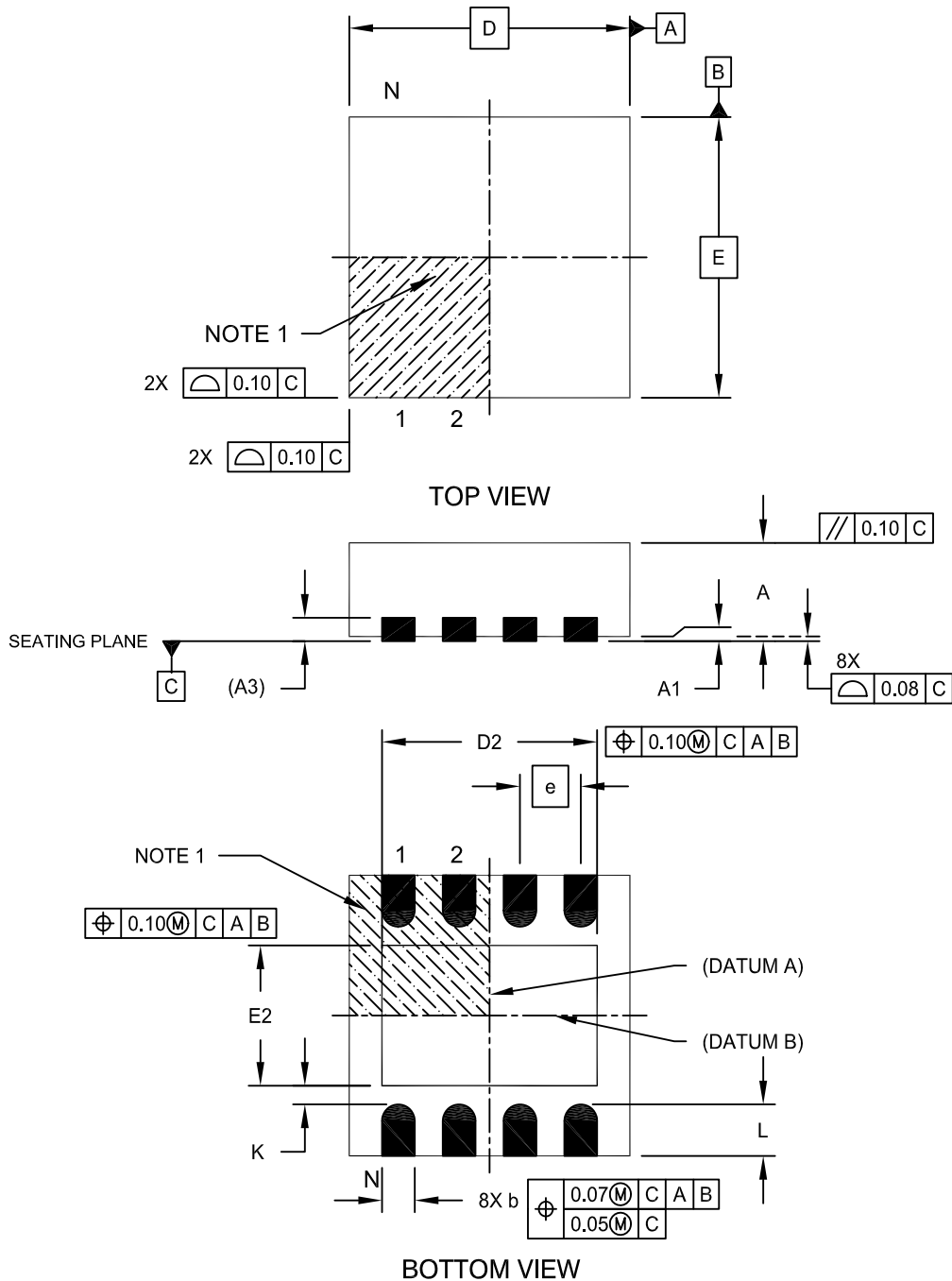
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP1726

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

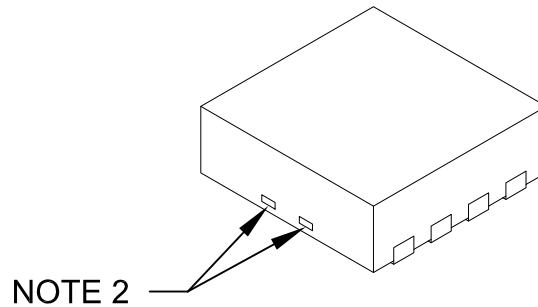
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 3.00 BSC | | |
| Exposed Pad Width | E2 | 1.34 | - | 1.60 |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.60 | - | 2.40 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.20 | 0.30 | 0.55 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

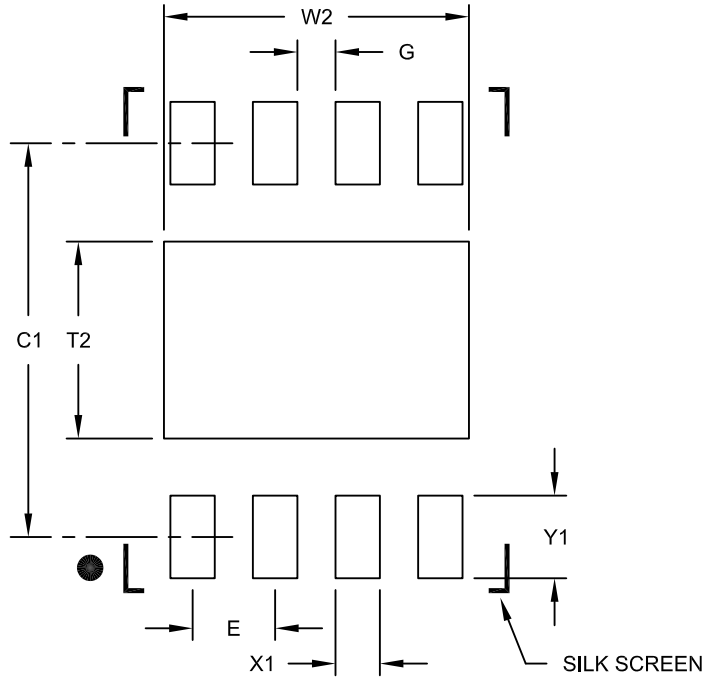
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

MCP1726

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 2.40 |
| Optional Center Pad Length | T2 | | | 1.55 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.65 |
| Distance Between Pads | G | 0.30 | | |

Notes:

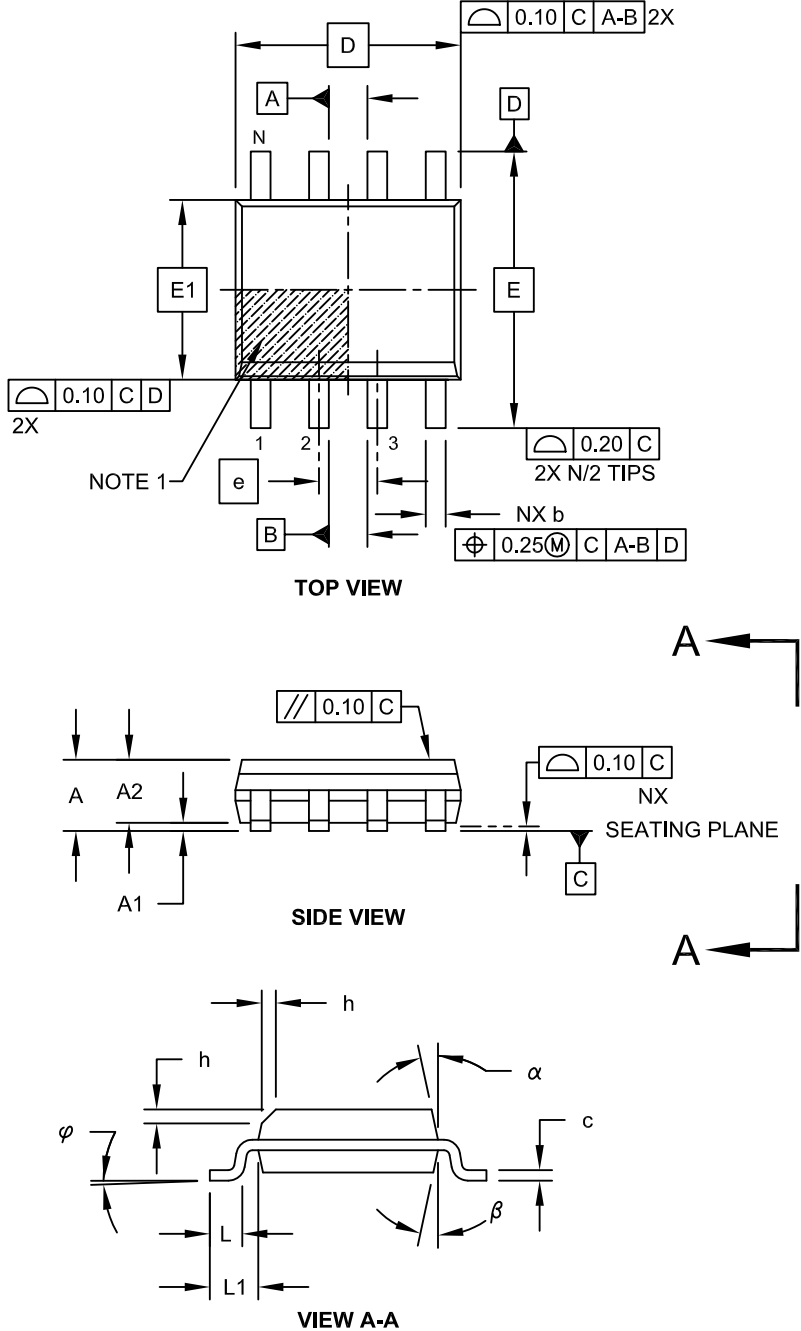
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

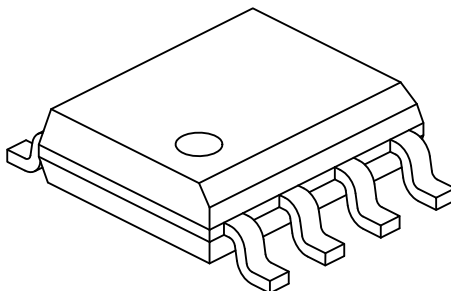


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

MCP1726

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|-----------|-------|-------------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | 1.27 BSC | | |
| Overall Height | A | | - | - | 1.75 |
| Molded Package Thickness | A2 | | 1.25 | - | - |
| Standoff § | A1 | | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | | |
| Molded Package Width | E1 | | 3.90 BSC | | |
| Overall Length | D | | 4.90 BSC | | |
| Chamfer (Optional) | h | | 0.25 | - | 0.50 |
| Foot Length | L | | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | | |
| Foot Angle | φ | | 0° | - | 8° |
| Lead Thickness | c | | 0.17 | - | 0.25 |
| Lead Width | b | | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | | 5° | - | 15° |
| Mold Draft Angle Bottom | β | | 5° | - | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

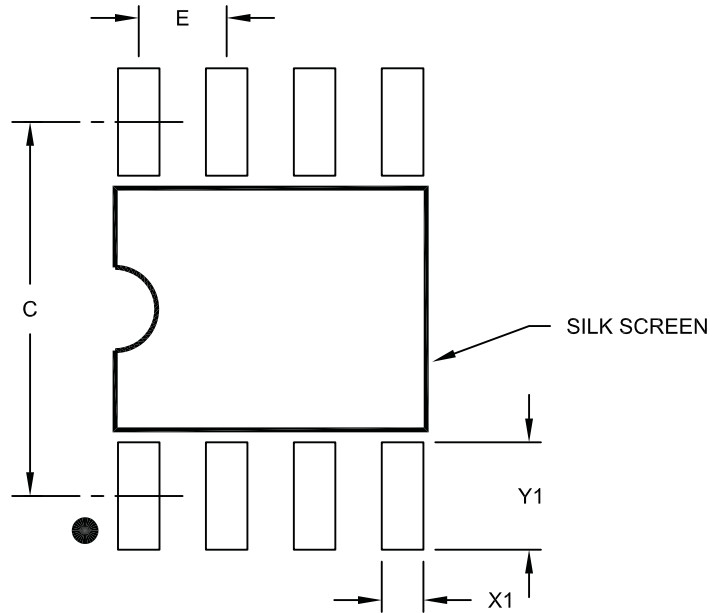
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

MCP1726

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (September 2014)

The following is the list of modifications:

1. Corrected the typical output voltage tolerance in the **Features** section to match the stated value in the **DC Characteristics** table.
2. Corrected illustrations of package markings in **Section 6.0, Packaging Information**.
3. Minor typographical changes.

Revision C (August 2007)

The following is the list of modifications:

1. Added 3.0V option to **Section 6.1, Package Marking Information**.
2. Updated package outline drawings.
3. Added 3.0V option to **Product Identification System (PIS)** section.

Revision B (March 2005)

The following is the list of modifications:

1. Replaced 3x3 DFN package diagram.
2. Emphasized (bolded) a few specifications of **Section 1.0, Electrical Characteristics** in the **DC Characteristics** table.

Revision A (February 2005)

- Original Release of this Document.

MCP1726

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | X | -XXX | X | X | XX | Examples: |
|----------------------------------|---|----------------|-----------|-------------------|---------|---|
| Device | Tape & Reel | Voltage Output | Tolerance | Temperature Range | Package | |
| Device: | MCP1726: 1A, Low Quiescent Current LDO Regulator | | | | | a) MCP1726-0802E/MF: 0.80V, 1A LDO, 8LD DFN Package |
| Tape & Reel Option: | T = Tape and Reel Blank = Tube | | | | | b) MCP1726T-1202E/MF: Tape and Reel, 1.20V, 1A LDO, 8LD DFN Package |
| Standard Output Voltage*: | 080 = 0.80V 120 = 1.20V 180 = 1.80V 250 = 2.50V 300 = 3.00V 330 = 3.30V 500 = 5.00V ADJ = Adjustable Voltage Version | | | | | c) MCP1726-3002E/MF: 3.00V, 1A LDO, 8LD DFN Package |
| | * Custom output voltages available upon request. Contact your local Microchip sales office for more information. | | | | | d) MCP1726T-3302E/MF: Tape and Reel, 3.30V, 1A LDO, 8LD DFN Package |
| Tolerance: | 2 = 2.0% | | | | | e) MCP1726-1802E/SN: 1.80V, 1A LDO, 8LD SOIC Package |
| Temperature Range: | E = -40° to +125°C | | | | | f) MCP1726T-2502E/SN: Tape and Reel, 2.50V, 1A LDO, 8LD SOIC Package |
| Package*: | SN = Plastic Small Outline – Narrow, 3.90 mm Body, 8-Lead (SOIC) MF = Plastic Dual Flat, No Lead Package – 3x3x0.9 mm Body, 8-Lead (DFN) *Both packages are Lead Free | | | | | g) MCP1726-5002E/SN: 5.00V, 1A LDO, 8LD SOIC Package |
| | | | | | | h) MCP1726T-ADJE/SN: Tape and Reel, Adjustable, 1A LDO, 8LD SOIC Package |
| | | | | | | Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. |

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC³² logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2005-2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63276-576-5

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Pforzheim
Tel: 49-7231-424750

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

03/25/14