ZL38065
32 Channel Voice Echo Canceller

Data Sheet

January 2006

Features

- Independent multiple channels of echo cancellation; from 32 channels of 64 ms to 16 channels of 128 ms with the ability to mix channels at 128 ms or 64 ms in any combination
- Fully compliant to ITU-T G.165, G.168 (2000) and (2002) specifications
- Passed all AT&T voice quality tests for carrier grade echo canceller systems.
- Unparalleled in-system tunability
- Sub 50 ms initial convergence times under many typical network conditions
- Fast reconvergence on echo path changes
- Patented Advanced Non-Linear Processor with high quality subjective performance
- Superior noise matching algorithm
- PCM coding, μ/A-Law ITU-T G.711 or sign magnitude
- Per channel Fax/Modem G.164 2100 Hz or G.165 2100 Hz phase reversal Tone Disable
- Per channel echo canceller parameters control
- Transparent data transfer and mute
- Protection against narrow band signal divergence and instability in high echo environments

Ordering Information

ZL38065QCG	100 Pin LQFP	Trays, Bake & Drypack
ZL38065GDG	208 Ball LBGA	Trays, Bake & Drypack
ZL38065QCG1	100 Pin LQFP*	Trays, Bake & Drypack
ZL38065GDG2	208 Ball LBGA**	Trays, Bake & Drypack

*Pb Free Matte Tin

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- +9 dB to -12 dB level adjusters (3 dB steps) at all signal ports
- Offset nulling of all PCM channels
- Independent Power Down mode for each group of 2 channels for power management
- Compatible to ST-BUS and GCI interface at 2 Mbps serial PCM
- 3.3 V pads and 1.8 V Logic core operation with 5 V tolerant inputs
- IEEE-1149.1 (JTAG) Test Access Port

Applications

- Voice over IP network gateways
- Voice over ATM, Frame Relay
- T1/E1/J1 multichannel echo cancellation

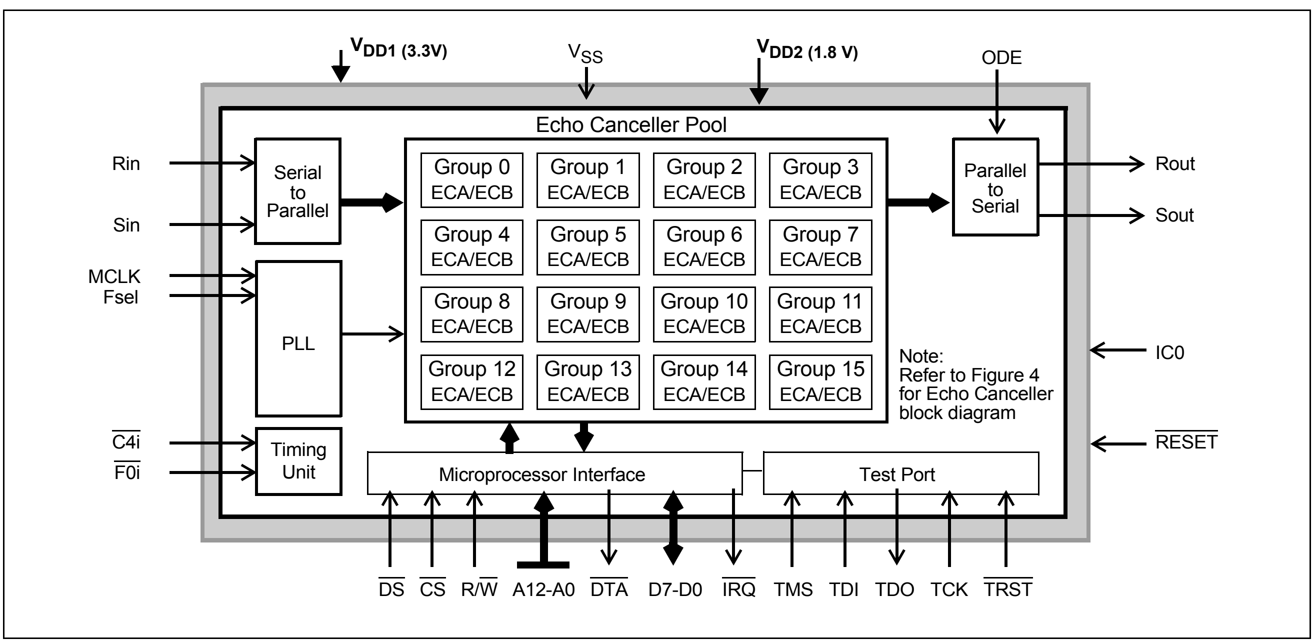

Figure 1 - ZL38065 Device Overview

- Wireless base stations
- Echo Canceller pools

Description

The ZL38065 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.168 requirements. The ZL38065 architecture contains 16 groups of two echo cancellers (ECA and ECB) which can be configured to provide two channels of 64 ms or one channel of 128 ms echo cancellation. This provides 32 channels of 64 ms to 16 channels of 128 ms echo cancellation or any combination of the two configurations. The ZL38065 supports ITU-T G.165 and G.164 tone disable requirements.

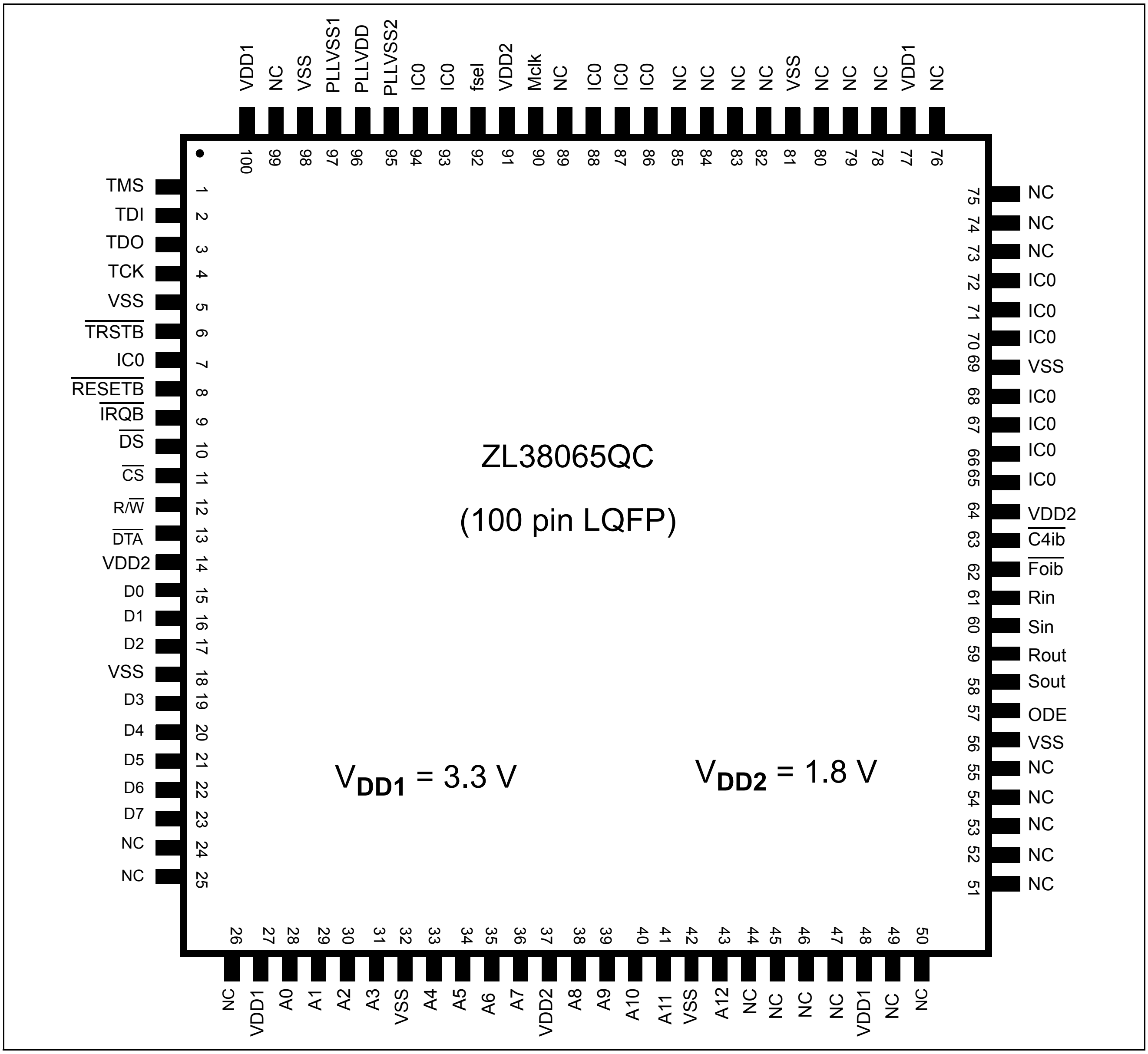

Figure 2 - 100 Pin LQFP

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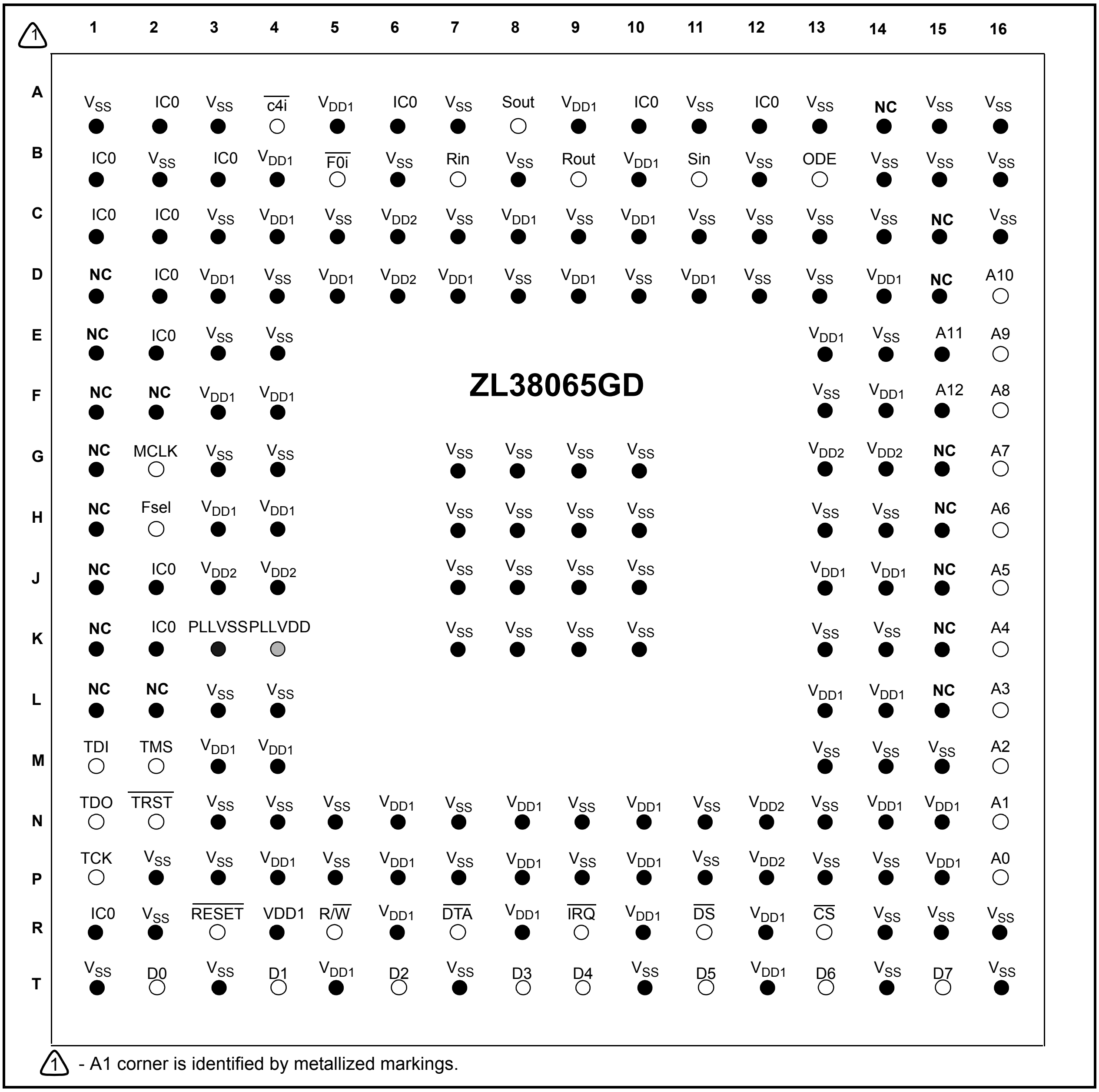


Figure 3 - 208 Ball LBGA

Pin Description

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
V_{SS}	A1, A3,A7,A11, A13, A15, A16, B2, B6, B8, B12, B14, B15, B16, C3, C5, C7, C9, C11, C12, C13, C14, C16, D4, D8, D10, D12, D13, E3, E4, E14, F13, G3, G4, G7, G8, G9, G10, H7, H8, H9, H10, H13, H14, J7, J8, J9, J10, K7, K8, K9, K10, K13, K14, L3, L4, M13, M14, M15, N3, N4, N5, N7, N9, N11, N13, P2, P3, P5, P7, P9.P11, P13, P14, R2, R14, R15, R16, T1, T3, T7, T10, T14, T16	5, 18, 32, 42, 56, 69, 81, 98	**Ground.**
V_{DD1}	A5, A9, B10, C4, C8, B4, C10, D3, D5, D7, D9, D11, D14, E13, F3, F4, F14, H3, H4, J13, J14, L13, L14, M3, M4, N6, N8, N10, N14, N15, P4, P6, P8, P10, P15, R4, R6, R8, R10, R12, T5, T12	27, 48, 77, 100	**Positive Power Supply.** Nominally 3.3 V (I/O Voltage).
V_{DD2}	C6, D6, J3, J4, N12, P12, G13, G14	14, 37, 64, 91	**Positive Power Supply.** Nominally 1.8 V (Core Voltage).
IC0	A12, A10, A6, A2, B1, B3, C1, C2, D2, E2, J2, K2, R1	7, 65, 66, 67, 68, 70, 71, 72, 86, 87, 88, 93, 94	**Internal Connection.** These pins must be connected to V_{SS} for normal operation.
NC	A14, C15, D1, D15, E1, F1, G1, G15, H1, H15, J1, J15, K1, K15,L1,L15,F2,L2	24, 25, 26, 44, 45, 46, 47, 49, 51, 52, 53, 54, 55, 73, 74, 75, 76, 78, 79, 80, 82, 83, 84, 85, 89, 99, 50	**No connection.** These pins must be left open for normal operation.

Pin Description (continued)

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
$\overline{\text{IRQ}}$	R9	9	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
$\overline{\text{DS}}$	R11	10	**Data Strobe (Input)**. This active low input works in conjunction with $\overline{\text{CS}}$ to enable the read and write operations.
$\overline{\text{CS}}$	R13	11	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/$\overline{\text{W}}$	R5	12	**Read/$\overline{\text{Write}}$ (Input)**. This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
$\overline{\text{DTA}}$	R7	13	**Data Transfer Acknowledgment (Open Drain Output)**. This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D0..D7	T2,T4,T6,T8,T9,T11, T13,T15	15, 16, 17, 19, 20, 21, 22, 23	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8 bit bidirectional data bus of the microprocessor port.
A0..A12	P16,N16,M16,L16,K16, J16,H16,G16,F16,E16, D16, E15, F15	28, 29, 30, 31, 33, 34, 35, 36, 38, 39, 40, 41, 43	**Address A0 to A12 (Input)**. These inputs provide the A12 - A0 address lines to the internal registers.
ODE	B13	57	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout	A8	58	**Send PCM Signal Output (Output)**. Port 1 TDM data output streams. Sout pin outputs serial TDM data streams at 2.048 Mbps with 32 channels per stream.
Rout	B9	59	**Receive PCM Signal Output (Output)**. Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mbps with 32 channels per stream.
Sin	B11	60	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mbps with 32 channels per stream.
Rin	B7	61	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams. Rin pin receives serial TDM data streams at 2.048 Mbps with 32 channels per stream.

Pin Description (continued)

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
$\overline{\text{F0i}}$	B5	62	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
$\overline{\text{C4i}}$	A4	63	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
MCLK	G2	90	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel	H2	92	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
PLLVss1 PLLVss2	K3	97, 95	**PLL Ground.** Must be connected to V_{SS}
$PLLV_{DD}$	K4	96	**PLL Power Supply.** Must be connected to V_{DD2} = 1.8 V
TMS	M2	1	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI	M1	2	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO	N1	3	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK	P1	4	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
$\overline{\text{TRST}}$	N2	6	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the ZL38065 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
$\overline{\text{RESET}}$	R3	8	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the ZL38065 into a low-power stand-by mode. When the $\overline{\text{RESET}}$ pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Main Control and Status Registers to their default power-up values.

1.0 Device Overview

The ZL38065 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers, Echo Canceller A and Echo Canceller B. Each group can be configured in Normal, Extended Delay or Back-to-Back configurations. In **Normal configuration**, a group of echo cancellers provides two channels of 64 ms echo cancellation, which run independently on different channels. In **Extended Delay** configuration, a group of echo cancellers achieves 128 ms of echo cancellation by cascading the two echo cancellers (A & B). In **Back-to-Back** configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel, providing full-duplex 64 ms echo cancellation.

Each echo canceller contains the following main elements (see Figure 4).

- Adaptive Filter for estimating the echo channel
- Subtractor for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Path Change detector for fast reconvergence on major echo path changes
- Instability Detector to combat instability in very low ERL environments
- Patented Advanced Non-Linear Processor for suppression of residual echo, with comfort noise injection
- Disable Tone Detectors for detecting valid disable tones at send and receive path inputs
- Narrow-Band Detector for preventing Adaptive Filter divergence from narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- +9 to -12 dB level adjusters at all signal ports
- Parallel controller interface compatible with Motorola microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711 or Sign-Magnitude coding

Each echo canceller in the ZL38065 has four functional states: *Mute*, *Bypass*, *Disable Adaptation* and *Enable Adaptation*. These are explained in section 3.0, “Echo Canceller Functional States“.

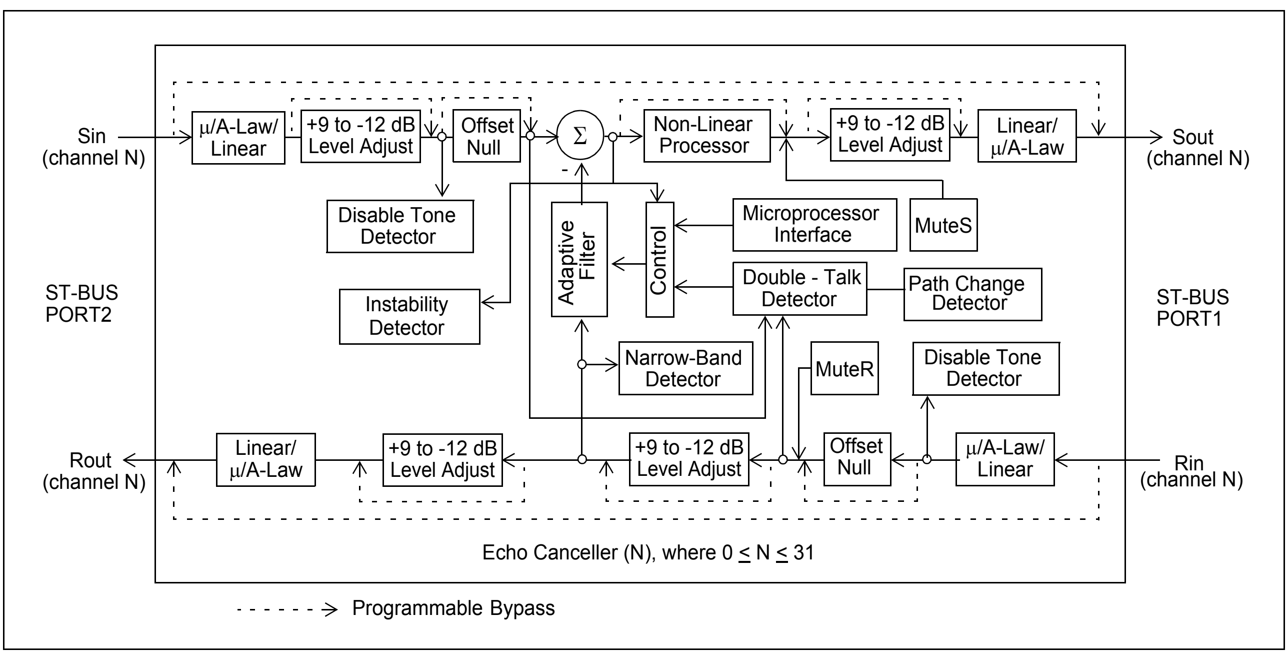


Figure 4 - Functional Block Diagram

1.1 Adaptive Filter

The adaptive filter adapts to the echo path and generates an estimate of the echo signal. This echo estimate is then subtracted from Sin. For each group of echo cancellers, the adaptive filter is a 1024 tap FIR adaptive filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In **Normal configuration**, the first section is dedicated to channel A and the second section to channel B. In **Extended Delay configuration**, both sections are cascaded to provide 128 ms of echo estimation in channel A. In **Back-to Back configuration**, the first section is used in the receive direction and the second section is used in the transmit direction for the same channel.

The ZL38065 offers industry leading convergence speeds, both in initial convergence and reconvergence. A sample test result from G.168-2002 Test 2A can be seen in Figure 5. This test result demonstrates one of the many conditions where the Zarlink device offer sub 50 ms initial convergence times (G.168 Test 2A, Hybrid 5, 40 ms delay, ERL=24dB, Lrin=0dBm0). Full G.168 test results across all hybrids and test conditions are available upon request.

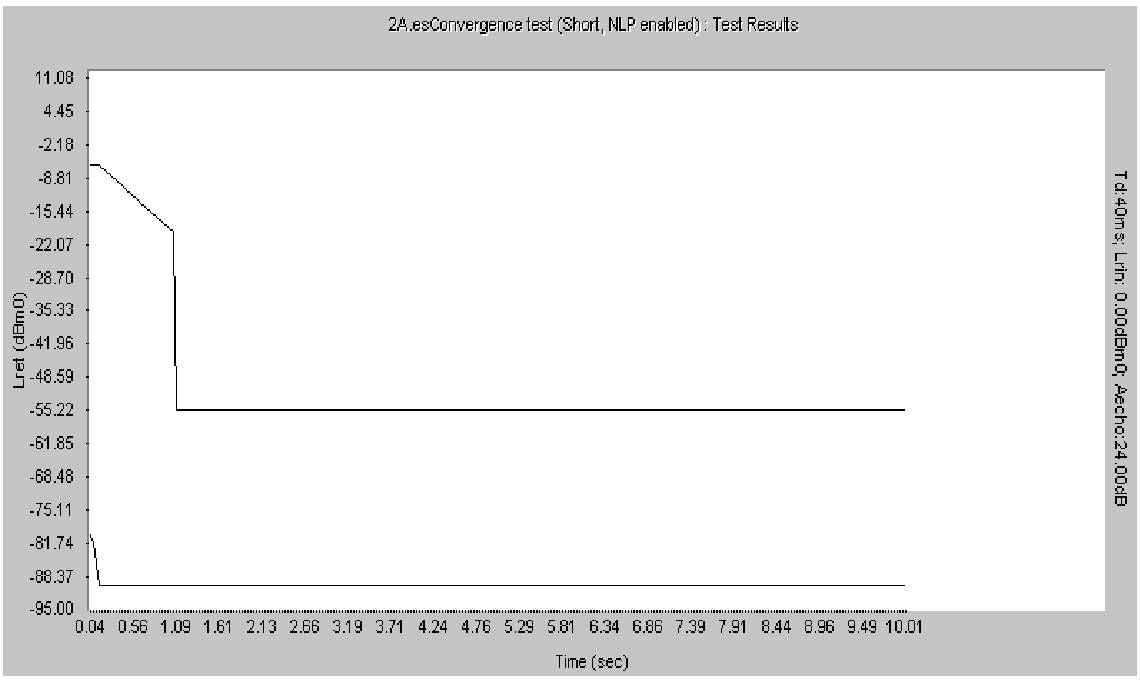


Figure 5 - Sample G.168 Test 2A Convergence Result

1.2 Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the Adaptive Filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo using the previous converged echo profile. A double-talk condition exists whenever the relative signal levels of Rin (Lrin) and Sin (Lsin) meet the following condition:

$$Lsin > Lrin + 20log_{10}(DTDT)$$

where DTDT is the Double-Talk Detection Threshold. Lsin and Lrin are signal levels expressed in dBm0.

A different method is used when it is uncertain whether Sin consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted. The slow convergence speed is set using the Slow sub-register in Control Register 4. During slow convergence, the adaptation speed is reduced by a factor of 2^{Slow} relative to normal convergence for non-zero values of Slow. If Slow equals zero, adaptation is halted completely.

In the G.168 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to achieve additional guardband, the DTDT is set internally to 0.5625 (-5 dB).

In some applications the return loss can be higher or lower than 6 dB. The ZL38065 allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT_{(hex)} = hex(DTDT_{(dec)} * 32768)$$

where $0 < DTDT_{(dec)} < 1$

Example:For DTDT = 0.5625 (-5 dB), the

hexadecimal value becomes

$hex(0.5625 * 32768) = 4800_{hex}$

1.3 Path Change Detector

Integrated into the ZL38065 is a Path Change Detector. This permits fast reconvergence when a major change occurs in the echo channel. Subtle changes in the echo channel are also tracked automatically once convergence is achieved, but at a much slower speed.

The Path Change Detector is activated by setting the PathDet bit in Control Register 3 to "1". An optional path clearing feature can be enabled by setting the PathClr bit in Control Register 3 to "1". With path clearing turned on, the existing echo channel estimate will also be cleared (i.e. the adaptive filter will be filled with zeroes) upon detection of a major path change.

1.4 Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The ZL38065 uses **Zarlink's patented Advanced NLP** to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.168). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20log_{10}(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value and Lrin is the relative power level expressed in dBm0. The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR_{(hex)} = hex(NLPTHR_{(dec)} * 32768)$$

where $0 < NLPTHR_{(dec)} < 1$

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal by an additional 30 dB. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

The NLP processor can be disabled by setting the NLPDis bit to "1" in Control Register 2.

The comfort noise injector can be disabled by setting the INJDis bit to “1” in Control Register 1. It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

The Advanced NLP uses an exponential noise ramping scheme to quickly and more accurately estimate the background noise level. A linear noise ramping method can also be used. The InjCtrl bit in Control Register 3 selects the ramping scheme.

The NLINC register is used to set the ramping speed. When InjCtrl = 1, a lower value will give faster ramping. The Noise Scaling register can be used to adjust the relative volume of the comfort noise. Lowering this value will scale the injected noise level down, conversely, raising the value will scale the comfort noise up.

IMPORTANT NOTE: The Noise Scaling register has been pre-programmed with G.168 compliant values. Changing this value may result in undesirable comfort noise performance and G.168 test failures.

The Advanced NLP also contains safeguards to prevent double-talk and uncancelled echo from being mistaken for background noise. These features can be disabled by setting the NLRun1 and NLRun2 bits in Control Register 3 to “0”.

1.5 Disable Tone Detector

The G.165 recommendation defines the disable tone as having the following characteristics: 2100 Hz (±21 Hz) sine wave, a power level between -6 to -31 dBm0, and a phase reversal of 180 degrees (±25 degrees) every 450 ms (±25 ms). If the disable tone is present for a minimum of one second with at least one phase reversal, the Tone Detector will trigger.

The G.164 recommendation defines the disable tone as a 2100 Hz (±21 Hz) sine wave with a power level between 0 to -31 dBm0. If the disable tone is present for a minimum of 400 ms, with or without phase reversal, the Tone Detector will trigger.

The ZL38065 has two Tone Detectors per channels (for a total of 64) in order to monitor the occurrence of a valid disable tone on both Rin and Sin. Upon detection of a disable tone, TD bit of the Status Register will indicate logic high and an interrupt is generated (i.e., $\overline{IRQ}$ pin low). Refer to Figure 6 and to the **Interrupts** section.

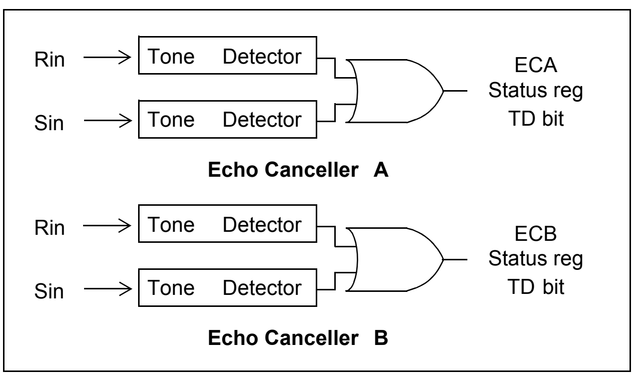


Figure 6 - Disable Tone Detection

Once a Tone Detector has been triggered, there is no longer a need for a valid disable tone (G.164 or G.165) to maintain Tone Detector status (i.e., TD bit high). The Tone Detector status will only release (i.e., TD bit low) if the signals Rin and Sin fall below -30 dBm0, in the frequency range of 390 Hz to 700 Hz, and below -34 dBm0, in the frequency range of 700 Hz to 3400 Hz, for at least 400 ms. Whenever a Tone Detector releases, an interrupt is generated (i.e., $\overline{IRQ}$ pin low).

The selection between G.165 and G.164 tone disable is controlled by the PHDis bit in Control Register 2 on a per channel basis. When the PHDis bit is set to “1”, G.164 tone disable requirements are selected.

In response to a valid disable tone, the echo canceller must be switched from the Enable Adaptation state to the Bypass state. This can be done in two ways, automatically or externally. In automatic mode, the Tone Detectors internally control the switching between Enable Adaptation and Bypass states. The automatic mode is activated by setting the AutoTD bit in Control Register 2 to high. In external mode, an external controller is needed to service the interrupts and poll the TD bits in the Status Registers. Following the detection of a disable tone (TD bit high) on a given channel, the external controller must switch the echo canceller from Enable Adaptation to Bypass state.

1.6 Instability Detector

In systems with very low echo channel return loss (ERL), there may be enough feedback in the loop to cause stability problems in the adaptive filter. This instability can result in variable pitched ringing or oscillation. Should this ringing occur, the Instability Detector will activate and suppress the oscillations.

The Instability Detector is activated by setting the RingClr bit in Control Register 3 to “1”.

1.7 Narrow Band Signal Detector (NBSD)

Single or dual frequency tones (i.e., DTMF tones) present in the receive input (Rin) of the echo canceller for a prolonged period of time may cause the Adaptive Filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this by detecting single or dual tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, adaptation is halted but the echo canceller continues to cancel echo.

The NBSD will be active regardless of the Echo Canceller functional state. However the NBSD can be disabled by setting the NBDis bit to “1” in Control Register 2.

1.8 Offset Null Filter

Adaptive filters in general do not operate properly when a DC offset is present at any input. To remove the DC component, the ZL38065 incorporates Offset Null filters in both Rin and Sin inputs.

The offset null filters can be disabled by setting the HPFDis bit to “1” in Control Register 2.

1.9 Adjustable Level Pads

The ZL38065 provides adjustable level pads at Rin, Rout, Sin and Sout. This setup allows signal strength to be adjusted both inside and outside the echo path. Each signal level may be independently scaled with anywhere from +9 dB to -12 dB level, in 3 dB steps. Level values are set using the Gains register.

CAUTION: Gain adjustment can help interface the ZL38065 to a particular system in order to provide optimum echo cancellation, but it can also degrade performance if not done carefully. Excessive loss may cause low signal levels and slow convergence. Exercise great care when adjusting these values. Also, due to internal signal routings in Back to Back mode, it is not recommended that gain adjustments be used on Rin or Sout in this mode.

The -12 dB PAD bit in Control Register 1 is still supported as a legacy feature. Setting this bit will provide 12 dB of attenuation at Rin, and override the values in the Gains register.

1.10 ITU-T G.168 Compliance

The ZL38065 has been certified G.168 (1997), (2000) and (2002) compliant in all 64 ms cancellation modes (i.e., Normal and Back-to-Back configurations) by in-house testing with the DSPG ECT-1 echo canceller tester.

The ZL38065 has also been tested for G.168 compliance and all voice quality tests at AT&T Labs. The ZL38065 was classified as “carrier grade” echo canceller.

2.0 Device Configuration

The ZL38065 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers which can be individually controlled (Echo Canceller A (ECA) and Echo Canceller B (ECB)). They can be set in three distinct configurations: **Normal, Back-to-Back,** and **Extended Delay**. See Figures 7, 8 and 9.

2.1 Normal Configuration

In Normal configuration, the two echo cancellers (Echo Canceller A and B) are positioned in parallel, as shown in Figure 7, providing 64 milliseconds of echo cancellation in two channels simultaneously.

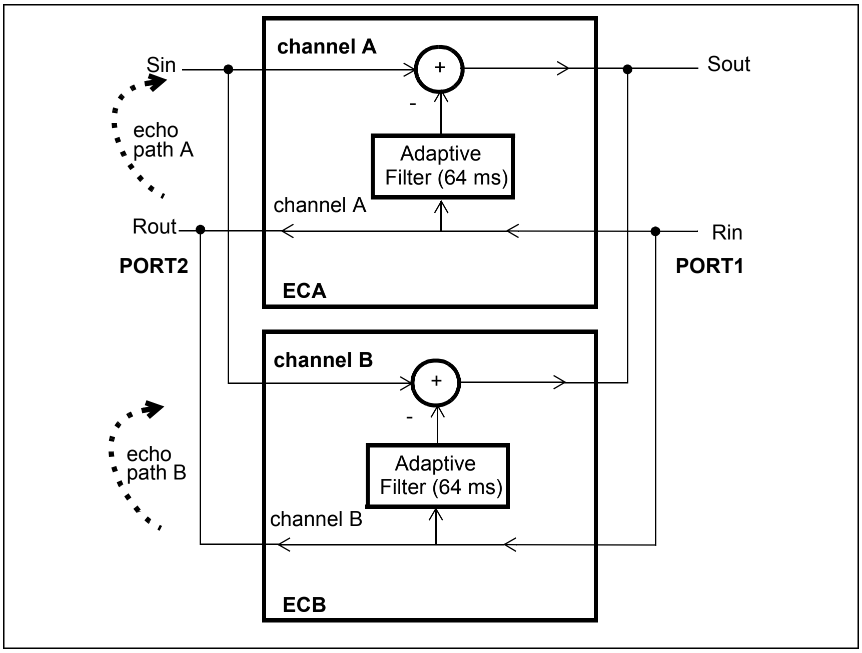


Figure 7 - Normal Device Configuration (64 ms)

2.2 Back-to-Back Configuration

In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel providing full-duplex 64 ms echo cancellation. See Figure 8. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains zero code. Back-to-Back configuration allows a no-glue interface for applications where bidirectional echo cancellation is required.

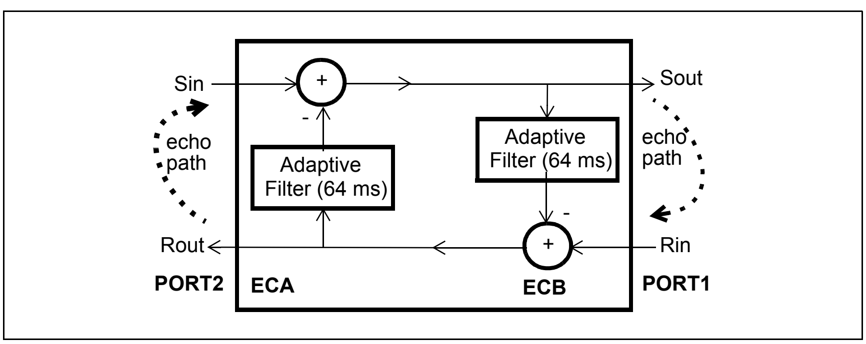


Figure 8 - Back-to-Back Device Configuration (64 ms)

Back-to-Back configuration is selected by writing a “1” into the BBM bit of Control Register 1 for **both** Echo Canceller A and Echo Canceller B for a given group of echo canceller. Table 3 shows the 16 groups of 2 cancellers that can be configured into Back-to-Back.

Examples of Back-to-Back configuration include positioning one group of echo cancellers between a codec and a transmission device or between two codecs for echo control on analog trunks.

2.3 Extended Delay Configuration

In this configuration, the two echo cancellers from the same group are internally cascaded into one 128 milliseconds echo canceller. See Figure 9. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains quiet code.

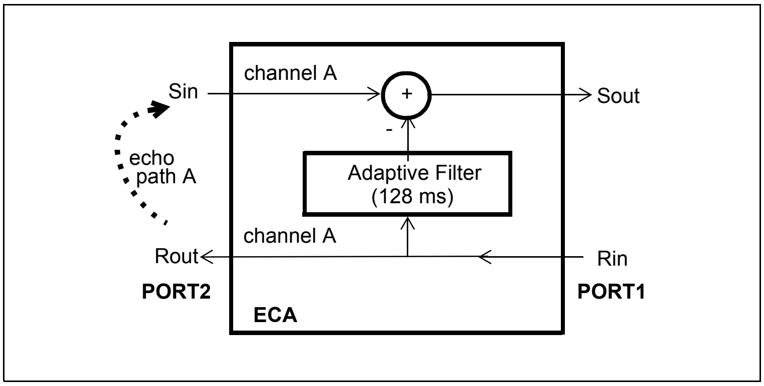


Figure 9 - Extended Delay Configuration (128 ms)

Extended Delay configuration is selected by writing a “1” into the ExtDl bit in Echo Canceller A, Control Register 1. For a given group, only Echo Canceller A, Control Register 1, has the ExtDl bit. For Echo Canceller B Control Register 1, Bit 0 must always be set to zero.

Table 3 shows the 16 groups of 2 cancellers that can each be configured into 64 ms or 128 ms echo tail capacity.

3.0 Echo Canceller Functional States

Each echo canceller has four functional states: **Mute, Bypass, Disable Adaptation** and **Enable Adaptation**.

3.1 Mute

In Normal and in Extended Delay configurations, writing a “1” into the MuteR bit replaces Rin with quiet code which is applied to both the Adaptive Filter and Rout. Writing a “1” into the MuteS bit replaces the Sout PCM data with quiet code.

	LINEAR 16 bits 2’s complement	**SIGN/ MAGNITUDE μ-Law A-Law**	**CCITT (G.711)**	
			μ-Law	**A-Law**
+Zero (quiet code)	0000_{hex}	80_{hex}	FF_{hex}	$D5_{hex}$

Table 1 - Quiet PCM Code Assignment

In Back-to-Back configuration, writing a “1” into the MuteR bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Rout. Writing a “1” into the MuteS bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Sout.

In Extended Delay and in Back-to-Back configurations, MuteR and MuteS bits of Echo Canceller B must always be “0”. Refer to Figure 4 and to Control Register 2 for bit description.

3.2 Bypass

The Bypass state directly transfers PCM codes from Rin to Rout and from Sin to Sout. **When Bypass state is selected, the Adaptive Filter coefficients are reset to zero.** Bypass state must be selected for at least one frame (125 μs) in order to properly clear the filter.

3.3 Disable Adaptation

When the Disable Adaptation state is selected, the Adaptive Filter coefficients are frozen at their current value. The adaptation process is halted, however, the echo canceller continues to cancel echo.

3.4 Enable Adaptation

In Enable Adaptation state, the Adaptive Filter coefficients are continually updated. This allows the echo canceller to model the echo return path characteristics in order to cancel echo. This is the normal operating state.

The echo canceller functions are selected in Control Register 1 and Control Register 2 through four control bits: MuteS, MuteR, Bypass and AdaptDis. Refer to the Registers Description for details.

4.0 ZL38065 Throughput Delay

The throughput delay of the ZL38065 varies according to the device configuration. For all device configurations, Rin to Rout has a delay of two frames and Sin to Sout has a delay of three frames. In Bypass state, the Rin to Rout and Sin to Sout paths have a delay of two frames.

5.0 Serial PCM I/O channels

There are two sets of TDM I/O streams, each with channels numbered from 0 to 31. One set of input streams is for Receive (Rin) channels, and the other set of input streams is for Send (Sin) channels. Likewise, one set of output streams is for Rout PCM channels, and the other set is for Sout channels. See Figure 10 for channel allocation.

The arrangement and connection of PCM channels to each echo canceller is a 2 port I/O configuration for each set of PCM Send and Receive channels, as illustrated in Figure 4.

5.1 Serial Data Interface Timing

The ZL38065 provides ST-BUS and GCI interface timing. The Serial Interface clock frequency, $\overline{\text{C4i}}$, is 4.096 MHz. The input and output data rate of the ST-BUS and GCI bus is 2.048 Mbps.

The 8 KHz input frame pulse can be in either ST-BUS or GCI format. The ZL38065 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS or GCI. In ST-BUS format, every second falling edge of the $\overline{\text{C4i}}$ clock marks a bit boundary, and the data is clocked in on the rising edge of $\overline{\text{C4i}}$, three quarters of the way into the bit cell (See Figure 14). In GCI format, every second rising edge of the $\overline{\text{C4i}}$ clock marks the bit boundary, and data is clocked in on the second falling edge of $\overline{\text{C4i}}$, half the way into the bit cell (see Figure 15).

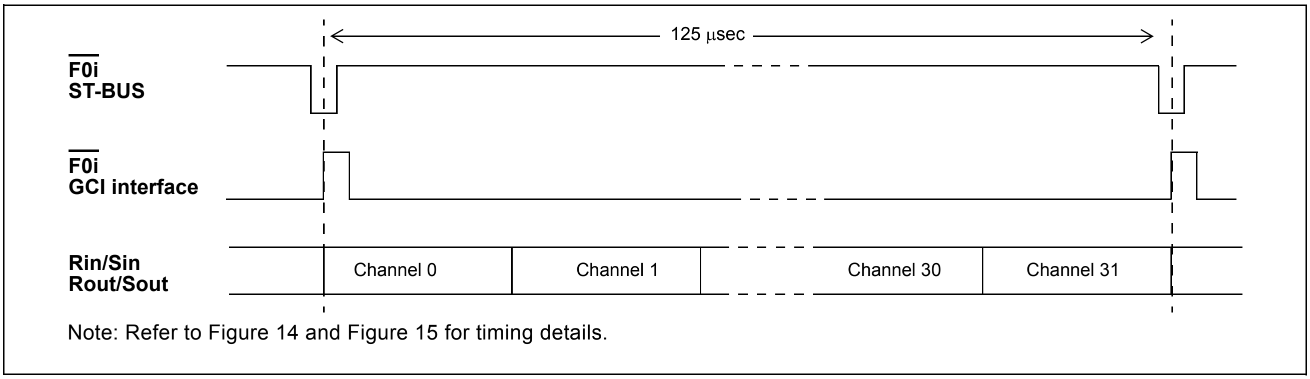


Figure 10 - ST-BUS and GCI Interface Channel Assignment for 2 Mbps Data Streams

6.0 Memory Mapped Control and Status Registers

Internal memory and registers are memory mapped into the address space of the HOST interface. The internal dual ported memory is mapped into segments on a “per channel” basis to monitor and control each individual echo canceller and associated PCM channels. For example, in **Normal configuration**, echo canceller #5 makes use of Echo Canceller B from group 2. It occupies the internal address space from $0A0_{hex}$ to $0BF_{hex}$ and interfaces to PCM channel #5 on all serial PCM I/O streams.

Page	A12	A11
0	0	0
1	0	1
2	1	0
3	1	1

Table 2 - Memory Page Selection

As illustrated in Table 4, the “per channel” registers provide independent control and status bits for each echo canceller. Figure 11 shows the memory map of the control/status register blocks for all echo cancellers.

Each internal echo canceller has four pages of registers. Page access control is done through address lines A11 and A12. The majority of registers are located on page 0 (A11=0, A12=0). Figure 11 shows which page each of the relevant registers are mapped to respectively. Table 2 shows how the memory pages are related to address lines A11 and A12.

When **Extended Delay** or **Back-to-Back** configuration is selected, Control Register 1 of ECA and ECB and Control Register 2 of the selected group of echo cancellers require special care. Refer to the Register description section.

Table 3 is a list of the channels used for the 16 groups of echo cancellers when they are configured as **Extended Delay** or **Back-to-Back.**

6.1 Normal Configuration

For a given group (group 0 to 15), 2 PCM I/O channels are used. For example, group 1 Echo Cancellers A and B, channels 2 and 3 are active.

Group	Channels	Group	Channels
0	0, 1	8	16, 17
1	2, 3	9	18, 19
2	4, 5	10	20, 21
3	6, 7	11	22, 23
4	8, 9	12	24, 25
5	10, 11	13	26, 27
6	12, 13	14	28, 29
7	14, 15	15	30, 31

Table 3 - Group and Channel Allocation

6.2 Extended Delay Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 2, Echo Canceller A (Channel 4) will be active and Echo Canceller B (Channel 5) will carry quiet code.

6.3 Back-to-Back Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 5, Echo Canceller A (Channel 10) will be active and Echo Canceller B (Channel 11) will carry quiet code.

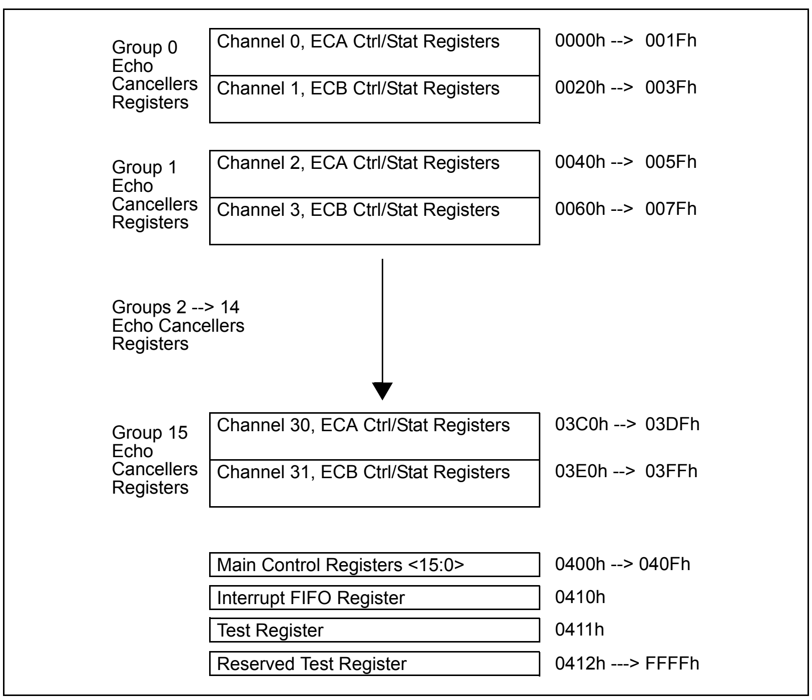


Figure 11 - Memory Mapping

Base Address +			Echo Canceller A		Base Address +			Echo Canceller B
Page	MS Byte	LS Byte	Register Name		Page	MS Byte	LS Byte	Register Name
0	-	00h	Control Reg 1		0	-	20h	Control Reg 1
0	-	01h	Control Reg 2		0	-	21h	Control Reg 2
0	-	02h	Status Reg		0	-	22h	Status Reg
0	-	04h	Flat Delay Reg		0	-	24h	Flat Delay Reg
0	-	06h	Decay Step Size Reg		0	-	26h	Decay Step Size Reg
0	-	07h	Decay Step Number		0	-	27h	Decay Step Number
0	-	08h	Control Reg 3		0	-	28h	Control Reg 3
0	-	09h	Control Reg 4		0	-	29h	Control Reg 4
0	0Dh	0Ch	Rin Peak Detect Reg		0	2Dh	2Ch	Rin Peak Detect Reg
0	0Fh	0Eh	Sin Peak Detect Reg		0	2Fh	2Eh	Sin Peak Detect Reg
0	11h	10h	Error Peak Detect Reg		0	31h	30h	Error Peak Detect Reg
0	-	12h	Path Change Timer		0	-	32h	Path Change Timer
0	-	13h	Path Change Sensitivity		0	-	33h	Path Change Sensitivity
0	15h	14h	DTDT/ERL		0	35h	34h	DTDT/ERL
0	17h	16h	ERLLOW		0	37h	36h	ERLLOW
0	19h	18h	NLP Threshold		0	39h	38h	NLP Threshold
0	1Bh	1Ah	Step Size, MU		0	3Bh	3Ah	Step Size, MU
0	1Dh	1Ch	Gain Pad Control		0	3Dh	3Ch	Gain Pad Control
0	-	1Eh	NLP Threshold 2		0	-	3Eh	NLP Threshold 2
0	-	1Fh	RIN Low Power Threshold		0	-	3Fh	RIN Low Power Threshold
1	05h	04h	Estimated Cancellation		1	25h	24h	Estimated Cancellation
1	07h	06h	Residual Error Signal		1	27h	26h	Residual Error Signal
2	11h	10h	NLINC		2	11h	10h	NLINC
2	19h	18h	Maximum Comfort Noise		2	39h	38h	Maximum Comfort Noise
2	1Bh	1Ah	NLP Ramp-out Speed		2	3Bh	3Ah	NLP Ramp-out Speed
2	1Dh	1Ch	NLP Ramp-in Speed		2	3Dh	3Ch	NLP Ramp-in Speed
3	03h	02h	Noise Level Estimate		3	23h	22h	Noise Level Estimate
3	05h	04h	NLP Gain Factor		3	25h	24h	NLP Gain Factor
3	0Dh	0Ch	Noise Level Scaling Factor		3	2Dh	2Ch	Noise Level Scaling Factor

Table 4 - Memory Mapping of Per Channel Control and Status Registers

6.4 Power Up Sequence

On power up, the RESET pin must be held low for 100 µs. Forcing the RESET pin low will put the ZL38065 in power down state. In this state, all internal clocks are halted, D<7:0>, Sout, Rout, DTA and IRQ pins are tristated. The 16 Main Control Registers, the Interrupt FIFO Register and the Test Register are reset to zero.

When the RESET pin returns to logic high and a valid MCLK is applied, the user must wait 500 µs for the PLL to lock. C4i and F0i can be active during this period. At this point, the echo canceller must have the internal registers reset to an initial state. This is accomplished by one of two methods. The user can either issue a second hardware reset or perform a software reset. A second hardware reset is performed by driving the RESET pin low for at least 500 ns and no more than 1500 ns before being released. A software reset is accomplished by programming a “1” to each of the PWUP bits in the Main Control Registers, waiting 250 µs (2 frames) and then programming a “0” to each of the PWUP bits.

The user must then wait 500 µs for the PLL to relock. Once the PLL has locked, the user can power up the 16 groups of echo cancellers individually by writing a “1” into the PWUP bit in Main Control Register of each echo canceller group.

For each group of echo cancellers, when the PWUP bit toggles from zero to one, echo cancellers A and B execute their initialization routine. The initialization routine sets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to the default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly.

Once the initialization routine is executed, the user can set the per channel Control Registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, for the specific application.

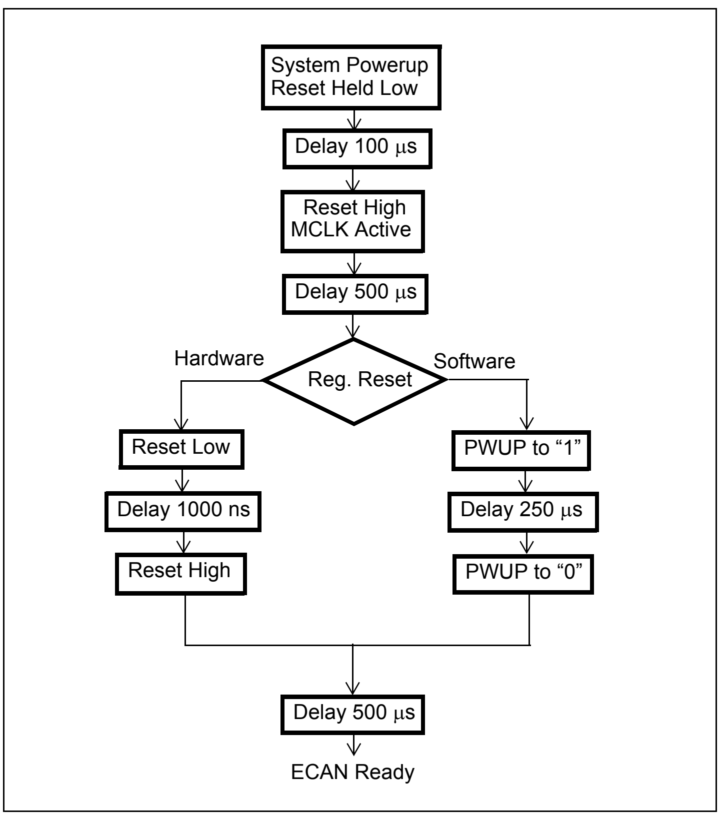


Figure 12 - Power Up Sequence Flow Diagram

6.5 Power Management

Each group of echo cancellers can be placed in Power Down mode by writing a “0” into the PWUP bit in their respective Main Control Register. When a given group is in Power Down mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. Refer to the Main Control Register section on page 38 for description.

The typical power consumption can be calculated with the following equation:

$$P_C = 9 * Nb\_of\_groups + 3.6, \text{ in } mW$$

where $0 \leq Nb\_of\_groups \leq 16$.

6.6 Call Initialization

To ensure fast initial convergence on a new call, it is important to clear the Adaptive Filter. This is done by putting the echo canceller in bypass mode for at least one frame (125 μs) and then enabling adaptation.

Since the Narrow Band Detector is “ON” regardless of the functional state of Echo Canceller it is recommended that the Echo cancellers are reset before any call progress tones are applied.

6.7 Interrupts

The ZL38065 provides an interrupt pin ($\overline{IRQ}$) to indicate to the HOST processor when a G.164 or G.165 Tone Disable is detected and released.

Although the ZL38065 may be configured to react automatically to tone disable status on any input PCM voice channels, the user may want for the external HOST processor to respond to Tone Disable information in an appropriate application-specific manner.

Each echo canceller will generate an interrupt when a Tone Disable occurs and will generate another interrupt when a Tone Disable releases.

Upon receiving an $\overline{IRQ}$, the HOST CPU should read the Interrupt FIFO Register. This register is a FIFO memory containing the channel number of the echo canceller that has generated the interrupt.

All pending interrupts from any of the echo cancellers and their associated input channel number are stored in this FIFO memory. The $\overline{IRQ}$ always returns high after a read access to the Interrupt FIFO Register. The $\overline{IRQ}$ pin will toggle low for each pending interrupt.

After the HOST CPU has received the channel number of the interrupt source, the corresponding per channel Status Register can be read from internal memory to determine the cause of the interrupt (see Table 4 for address mapping of Status register). The TD bit indicates the presence of a Tone Disable.

The MIRQ bit 5 in the Main Control Register 0 masks interrupts from the ZL38065. To provide more flexibility, the MTDBI (bit-4) and MTDAI (bit-3) bits in the Main Control Register<15:0> allow Tone Disable to be masked or unmasked from generating an interrupt on a per channel basis. Refer to the Registers Description section on page 38.

7.0 JTAG Support

The ZL38065 JTAG interface conforms to the Boundary-Scan standard IEEE1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the Boundary Scan circuitry is controlled by an Test Access Port (TAP) controller. JTAG inputs are **3.3 V** compliant only.

7.1 Test Access Port (TAP)

The TAP provides access to many test functions of the ZL38065. It consists of four input pins and one output pin. The following pins are found on the TAP.

- Test Clock Input (TCK)
  The TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrent with the operation of the device and without interfering with the on-chip logic.
- Test Mode Select Input (TMS)
  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to V_{DD1} when it is not driven from an external source.
- Test Data Input (TDI)
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD1} when it is not driven from an external source.
- Test Data Output (TDO)
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data from the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the Boundary Scan cells, the TDO driver is set to a high impedance state.
- Test Reset (TRST)
  This pin is used to reset the JTAG scan structure. This pin is internally pulled to V_{SS}.

7.2 Instruction Register

In accordance with the IEEE 1149.1 standard, the ZL38065 uses public instructions. The JTAG Interface contains a 3-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that will operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

7.3 Test Data Registers

As specified in IEEE 1149.1, the ZL38065 JTAG Interface contains three test data registers:

- Boundary-Scan register
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL38065 core logic.
- Bypass Register
  The Bypass register is a single stage shift register that provides a one-bit path from TDI to TDO.
- Device Identification register
  The Device Identification register provides access to the following encoded information:
  device version number, part number and manufacturer's name.

8.0 Register Description

Power-up 00$_{hex}$	**ECA: Control Register 1**				**Page 0 A12=0 A11=0**	**R/W Address: 00$_{hex}$ + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	INJDis	BBM	PAD	Bypass	AdpDis	0	ExtDis

Functional Description of Register Bits	
Reset	When high, the power-up initialization is executed. This presets all register bits including this bit and clears the Adaptive Filter coefficients.
INJDis	When high, the noise injection process is disabled. When low noise injection is enabled.
BBM	When high, the Back to Back configuration is enabled. When low, the Normal configuration is enabled. Note: Do not enable Extended-Delay and BBM configurations at the same time. Always set **both** BBM bits of the two echo cancellers (Control Register 1) of the same group to the same logic value to avoid conflict.
PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low, the Gains register controls the signal levels.
Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. The Adaptive Filter coefficients are set to zero and the filter adaptation is stopped. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.
AdpDis	When high, echo canceller adaptation is disabled. The Voice Processor cancels echo. When low, the echo canceller dynamically adapts to the echo path characteristics.
0	Bits marked as “1” or “0” are reserved bits and should be written as indicated.
ExtDI	When high, Echo Cancellers A and B of the same group are internally cascaded into one 128 ms echo canceller. When low, Echo Cancellers A and B of the same group operate independently.

Power-up 02$_{hex}$	**ECB: Control Register 1**				**Page 0 A12=0 A11=0**	**R/W Address: 20$_{hex}$ + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	INJDis	BBM	PAD	Bypass	AdpDis	1	0

Functional Description of Register Bits	
Reset	When high, the power-up initialization is executed which presets all register bits including this bit and clears the Adaptive Filter coefficients.
INJDis	When high, the noise injection process is disabled. When low, noise injection is enabled.
BBM	When high, the Back to Back configuration is enabled. When low, the Normal configuration is enabled. Note: Do not enable Extended-Delay and BBM configurations at the same time. Always set **both** BBM bits of the two echo cancellers (Control Register 1) of the same group to the same logic value to avoid conflict.
PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low, the Gains register controls the signal levels.
Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. The Adaptive Filter coefficients are set to zero and the filter adaptation is stopped. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.
AdpDis	When high, echo canceller adaptation is disabled. The Voice Processor cancels echo. When low, the echo canceller dynamically adapts to the echo path characteristics.
1	Bits marked as “1” or “0” are reserved bits and should be written as indicated.
0	Control Register 1 (Echo Canceller B) Bit 0 is a reserved bit and should be written “0”.

Power-up 00_{hex}	ECA: Control Register 2				Page 0	R/W Address: 01_{hex} + Base Address	
	ECB: Control Register 2				A12=0 A11=0	R/W Address: 21_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDis	PHDis	NLPDis	AutoTD	NBDis	HPFDis	MuteS	MuteR
Functional Description of Register Bits							
TDis	When high, tone detection is disabled. When low, tone detection is enabled. When both Echo Cancellers A and B TDis bits are high, Tone Disable processors are disabled entirely and are put into Power Down mode.						
PHDis	When high, the tone detectors will trigger upon the presence of a 2100 Hz tone regardless of the presence/absence of periodic phase reversals. When low, the tone detectors will trigger only upon the presence of a 2100 Hz tone with periodic phase reversals.						
NLPDis	When high, the non-linear processor is disabled. When low, the non-linear processors function normally. Useful for G.165 conformance testing.						
AutoTD	When high, the echo canceller puts itself in Bypass mode when the tone detectors detect the presence of 2100 Hz tone. See PHDis for qualification of 2100 Hz tones. When low, the echo canceller algorithm will remain operational regardless of the state of the 2100 Hz tone detectors.						
NBDis	When high, the narrow-band detector is disabled. When low, the narrow-band detector is enabled.						
HPFDis	When high, the offset nulling high pass filters are bypassed in the Rin and Sin paths. When low, the offset nulling filters are active and will remove DC offsets on PCM input signals.						
MuteS	When high, data on Sout is muted to quiet code. When low, Sout carries active code.						
MuteR	When high, data on Rout is muted to quiet code. When low, Rout carries active code.						

Note: In order to correctly write to Control Register 1 and 2 of ECB, it is necessary to write the data twice to the register, one immediately after another. The two writes must be separated by at least 350 ns and no more than 20 us.

Power-up N/A	ECA: Status Register				Page 0	Read Address: 02_{hex} + Base Address	
	ECB: Status Register				A12=0 A11=0	Read Address: 22_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TD	DTDet	Reserved	Reserved	ACTIVE	TDG	NB
Functional Description of Register Bits							
Reserved	Reserved bit.						
TD	Logic high indicates the presence of a 2100 Hz tone.						
DTDet	Logic high indicates the presence of a double-talk condition.						
Reserved	Reserved bit.						
Reserved	Reserved bit.						
ACTIVE	Logic high indicates that the level on Rin has exceeded the LP threshold.						
TDG	Tone detection status bit gated with the AutoTD bit. (Control Register 2) Logic high indicates that AutoTD has been enabled and the tone detector has detected the presence of a 2100 Hz tone.						
NB	Logic high indicates the presence of a narrow-band signal on Rin.						

Power-up 00_{hex}	ECA: Flat Delay Register (FD)					Page 0	R/W Address: 04_{hex} + Base Address
	ECB: Flat Delay Register (FD)					A12=0 A11=0	R/W Address: 24_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Power-up 00_{hex}	ECA: Decay Step Number Register (NS))					Page 0	R/W Address: 07_{hex} + Base Address
	ECB: Decay Step Number Register (NS)					A12=0 A11=0	R/W Address: 27_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Power-up 04_{hex}	ECA: Decay Step Size Control Register (SSC)					Page 0	R/W Address: 06_{hex} + Base Address
	ECB: Decay Step Size Control Register (SSC)					A12=0 A11=0	R/W Address: 26_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	SSC2	SSC1	SSC0

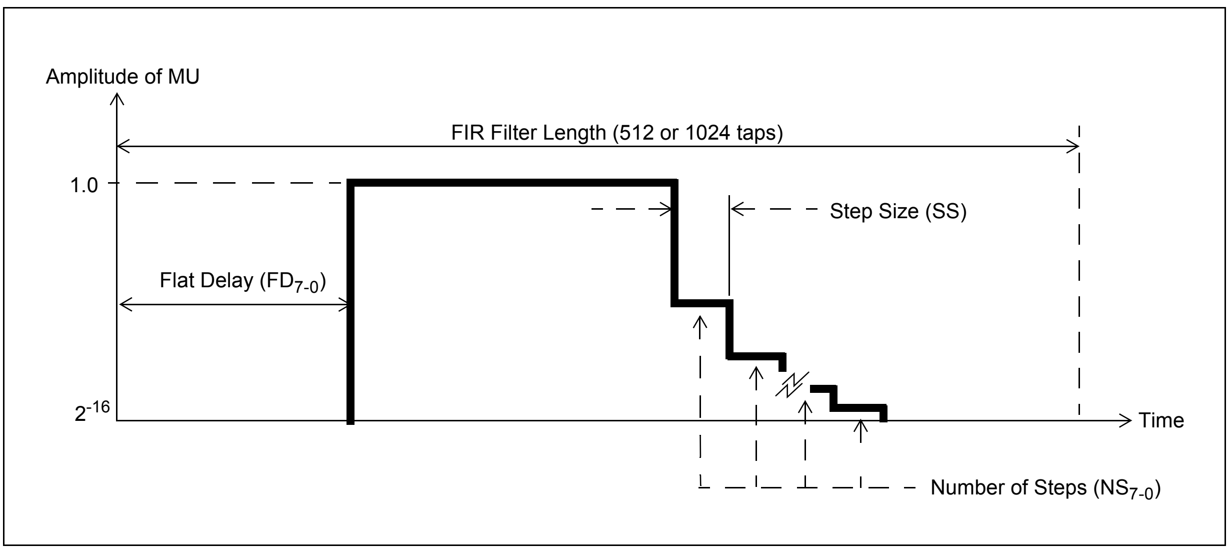


Figure 13 - The MU Profile

Functional Description of Register Bits

The Exponential Decay registers (Decay Step Number and Decay Step Size) and Flat Delay register allow the LMS adaptation step-size (MU) to be programmed over the length of the FIR filter. A programmable MU profile allows the performance of the echo canceller to be optimized for specific applications. For example, if the characteristic of the echo response is known to have a flat delay of several milliseconds and a roughly exponential decay of the echo impulse response, then the MU profile can be programmed to approximate this expected impulse response thereby improving the convergence characteristics of the Adaptive Filter. Note that in the following register descriptions, one tap is equivalent to 125 μs (64 ms/512 taps).

FD_{7-0} **Flat Delay**: This register defines the flat delay of the MU profile, (i.e., where the MU value is 2^{-16}). The delay is defined as FD_{7-0} x 8 taps. For example; If FD_{7-0} = 5, then MU=2^{-16} for the first 40 taps of the echo canceller FIR filter. The valid range of FD_{7-0} is: $0 \le FD_{7-0} \le 64$ in normal mode and $0 \le FD_{7-0} \le 128$ in extended-delay mode. The default value of FD_{7-0} is zero.

SSC_{2-0} **Decay Step Size Control**: This register controls the step size (SS) to be used during the exponential decay of MU. The decay rate is defined as a decrease of MU by a factor of 2 every SS taps of the FIR filter, where SS = 4 $x2^{SSC_{2-0}}$. For example; If SSC_{2-0} = 4, then MU is reduced by a factor of 2 every 64 taps of the FIR filter. The default value of SSC_{2-0} is 04_{hex}.

NS_{7-0} **Decay Step Number**: This register defines the number of steps to be used for the decay of MU where each step has a period of SS taps (see SSC_{2-0}). The start of the exponential decay is defined as: Filter Length (512 or 1024) - [Decay Step Number (NS_{7-0}) x Step Size (SS)] where SS = 4 $x2^{SSC_{2-0}}$.
For example; If NS_{7-0}=4 and SSC_{2-0}=4, then the exponential decay start value is 512 - [NS_{7-0} x SS] = 512 - [4 x ($4x2^4$)] = 256 taps for a filter length of 512 taps.

Power-up DB_{hex}	ECA: Control Register 3				Page 0	R/W Address: 08_{hex} + Base Address	
	ECB: Control Register 3				A12=0 A11=0	R/W Address: 28_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLRun2	InjCtrl	NLRun1	RingClr	Reserve	PathClr	PathDet	NMatcj

Functional Description of Register Bits	
Reserved	Reserved bit.
Reserved	Reserved bit.
NLRun1	When high, the comfort noise level estimator actively rejects uncancelled echo as being background noise. When low, the noise level estimator makes no such distinction.
RingClr	When high, the instability detector is activated. When low, the instability detector is disabled.
Reserve	Reserved bit. Must always be set to one for normal operation.
PathClr	When high, the current echo channel estimate will be cleared and the echo canceller will enter fast convergence mode upon detection of a path change. When low, the echo canceller will keep the current path estimate but revert to fast convergence mode upon detection of a path change. Note: this bit is ignored if PathDet is low.
PathDet	When high, the path change detector is activated. When low, the path change detector is disabled.
Reserved	Reserved bit.

Power-up 54_{hex}	ECA: Control Register 4				Page 0	R/W Address: 09_{hex} + Base Address	
	ECB: Control Register 4				A12=0 A11=0	R/W Address: 29_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SD2	SD1	SD0	0	Slow2	Slow1	Slow0
Functional Description of Register Bits							
0	Must be set to zero.						
SupDec	These three bits (SD2,SD1,SD0) control how long the echo canceller remains in a fast convergence state following a path change, Reset or Bypass operation. A value of zero will keep the echo canceller in fast convergence indefinitely.						
0	Must be set to zero.						
Slow	Slow convergence mode speed adjustment.(Bits Slow2, Slow1,Slow0) For Slow = 1, 2, ..., 7, slow convergence speed is reduced by a factor of 2^{Slow} as compared to normal adaptation. For Slow = 0, no adaptation occurs during slow convergence.						

Power-up N/A	ECA: Rin Peak Detect Register 2 (RP)				Page 0	Read Address: $0D_{hex}$ + Base Address	
	ECB: Rin Peak Detect Register 2 (RP)				A12=0 A11=0	Read Address: $2D_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
Power-up N/A	ECA: Rin Peak Detect Register 1 (RP)				Page 0	Read Address: $0C_{hex}$ + Base Address	
	ECB: Rin Peak Detect Register 1 (RP)				A12=0 A11=0	Read Address: $2C_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the receive in (Rin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up N/A	ECA: Sin Peak Detect Register 2 (SP)				Page 0	Read Address: 0F$_{hex}$ + Base Address	
	ECB: Sin Peak Detect Register 2 (SP)				A12=0 A11=0	Read Address: 2F$_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
Power-up N/A	ECA: Sin Peak Detect Register 1 (SP)				Page 0	R/W Address: 0E$_{hex}$ + Base Address	
	ECB: Sin Peak Detect Register 1 (SP)				A12=0 A11=0	R/W Address: 2E$_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the send in (Sin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up N/A	ECA: Error Peak Detect Register 2 (EP)				Page 0	Read Address: 11$_{hex}$ + Base Address	
	ECB: Error Peak Detect Register 2 (EP))				A12=0 A11=0	Read Address: 21$_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8
Power-up N/A	ECA: Error Peak Detect Register 1 (EP)				Page 0	Read Address: 10$_{hex}$ + Base Address	
	ECB: Error Peak Detect Register 1 (EP)				A12=0 A11=0	Read Address: 30$_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the error signal peak level. The information is in 16 bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller.							

Power-up 10$_{hex}$	ECA: Path Change Timer (PATHTMR)				Page 0	R/W Address: 12$_{hex}$ + Base Address	
	ECB: Path Change Timer (PATHTMR)				A12=0 A11=0	R/W Address: 32$_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTMR7	PTMR6	PTMR5	PTMR4	PTMR3	PTMR2	PTMR1	PTMR0
Functional Description of Register Bits							
Negative ERLE time required to declare a path change. Raising this value decreases the path change sensitivity.							

Power-up 41_{hex}	**ECA: Path Change Sensitivity (PTHSENS)**				**Page 0**	**R/W Address: 13_{hex} + Base Address**	
	ECB: Path Change Sensitivity (PTHSENS)				**A12=0 A11=0**	**R/W Address: 33_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSENS7	PSENS6	PSENS5	PSENS4	PSENS3	PSENS2	PSENS1	PSENS0
Functional Description of Register Bits							
This register sets the negative ERLE sensitivity value. Raising this value decreases path change sensitivity.							

Power-up 48_{hex}	**ECA: Double-Talk Detection Threshold Register 2 (DTDT or ERL)**				**Page 0**	**R/W Address: 15_{hex} + Base Address**	
	ECB: Double-Talk Detection Threshold Register 2 (DTDT or ERL)				**A12=0 A11=0**	**R/W Address: 35_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTDT15	DTDT14	DTDT13	DTDT12	DTDT11	DTDT10	DTDT9	DTDT8
Power-up 00_{hex}	**ECA: Double-Talk Detection Threshold Register 1 (DTDT or ERL)**				**Page 0**	**R/W Address: 14_{hex} + Base Address**	
	ECB: Double-Talk Detection Threshold Register 1 (DTDT or ERL)				**A12=0 A11=0**	**R/W Address: 34_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTDT7	DTDT6	DTDT5	DTDT4	DTDT3	DTDT2	DTDT1	DTDT0
Functional Description of Register Bits							
This register should reflect the minimum return echo level (SIN) relative to ROUT expected in the system. The default value of 4800_{hex}= 0.5625 represents a path loss of -5 dB. This value sets the high-level double-talk detection threshold (DTDT). The information is in 16 bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The maximum value is $7FFF_{hex}$ = 0.9999 or 0 dB.							

Power-up 04_{hex}	**ECA: SUP Lower Limit 2 (ERLLOW)**				**Page 0**	**R/W Address: 17_{hex} + Base Address**	
	ECB: SUP Lower Limit 2 (ERLLOW)				**A12=0 A11=0**	**R/W Address: 37_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERLW15	ERLW14	ERLW13	ERLW12	ERLW11	ERLW10	ERLW9	ERLW8
Power-up 00_{hex}	**ECA: SUP Lower Limit 1 (ERLLOW)**				**Page 0**	**R/W Address: 16_{hex} + Base Address**	
	ECB: SUP Lower Limit 1 (ERLLOW)				**A12=0 A11=0**	**R/W Address: 36_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERLW7	ERLW6	ERLW5	ERLW4	ERLW3	ERLW2	ERLW1	ERLW0
Functional Description of Register Bits							
This register sets the lower limit on SUP, which marks the region below which fast convergence always occurs (provided a signal is present). If ERLLOW is set to the DTDT starting value (4800_{hex}), the echo canceller will remain in fast convergence mode and will not switch to slow convergence. The information is in 16 bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller.							

Power-up $0C_{hex}$	ECA: Non-Linear Processor Threshold Register 2 (NLPTHR)				Page 0 A12=0 A11=0	R/W Address: 19_{hex} + Base Address	
	ECB: Non-Linear Processor Threshold Register 2 (NLPTHR)					R/W Address: 39_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLP15	NLP14	NLP13	NLP12	NLP11	NLP10	NLP9	NLP8
Power-up $E0_{hex}$	ECA: Non-Linear Processor Threshold Register 1 (NLPTHR)				Page 0 A12=0 A11=0	R/W Address: 18_{hex} + Base Address	
	ECB: Non-Linear Processor Threshold Register 1 (NLPTHR)					R/W Address: 38_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLP7	NLP6	NLP5	NLP4	NLP3	NLP2	NLP1	NLP0
Functional Description of Register Bits							
This register allows the user to program the level of the Non-Linear Processor Threshold (NLPTHR). The 16 bit 2's complement linear value defaults to $0CE0_{hex}$ = 0.1 or -20.0 dB. The maximum value is $7FFF_{hex}$ = 0.9999 or 0 dB.							

Power-up 40_{hex}	ECA: Adaptation Step Size Register 2 (MU)				Page 0 A12=0 A11=0	R/W Address: $1B_{hex}$ + Base Address	
	ECB: Adaptation Step Size Register 2 (MU)					R/W Address: $3B_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MU15	MU14	MU13	MU12	MU11	MU10	MU9	MU8
Power-up 00_{hex}	ECA: Adaptation Step Size Register 1 (MU)				Page 0 A12=0 A11=0	R/W Address: $1A_{hex}$ + Base Address	
	ECB: Adaptation Step Size Register 1 (MU)					R/W Address: $3A_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MU7	MU6	MU5	MU4	MU3	MU2	MU1	MU0
Functional Description of Register Bits							
This register allows the user to program the level of MU, which is the LMS filter step size. Increasing this value can speed up convergence times, but can also potentially decrease VEC stability. MU is a 16 bit 2's complement value which defaults to 4000_{hex} = 1.0 The maximum value is $7FFF_{hex}$ or 1.9999 decimal. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up 40_{hex}	ECA: Gains Register 2				Page 0	R/W Address: $1D_{hex}$ + Base Address	
	ECB: Gains Register 2				A12=0 A11=0	R/W Address: $3D_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Rin2	Rin1	Rin0	0	Rout2	Rout1	Rout0
Power-up 00_{hex}	ECA: Gains Register1				Page 0	R/W Address: $1C_{hex}$ + Base Address	
	ECB: Gains Register 1				A12=0 A11=0	R/W Address: $3C_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Sin2	Sin1	Sin0	0	Sout2	Sout1	Sout0
Functional Description of Register Bits							
This register is used to select gain values on RIN, ROUT, SIN and SOUT.							
Gains is split into four groups of four bits. Each group maps to a different signal port (as indicated above), and has three gain bits. The following table indicates how these gain bits are used: Bit2 Bit1 Bit0 Gain Level 1 1 1 +9 dB 1 1 0 +6 dB) 1 0 1 +3 dB 1 0 0 0 dB (default) 0 1 1 -3 dB 0 1 0 -6 dB 0 0 1 -9 dB 0 0 0 -12 dB Note that the -12 dB PAD bit in Control Register 1 provides 12 dB of attenuation in the Rin to Rout path, and will override the settings in Gains.							

Power-up 08_{hex}	ECA: NLP Threshold 2 (NLPTHR2)				Page 0	R/W Address: $1E_{hex}$ + Base Address	
	ECB: NLP Threshold 2 (NLPTHR2)				A12=0 A11=0	R/W Address: $3E_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLPTH7	NLPTH6	NLPTH5	NLPTH4	NLPTH3	NLPTH2	NLPTH1	NLPTH0
Functional Description of Register Bits							
This register is used to force the NLP off when very small signals exist on RIN. NLP is forced off if RIN is below NLPTHR2 << 4. Raising this value can help prevent NLP masking at very low signal levels.							

Power-up 08_{hex}	ECA: Low Power Threshold (LPTHRES)					Page 0	R/W Address: $1F_{hex}$ + Base Address
	ECB: Low Power Threshold (LPTHRES)					A12=0 A11=0	R/W Address: $3F_{hex}$ + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPTH7	LPTH6	LPTH5	LPTH4	LPTH3	LPTH2	LPTH1	LPTH0
Functional Description of Register Bits							
This register is used to control the RIN low power threshold. The threshold is set by LPTHRES << 4 and is compared to RIN. Raising LPTHRES makes the VEC less responsive to very small signals.							

Power-up N/A	ECA: Estimated Echo Cancellation Level 2 (SUP)					Page 1	R/W Address: 05_{hex} + Base Address
	ECB: Estimated Echo Cancellation Level 2 (SUP)					A12=0 A11=1	R/W Address: 25_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SUP15	SUP14	SUP13	SUP12	SUP11	SUP10	SUP9	SUP8
Power-up N/A	ECA: Estimated Echo Cancellation Level 1 (SUP)					Page 1	Read Address: 04_{hex} + Base Address
	ECB: Estimated Echo Cancellation Level 1 (SUP)					A12=0 A11=1	Read Address: 24_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SUP7	SUP6	SUP5	SUP4	SUP3	SUP2	SUP1	SUP0
Functional Description of Register Bits							
This register is the estimate of the level of error as compared to RUN. SUP is used to detect low-level double-talk and to select convergence speed (fast or slow). This register is a 16 bit 2's complement linear value and defaults to 4800_{hex} = 0 dB. As cancellation progresses, this value decreases with its lower limit set by ERLLOW. It is reset after a path change or reset/bypass operation.							

Power-up N/A	ECA: Residual Error Signal 2 (ERR)					Page 1	Read Address: 07_{hex} + Base Address
	ECB: Residual Error Signal 2 (ERR)					A12=0 A11=1	Read Address: 27_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERR15	ERR14	ERR13	ERR12	ERR11	ERR10	ERR9	ERR8
Power-up N/A	ECA: Residual Error Signal 1 (ERR)					Page 1	Read Address: 06_{hex} + Base Address
	ECB: Residual Error Signal 1 (ERR)					A12=0 A11=1	Read Address: 26_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERR7	ERR6	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0
Functional Description of Register Bits							
This register represents the error signal after the filter and prior to NLP. This register is a 16 bit 2's complement linear value.							

Power-up	ECA/ECB register	Page	R/W Address
Power-up 00_{hex}	**ECA: Noise Level Control 2 (NLINC)**	**Page 2 A12=1 A11=0**	**R/W Address: 11_{hex} + Base Address**
	ECB: Noise Level Control 2 (NLINC)		**R/W Address: 31_{hex} + Base Address**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLINC15	NLINC14	NLINC13	NLINC12	NLINC11	NLINC10	NLINC9	NLINC8

Power-up	ECA/ECB register	Page	R/W Address
Power-up 04_{hex}	**ECA: Noise Level Control 1 (NLINC)**	**Page 2 A12=1 A11=0**	**R/W Address: 10_{hex} + Base Address**
	ECB: Noise Level Control 1 (NLINC)		**R/W Address: 30_{hex} + Base Address**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLINC7	NLINC6	NLINC5	NLINC4	NLINC3	NLINC2	NLINC1	NLINC0

Functional Description of Register Bits

Noise level estimator ramping rate. A lower value will give faster ramping. The default value of 4_{hex} will provide G.168 compliance.

Power-up	ECA/ECB register	Page	R/W Address
Power-up 40_{hex}	**ECA: Maximum Comfort Noise Level 2 (NLIMIT)**	**Page 2 A12=1 A11=0**	**R/W Address: 19_{hex} + Base Address**
	ECB: Maximum Comfort Noise Level 2 (NLIMIT)		**R/W Address: 39_{hex} + Base Address**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLIMIT15	NLIMIT14	NLIMIT13	NLIMIT12	NLIMIT11	NLIMIT10	NLIMIT9	NLIMIT8

Power-up	ECA/ECB register	Page	R/W Address
Power-up 00_{hex}	**ECA: Maximum Comfort Noise Level 1 (NLIMIT)**	**Page 2 A12=1 A11=0**	**R/W Address: 18_{hex} + Base Address**
	ECB: Maximum Comfort Noise Level 1 (NLIMIT)		**R/W Address: 38_{hex} + Base Address**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLIMIT7	NLIMIT6	NLIMIT5	NLIMIT4	NLIMIT3	NLIMIT2	NLIMIT1	NLIMIT0

Functional Description of Register Bits

This register controls the maximum comfort noise injection value that the VEC is able to use. This register is a 16-bit linear value.

Power-up $3E_{hex}$	ECA: NLP Ramp-out Rate 2 (RAMPOUT)					Page 2	R/W Address: $1B_{hex}$ + Base Address
	ECB: NLP Ramp-out Rate 2 (RAMPOUT)					A12=1 A11=0	R/W Address: $3B_{hex}$ + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RMPO15	RMPO14	RMPO13	RMPO12	RMPO11	RMPO10	RMPO9	RMPO8
Power-up 00_{hex}	ECA: NLP Ramp-out Rate 1 (RAMPOUT)					Page 2	R/W Address: $1A_{hex}$ + Base Address
	ECB: NLP Ramp-out Rate 1 (RAMPOUT)					A12=1 A11=0	R/W Address: $3A_{hex}$ + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RMPO7	RMPO6	RMPO5	RMPO4	RMPO3	RMPO2	RMPO1	RMPO0
Functional Description of Register Bits							
This register controls how quickly the NLP turns on. RAMPOUT is nomalized to 4000_{hex} = 1 and only values lower than this are valid. Lowering this value will cause the NLP to turn on more quickly.							

Power-up 41_{hex}	ECA: NLP Ramp-in Rate 2 (RAMPIN)					Page 2	R/W Address: $1D_{hex}$ + Base Address
	ECB: NLP Ramp-in Rate 2 (RAMPIN)					A12=1 A11=0	R/W Address: $3D_{hex}$ + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RMPI15	RMPI14	RMPI13	RMPI12	RMPI11	RMPI10	RMPI9	RMPI8
Power-up 00_{hex}	ECA: NLP Ramp-in Rate 2 (RAMPIN)					Page 2	R/W Address: $1C_{hex}$ + Base Address
	ECB: NLP Ramp-in Rate 2 (RAMPIN)					A12=1 A11=0	R/W Address: $3C_{hex}$ + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RMPI7	RMPI6	RMPI5	RMPI4	RMPI3	RMPI2	RMPI1	RMPI0
Functional Description of Register Bits							
This register controls how quickly the NLP turns off. RAMPIN is nomalized to 4000_{hex} = 1 and only values higher than this are valid. Raising this value will cause the NLP to turn off more quickly.							

Power-up N/A	ECA: Background Noise Level Estimate 2 (NOISLEV)					Page 3 A12=1 A11=1	Read Address: 03_{hex} + Base Address
	ECB: Background Noise Level Estimate 2 (NOISLEV)						Read Address: 23_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NSL15	NSL14	NSL13	NSL12	NSL11	NSL10	NSL9	NSL8
Power-up N/A	ECA: Background Noise Level Estimate 1 (NOISLEV)					Page 3 A12=1 A11=1	Read Address: 02_{hex} + Base Address
	ECB: Background Noise Level Estimate 1 (NOISLEV)						Read Address: 22_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0
Functional Description of Register Bits							
This register reflects the VEC's current estimation of background noise as a 16 bit linear value.							

Power-up N/A	ECA: NLP Signal Scaling Factor 2 (NLPGAIN)					Page 3 A12=1 A11=1	Read Address: 05_{hex} + Base Address
	ECB: NLP Signal Scaling Factor 2 (NLPGAIN)						Read Address: 25_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLPSS15	NLPSS14	NLPSS13	NLPSS12	NLPSS11	NLPSS10	NLPSS9	NLPSS8
Power-up N/A	ECA: NLP Signal Scaling Factor 1 (NLPGAIN)					Page 3 A12=1 A11=1	Read Address: 04_{hex} + Base Address
	ECB: NLP Signal Scaling Factor 1 (NLPGAIN)						Read Address: 24_{hex} + Base Address
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLPSS7	NLPSS6	NLPSS5	NLPSS4	NLPSS3	NLPSS2	NLPSS1	NLPSS0
Functional Description of Register Bits							
This register reflects the NLP attenuation, and is affected by the RAMPIN and RAMPOUT values. NLPGAIN is a 16-bit linear value which is normalized to 4000_{hex} = 1 (no attenuation). Lower values reflect more attenuation.							

Power-up 01_{hex}	ECA: Noise Level Scaling Factor 2 (NLSCALE)				Page 3 A12=1 A11=1	R/W Address: $0D_{hex}$ + Base Address	
	ECB: Noise Level Scaling Factor 2 (NLSCALE)					R/W Address: $2D_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLS15	NLS14	NLS13	NLS12	NLS11	NLS10	NLS9	NLS8
Power-up AA_{hex}	ECA: Noise Level Scaling Factor 1 (NLSCALE)				Page 3 A12=1 A11=1	R/W Address: $0C_{hex}$ + Base Address	
	ECB: Noise Level Scaling Factor 1 (NLSCALE)					R/W Address: $2C_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLS7	NLS6	NLS5	NLS4	NLS3	NLS2	NLS1	NLS0
Functional Description of Register Bits							
This register is used to scale the comfort noise up or down. Larger values will increase the relative level of comfort noise. The default value of $01AA_{hex}$ will provide G.168 compliance with the Advanced NLP. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up 00_{hex}	Main Control Register 0 (EC Group 0)				Page 0 A12=0 A11=0	R/W Address: 400_{hex}	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR_all	ODE	MIRQ	MTDBI	MTDAI	Format	Law	PWUP
Functional Description of Register Bits							
WR_all	Write all control bit: When high, Group 0-15 Echo Cancellers Registers are mapped into 0000_{hex} to $0003F_{hex}$ which is Group 0 address mapping. Useful to initialize the 16 Groups of Echo Cancellers as per Group 0. When low, address mapping is per Figure 11. Note: Only the Main Control Register 0 has the WR_all bit.						
ODE	Output Data Enable: This control bit is logically AND'd with the ODE input pin. When both ODE bit and ODE input pin are high, the Rout and Sout outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout outputs are high impedance. Note: Only the Main Control Register 0 has the ODE bit.						
MIRQ	Mask Interrupt: When high, all the interrupts from the Tone Detectors output are masked. The Tone Detectors operate as specified in their Echo Canceller B, Control Register 2. When low, the Tone Detectors Interrupts are active. Note: Only the Main Control Register 0 has the MIRQ bit.						
MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.						
MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.						
Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, accept ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, accept sign-magnitude PCM code.						
Law	A/μ Law: When high, both Echo Cancellers A and B for a given group, accept A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, accept μ-Law companded PCM code.						
PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo canceller A and B execute their initialization routine which presets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to default power up value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.						

Power-up	Register	Page	Address
Power-up 00_{hex}	**Main Control Register 1 (EC Group 1)**	**Page0 A12=0 A11=0**	**R/W Address: 401_{hex}**
	Main Control Register 2 (EC Group 1)		**R/W Address: 402_{hex}**
	Main Control Register 3 (EC Group 1)		**R/W Address: 403_{hex}**
	Main Control Register 4 (EC Group 1)		**R/W Address: 404_{hex}**
	Main Control Register 5 (EC Group 1)		**R/W Address: 405_{hex}**
	Main Control Register 6 (EC Group 1)		**R/W Address: 406_{hex}**
	Main Control Register 7 (EC Group 1)		**R/W Address: 407_{hex}**
	Main Control Register 8 (EC Group 1)		**R/W Address: 408_{hex}**
	Main Control Register 9 (EC Group 1)		**R/W Address: 409_{hex}**
	Main Control Register 10 (EC Group 1)		**R/W Address: $40A_{hex}$**
	Main Control Register 11 (EC Group 1)		**R/W Address: $40B_{hex}$**
	Main Control Register 12 (EC Group 1)		**R/W Address: $40C_{hex}$**
	Main Control Register 13 (EC Group 1)		**R/W Address: $40D_{hex}$**
	Main Control Register 14 (EC Group 1)		**R/W Address: $40E_{hex}$**
	Main Control Register 15 (EC Group 1)		**R/W Address: $40F_{hex}$**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Unused	MTDBI	MTDAI	Format	Law	PWUP

Functional Description of Register Bits	
Unused	Unused bits
MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.
MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.
Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, accept ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, accept sign-magnitude PCM code.
Law	A/μ Law: When high, both Echo Cancellers A and B for a given group, accept A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, accept μ-Law companded PCM code.
PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo cancellers A and B execute their initialization routine which presets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.

Power-up 00_{hex}	**Interrupt FIFO Register**				**Page 0 A12=0 A11=0**	**R/W Address: 410_{hex}**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ	0	0	I4	I3	I2	I1	I0
Functional Description of Register Bits							
IRQ	Write all control bit: When high, Group 0-15 Echo Cancellers Registers are mapped into 0000_{hex} to $0003F_{hex}$ which is Group 0 address mapping. Useful to initialize the 16 Groups of Echo Cancellers as per Group 0. When low, address mapping is per Figure 11. Note: Only the Main Control Register 0 has the WR_all bit.						
0	Unused bits. Always zero.						
I<4:0>	I<4:0> binary code indicates the channel number at which a Tone Detector state change has occurred. Note: Whenever a Tone Disable is detected or released, an interrupt is generated.						

Power-up 00_{hex}	**Test Register**				**Page 0 A12=0 A11=0**	**R/W Address: 411_{hex}**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Functional Description of Register Bits							
Reserved	Reserved bits. Must always be set to zero for normal operation.						
Tirq	Test IRQ: Useful for the application engineer to verify the interrupt service routine. When high, any change to MTDBI and MTDAI bits of the Main Control Register will cause an interrupt and its corresponding channel number will be available from the Interrupt FIFO Register. When low, normal operation is selected.						

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage (V_{DD1})	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage (V_{DD2})	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I3}	V_{SS} - 0.5	V_{DD1}+0.5	V
4	Input Voltage on any 5 V Tolerant I/O pins	V_{I5}	V_{SS} - 0.3	7.0	V
5	Continuous Current at digital outputs	I_o		20	mA
6	Package power dissipation	P_D		2	W
7	Storage temperature	T_S	-55	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym.	Min,	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40		+85	°C
2	I/O Supply Voltage (V_{DD_IO})	V_{DD1}	3.0	3.3	3.6	V
3	Core Supply Voltage (V_{DD_CORE})	V_{DD2}	1.6	1.8	2.0	V
4	Input High Voltage on 3.3 V tolerant I/O	V_{IH3}	$0.7V_{DD1}$		V_{DD1}	V
5	Input High Voltage on 5 V tolerant I/O pins	V_{IH5}	$0.7V_{DD1}$		5.5	V
6	Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Static Supply Current	I_{CC}			250	µA	$\overline{RESET}$ = 0
		IDD_IO (V_{DD1} = 3.3 V)	I_{DD_IO}		10		mA	All 32 channels active
		IDD_CORE (V_{DD2} = 1.8 V)	I_{DD_CORE}		65		mA	All 32 channels active
2		Power Consumption	P_C		150		mW	All 32 channels active
3		Input High Voltage	V_{IH}	$0.7V_{DD1}$			V	
4		Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V	
5		Input Leakage Input Leakage on Pullup Input Leakage on Pulldown	I_{IH}/I_{IL} I_{LU} I_{LD}		 -30 30	10 -55 65	µA µA µA	V_{IN}=V_{SS} to V_{DD1}or 5.5 V V_{IN}=V_{SS} V_{IN}=V_{DD1} See Note 1
6		Input Pin Capacitance	C_I			10	pF	
7	OUTPUTS	Output High Voltage	V_{OH}	$0.8V_{DD1}$			V	I_{OH} = 12 mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
9		High Impedance Leakage	I_{OZ}			10	µA	V_{IN}=V_{SS} to 5.5 V
10		Output Pin Capacitance	C_O			10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD1} =3.3 V and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{TT}	$0.5V_{DD1}$	V	
2	CMOS Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD1}$	V	
3	CMOS Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD1}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - Frame Pulse and $\overline{C4i}$

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Frame pulse width (ST-BUS, GCI)	t_{FPW}	20		2* t_{CP}-20	ns	
2	$\overline{\text{Fra}}$me Pulse Setup time before $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPS}	10	122	150	ns	
3	Frame Pulse Hold Time from $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPH}	10	122	150	ns	
4	$\overline{C4i}$ Period	t_{CP}	190	244	300	ns	
5	$\overline{C4i}$ Pulse Width High	t_{CH}	85		150	ns	
6	$\overline{C4i}$ Pulse Width Low	t_{CL}	85		150	ns	
7	$\overline{C4i}$ Rise/Fall Time	t_r, t_f			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Serial Streams for ST-BUS and GCI Backplanes

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Rin/Sin Set-up Time	t_{SIS}	10			ns	
2	Rin/Sin Hold Time	t_{SIH}	10			ns	
3	Rout/Sout Delay - Active to Active	t_{SOD}			60	ns	C_L=150 pF
4	Output Data Enable (ODE) Delay	t_{ODE}			30	ns	C_L=150 pF, R_L=1 K See Note 1

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing.
* Note1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

AC Electrical Characteristics† - Master Clock - Voltages are with respect to ground (V_{SS}). unless otherwise stated.

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Master Clock Frequency, - Fsel = 0 - Fsel = 1	f_{MCF0} f_{MCF1}	19.0 9.5	20.0 10.0	21.0 10.5	MHz MHz	
2	Master Clock Low	t_{MCL}	20			ns	
3	Master Clock High	t_{MCH}	20			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from DS falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}	0			ns	
3	Address setup from DS falling	t_{ADS}	0			ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}	0			ns	
6	Address hold after DS rising	t_{ADH}	0			ns	
7	Data delay on read	t_{DDR}			79	ns	
8	Data hold on read	t_{DHR}	3		15	ns	
9	Data setup on write	t_{DSW}	0			ns	
10	Data hold on write	t_{DHW}	0			ns	
11	Acknowledgment delay	t_{AKD}			80	ns	
12	Acknowledgment hold time	t_{AKH}	0		8	ns	
13	$\overline{IRQ}$ delay	t_{IRD}	20		65	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing.

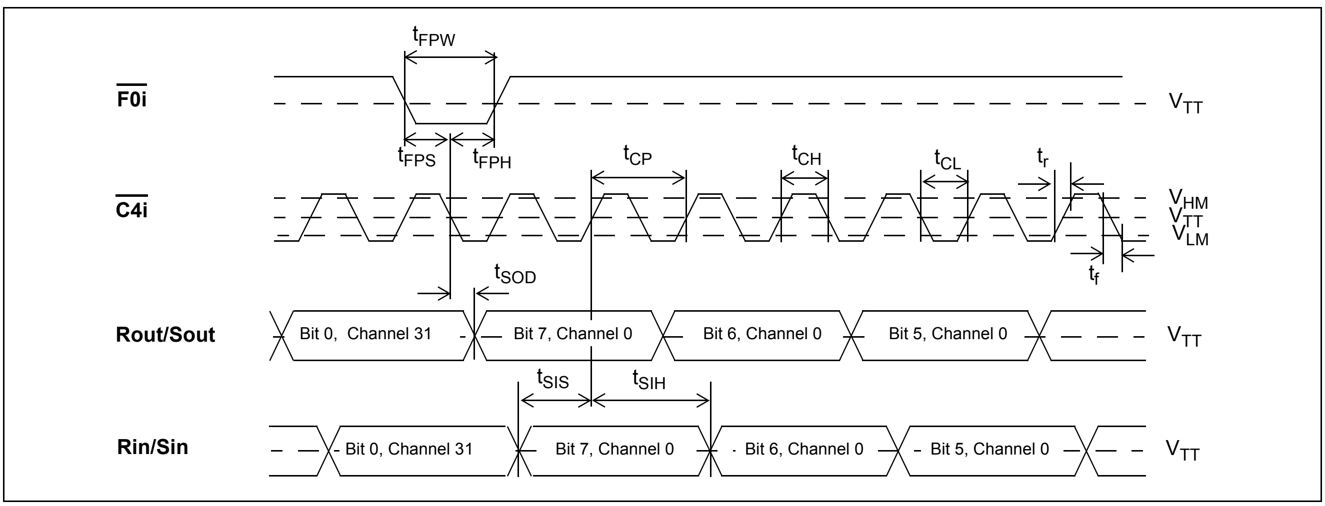


Figure 14 - ST-BUS Timing at 2.048 Mbps

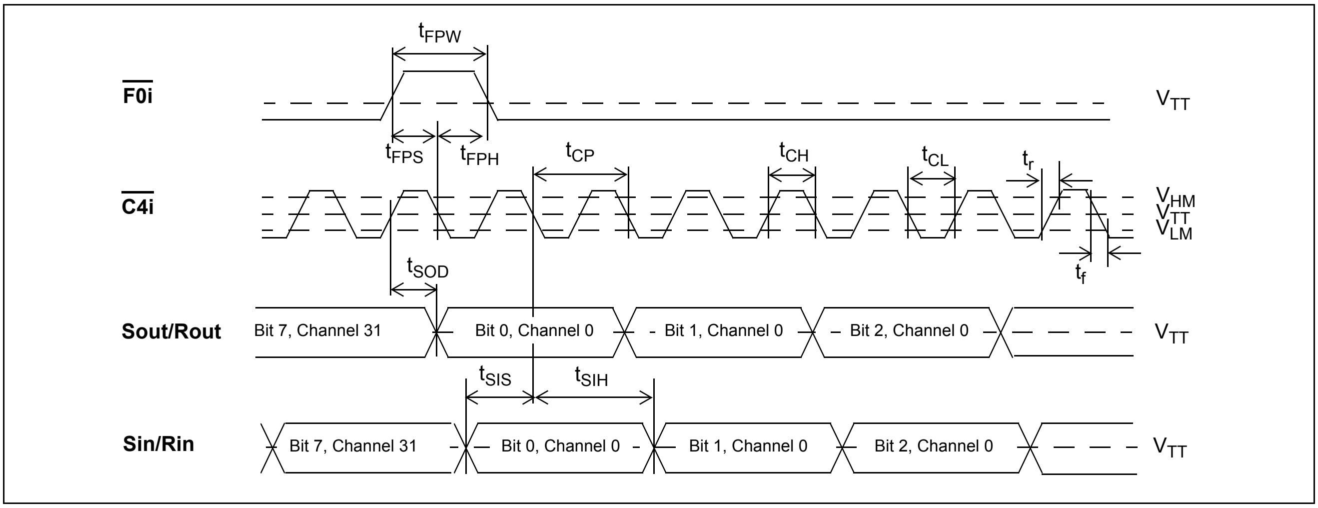


Figure 15 - GCI Interface Timing at 2.048 Mbps

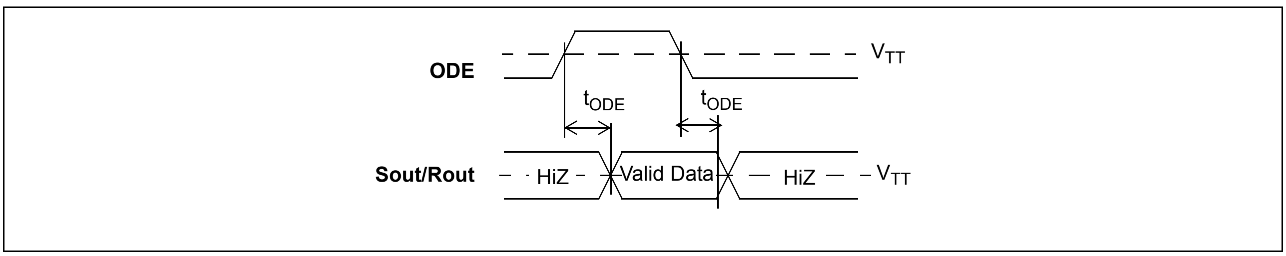


Figure 16 - Output Driver Enable (ODE)

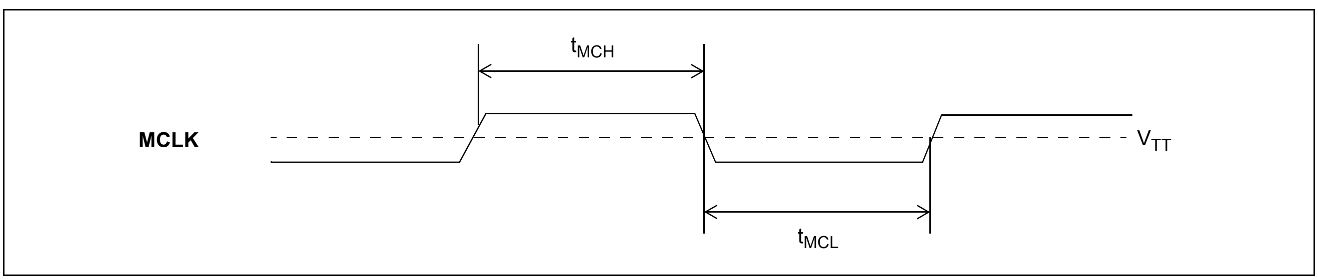


Figure 17 - Master Clock

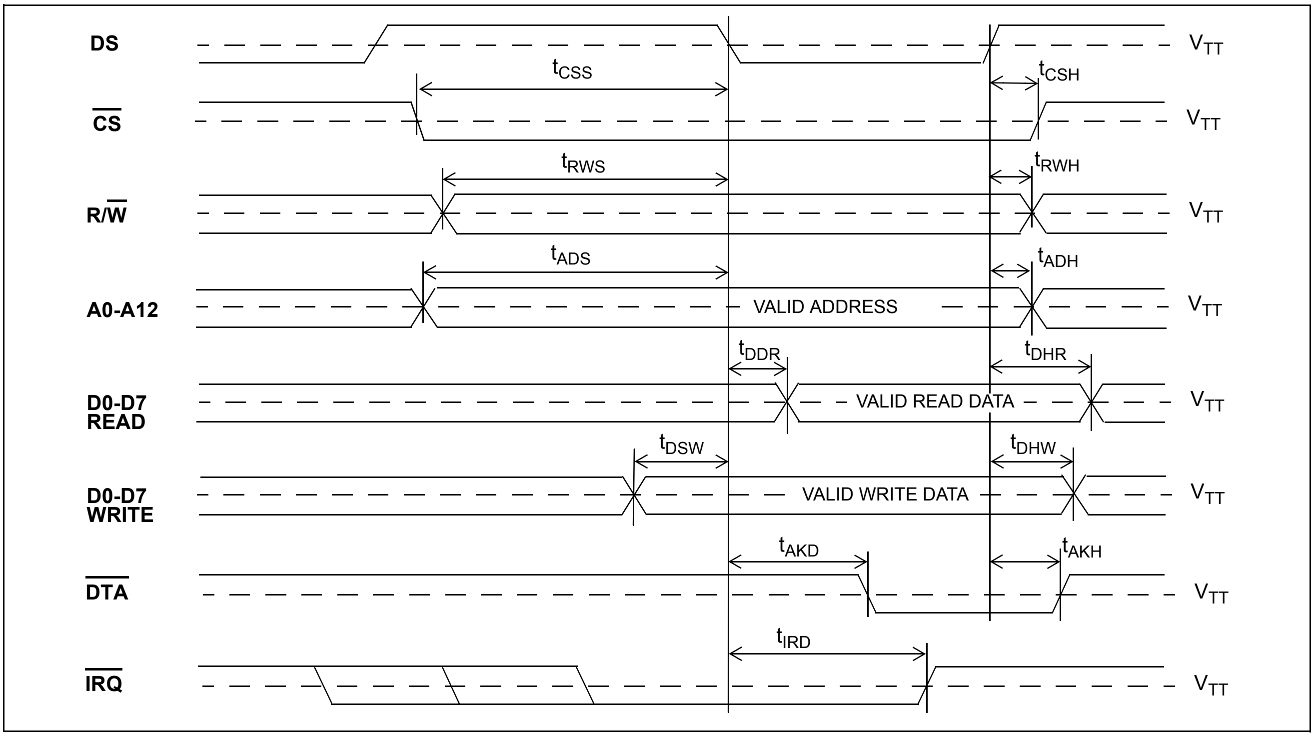
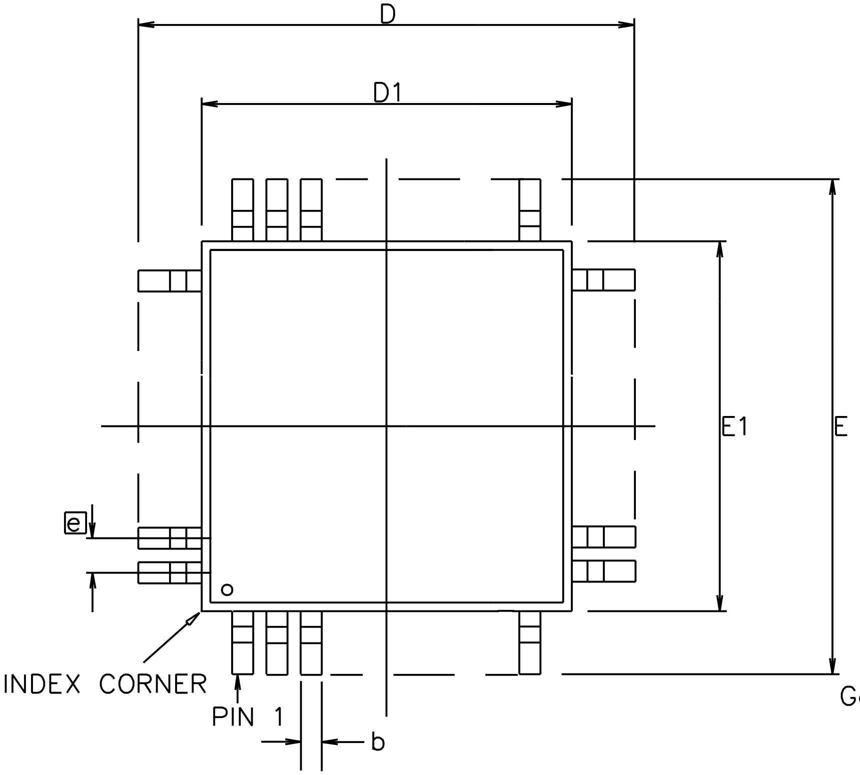
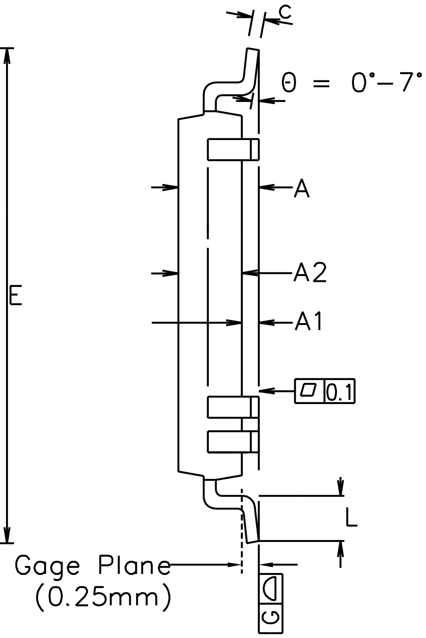


Figure 18 - Motorola Non-Multiplexed Bus Timing





Symbol	Control Dimensions in millimetres		Altern. Dimensions in inches	
	MIN	MAX	MIN	MAX
A	---	1.60	---	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
D	16.00 BSC		0.630 BSC	
D1	14.00 BSC		0.551 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
L	0.45	0.75	0.018	0.030
e	0.50 BSC		0.020 BSC	
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
	Pin features			
N	100			
ND	25			
NE	25			
NOTE	SQUARE			

Conforms to JEDEC MS-026 BED Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swindon)

ISSUE	1	2	3	
ACN	201373	207144	212447	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

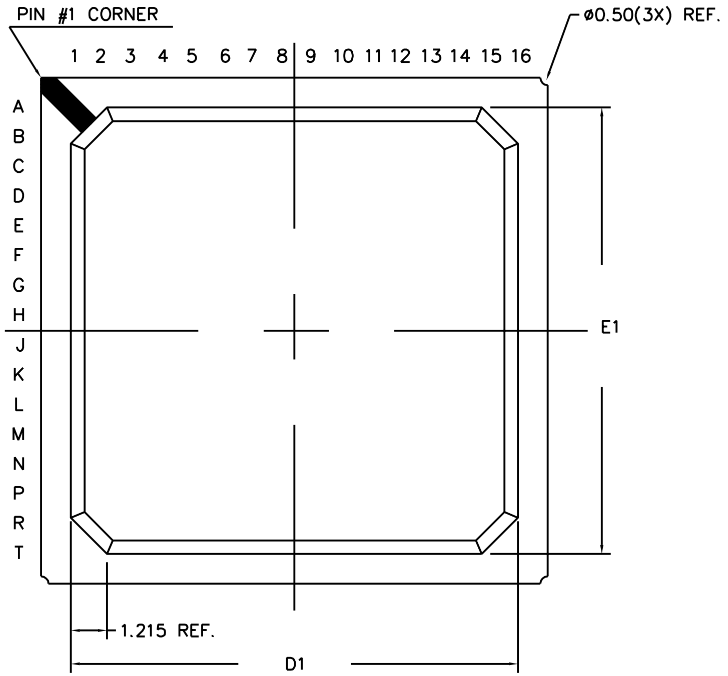
GP / B

Package Code QC

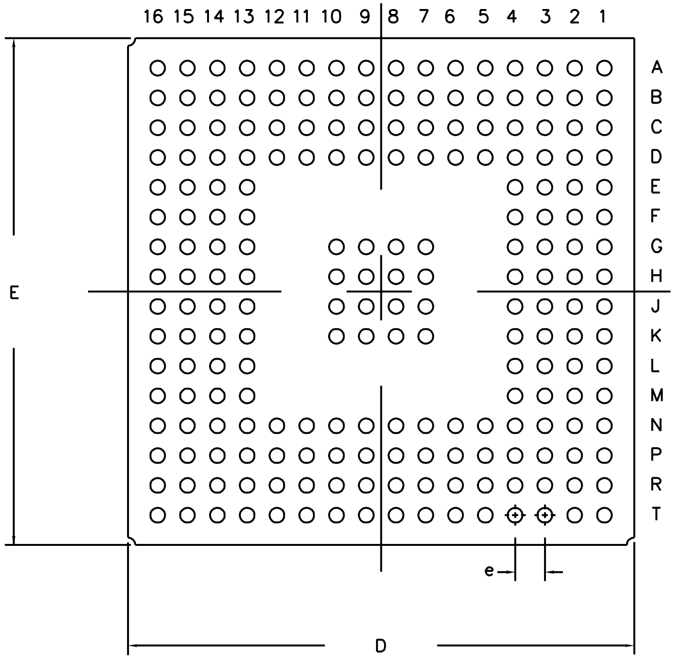
Package Outline for 100 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

GPD00253

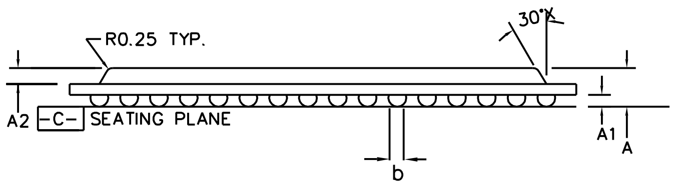
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.10	1.50
A1	0.30	0.50
A2	0.49	0.59
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	208	
Conforms to JEDEC MO-192		



SIDE VIEW

NOTES: -
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.
6. Ball diameter and standoff different from Jedec Spec MO-192

ISSUE	1			
ACN	26Sep02			
DATE	213468			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GD

Package Outline for 208 Ball LBGA (17 x 17 x 1.3mm)

GPD00799

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visit our Web Site at

www.zarlink.com