

BLF4G22-100; BLF4G22S-100

UHF power LDMOS transistor

Rev. 01 — 10 January 2006

Product data sheet

1. Product profile

1.1 General description

100 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1: Typical performance

$T_{case} = 25\text{ }^{\circ}\text{C}$; in a common source class-AB test circuit; $I_{Dq} = 900\text{ mA}$; typical values

Mode of operation	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	IMD3 (dBc)	ACPR (dBc)
2-carrier W-CDMA [1]	$f_1 = 2135$; $f_2 = 2145$	28	25 (AV)	13.5	26	-37	-41

[1] 10 MHz carrier spacing PAR 7 dB at 0.01 % probability on CCDF, 3GPP test model 1, 1 to 64 DPCH.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical 2-Carrier W-CDMA performance at a supply voltage of 28 V and an I_{Dq} of 900 mA:
 - ◆ Load power = 25 W (AV)
 - ◆ Gain = 13.5 dB (typ)
 - ◆ Efficiency = 26 % (typ)
 - ◆ ACPR = -41 dBc (typ)
 - ◆ IMD3 = -37 dBc (typ)
- Easy power control
- Integrated ESD protection
- Excellent ruggedness > 10 : 1 VSWR at 100 W CW
- High efficiency
- High peak power capability (> 150 W)
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use

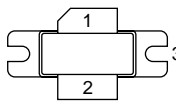
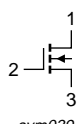
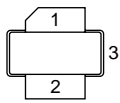
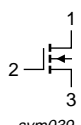
PHILIPS

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 MHz to 2200 MHz frequency range.

2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
BLF4G22-100 (SOT502A)			
1	drain		 sym039
2	gate		
3	source		
BLF4G22S-100 (SOT502B)			
1	drain		 sym039
2	gate		
3	source		

[1] Connected to flange

3. Ordering information

Table 3: Ordering information

Type number	Package		Version
	Name	Description	
BLF4G22-100	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF4G22S-100	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+15	V
I_D	drain current		-	12	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 25\text{ W}$; 2-carrier W-CDMA	-	0.76	0.85	K/W

6. Characteristics

Table 6: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 180\text{ mA}$	2.5	3.1	3.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 900\text{ mA}$	2.7	3.2	3.7	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	3	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $V_{DS} = 10\text{ V}$	27	30	-	A
I_{GSS}	gate leakage current	$V_{GS} = 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	transfer conductance	$V_{DS} = 10\text{ V}$; $I_D = 10\text{ A}$	-	9.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $I_D = 6\text{ A}$	-	0.09	-	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	-	2.5	-	pF

7. Application information

Table 7: Application information

Mode of operation: 2-Carrier W-CDMA, PAR 7 dB at 0.01 % probability on CCDF, 3GPP test model 1, 1-64 DPCH, $f_1 = 2112.5\text{ MHz}$, $f_2 = 2122.5\text{ MHz}$, $f_3 = 2157.5\text{ MHz}$, $f_4 = 2167.5\text{ MHz}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 25\text{ W}$	12.5	13.5	-	dB
IRL	input return loss	$P_{L(AV)} = 25\text{ W}$	9	15	-	dB
η_D	drain efficiency	$P_{L(AV)} = 25\text{ W}$	24	26	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)} = 25\text{ W}$	-	-37	-35	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)} = 25\text{ W}$	-	-41	-39	dBc

7.1 Ruggedness in class-AB operation

The BLF4G22-100/BLF4G22S-100 are capable of withstanding a load mismatch corresponding to VSWR > 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $P_L = 100\text{ W}$ (CW).

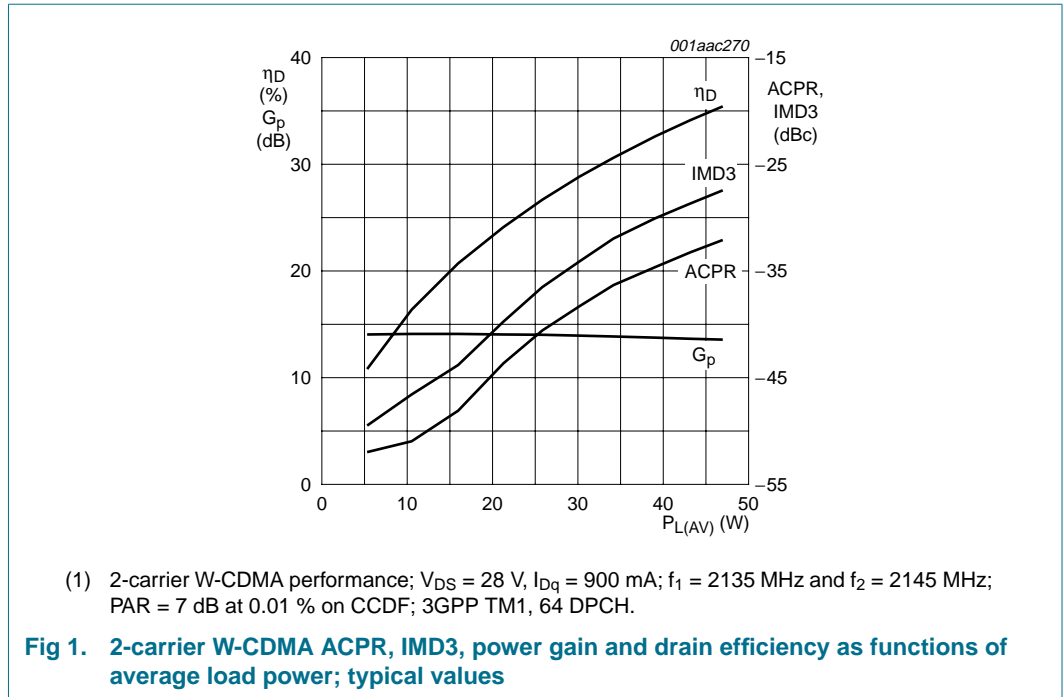


Table 8: Typical impedance values

$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $P_L = 25\text{ W (AV)}$; $T_{case} = 25\text{ °C}$.

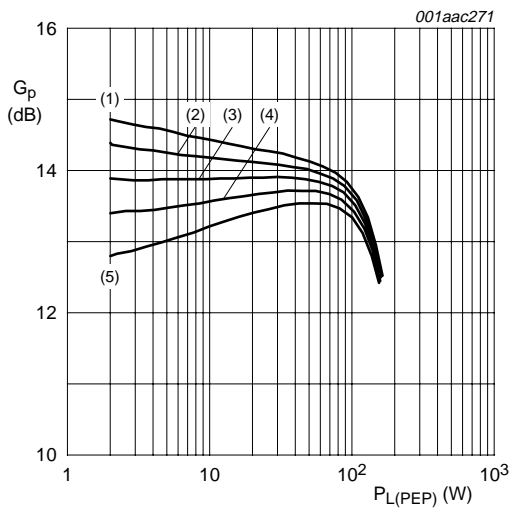
Frequency (MHz)	Z_S (Ω)	Z_L (Ω)
2110	2.2 + j4.8	1.5 - j2.6
2140	2.2 + j4.6	1.5 - j2.4
2170	2.2 + j4.5	1.4 - j2.2

Table 9: RF gain grouping

Code [1]	Gain (dB) [2]	
	Min	Max
A	12.5	13.0
B	13.0	13.5
C	13.5	14.0
D	14.0	14.5
E	14.5	-

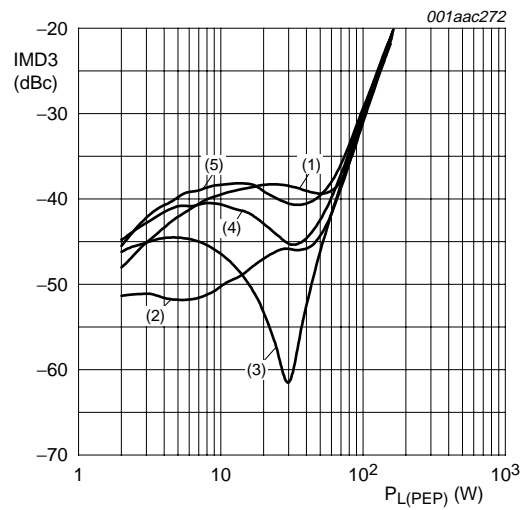
[1] 0.2 dB overlap is allowed for measurement reproducibility.

[2] For 2-carrier W-CDMA at $f_1 = 2157\text{ MHz}$, $f_2 = 2167.5\text{ MHz}$.



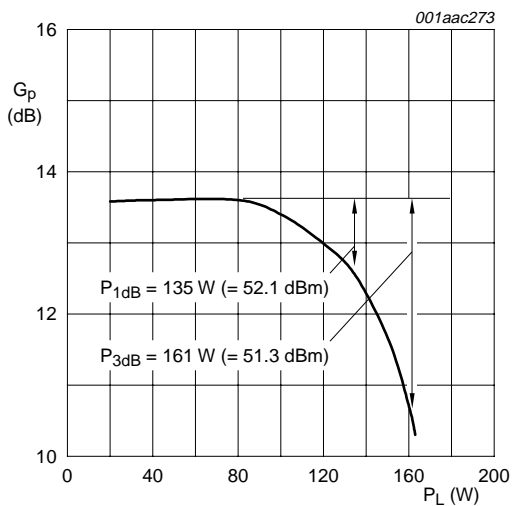
(1) $I_{Dq} = 600 \text{ mA}$
 (2) $I_{Dq} = 750 \text{ mA}$
 (3) $I_{Dq} = 900 \text{ mA}$
 (4) $I_{Dq} = 1050 \text{ mA}$
 (5) $I_{Dq} = 1200 \text{ mA}$
 Two-tone measurement;
 $V_{DS} = 28 \text{ V}$; $f_1 = 2140.0 \text{ MHz}$; $f_2 = 2140.1 \text{ MHz}$

Fig 2. Power gain as a function of peak envelope load power; typical values



(1) $I_{Dq} = 600 \text{ mA}$
 (2) $I_{Dq} = 750 \text{ mA}$
 (3) $I_{Dq} = 900 \text{ mA}$
 (4) $I_{Dq} = 1050 \text{ mA}$
 (5) $I_{Dq} = 1200 \text{ mA}$
 Two-tone measurement;
 $V_{DS} = 28 \text{ V}$; $f_1 = 2140.0 \text{ MHz}$; $f_2 = 2140.1 \text{ MHz}$

Fig 3. Third order intermodulation distortion as a function of peak envelope power; typical values



$t_{on} = 8 \mu\text{s}$
 $t_{off} = 1 \text{ ms}$

Fig 4. Pulsed peak power capability; typical values

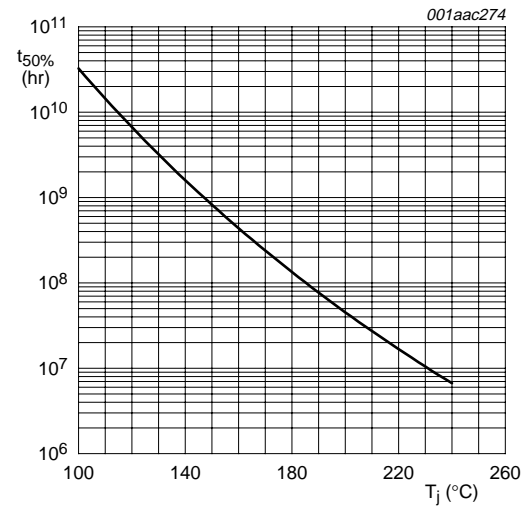
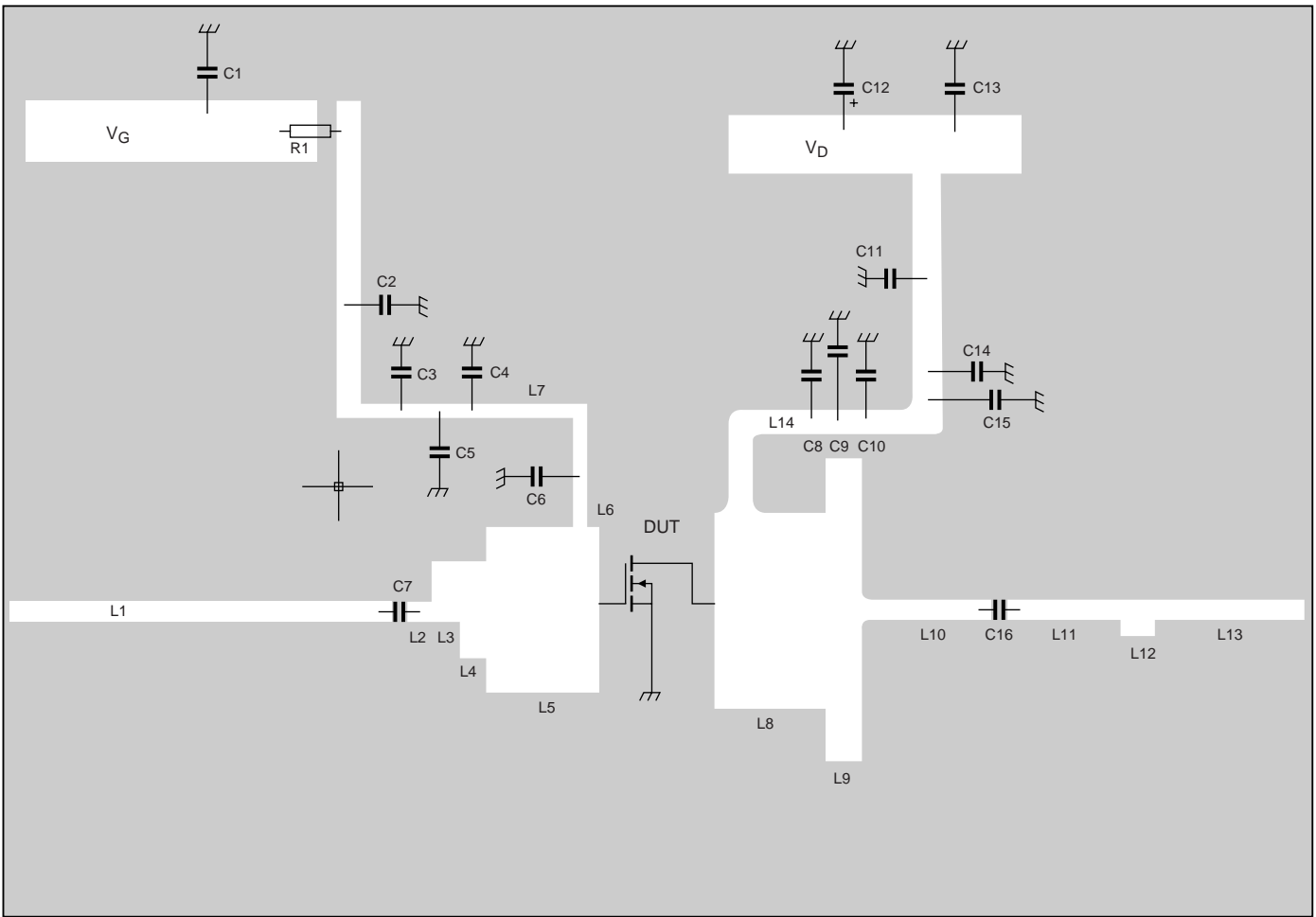


Fig 5. $t_{50\%}$ failures due to electromigration as a function of junction temperature

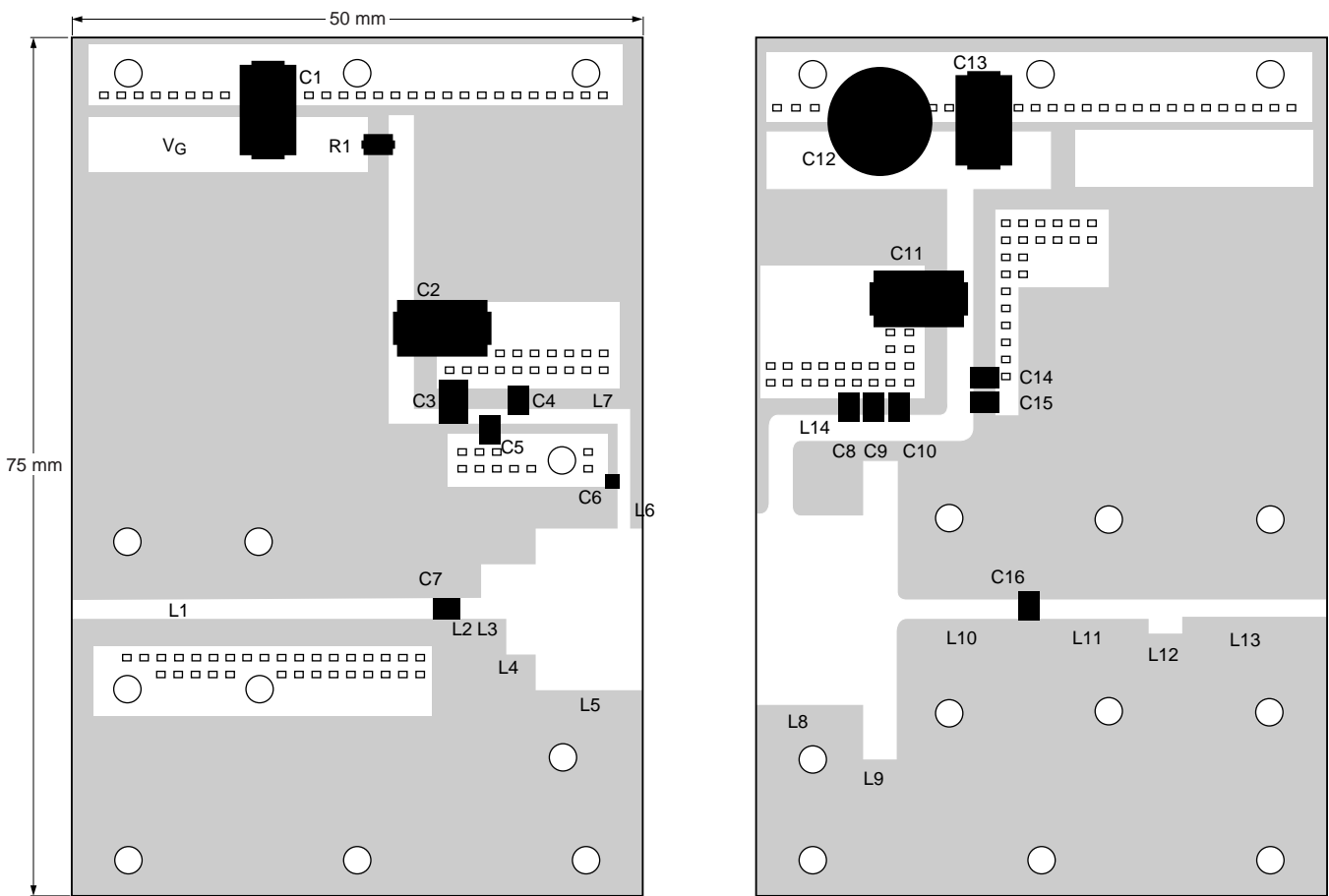
8. Test information



001aac275

See [Table 10](#) for list of components

Fig 6. Test circuit for operation at 2.14 GHz



001aac276

The components are situated on double copper-clad Taconic RF35 Printed-Circuit Board (PCB) ($\epsilon_r = 3.5$); thickness = 0.76 mm.

The other side is unetched and serves as a ground plane.

See [Table 10](#) for list of components.

Fig 7. Component layout for 2.14 GHz test circuit

Table 10: List of components (see Figure 6 and Figure 7)

Component	Description	Value	Dimensions
C1, C2, C11	tantalum capacitor	10 μ F; 35 V	
C3	multilayer ceramic chip capacitor	4.7 μ F; 25 V	
C4, C10	multilayer ceramic chip capacitor	[1] 8.2 pF	
C5, C8, C14, C15	multilayer ceramic chip capacitor	1.5 μ F; 50 V	
C6	multilayer ceramic chip capacitor	[2] 0.6 pF	
C7	multilayer ceramic chip capacitor	[1] 4.7 pF	
C9	multilayer ceramic chip capacitor	220 nF; 50 V	
C12	electrolytic capacitor	220 μ F; 63 V	
C13	tantalum capacitor	4.7 μ F; 50 V	
C16	multilayer ceramic chip capacitor	[3] 7.5 pF	
L1	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 32.3 mm \times 1.7 mm
L2	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 2.2 mm \times 1.7 mm
L3	stripline	[4] $Z_0 = 24 \Omega$	(W \times L) 2.3 mm \times 4.8 mm
L4	stripline	[4] $Z_0 = 15 \Omega$	(W \times L) 2.4 mm \times 8 mm
L5	stripline	[4] $Z_0 = 9.5 \Omega$	(W \times L) 9.3 mm \times 14 mm
L6	stripline	[4] $Z_0 = 60 \Omega$	(W \times L) 4 mm \times 1.2 mm
L7	stripline	[4] $Z_0 = 60 \Omega$	(W \times L) 14.5 mm \times 1.2 mm
L8	stripline	[4] $Z_0 = 8.2 \Omega$	(W \times L) 9.3 mm \times 16.8 mm
L9	stripline	[4] $Z_0 = 5.5 \Omega$	(W \times L) 3 mm \times 25.8 mm
L10	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 11 mm \times 1.7 mm
L11	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 9.5 mm \times 1.7 mm
L12	stripline	[4] $Z_0 = 34 \Omega$	(W \times L) 3 mm \times 3 mm
L13	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 12.7 mm \times 1.7 mm
L14	stripline	[4] $Z_0 = 43 \Omega$	(W \times L) 13.5 mm \times 2.1 mm
R1	SMD resistor	4.7 Ω ; 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 180R or capacitor of same quality.

[4] Striplines are on a double copper-clad Taconic RF35 PCB ($\epsilon_r = 3.5$); thickness = 0.76 mm.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

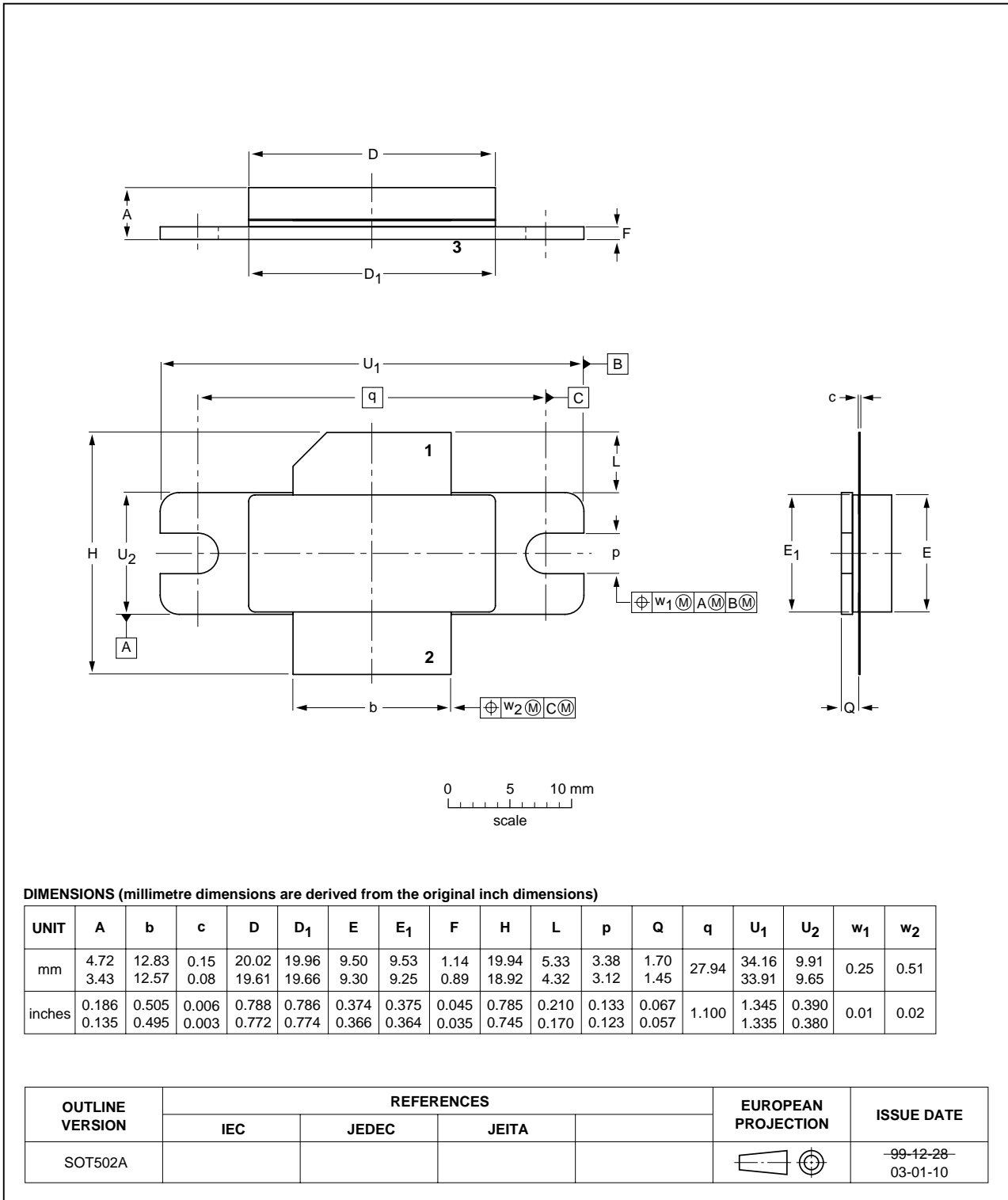


Fig 8. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

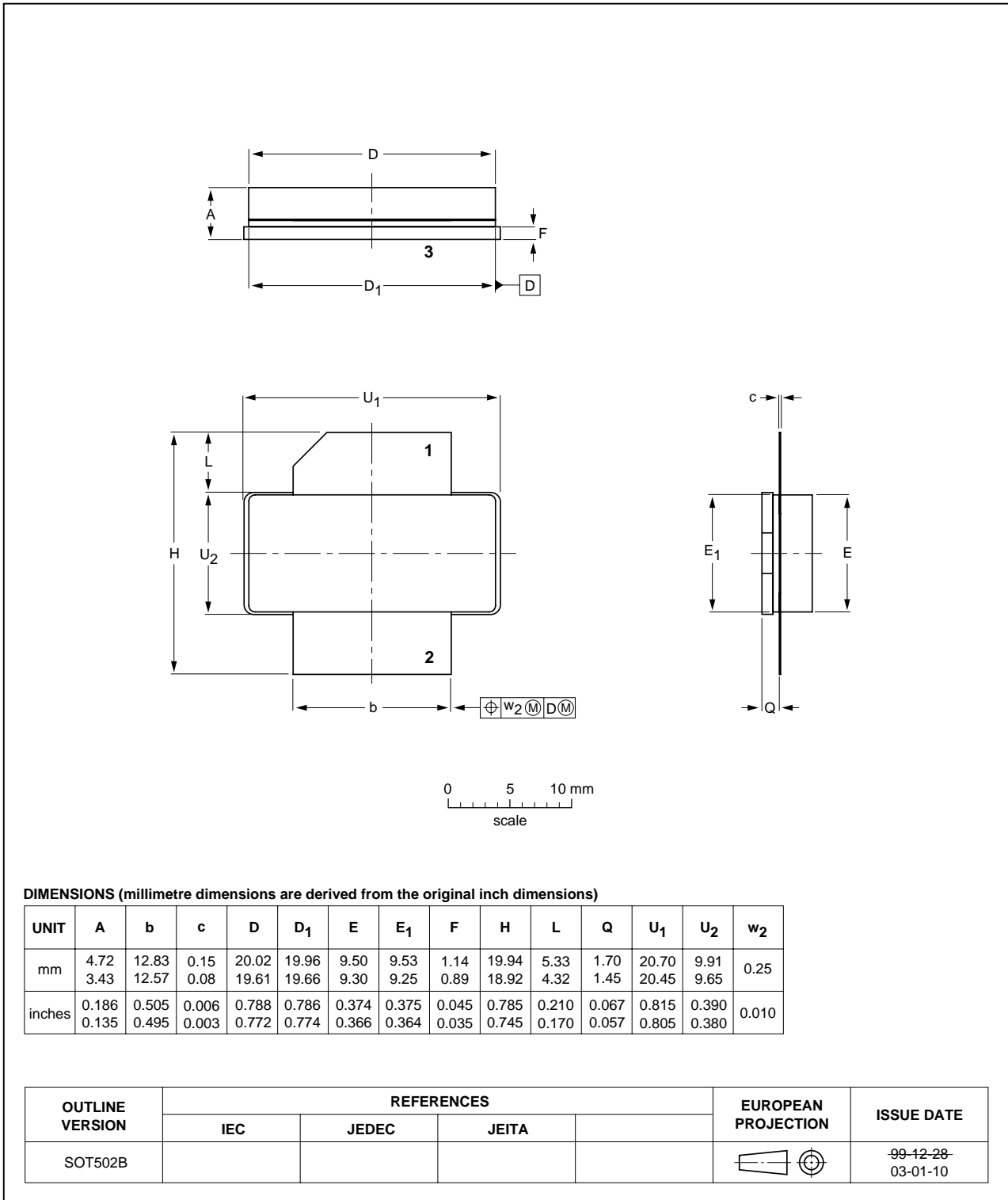


Fig 9. Package outline SOT502B

10. Abbreviations

Table 11: Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CW	Continuous Wave
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channels
I_{Dq}	quiescent drain current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
PEP	Peak Envelope Power
RF	Radio Frequency
TM1	Test Model 1
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLF4G22-100_4G22 S-100_1	20060110	Product data sheet	-	9397 750 14338	-

12. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

14. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

16. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

15. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	2
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Application information	3
7.1	Ruggedness in class-AB operation	3
8	Test information	6
9	Package outline	9
10	Abbreviations	11
11	Revision history	12
12	Data sheet status	13
13	Definitions	13
14	Disclaimers	13
15	Trademarks	13
16	Contact information	13



© Koninklijke Philips Electronics N.V. 2006

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 10 January 2006
Document number: 9397 750 14338

Published in The Netherlands