ZCU104 Evaluation Board

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/04/2018	1.0	Initial Xilinx release.

Table of Contents

Introduction

Overview

The embedded vision low cost (EVLC) development kit enables automotive, AR/VR, drones, machine vision, and industrial vision developers to build, prototype, and test their designs on a Zynq® UltraScale+™ MPSoC XCZU7EV-2FFVC1156 device. The ZU7EV device integrates a quad core ARM® Cortex™-A53 processing system (PS) and a dual-core ARM Cortex-R5 real-time processor, which provides application developers an unprecedented level of heterogeneous multiprocessing. The ZCU104 evaluation board provides a flexible prototyping platform with high-speed DDR4 memory interfaces, an FMC expansion port, multi-gigabit per second serial transceivers, a variety of peripheral interfaces, and FPGA fabric for customized designs. The ZCU104 reVISION package provides out-of-box SDSoC™ software development flow with OpenCV libraries, machine learning framework, and live sensor support.

Additional Resources

See Appendix D, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU104 evaluation board.

Block Diagram

The ZCU104 board block diagram is shown in Figure 1-1.

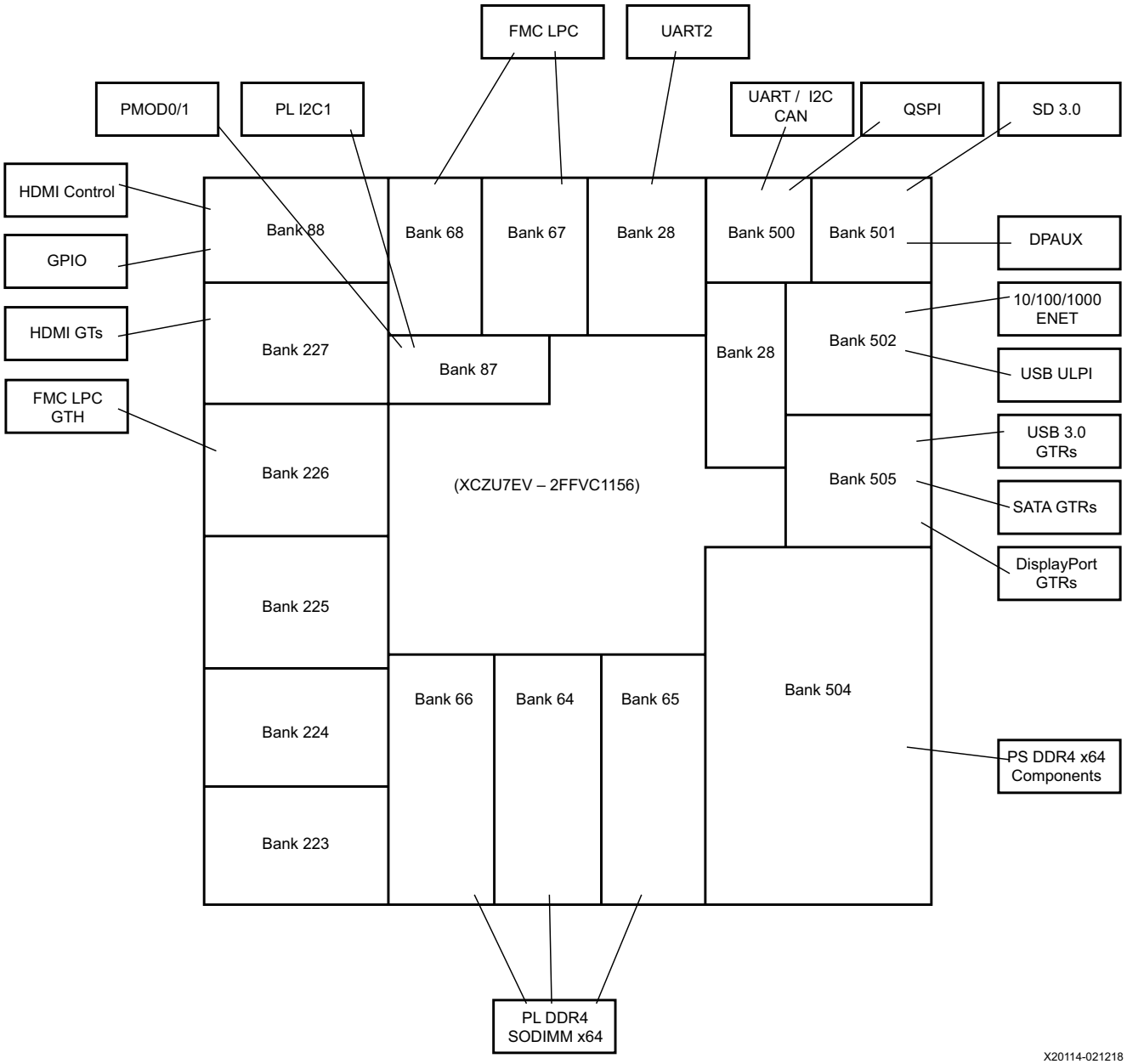


Figure 1-1: **ZCU104 Evaluation Board Block Diagram**

Board Features

The ZCU104 evaluation board features are listed here. Detailed information for each feature is provided in Component Descriptions in Chapter 3.

- XCZU7EV-2, FFVC1156 package
- PL V_{CCINT} for range in data sheet
- Rectangular form factor for benchtop use
- Configuration from Quad SPI
- Configuration from SD card
- Configuration over JTAG with platform cable USB header
- Configuration over USB-to-JTAG bridge
- IDT 8T49N287A clock chip
  - HDMI_DRU_CLOCK
  - PS_REF_CLK
  - GTR_REF_CLK_USB3
  - GTR_REF_CLK_DP
  - CLK_300
  - GTR_REF_CLK_SATA
  - CLK_125
- PS DDR4 64-bit component (4x16-bit)
- PL DDR4 64-bit SODIMM socket
- PS GTR assignment
  - DisplayPort (two GTRs)
  - USB3 (one GTR)
  - SATA (one GTR)
- PL GTH transceiver assignment (4 of 20 used)
  - High-definition multimedia interface (HDMI®) (three GTH transceivers)
  - FMC LPC DP (one GTH transceiver)
- PL FMC LPC connectivity - full LA bus
- PS MIO: single Quad SPI
- PS MIO: two channels of quad-UART bridge

- PS MIO: CAN
- PS MIO: I2C shared across PS and PL
- PS MIO: SD
- PS MIO: DisplayPort
- PS MIO: Ethernet
- PS MIO: USB3
- PS-side user LED (one)
- PL-side user LEDs (four)
- PL-side user DIP switch (4-position)
- PL-side user pushbuttons (four)
- PL-side CPU reset pushbutton
- PL-side PMOD headers
- PL-side bank 0 PROG_B pushbutton
- Security - PSBATT button battery backup
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (power status, INIT, DONE, PG, DDR power good)
- Power management

The ZCU104 provides a rapid prototyping platform for the embedded vision low cost (EVLC) market using the XCZU7EV-2FFVC1156 device. The ZU7EV contains PS hard block peripherals exposed through the multi-use I/O (MIO) interface and several FPGA programmable logic (PL), high-density (HD), and high-performance (HP) banks. Table 1-1 lists the resources available within the ZU7EV. See the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1] for a feature set overview, description, and ordering information.

Table 1-1: **Zynq UltraScale+ MPSoC ZU7EV Features and Resources**

Feature	Resource Count
Quad core ARM Cortex-A53 MPCore	1
Dual core ARM Cortex-R5 MPCore	1
Mali-400 MP2 GPU	1
H.264/H.265 VCU	1
HD banks	Two banks, total of 48 pins
HP banks	Six banks, total of 312 pins
MIO banks	Three banks, total of 78 pins
PS-GTR transceivers (6 Gb/s)	Four PS-GTR transceivers
GTH transceivers (16.3 Gb/s)	20 GTH transceivers
System logic cells	504K
CLB flip-flops	461K
Maximum distributed RAM	6.2 Mb
Total block RAM	11 Mb
UltraRAM	27 Mb
DSP slices	1,728

Board Specifications

Dimensions

Height: 5.90 inch (14.98 cm)

Length: 7.05 inch (17.91 cm)

Thickness: 0.062 inch ±0.005 inch (0.157 cm ±0.0127 cm)

Note: A 3D model of this board is not available.

See ZCU104 board documentation for XDC listing, schematics, layout files, board outline drawings, etc.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU104 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic (0381794) page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU104 version of interest for such details.*

CAUTION! *The ZCU104 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

(00) Round callout references a component on the front side of the board

[00] Square callout references a component on the back side of the board

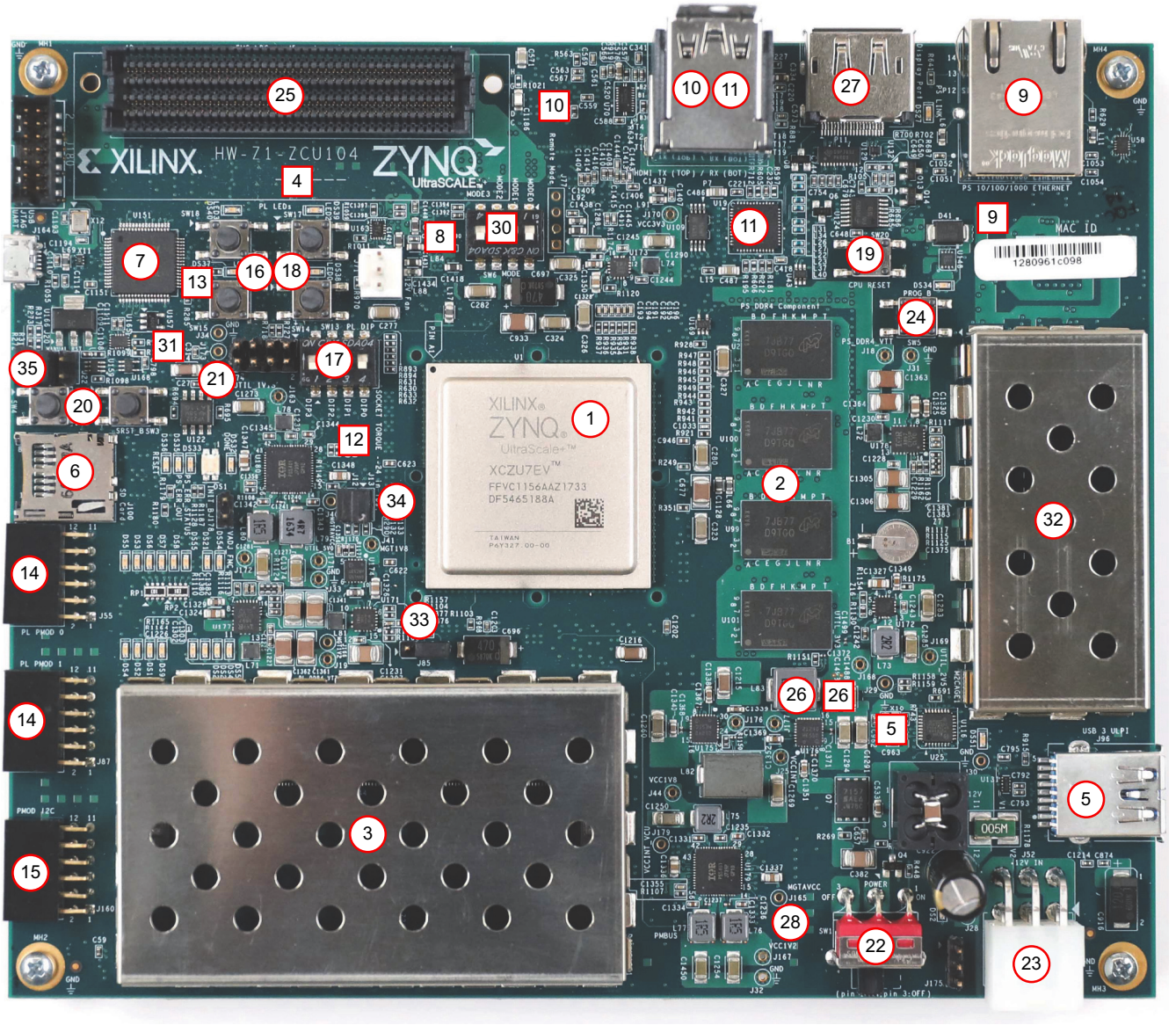


Figure 2-1: **ZCU104 Evaluation Board Components**

Table 2-1: **ZCU104 Board Component Locations**

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
1	U1	Zynq UltraScale+ XCZU7EV MPSoC with Radian fan sink	XCZU7EV-2FFVC1156 FA35+K52B+T725	3–18
2	U2, U99-U101	PS-Side: DDR4 Component Memory, (2 GB total)	Micron MT40A256M16GE-083E (DDR4-2400)	24–27
3	J1	PL-Side: DDR4 SODIMM Socket DDR4 SODIMM (not provided)	LOTES ADDR0067-P001A, supports MICRON MTA8ATF51264HZ-2G6B1	22
4	U119	Quad SPI Flash Memory (MIO 0–5) (512 Mb) [B]	Micron MT25QU512ABB8ESF-0SIT	36
5	U116, J96	USB 3.0 Transceiver and USB 2.0 ULPI PHY USB Micro-AB connector	SMSC USB3320-EZK, KYCON KMMX-AB10-SMT1SB30TR	40
6	J100	SD Card Interface connector	Hirose DMIAA-SF-PET(21)	37
7	U151, J164	Programmable Logic JTAG Programming Options	FTDI FT4232HL_64LQFP, Hirose ZX62D-AB-5P8	21
8	U182	IDT8T49N287 FemtoClock NG Octal Universal Frequency Translator [B]	IDT 8T49N287A-501NLGI	32
9	U98, P12	10/100/1000 MHz Tri-Speed Ethernet PHY [B], RJ45 with magnetics	TI DP83867IRPAP, Bel Fuse L829-1J1T-43	41
10	U94, P7	HDMI Video Output [B]	TI SN65DP159RGZ, TE Connectivity 1888811-1	29
11	U19, P7	HDMI Video Output	TI TMDS181IRGZT, TE Connectivity 1888811-1	30
12	U97	I2C1 (MIO 16-17) [B]	TI TCA6416APWR	44
13	U34	I2C1 (MIO 16-17) [B]	TI TCA9548APWR	45
14	J55, J87	User PMOD GPIO Connectors	SULLINS PPPC062LJBN-RC	43
15	J160	User I2C1 Receptacle	SULLINS PPPC062LJBN-RC	43
16	DS37-DS40	User I/O (4 x green 0603 LED)	LUMEX SML-LX0603GW	42
17	SW13	User I/O (4-pos. DIP switch)	CTS 218-4LPSTRF	42
18	SW14, 15, 17, 18	User I/O (4 X SPST pushbutton)	E-switch TL3301EP100QG	42
19	SW20	User I/O (CPU reset SPST pushbutton)	E-switch TL3301EP100QG	42
20	SW3, SW4	Switches (2 x SPST pushbutton, POR)	E-switch TL3301EP100QG	12
21	U122, J98	User I2C1 Receptacle	TI SN65HVD232, SULLINS PBC36DAAN	39

Table 2-1: **ZCU104 Board Component Locations *(Cont'd)***

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
22	SW1	Switches Power on/off slide switch)	C&K 1201M2S3AQE2	46
23	J52	Switches (2 x 3 mini-fit receptacle)	MOLEX 39-30-1060	46
24	SW5	Switches (PROG_B SPST pushbutton)	E-switch TL3301EP100QG	12
25	J5	FMC LPC Connector J5	Samtec ASP_134603_01	28
26	–	Board Power System (top and bottom of board)	Maxim Regulators	47–60
27	P11	DPAUX (MIO 27-30)	MOLEX 0472720001	34
28	J175	Monitoring Voltage and Current	Sullins PBC36SAAN (1x3 0.1 male pin header)	44
29	U181	HDMI Clock Recovery [B]	IDT8T49N241-994NLGI	31
30	SW6	Switches (MODE 4-pole DIP)	4-pole C&K SDA04H1SBD	12
31	U23	I2C1 (MIO 16-17) [B] (8 Kb EEPROM)	ST MICRO M24C08-WDW6TP	33
32	U170	PS M.2 SATA Connector	Amphenol MDT420M02001	38
33	J85	Jumpers (POR Override Sel)	Sullins PBC36SAAN (1x3 0.1 male pin header	3
34	J12, J13	Jumpers (SYSMON I2C ADDR)	Sullins PBC36SAAN (1x3 0.1 male pin header	3
35	J20, J21, J22	Jumpers (POR circuit)	Sullins PBC36SAAN (1x3 0.1 male pin header	12

Default Jumper and Switch Settings

Figure 2-1 shows the ZCU104 board jumper header and DIP switch locations. Each numbered component shown in the figure is keyed to Table 2-2 (for default jumper settings) or Table 2-3 (for default switch settings). Both tables reference the respective schematic page numbers.

Jumpers

Table 2-2: **Default Jumper Settings**

Number	Ref. Des.	Function	Default	Schematic Page
33	J85	POR_OVERRIDE • 1-2: Enable • 2-3: Disable	2-3	3
34	J12	SYSMON I2C address • Open: SYSMON_VP_R floating • 1-2: SYSMON_VP_P pulled down	1-2	3
34	J13	SYSMON I2C address • Open: SYSMON_VN_R floating • 1-2: SYSMON_VP_N pulled down	1-2	3
35	J20	Reset sequencer PS_POR_B • Open: Sequencer does not control PS_POR_B • 1-2: Sequencer can control PS_POR_B	1-2	12
35	J21	Reset sequencer PS_SRST_B • Open: Sequencer does not control PS_SRST_B • 1-2: Sequencer can control PS_SRST_B	1-2	12
35	J22	Reset sequencer inhibit • Open: Sequencer normal operation • 1-2: Sequencer inhibit (resets stay asserted)	Open	12

Switches

Table 2-3: **Default Switch Settings**

Number	Ref. Des.	Function	Default	Schematic Page
30	SW6	4-pole DIP switch PS_MODE select = [0010]		12
		(ON = pull down, OFF = pull up = 1)		
		4: PS_MODE3 PS_MODE[3:0] = 0010	On	
		3: PS_MODE2 = QSPI32 boot default	On	
		2: PS_MODE1	Off	
		1: PS_MODE0	On	
17	SW13	4-pole DIP switch GPIO	All Off	42
22	SW1	Main power slide switch	Off	46

MPSoC Device Configuration

Zynq UltraScale+ XCZU7EV MPSoC devices use a multi-stage boot process as described in the "Boot and Configuration" chapter of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2]. Switch SW6 configuration option settings are listed in Table 2-4.

Table 2-4: **Switch SW6 Configuration Option Settings**

Boot Mode	Mode Pins [3:0]	Mode SW6 [4:1]
JTAG	0000/0x0	ON,ON,ON,ON
QSPI32	0010/0x2(1)	ON,ON,OFF,ON
SD1	1110/0xE	OFF,OFF,OFF,ON

Notes:
1. Default switch setting.

JTAG

Vivado®, SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ MPSoC device through the FT4232 Quad USB to multipurpose UART (U151) with micro-USB connector (J164).

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid Zynq UltraScale+ MPSoC boot image in the Quad SPI flash device (U119) connected to the MIO Quad SPI interface.
2. Set the boot mode pins SW6 [4:1] PS_MODE[3:0] as indicated in Table 2-4 for Quad SPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton SW4. SW4 is callout 20 in Figure 2-1.

SD

To boot from an SD card:

1. Store a valid Zynq UltraScale+ MPSoC boot image file on to an SD card (plugged into SD socket J100) connected to the MIO SD interface.
2. Set the boot mode pins SW6 [4:1] PS_MODE[3:0] as indicated in Table 2-4 for SD1.
3. Either power-cycle or press the power-on reset (POR) pushbutton SW4. SW4 is callout 20 in Figure 2-1.

See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 13 identifies the components, references the respective schematic (0381794) page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Table 2-1, page 13.

Component Descriptions

Zynq UltraScale+ XCZU7EV MPSoC

[Figure 2-1, callout 1]

The ZCU104 board is populated with the Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Zynq UltraScale+ MPSoC features the ARM® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor. Support of multiple speed grades requires voltage adjustments.

The V_{CCINT} supplies are user adjustable via the PMBus with the voltage ranges listed in Table 3-1 to support multiple Zynq UltraScale+ MPSoC speed grades.

Table 3-1: **Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
Processing System					
$V_{CC\_PSINTFP}$	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V

The top-level block diagram is shown in Figure 3-1.

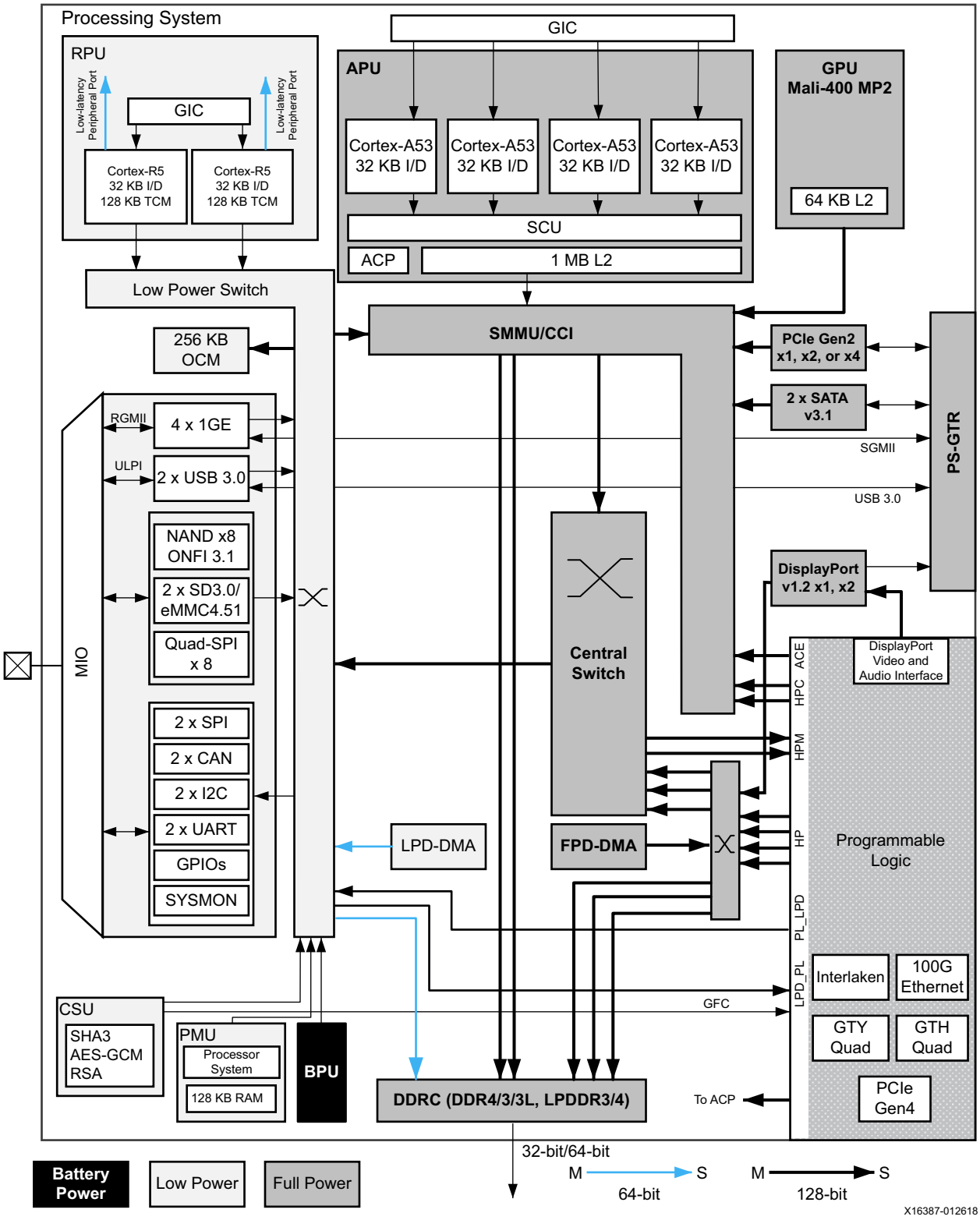


Figure 3-1: **Top-Level Block Diagram**

The Zynq UltraScale+ MPSoC PS block has three major processing units:

- Cortex-A53 application processing unit (APU)-ARM v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5 real-time processing unit (RPU)-ARM v7 architecture-based 32-bit dual real-time processing unit with dedicated tightly coupled memory (TCM).
- Mali-400 graphics processing unit (GPU)-graphics processing unit with pixel and geometry processor and 64 KB L2 cache.

The Zynq UltraScale+ MPSoC PS has four high-speed serial I/O (HSSIO) interfaces supporting these protocols:

- Integrated block for PCI Express® interface-PCIe™ base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- DisplayPort interface-implements a DisplayPort source-only interface with video resolution up to 4K x 2K-30 (300 MHz pixel rate).
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the PS. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ MPSoCs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO).and boots at power-up or reset.

For additional information on Zynq UltraScale+ MPSoC devices, see the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1]. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Encryption Key Battery Backup Circuit

The XCZU7EV MPSoC U1 implements bit stream encryption key technology. The ZCU104 board provides the encryption key backup battery circuit shown in Figure 3-2.

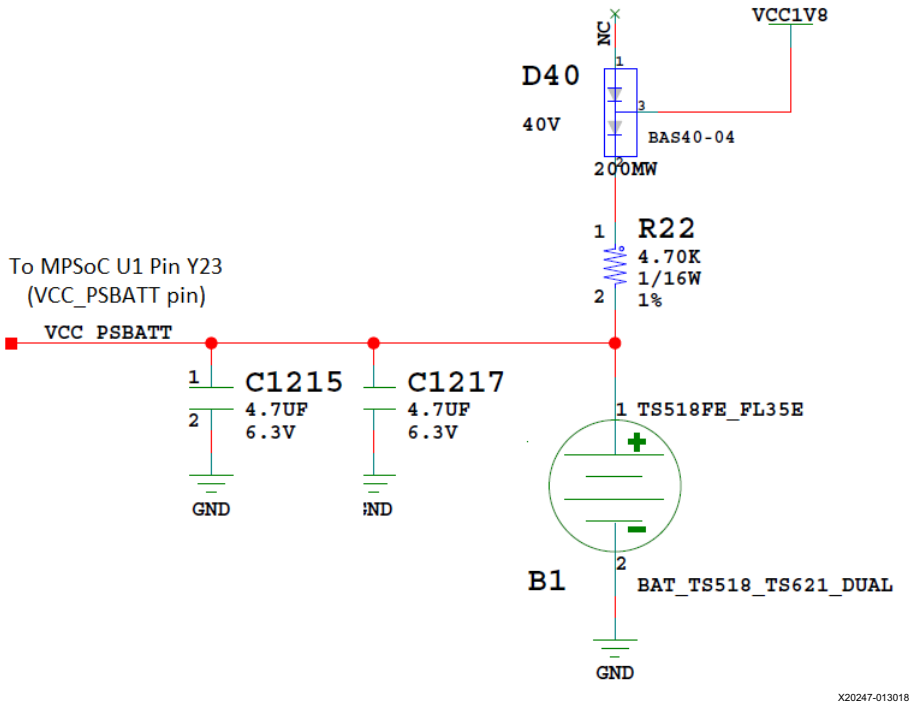


Figure 3-2: **Encryption Key Backup Circuit**

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCZU7EV MPSoC U1 V_{CC_PSBATT} pin Y23. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the UTIL_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 ΩK current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

The XCZU7EV MPSoC PL I/O bank voltages on the ZCU104 board are listed in Figure 3-2.

Table 3-2: **I/O Voltage Rails**

XCZU7EV	Power Net Name	Voltage	Connected To
PL Bank 28	V_{CC1V8}	1.8V	UART2 only (mostly NC pins)
PL Bank 64	V_{CC1V2}	1.2V	DDR4 SODIMM DQ[0:31] (PL)
PL Bank 65	V_{CC1V2}	1.2V	DDR4 SODIMM DQ[32:63] (PL)
PL Bank 66	V_{CC1V2}	1.2V	DDR4 SODIMM ADDR/CTRL (PL)
PL Bank 67	V_{ADJ_FMC}(1)	1.8V	FMC_LPC LA BUS
PL Bank 68	V_{ADJ_FMC}(1)	1.8V	FMC_LPC LA BUS
PL Bank 87	V_{CC3V3}	3.3V	PMOD0, PMOD1, HDMI CTRL, PL_I2C1
PL Bank 88	V_{CC3V3}	3.3V	HDMI, GPIO LED/DIP SW/PB SW
PS Bank 500	V_{CC1V8}	1.8V	CAN, UART0/1, I2C0/1, QSPI LWR
PS Bank 501	V_{CC1V8}	1.8V	SDIO, DP
PS Bank 502	V_{CC1V8}	1.8V	ENET, USB_DATA[0:7], USB_CTRL
PS Bank 503	V_{CC1V8}	1.8V	PS CONFIG I/F
PS Bank 504	V_{CC1V2}	1.2V	DDR4 (4x16-BIT) 64-BIT COMPONENT I/F (PS)

Notes:

1. The ZCU104 board is shipped with V_{ADJ_FMC} set to 1.8V.

PS-Side: DDR4 Component Memory

[Figure 2-1, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ DDRC bank 504 hard memory controller. PS-side memory is a 2 GB, 64-bit wide DDR4 memory system comprised of four 256 Mb x 16 SDRAMs (Micron MT40A256M16HA-083E) U2, and 99-101. The DDR4 0.6V VTT termination voltage is supplied from sink-source regulator U178. The connections between the DDR4 memory and the U1 XCZU7EV bank 504 are listed in Table 3-3.

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504**

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AN34	DDR4_A0	P3	A0	U2,U99-U101
AM34	DDR4_A1	P7	A1	U2,U99-U101
AM33	DDR4_A2	R3	A2	U2,U99-U101
AL34	DDR4_A3	N7	A3	U2,U99-U101
AL33	DDR4_A4	N3	A4	U2,U99-U101
AK33	DDR4_A5	P8	A5	U2,U99-U101
AK30	DDR4_A6	P2	A6	U2,U99-U101
AJ30	DDR4_A7	R8	A7	U2,U99-U101
AJ31	DDR4_A8	R2	A8	U2,U99-U101
AH31	DDR4_A9	R7	A9	U2,U99-U101
AG31	DDR4_A10	M3	A10/AP	U2,U99-U101
AF31	DDR4_A11	T2	A11	U2,U99-U101
AG30	DDR4_A12	M7	A12/BC_B	U2,U99-U101
AF30	DDR4_A13	T8	A13	U2,U99-U101
AE27	DDR4_BA0	N2	BA0	U2,U99-U101
AE28	DDR4_BA1	N8	BA1	U2,U99-U101
AD27	DDR4_BG0	M2	BG0	U2,U99-U101
AP27	DDR4_DQ0	G2	DQL0	U101
AP25	DDR4_DQ1	F7	DQL1	U101
AP26	DDR4_DQ2	H3	DQL2	U101
AM26	DDR4_DQ3	H7	DQL3	U101
AP24	DDR4_DQ4	H2	DQL4	U101
AL25	DDR4_DQ5	H8	DQL5	U101
AM25	DDR4_DQ6	J3	DQL6	U101
AM24	DDR4_DQ7	J7	DQL7	U101
AM28	DDR4_DQ8	A3	DQU0	U101

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AN28	DDR4_DQ9	B8	DQU1	U101
AP29	DDR4_DQ10	C3	DQU2	U101
AP28	DDR4_DQ11	C7	DQU3	U101
AM31	DDR4_DQ12	C2	DQU4	U101
AP31	DDR4_DQ13	C8	DQU5	U101
AN31	DDR4_DQ14	D3	DQU6	U101
AM30	DDR4_DQ15	D7	DQU7	U101
AF25	DDR4_DQ16	G2	DQL0	U99
AG25	DDR4_DQ17	F7	DQL1	U99
AG26	DDR4_DQ18	H3	DQL2	U99
AJ25	DDR4_DQ19	H7	DQL3	U99
AG24	DDR4_DQ20	H2	DQL4	U99
AK25	DDR4_DQ21	H8	DQL5	U99
AJ24	DDR4_DQ22	J3	DQL6	U99
AK24	DDR4_DQ23	J7	DQL7	U99
AH28	DDR4_DQ24	A3	DQU0	U99
AH27	DDR4_DQ25	B8	DQU1	U99
AJ27	DDR4_DQ26	C3	DQU2	U99
AK27	DDR4_DQ27	C7	DQU3	U99
AL26	DDR4_DQ28	C2	DQU4	U99
AL27	DDR4_DQ29	C8	DQU5	U99
AH29	DDR4_DQ30	D3	DQU6	U99
AL28	DDR4_DQ31	D7	DQU7	U99
AB29	DDR4_DQ32	G2	DQL0	U100
AB30	DDR4_DQ33	F7	DQL1	U100
AC29	DDR4_DQ34	H3	DQL2	U100
AD32	DDR4_DQ35	H7	DQL3	U100
AC31	DDR4_DQ36	H2	DQL4	U100
AE30	DDR4_DQ37	H8	DQL5	U100
AC28	DDR4_DQ38	J3	DQL6	U100
AE29	DDR4_DQ39	J7	DQL7	U100
AC27	DDR4_DQ40	A3	DQU0	U100
AA27	DDR4_DQ41	B8	DQU1	U100
AA28	DDR4_DQ42	C3	DQU2	U100

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AB28	DDR4_DQ43	C7	DQU3	U100
W27	DDR4_DQ44	C2	DQU4	U100
W29	DDR4_DQ45	C8	DQU5	U100
W28	DDR4_DQ46	D3	DQU6	U100
V27	DDR4_DQ47	D7	DQU7	U100
AA32	DDR4_DQ48	G2	DQL0	U2
AA33	DDR4_DQ49	F7	DQL1	U2
AA34	DDR4_DQ50	H3	DQL2	U2
AE34	DDR4_DQ51	H7	DQL3	U2
AD34	DDR4_DQ52	H2	DQL4	U2
AB31	DDR4_DQ53	H8	DQL5	U2
AC34	DDR4_DQ54	J3	DQL6	U2
AC33	DDR4_DQ55	J7	DQL7	U2
AA30	DDR4_DQ56	A3	DQU0	U2
Y30	DDR4_DQ57	B8	DQU1	U2
AA31	DDR4_DQ58	C3	DQU2	U2
W30	DDR4_DQ59	C7	DQU3	U2
Y33	DDR4_DQ60	C2	DQU4	U2
W33	DDR4_DQ61	C8	DQU5	U2
W34	DDR4_DQ62	D3	DQU6	U2
Y34	DDR4_DQ63	D7	DQU7	U2
AN24	DDR4_DM0	E7	DML_B/DBIL_B	U101
AM29	DDR4_DM1	E2	DMU_B/DBIU_B	U101
AH24	DDR4_DM2	E7	DML_B/DBIL_B	U99
AJ29	DDR4_DM3	E2	DMU_B/DBIU_B	U99
AD29	DDR4_DM4	E7	DML_B/DBIL_B	U100
Y29	DDR4_DM5	E2	DMU_B/DBIU_B	U100
AC32	DDR4_DM6	E7	DML_B/DBIL_B	U2
Y32	DDR4_DM7	E2	DMU_B/DBIU_B	U2
AN26	DDR4_DQS0_T	G3	DQSL_T	U101
AN27	DDR4_DQS0_C	F3	DQSL_C	U101
AN29	DDR4_DQS1_T	B7	DQSU_T	U101
AP30	DDR4_DQS1_C	A7	DQSU_C	U101
AH26	DDR4_DQS2_T	G3	DQSL_T	U99

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AJ26	DDR4_DQS2_C	F3	DQSL_C	U99
AK28	DDR4_DQS3_T	B7	DQSU_T	U99
AK29	DDR4_DQS3_C	A7	DQSU_C	U99
AD30	DDR4_DQS4_T	G3	DQSL_T	U100
AD31	DDR4_DQS4_C	F3	DQSL_C	U100
Y27	DDR4_DQS5_T	B7	DQSU_T	U100
Y28	DDR4_DQS5_C	A7	DQSU_C	U100
AB33	DDR4_DQS6_T	G3	DQSL_T	U2
AB34	DDR4_DQS6_C	F3	DQSL_C	U2
W31	DDR4_DQS7_T	B7	DQSU_T	U2
W32	DDR4_DQS7_C	A7	DQSU_C	U2
AL31	DDR4_CK_T	K7	CK_T	U2,U99-U101
AN32	DDR4_CK_C	K8	CK_C	U2,U99-U101
AN33	DDR4_CKE	K2	CKE	U2,U99-U101
AP32	DDR4_ODT	K3	ODT	U2,U99-U101
AF28	DDR4_A16_RAS_B	L8	RAS_B/A16	U2,U99-U101
AG28	DDR4_A15_CAS_B	M8	CAS_B_A15	U2,U99-U101
AG29	DDR4_A14_WE_B	L2	WE_B/A14	U2,U99-U101
AE25	DDR4_ACT_B	L3	ACT_B	U2,U99-U101
AB26	DDR4_ALERT_B	P9	ALERT_B	U2,U99-U101
AA26	DDR4_PAR	T3	PAR	U2,U99-U101
AD26	DDR4_RESET_B	P1	RESET_B	U2,U99-U101
AP33	DDR4_CS_B	L7	CS_B	U2,U99-U101
R156 P/D	DDR4_TEN	N9	TEN	U2,U99-U101

The ZCU104 board DDR4 64-bit component PS memory interface adheres to the constraints guidelines documented in the "PCB Guidelines for DDR4" section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3]. The ZCU104 DDR4 PS component interface is a 40Ω impedance implementations. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Product Guide* (PG150) [Ref 4]. For more details, see the Micron MT40A256M16HA-083E data sheet at the Micron website [Ref 10].

PL-Side: DDR4 SODIMM Socket

[Figure 2-1, callout 3]

PL-side banks 64, 65, and 66 are wired to DDR4 SODIMM socket J1. The ZCU104 kit is shipped without a DDR4 SODIMM. The recommended SODIMM is:

- Manufacturer: Micron
- Part Number: MTA8ATF51264HZ-2G6B1
- Description:
  - 4 GByte (x64)
  - 512 Meg x 8
  - Single rank
  - PC4-2666 260-Pin

The DDR4 SODIMM socket J1 connections are listed in Table 3-4.

Table 3-4: **DDR4 SODIMM Socket J1 Connections to FPGA PL Banks 64, 65, and 66**

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 SODIMM Memory J1	
			Pin Number	Pin Name
AH8	DDR4_SODIMM_A0	SSTL12_DCI	144	A0
AG8	DDR4_SODIMM_A1	SSTL12_DCI	133	A1
AF8	DDR4_SODIMM_A2	SSTL12_DCI	132	A2
AG10	DDR4_SODIMM_A3	SSTL12_DCI	131	A3
AG11	DDR4_SODIMM_A4	SSTL12_DCI	128	A4
AH9	DDR4_SODIMM_A5	SSTL12_DCI	126	A5
AG9	DDR4_SODIMM_A6	SSTL12_DCI	127	A6
AH13	DDR4_SODIMM_A7	SSTL12_DCI	122	A7
AK10	DDR4_SODIMM_A8	SSTL12_DCI	125	A8
AJ10	DDR4_SODIMM_A9	SSTL12_DCI	121	A9
AL8	DDR4_SODIMM_A10	SSTL12_DCI	146	A10/AP
AK8	DDR4_SODIMM_A11	SSTL12_DCI	120	A11
AL12	DDR4_SODIMM_A12	SSTL12_DCI	119	A12
AK12	DDR4_SODIMM_A13	SSTL12_DCI	158	A13
AL10	DDR4_SODIMM_BA0	SSTL12_DCI	150	BA0
AL11	DDR4_SODIMM_BA1	SSTL12_DCI	145	BA1
AE14	DDR4_SODIMM_BG0	SSTL12_DCI	115	BG0
AE13	DDR4_SODIMM_BG1	SSTL12_DCI	113	BG1

Table 3-4: **DDR4 SODIMM Socket J1 Connections to FPGA PL Banks 64, 65, and 66 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 SODIMM Memory J1	
			Pin Number	Pin Name
AG14	DDR4_SODIMM_DQ0	POD12_DCI	8	DQ0
AG15	DDR4_SODIMM_DQ1	POD12_DCI	7	DQ1
AF15	DDR4_SODIMM_DQ2	POD12_DCI	20	DQ2
AF16	DDR4_SODIMM_DQ3	POD12_DCI	21	DQ3
AF17	DDR4_SODIMM_DQ4	POD12_DCI	4	DQ4
AE17	DDR4_SODIMM_DQ5	POD12_DCI	3	DQ5
AG18	DDR4_SODIMM_DQ6	POD12_DCI	16	DQ6
AF18	DDR4_SODIMM_DQ7	POD12_DCI	17	DQ7
AD16	DDR4_SODIMM_DQ8	POD12_DCI	28	DQ8
AD17	DDR4_SODIMM_DQ9	POD12_DCI	29	DQ9
AB14	DDR4_SODIMM_DQ10	POD12_DCI	41	DQ10
AA14	DDR4_SODIMM_DQ11	POD12_DCI	42	DQ11
AB15	DDR4_SODIMM_DQ12	POD12_DCI	24	DQ12
AB16	DDR4_SODIMM_DQ13	POD12_DCI	25	DQ13
AC16	DDR4_SODIMM_DQ14	POD12_DCI	38	DQ14
AC17	DDR4_SODIMM_DQ15	POD12_DCI	37	DQ15
AJ15	DDR4_SODIMM_DQ16	POD12_DCI	50	DQ16
AJ16	DDR4_SODIMM_DQ17	POD12_DCI	49	DQ17
AK17	DDR4_SODIMM_DQ18	POD12_DCI	62	DQ18
AJ17	DDR4_SODIMM_DQ19	POD12_DCI	63	DQ19
AL18	DDR4_SODIMM_DQ20	POD12_DCI	46	DQ20
AK18	DDR4_SODIMM_DQ21	POD12_DCI	45	DQ21
AL15	DDR4_SODIMM_DQ22	POD12_DCI	58	DQ22
AL16	DDR4_SODIMM_DQ23	POD12_DCI	59	DQ23
AN16	DDR4_SODIMM_DQ24	POD12_DCI	70	DQ24
AN17	DDR4_SODIMM_DQ25	POD12_DCI	71	DQ25
AP15	DDR4_SODIMM_DQ26	POD12_DCI	83	DQ26
AP16	DDR4_SODIMM_DQ27	POD12_DCI	84	DQ27
AN18	DDR4_SODIMM_DQ28	POD12_DCI	66	DQ28
AM18	DDR4_SODIMM_DQ29	POD12_DCI	67	DQ29
AP13	DDR4_SODIMM_DQ30	POD12_DCI	79	DQ30
AN13	DDR4_SODIMM_DQ31	POD12_DCI	80	DQ31
AA20	DDR4_SODIMM_DQ32	POD12_DCI	174	DQ32
AA19	DDR4_SODIMM_DQ33	POD12_DCI	173	DQ33

Table 3-4: **DDR4 SODIMM Socket J1 Connections to FPGA PL Banks 64, 65, and 66 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 SODIMM Memory J1	
			Pin Number	Pin Name
AD19	DDR4_SODIMM_DQ34	POD12_DCI	187	DQ34
AC18	DDR4_SODIMM_DQ35	POD12_DCI	186	DQ35
AE20	DDR4_SODIMM_DQ36	POD12_DCI	170	DQ36
AD20	DDR4_SODIMM_DQ37	POD12_DCI	169	DQ37
AC19	DDR4_SODIMM_DQ38	POD12_DCI	183	DQ38
AB19	DDR4_SODIMM_DQ39	POD12_DCI	182	DQ39
AE24	DDR4_SODIMM_DQ40	POD12_DCI	195	DQ40
AE23	DDR4_SODIMM_DQ41	POD12_DCI	194	DQ41
AF22	DDR4_SODIMM_DQ42	POD12_DCI	207	DQ42
AF21	DDR4_SODIMM_DQ43	POD12_DCI	208	DQ43
AG20	DDR4_SODIMM_DQ44	POD12_DCI	191	DQ44
AG19	DDR4_SODIMM_DQ45	POD12_DCI	190	DQ45
AH21	DDR4_SODIMM_DQ46	POD12_DCI	203	DQ46
AG21	DDR4_SODIMM_DQ47	POD12_DCI	204	DQ47
AJ22	DDR4_SODIMM_DQ48	POD12_DCI	216	DQ48
AJ21	DDR4_SODIMM_DQ49	POD12_DCI	215	DQ49
AK20	DDR4_SODIMM_DQ50	POD12_DCI	228	DQ50
AJ20	DDR4_SODIMM_DQ51	POD12_DCI	229	DQ51
AK19	DDR4_SODIMM_DQ52	POD12_DCI	211	DQ52
AJ19	DDR4_SODIMM_DQ53	POD12_DCI	212	DQ53
AL23	DDR4_SODIMM_DQ54	POD12_DCI	224	DQ54
AL22	DDR4_SODIMM_DQ55	POD12_DCI	225	DQ55
AN23	DDR4_SODIMM_DQ56	POD12_DCI	237	DQ56
AM23	DDR4_SODIMM_DQ57	POD12_DCI	236	DQ57
AP23	DDR4_SODIMM_DQ58	POD12_DCI	249	DQ58
AN22	DDR4_SODIMM_DQ59	POD12_DCI	250	DQ59
AP22	DDR4_SODIMM_DQ60	POD12_DCI	232	DQ60
AP21	DDR4_SODIMM_DQ61	POD12_DCI	233	DQ61
AN19	DDR4_SODIMM_DQ62	POD12_DCI	245	DQ62
AM19	DDR4_SODIMM_DQ63	POD12_DCI	246	DQ63
AH18	DDR4_SODIMM_DM0_B	POD12_DCI	12	DM0_N/DBI0_N
AD15	DDR4_SODIMM_DM1_B	POD12_DCI	33	DM1_N/DBI1_N
AM16	DDR4_SODIMM_DM2_B	POD12_DCI	54	DM2_N/DBI2_N
AP18	DDR4_SODIMM_DM3_B	POD12_DCI	75	DM3_N/DBI3_N

Table 3-4: **DDR4 SODIMM Socket J1 Connections to FPGA PL Banks 64, 65, and 66 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 SODIMM Memory J1	
			Pin Number	Pin Name
AE18	DDR4_SODIMM_DM4_B	POD12_DCI	178	DM4_N/DBI4_N
AH22	DDR4_SODIMM_DM5_B	POD12_DCI	199	DM5_N/DBI5_N
AL20	DDR4_SODIMM_DM6_B	POD12_DCI	220	DM6_N/DBI6_N
AP19	DDR4_SODIMM_DM7_B	POD12_DCI	241	DM7_N/DBI7_N
AH14	DDR4_SODIMM_DQS0_T	DIFF_POD12_DCI	13	DQS0_T
AJ14	DDR4_SODIMM_DQS0_C	DIFF_POD12_DCI	11	DQS0_C
AA16	DDR4_SODIMM_DQS1_T	DIFF_POD12_DCI	34	DQS1_T
AA15	DDR4_SODIMM_DQS1_C	DIFF_POD12_DCI	32	DQS1_C
AK15	DDR4_SODIMM_DQS2_T	DIFF_POD12_DCI	55	DQS2_T
AK14	DDR4_SODIMM_DQS2_C	DIFF_POD12_DCI	53	DQS2_C
AM14	DDR4_SODIMM_DQS3_T	DIFF_POD12_DCI	76	DQS3_T
AN14	DDR4_SODIMM_DQS3_C	DIFF_POD12_DCI	74	DQS3_C
AA18	DDR4_SODIMM_DQS4_T	DIFF_POD12_DCI	179	DQS4_T
AB18	DDR4_SODIMM_DQS4_C	DIFF_POD12_DCI	177	DQS4_C
AF23	DDR4_SODIMM_DQS5_T	DIFF_POD12_DCI	200	DQS5_T
AG23	DDR4_SODIMM_DQS5_C	DIFF_POD12_DCI	198	DQS5_C
AK22	DDR4_SODIMM_DQS6_T	DIFF_POD12_DCI	221	DQS6_T
AK23	DDR4_SODIMM_DQS6_C	DIFF_POD12_DCI	219	DQS6_C
AM21	DDR4_SODIMM_DQS7_T	DIFF_POD12_DCI	242	DQS7_T
AN21	DDR4_SODIMM_DQS7_C	DIFF_POD12_DCI	240	DQS7_C
AH11	DDR4_SODIMM_CK0_T	DIFF_SSTL12_DCI	139	CK0_C
AJ11	DDR4_SODIMM_CK0_C	DIFF_SSTL12_DCI	137	CK0_T
AJ9	DDR4_SODIMM_CK1_T	DIFF_SSTL12_DCI	140	CK1_C/NF
AK9	DDR4_SODIMM_CK1_C	DIFF_SSTL12_DCI	138	CK1_T/NF
AB13	DDR4_SODIMM_CKE0	SSTL12_DCI	109	CKE0
AL13	DDR4_SODIMM_CKE1	SSTL12_DCI	110	CKE1
AF10	DDR4_SODIMM_ODT0	SSTL12_DCI	155	ODT0
AK13	DDR4_SODIMM_ODT1	SSTL12_DCI	161	ODT1
AF11	DDR4_SODIMM_RAS_B	SSTL12_DCI	152	RAS_N/A16
AE12	DDR4_SODIMM_CAS_B	SSTL12_DCI	156	CAS_N/A15
AC12	DDR4_SODIMM_WE_B	SSTL12_DCI	151	WE_N/A14
AD14	DDR4_SODIMM_ACT_B	SSTL12_DCI	114	ACT_N
AF13	DDR4_SODIMM_ALERT_B	SSTL12_DCI	116	ALERT_N
AC13	DDR4_SODIMM_PARITY	SSTL12_DCI	143	PARITY

Table 3-4: **DDR4 SODIMM Socket J1 Connections to FPGA PL Banks 64, 65, and 66 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 SODIMM Memory J1	
			Pin Number	Pin Name
AD12	DDR4_SODIMM_CS0_B	SSTL12_DCI	149	CS0_N
AM13	DDR4_SODIMM_CS1_B	SSTL12_DCI	157	CS1_N
AF12	DDR4_SODIMM_RESET_B	LVCMOS12	108	RESET_N

The ZCU104 board PL DDR4 SODIMM interface adheres to the constraints guidelines documented in the "PCB Guidelines for DDR4" section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3]. The PL DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Product Guide* (PG150) [Ref 4].

PSMIO

Table 3-5 provides PS MIO peripheral mapping implemented on the ZCU104 board. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information on PS MIO peripheral mapping.

Table 3-5: **MIO Connections**

MIO [25:0] Bank 500	ZU7EV U1 Pin No.	Schematic Net Name	Type	MI [51:26] Bank 501	ZU7EV U1 Pin No.	Schematic Net Name	Type	MIO [77:52] Bank 502	ZU7EV U1 Pin No.	Schematic Net Name	Type
MIO25	D29	MIO25_CAN_RX	CAN	MIO51	F34	MIO51_SDIO_CLK_R	SD1	MIO77	L34	MIO77_ENET_MDIO	MDIO3
MIO24	E28	MIO24_CAN_TX	CAN	MIO50	F33	MIO50_SDIO_CMD_R	SD1	MIO76	L33	MIO76_ENET_MDC	MDIO3
MIO23	B29	Not Connected	NC	MIO49	F32	MIO49_SDIO_DAT3_R	SD1	MIO75	L30	MIO75_ENET_RX_CTRL	GEM3
MIO22	F28	Not Connected	NC	MIO48	F31	MIO48_SDIO_DAT2_R	SD1	MIO74	L29	MIO74_ENET_RX_D3	GEM3
MIO21	C28	UART1_TXD_MIO21_RXD	UART1	MIO47	F30	MIO47_SDIO_DAT1_R	SD1	MIO73	K34	MIO73_ENET_RX_D2	GEM3
MIO20	E29	UART1_RXD_MIO20_TXD	UART1	MIO46	E34	MIO46_SDIO_DAT0_R	SD1	MIO72	K33	MIO72_ENET_RX_D1	GEM3
MIO19	B28	UART0_RXD_MIO19_TXD	UART0	MIO45	E33	MIO45_SDIO_DETECT	SD1	MIO71	K32	MIO71_ENET_RX_D0	GEM3
MIO18	F27	UART0_TXD_MIO18_RXD	UART0	MIO44	E32	Not Connected	NC	MIO70	K31	MIO70_ENET_RX_CLK	GEM3
MIO17	C29	MIO17_I2C1_SDA	I2C1	MIO43	E30	Not Connected	NC	MIO69	K30	MIO69_ENET_TX_CTRL	GEM3
MIO16	A28	MIO16_I2C1_SCL	I2C1	MIO42	D34	Not Connected	NC	MIO68	K29	MIO68_ENET_TX_D3	GEM3
MIO15	E27	Not Connected	NC	MIO41	D32	Not Connected	NC	MIO67	K28	MIO67_ENET_TX_D2	GEM3
MIO14	A27	Not Connected	NC	MIO40	D31	Not Connected	NC	MIO66	J34	MIO66_ENET_TX_D1	GEM3
MIO13	D27	Not Connected	NC	MIO39	D30	Not Connected	NC	MIO65	J32	MIO65_ENET_TX_D0	GEM3
MIO12	C27	Not Connected	NC	MIO38	C34	Not Connected	NC	MIO64	J31	MIO64_ENET_TX_CLK	GEM3
MIO11	B26	Not Connected	NC	MIO37	C33	Not Connected	NC	MIO63	J30	MIO63_USB_DATA7_R	USB0
MIO10	F26	Not Connected	NC	MIO36	C32	Not Connected	NC	MIO62	J29	MIO62_USB_DATA6_R	USB0
MIO9	C26	Not Connected	NC	MIO35	C31	Not Connected	NC	MIO61	H34	MIO61_USB_DATA5_R	USB0
MIO8	D26	Not Connected	NC	MIO34	B34	Not Connected	NC	MIO60	H33	MIO60_USB_DATA4_R	USB0
MIO7	B25	Not Connected	NC	MIO33	B33	Not Connected	NC	MIO59	H32	MIO59_USB_DATA3_R	USB0
MIO6	A26	Not Connected	NC	MIO32	B31	Not Connected	NC	MIO58	H31	MIO58_USB_STP_R	USB0
MIO5	D25	MIO5_QSPI_LWR_CS_B	QSPI	MIO31	B30	Not Connected	NC	MIO57	H29	MIO57_USB_DATA1_R	USB0

Table 3-5: **MIO Connections *(Cont'd)***

MIO [25:0] Bank 500	ZU7EV U1 Pin No.	Schematic Net Name	Type	MI [51:26] Bank 501	ZU7EV U1 Pin No.	Schematic Net Name	Type	MIO [77:52] Bank 502	ZU7EV U1 Pin No.	Schematic Net Name	Type
MIO4	A25	MIO4_QSPI_LWR_DQ0	QSPI	MIO30	A33	MIO30_DP_AUX_IN	DPAUX	MIO56	G34	MIO56_USB_DATA0_R	USB0
MIO3	E25	MIO3_QSPI_LWR_DQ3	QSPI	MIO29	A32	MIO29_DP_OE	DPAUX	MIO55	G33	MIO55_USB_NXT	USB0
MIO2	B24	MIO2_QSPI_LWR_DQ2	QSPI	MIO28	A31	MIO28_DP_HPD	DPAUX	MIO54	G31	MIO54_USB_DATA2_R	USB0
MIO1	C24	MIO1_QSPI_LWR_DQ1	QSPI	MIO27	A30	MIO27_DP_AUX_OUT	DPAUX	MIO53	G30	MIO53_USB_DIR	USB0
MIO0	A24	MIO0_QSPI_LWR_CLK	QSPI	MIO26	A29	Not Connected	NC	MIO52	G29	MIO52_USB_CLK	USB0

Quad SPI Flash Memory (MIO 0–5)

[Figure 2-1, callout 4]

The Micron MT25QU512ABB8ESF serial NOR flash Quad SPI flash memory can hold the boot image for the MPSoC system. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2].

The Quad SPI flash memory (U119) is located on the bottom of the board, and provides 512 Mb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABB8ESF-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: Various depending on single, dual, or quad mode

The connections between the SPI flash memory and the XCZU7EV MPSoC are listed in Table 3-6.

Table 3-6: **Quad SPI Flash Memory Component Connections to MPSoC U1**

XCZU7EV (U1) Pin	Net Name	Quad SPI U119 (LWR), U120 (UPR)	
		Pin #	Pin Name
A25	MIO4_QSPI_LWR_DQ0	15	DQ0
C24	MIO1_QSPI_LWR_DQ1	8	DQ1
B24	MIO2_QSPI_LWR_DQ2	9	DQ2_WP_B
E25	MIO3_QSPI_LWR_DQ3	1	DQ3_RST_HOLD_B
A24	MIO0_QSPI_LWR_CLK	16	C
D25	MIO5_QSPI_LWR_CS_B	7	S_B

The configuration and Quad SPI flash memory section of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] provides details on using the memory. For more Quad SPI details, see the Micron MT25QU512ABB8ESF-0SIT data sheet at the Micron website [Ref 10].

USB0 (MIO 52-63)

The USB interface on the PS-side serves multiple roles as a host or device controller. The USB 3.0 interface is supported by the MPSoC GTR interface while the USB 2.0 capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 USB type AB connector (J96).

USB 3.0 Transceiver and USB 2.0 ULPI PHY

[Figure 2-1, callout 5]

The ZCU104 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver at U116 to support a USB connection to the host computer (see Figure 3-3). A USB cable is supplied in the ZCU104 evaluation kit (standard-A connector to host computer, micro-B connector to ZCU104 board connector J96). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

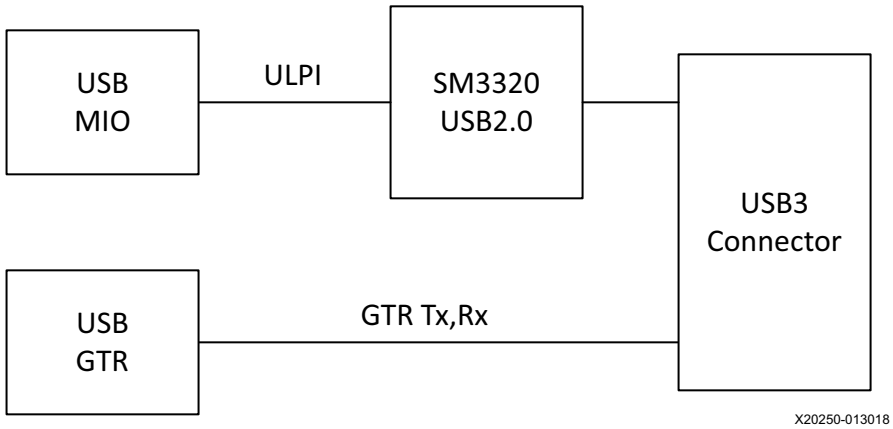


Figure 3-3: **USB Interface**

The USB3320 is clocked by a 24 MHz crystal. See the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [Ref 11]. The interface to the USB3320 PHY is implemented through the IP in the XCZU7EV MPSoC PS. The ZCU104 USB3320 PHY supports host only mode. The connections between the USB 2.0 PHY at U116 and the XCZU7EV MPSoC are listed in Table 3-7.

Table 3-7: **USB 2.0 ULPI Transceiver Connections to XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	USB3320 U116	
		Pin #	Pin Name
U168.4	ULPI0_RST_B(1)	27	RESET_B
H31	MIO58_USB_STP(2)	29	STP
G30	MIO53_USB_DIR	31	DIR
G29	MIO52_USB_CLK	1	CLKOUT
G33	MIO55_USB_NXT	2	NXT
G34	MIO56_USB_DATA0(2)	3	DATA0
H29	MIO57_USB_DATA1(2)	4	DATA1
G31	MIO54_USB_DATA2(2)	5	DATA2
H32	MIO59_USB_DATA3(2)	6	DATA3
H33	MIO60_USB_DATA4(2)	7	DATA4
H34	MIO61_USB_DATA5(2)	9	DATA5
J29	MIO62_USB_DATA6(2)	10	DATA6
J30	MIO63_USB_DATA7(2)	13	DATA7

Notes:

1. PS_POR_B (U1.M24) or PS_MODE1 (DIP SW6.2) drive U116 RST_B via OR gate U168.
2. These nets are 30Ω series resistor coupled.

The USB3320 ULPI U116 transceiver circuit (see Figure 3-4) has a Micrel MIC2544 high-side programmable current limit switch (U121). This switch has an open-drain output fault flag on pin 2, which turns on LED DS51 if over current or thermal shutdown conditions are detected. DS51 is located in the U116 circuit area near pushbutton SW4 (Figure 2-1, callout 20).

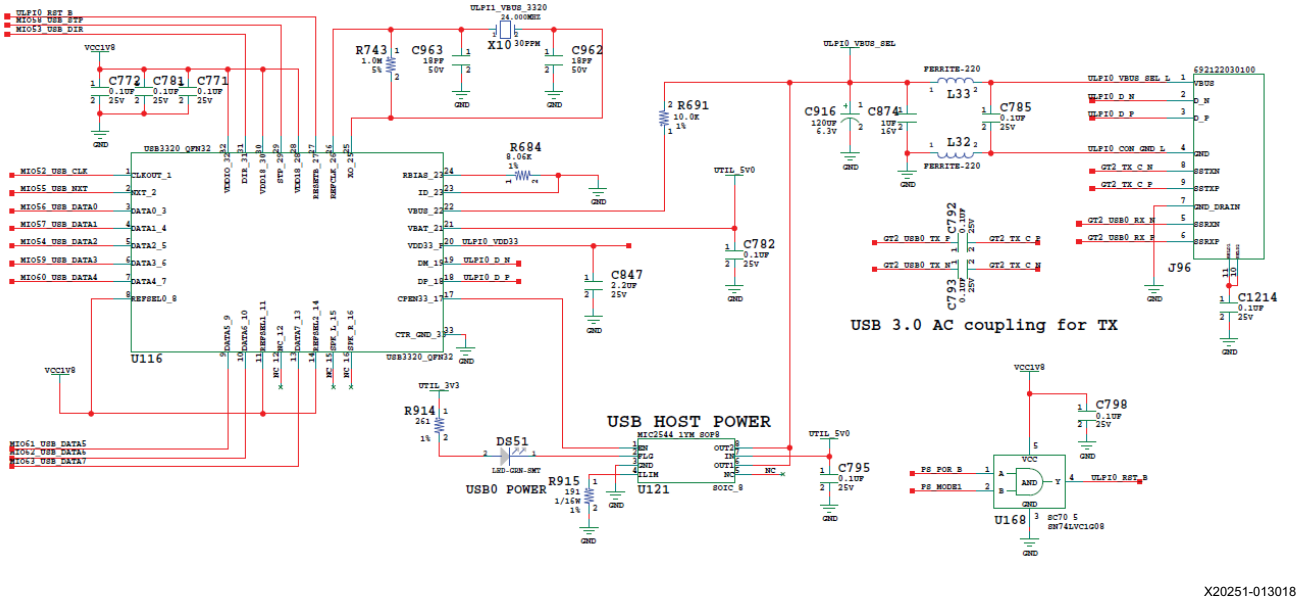


Figure 3-4: **ULPI U116 Transceiver Circuit**

SD1 (MIO 45-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

SD Card Interface

[Figure 2-1, callout 6]

The ZCU104 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. See the SanDisk Corporation [Ref 12] or SD Association [Ref 13] websites for more information on the SD I/O card specification. The ZCU104 SD card interface supports the SD1_LS configuration boot mode documented in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2].

The SDIO signals are connected to XCZU7EV MPSoC PS bank 501, which has its V_{CCMIO} set to 1.8V. Each of the six MIOxx_SDIO_* nets has a series 30Ω resistor at the source. A MAX13035E voltage level-translator (U145) is present between the XCZU7EV MPSoC and the SD card connector (J100).

Figure 3-5 shows the connections of the SD card interface on the ZCU104 board.

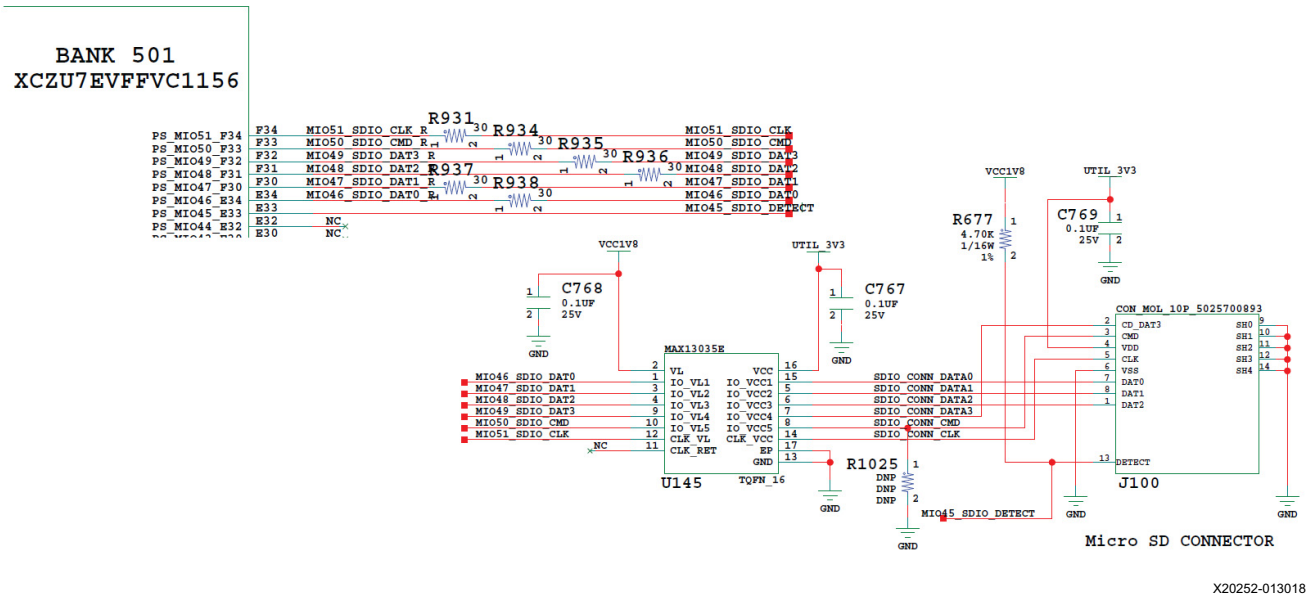


Figure 3-5: **SD Card Interface**

Table 3-8 lists the SD card interface connections to the XCZU7EV MPSoC.

Table 3-8: **XCZU7EV MIO Connections to SD Socket via U145**

XCZU7EV (U1) Pin	Net Name	J100 SD Card Socket	
		Pin #	Pin Name
E34	MIO46_SDIO_DAT0	7	DAT0
F30	MIO47_SDIO_DAT1	8	DAT1
F31	MIO48_SDIO_DAT2	1	DAT2
F32	MIO49_SDIO_DAT3	2	CD_DAT3
F33	MIO50_SDIO_CMD	3	CMD
F34	MIO51_SDIO_CLK	5	CLK
E33	MIO45_SDIO_DETECT	13	DETECT

Programmable Logic JTAG Programming Options

[Figure 2-1, callouts 7 and 25]

The ZCU104 board JTAG chain is shown in Figure 3-6.

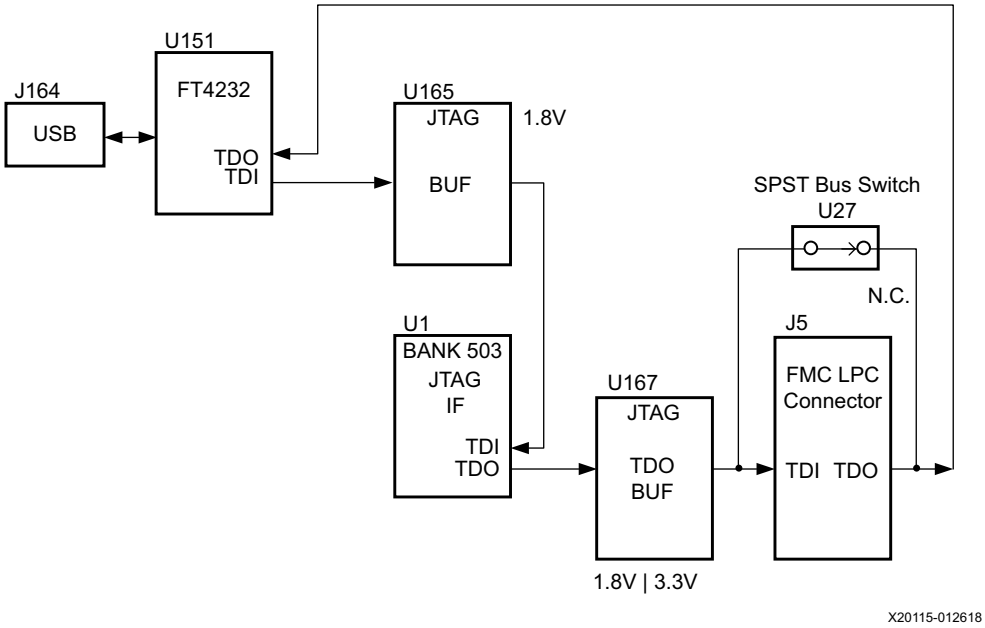


Figure 3-6: **JTAG Chain Block Diagram**

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J5, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switch U27. The SPST switch is normally closed and transitions to an open state when an FMC is attached. Switch U27 adds an attached FMC to the JTAG chain as determined by the FMC_LPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the U1 XCZU7EV MPSoC.

PS M.2 SATA Connector

[Figure 2-1, callout 32]

The M.2 SATA interface is provided for SATA SSD access using the PS-side bank 505 GTR transceiver. Figure 3-7 shows M.2 connector U170.

The socket 2 SATA adapter pinout with key M is shown in Table 3-9. SATA-A data connection is used for TX and SATA-B for RX. The M.2 connector U170 is a type 2242 (active component section 22 mm wide with overall length 42 mm form factor) used on socket 2.

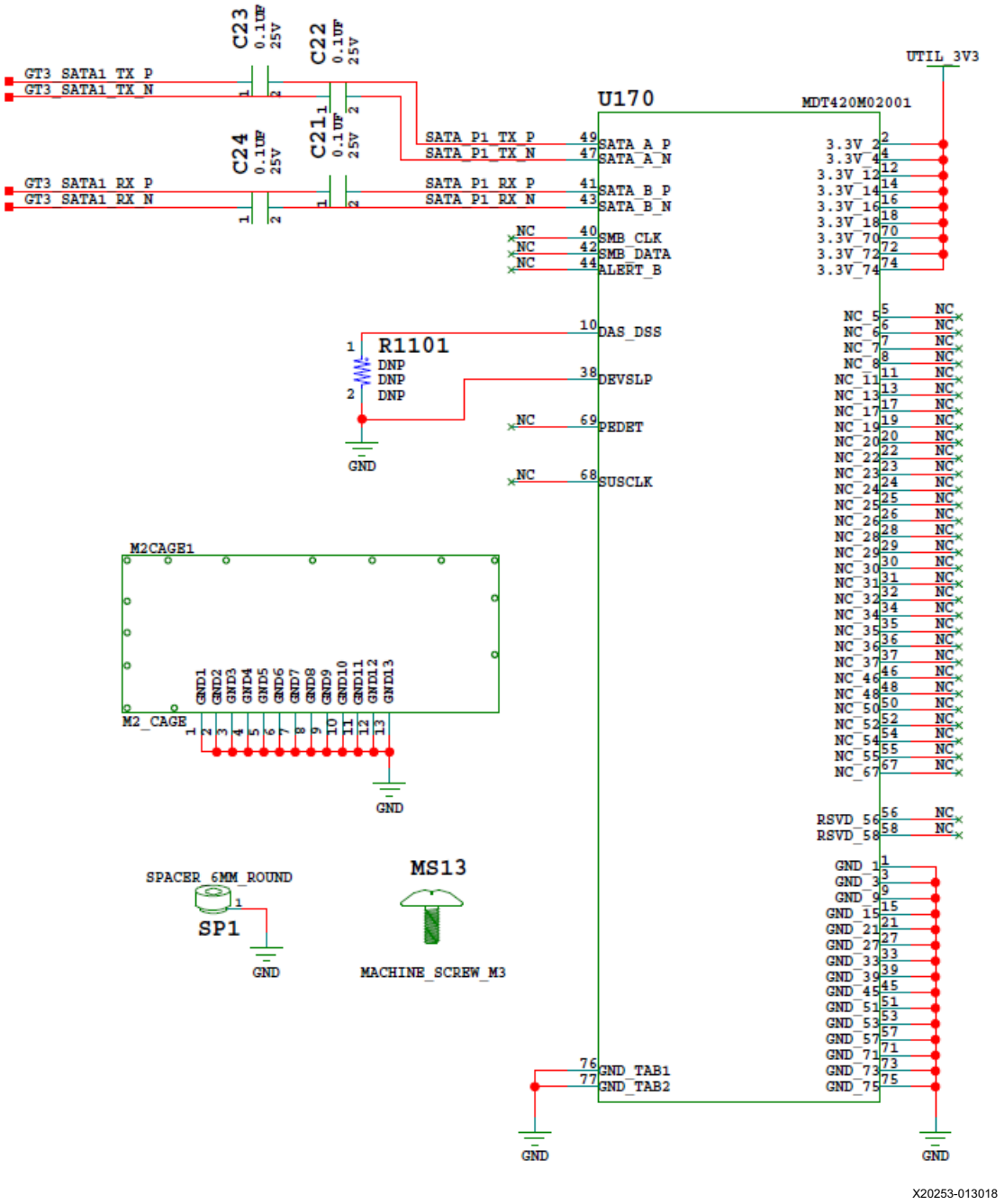


Figure 3-7: **M.2 Connector U170**

The M.2 U170 connector pinout is listed in Table 3-9.

Table 3-9: **M.2 Connector U170 Pinout**

Pin	Signal
74	3.3V
72	3.3V
70	3.3V
68	SUSCLK(32 kHz) (I)(0/3.3V)
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
58	Reserved for MGFG_CLOCK
56	Reserved for MGFG_DATA
54	NC
52	NC
50	NC
48	NC
46	NC
44	ALERT# (O) (0/1.8V)
42	SMB_DATA (I/O) (0/1.8V)
40	SMB_CLK (I/O) (0/1.8V)
38	DEVSLP (I)
36	NC
34	NC
32	NC
30	NC
28	NC
26	NC
24	NC
22	NC
20	NC
18	3.3V
16	3.3V
14	3.3V
12	3.3V
10	DAS/DSS (I/O)

Table 3-9: **M.2 Connector U170 Pinout *(Cont'd)***

Pin	Signal
8	NC
6	NC
4	3.3V
2	3.3V
75	GND
73	GND
71	GND
69	PEDET (GND-SATA)
67	NC
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
57	GND
55	NC
53	NC
51	GND
49	SATA-A+
47	SATA-A-
45	GND
43	SATA-B+
41	SATA-B-
39	GND
37	NC
35	NC
33	GND
31	NC
29	NC
27	GND
25	NC
23	NC
21	GND
19	NC
17	NC
15	GND

Table 3-9: **M.2 Connector U170 Pinout *(Cont'd)***

Pin	Signal
13	NC
11	NC
9	GND
7	NC
5	NC
3	GND
1	GND

The M.2 adapter tie-offs as implemented on the ZCU104 board are listed in Table 3-10.

Table 3-10: **M.2 U170 Connector Tie-offs**

M.2 Signal Name	ZCU104 Tie-Off	U170 Pin
SUSCLK	No Connect	68
ALERT#	No Connect	44
SMB_DATA	No Connect	42
SMB_CLK	No Connect	40
DEVSLP	GND	38
DAS/DSS	DNP Res to GND	10
PEDET	No Connect	69
SATA-A	GTR TX	49, 47
SATA-B	GTR RX	43, 41

The M.2 U170 connector to MPSoC connections are listed in Table 3-11.

Table 3-11: **M.2 U170 Connections to XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	I/O Standard	M.2 Connector U170	
			Pin Number	Pin Name
N29	GT3_SATA1_TX_P	(1)	49	SATA-A+
N30	GT3_SATA1_TX_N	(1)	47	SATA-A-
N33	GT3_SATA1_RX_P	(1)	41	SATA-B+
N34	GT3_SATA1_RX_N	(1)	43	SATA-B-

Notes:
1. Series capacitor coupled, MGT I/F, I/O standards do not apply.

For more information, see PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB [Ref 16].

Clock Generation

The ZCU104 board provides an IDT8T49N287 FemtoClock® NG octal universal frequency translator (U182) clock generator. Table 3-12 lists the frequency for each clock.

Table 3-12: **Clock Sources**

Clock (Net) Name	Frequency	IDT8T49N287 U182 Clock Output
HDMI_DRU_CLOCK	156.25 MHz	Q0
PS_REF_CLK	33.33 MHz	Q1
GTR_REF_CLK_USB3	24 MHz	Q2
GTR_REF_CLK_DP	27 MHz	Q3
CLK_300_P	300 MHz	Q4
GTR_REF_CLK_SATA	125 MHz	Q5
CLK_125	125 MHz	Q6

Table 3-13 lists the connectivity for each clock.

Table 3-13: **Clock Connections, Source to XCZU7EV MPSoC**

Clock Source Pin	Net Name	I/O Standard	XCZU7EV (U1) Pin
U182.48	HDMI_DRU_CLOCK_P	(2)	U10
U182.47	HDMI_DRU_CLOCK_N	(2)	U9
U182.44	PS_REF_CLK	LVCMOS18(1)	R24
U182.27	GTR_REF_CLK_USB3_P	(2)	M27
U182.28	GTR_REF_CLK_USB3_N	(2)	M28
U182.23	GTR_REF_CLK_DP_P	(2)	M31
U182.24	GTR_REF_CLK_DP_N	(2)	M32
U182.40	CLK_300_C_P	(2)	AH12
U182.39	CLK_300_C_N	(2)	AJ12
U182.37	GTR_REF_CLK_SATA_P	(2)	P27
U182.36	GTR_REF_CLK_SATA_N	(2)	P28
U182.34	CLK_125_P	LVDS	H11
U182.33	CLK_125_N	LVDS	G11

Notes:

1. U1 XCU7EV Bank 503 supports LVCMOS level inputs.
2. U1 MGT (I/O standards do not apply).

IDT8T49N287 FemtoClock NG Octal Universal Frequency Translator

[Figure 2-1, callout 8]

- Clock generator: IDT8T49N287A-501NLGI
- Jitter: <0.3 ps RMS typical

The IDT8T49N287A-501NLGI U182 (located on the bottom of the board) is a one-time programmable clock source with frequency adjustment available over the I2C bus. The clock circuit is shown in Figure 3-8.

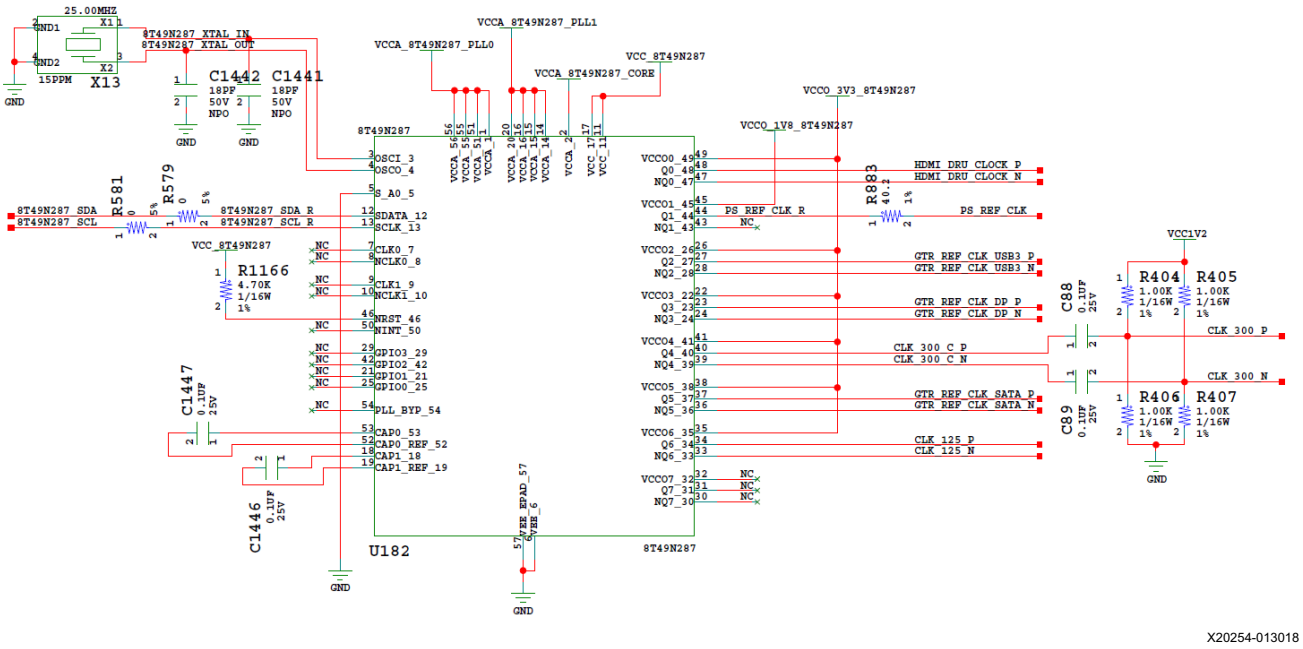


Figure 3-8: **IDT8T49N287 Clock Generator**

For more details, see the IDT8T49N287A data sheet [Ref 20].

GEM3 Ethernet (MIO 64-77)

The PS-side Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (see Figure 3-9), which connects to a TI DP83867IRPAP Ethernet RGMII PHY U98 routed to an RJ45 Ethernet connector. The RGMII Ethernet PHY is boot strapped to PHY address `5'b01100` (`0x0C`) and Auto Negotiation is set to *Enable*. The communication with the device is described in the DP83867 RGMII PHY data sheet [Ref 15].

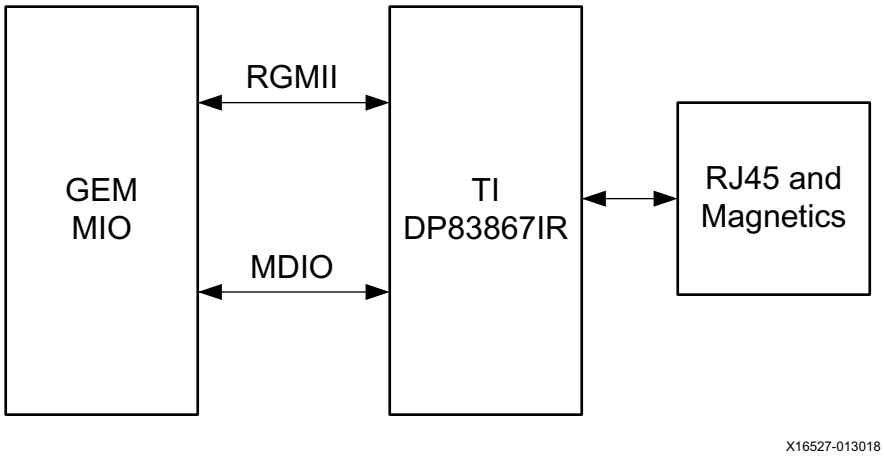


Figure 3-9: **Ethernet Block Diagram**

10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2-1, callout 9]

The ZCU104 board uses the TIDP83867IRPAP Ethernet RGMII PHY [Ref 15] (U98) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Bel Fuse L829-1J1T-43 RJ-45 connector (P12) with built-in magnetics and LED indicators. The connections from XCZU7EV MPSoC U1 to the DP83867IRPAP PHY device U98 (bottom of the board) are listed in Table 3-14.

Table 3-14: **DP83867 PHY Connections to XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	DP83867 PHY U98	
		Pin #	Pin Name
J31	MIO64_ENET_TX_CLK	40	GTX_CLK
J32	MIO65_ENET_TX_D0	38	TX_DO
J34	MIO66_ENET_TX_D1	37	TX_D1
K28	MIO67_ENET_TX_D2	36	TX_D2
K29	MIO68_ENET_TX_D3	35	TX_D3
K30	MIO69_ENET_TX_CTRL	52	TX_EN_TX_CTRL

Table 3-14: **DP83867 PHY Connections to XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DP83867 PHY U98	
		Pin #	Pin Name
K31	MIO70_ENET_RX_CLK	43	RX_CLK
K32	MIO71_ENET_RX_D0	44	RX_DO
K33	MIO72_ENET_RX_D1	45	RX_D1
K34	MIO73_ENET_RX_D2	46	RX_D2
L29	MIO74_ENET_RX_D3	47	RX_D3
L30	MIO75_ENET_RX_CTRL	53	RX_DV_RX_CTRL
L33	MIO76_ENET_MDC	20	MDC
L34	MIO77_ENET_MDIO	21	MDIO

Ethernet PHY Reset

The DP83867IRPAP PHY reset gate U169 is shown in Figure 3-10. The DP83867IRPAP can be reset by the MAX16025 U22 MPSoC PS-side POR reset device (PS_POR_B) or the I2C0 connected U97 TCA6416A I/O expander pin 10 port P06 (GEM3_EXP_RESET_B).

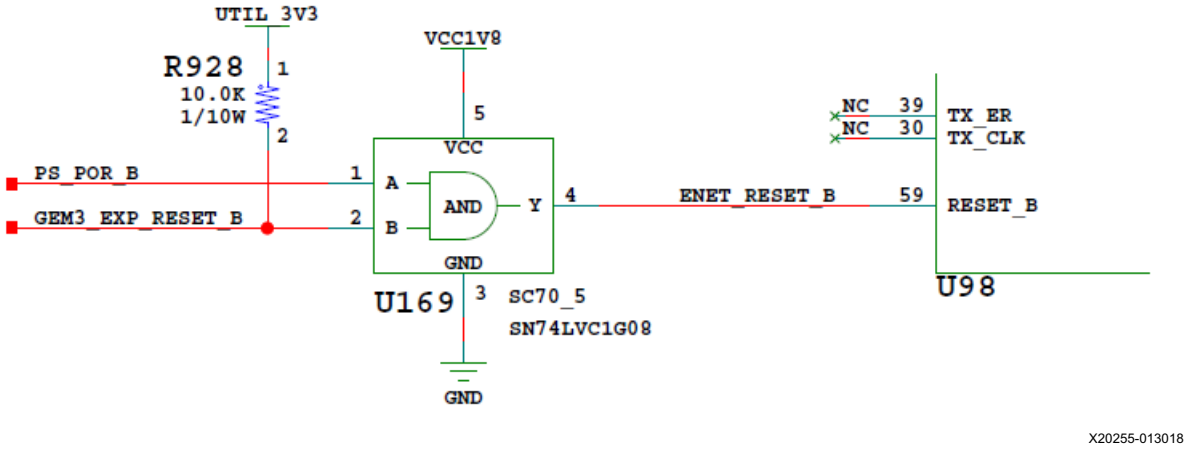


Figure 3-10: **Ethernet PHY Reset Circuit**

Ethernet PHY LED Interface

[Figure 2-1, callout 9]

The DP83867IRPAP PHY U98 LED interface (LED_0, LED_2) uses the two LEDs embedded in the P12 RJ45 connector bezel. The LED functional description is listed in Table 3-15.

Table 3-15: **Ethernet PHY LED Functional Description**

Pin		Type	Description
Name	Number		
LED_2	61	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits. ***Note:*** This pin is a strap configuration pin for RGZ devices only.
LED_1	62	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	63	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. LED_2 is assigned to the activity indicator (ACT) and LED_0 indicates link established. For more Ethernet PHY details, see the TI DS83867 data sheet [Ref 15].

The DP83867IRPAP PHY LED indicators are shown in Figure 3-11.

- LED_0 is the RJ-45 P12 bezel right-side yellow LED, link established indicator.
- LED_2 is the RJ-45 P12 bezel left-side green LED, TX/RX activity indicator.
- LED_1 is the green DS27 LED, mounted on the ZCU104 board top between the display port connector P11 and the Ethernet RJ-45 connector P12, indicates the 1000BASE-T link is established.

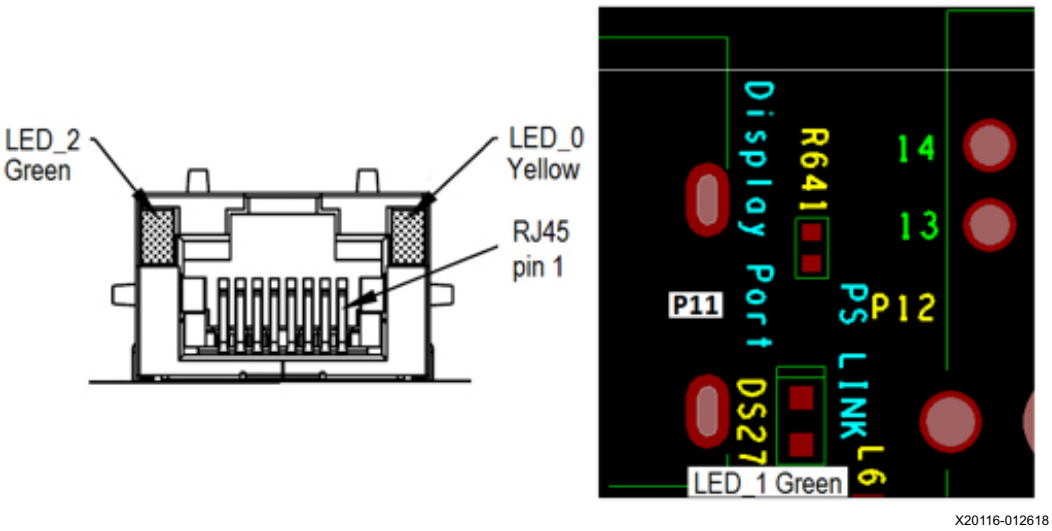


Figure 3-11: **Ethernet PHY Status LEDs**

I2C1 (MIO 16-17)

[Figure 2-1, callouts 12 and 13]

The I2C1 interface provides access to I2C peripherals through I2C switch TCA9548A U34. A TCA6416A port expander U97 is also attached to the I2C1 bus. The I2C1 PS-side bank 500 connection is shared with PL-side bank 87. Figure 3-12 shows a high-level view of the I2C1 bus connectivity represented in Table 3-16 and Table 3-17. TCA9548A U34 is set to `0x74` and the TCA6416A is set to `0x20`.

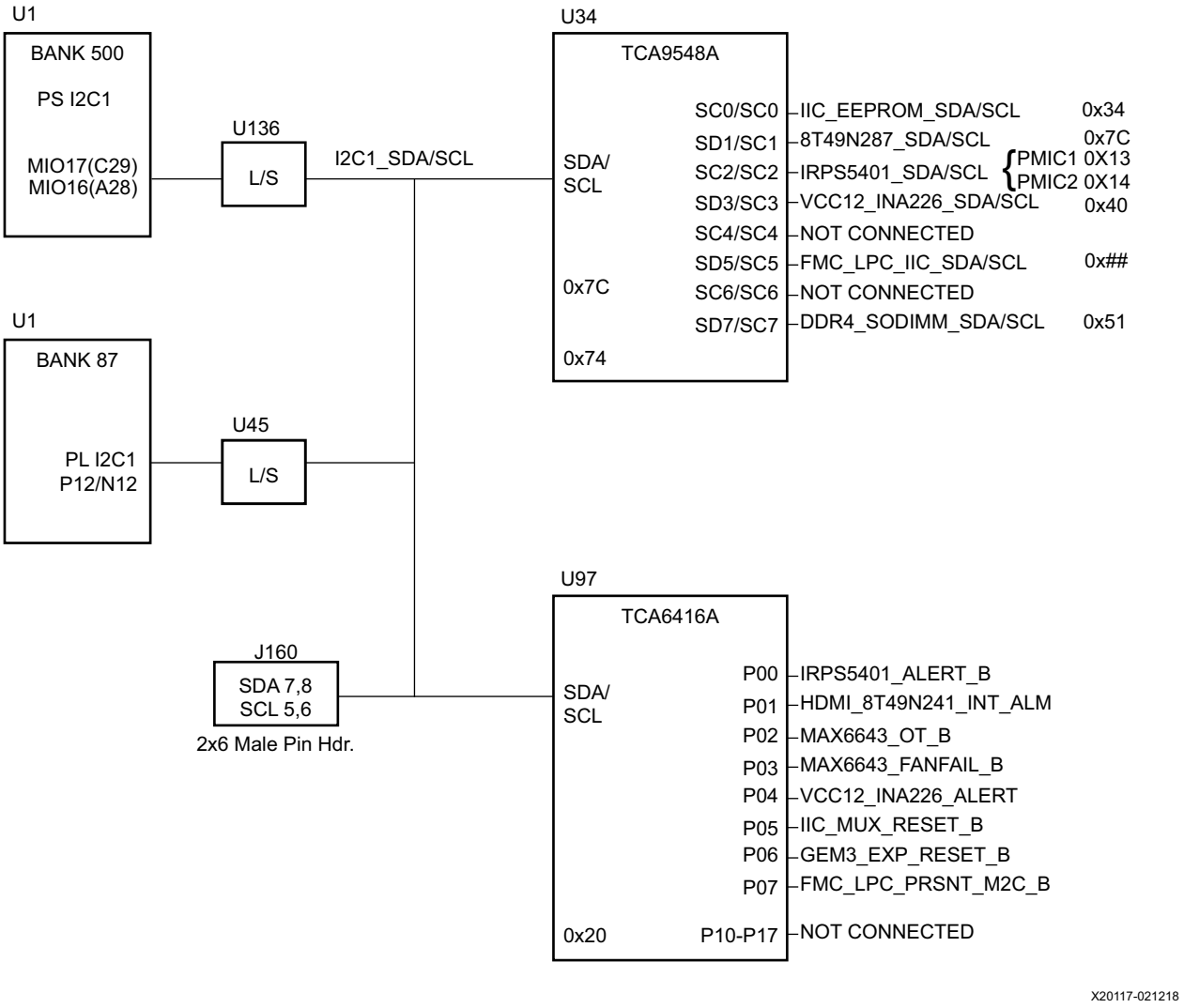


Figure 3-12: **I2C1 Bus Topology**

Table 3-16 and Table 3-17 show U34 and U97 (located on the bottom of the board) connections, respectively.

Table 3-16: **I2C1 TCA9548A U34 Multiplexer Connections**

U34 I2C1 Mux (Addr 0x74) Port	I2C1 Bus Device	Target Device Address
0	EEPROM U23	0X34
1	IDT8T49N287 Clock U182	0X7C
2	IRP5401 PMICs	PMIC1 0x13; PMIC2 0x14
3	VCC12 INA226 U183	0X40
4	No connection	NA
5	FMC LPC J5	0x##
6	No connection	NA
7	DDR4 SODIMM J1	0x51

Table 3-17: **TCA6416A U97 I2C Expander**

U97 I2C1 Expander (Addr 0x20) Port	Schematic Net Name	Target Device Pin
P00	IRP5401_ALERT_B	U179.17
P01	HDMI_8T49N241_INT_ALM	U181.29
P02	MAX6643_OT_B	U128.9
P03	MAX6643_FANFAIL_B	U128.4
P04	VCC12_INA226_ALERT	U183.3
P05	IIC_MUX_RESET_B	U34.3
P06	GEM3_EXP_RESET_B	U169.2
P07	FMC_LPC_PRSNT_M2C_B	J5.H2

FT4232HL USB UART Interface (MIO 18-21)

[Figure 2-1, callout 7]

The FT4232HL U151 quad USB-UART on the ZCU104 board provides three level-shifted UART connections through the single micro-AB USB connector J164.

- Channel A is configured to support the JTAG chain.
- Channel B implements UART0 MIO18/19 connections.
- Channel C implements UART1 MIO20/21 connections.
- Channel D implements UART2 PL-side bank 28 4-wire interface.

The USB UART interface circuit is shown in Figure 3-13. The FTDI FT4232HL data sheet is available on the Silicon Labs website [Ref 14].

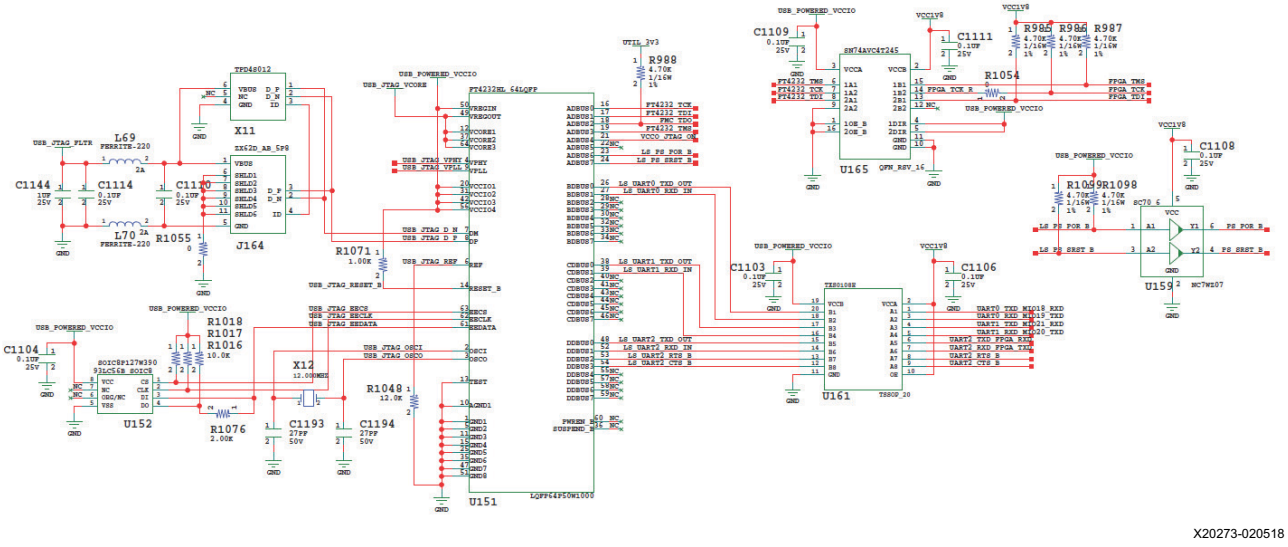


Figure 3-13: **Quad USB UART Interface**

The nets of the three UART channel are level-shifted by U161. The UART connections from XCZU7EV MPSoC U1 PL-side bank 28 to the FT4232HL device through U161 are listed in Table 3-18.

Table 3-18: **XCZU7EV U1 PL-side to FT4232HL U151 Connections via L/S U161**

XCZU7EV (U1) Pin	Net Name	FT4232HL U151	
		Pin Name	Pin #
A20	UART2_TXD_FPGA_RXD	DDBUS1	52
C19	UART2_RXD_FPGA_TXD	DDBUS0	48
C18	UART2_RTS_B	DDBUS2	53
A19	UART2_CTS_B	DDBUS3	54

UART0 (MIO 18-19)

This is the primary Zynq UltraScale+ MPSoC PS-side UART interface and is connected to the U151 FT4232HL USB-to-Quad-UART with port assignments as listed in Table 3-19. PS-side UART0 is accessed through the U151 FT4232HL USB-to-Quad-UART bridge BDBUS port. The UART connections from XCZU7EV MPSoC U1 PS-side MIO 18 and 19 to the FT4232HL device through level-shifter U161 are listed in Table 3-19.

Table 3-19: **XCZU7EV U1 PS-side MIO 18, 19 to FT4232HL U151 Connections via L/S U161**

XCZU7EG U1		Schematic Net Name	FT4232HL U151	
Pin Name	Pin#		Pin Name	Pin #
PS_MIO18	F27	UART0_TXD_MIO18_RXD	BDBUS1	27
PS_MIO19	B28	UART0_RXD_MIO19_TXD	BDBUS0	26

UART1 (MIO 20-21)

PS-side UART1 is accessed through the U151 FT4232HL USB-to-Quad-UART bridge CDBUS port. The UART connections from XCZU7EV MPSoC U1 PS-side MIO 20 and 21 to the FT4232HL device through level-shifter U161 are listed in Table 3-20.

Table 3-20: **XCZU7EV U1 PS-side MIO 20, 21 to FT4232HL U151 Connections via L/S U161**

XCZU7EG U1		Schematic Net Name	FT4232HL U151	
Pin Name	Pin#		Pin Name	Pin #
PS_MIO21	C28	UART1_TXD_MIO21_RXD	CDBUS1	39
PS_MIO20	E29	UART1_RXD_MIO20_TXD	CDBUS0	38

CAN1 (MIO 24-25)

The PS-side CAN bus TX (MIO24, U1 pin E28) and RX (MIO25, U1 pin D29) signals are routed through TXS0104E level-translator U33 and TI SN65HVD232 CAN-bus transceiver U122 to the 0.1 inch centered 8-pin male header J98 as shown in Figure 3-14.

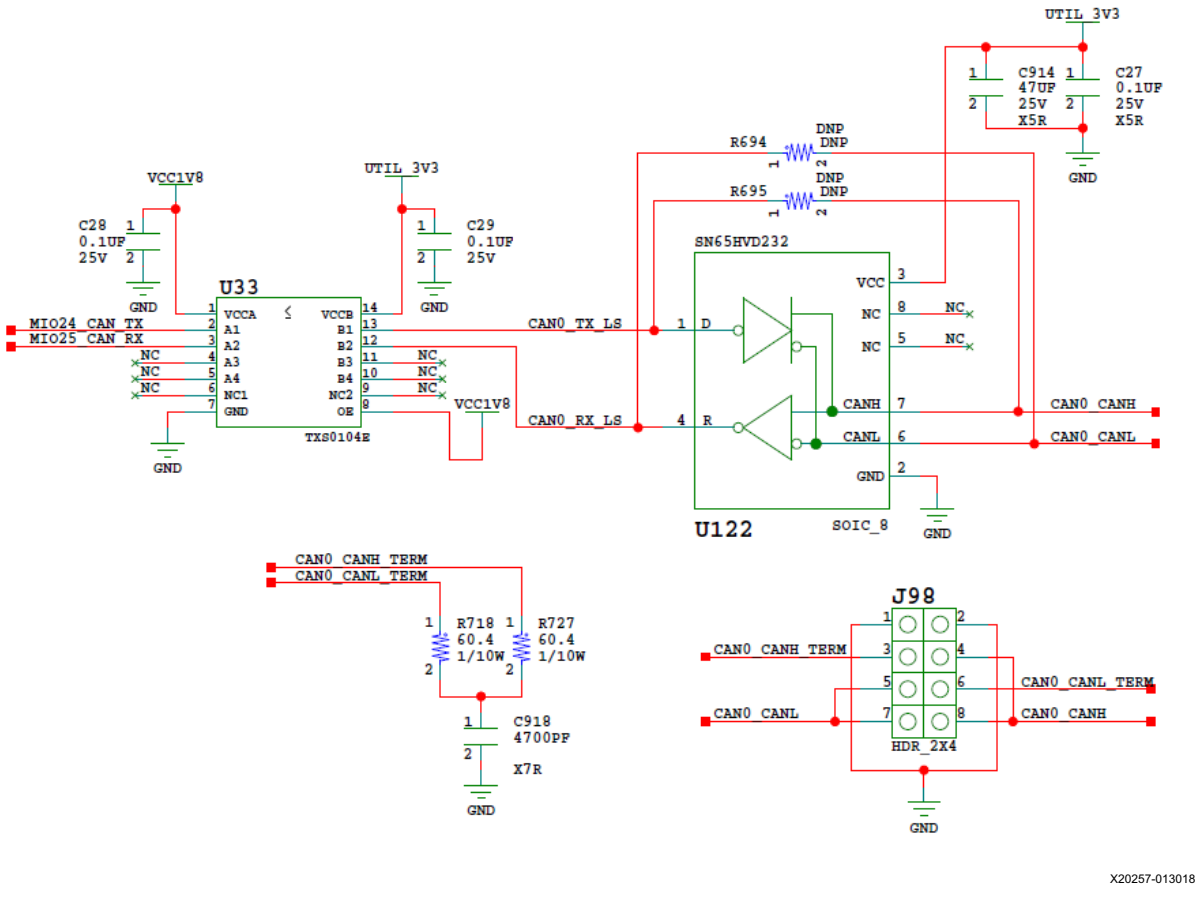


Figure 3-14: **PS-Side CAN Bus Circuit**

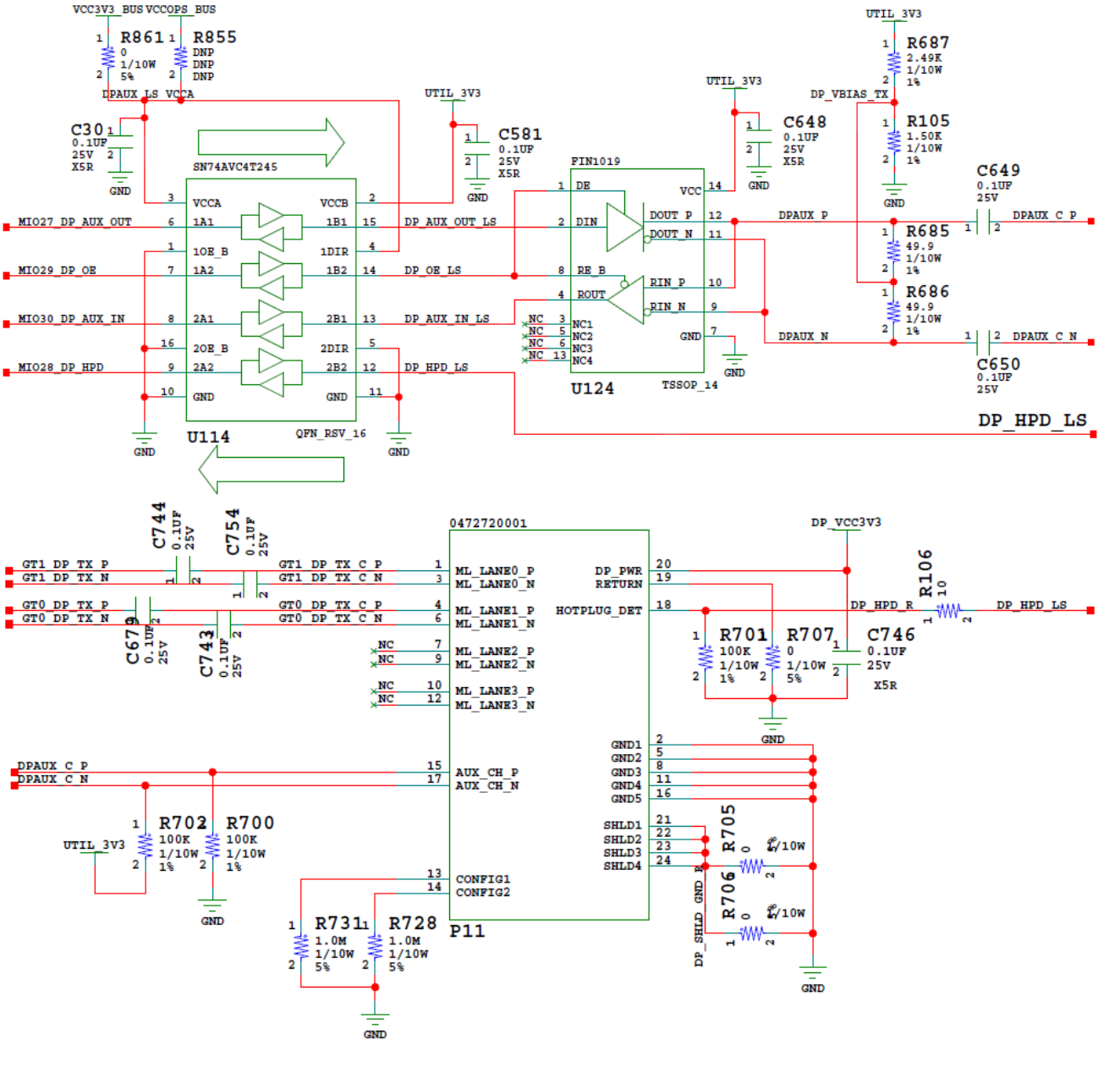
DPAUX (MIO 27-30)

[Figure 2-1, callout 27]

The Zynq UltraScale+ MPSoC provides a VESA DisplayPort 1.2 source-only controller that supports up to two lanes of main link data at rates of 1.62 Gb/s, 2.70 Gb/s, or 5.40 Gb/s. The DisplayPort standard defines an auxiliary channel that uses LVDS signaling at a 1 Mb/s data rate, which is translated from single-ended MIO signals to the differential DisplayPort AUX channel, DPAUX (see Table 3-21). The DisplayPort circuit is shown in Figure 3-15.

Table 3-21: **DPAUX/MIO Connections**

XCZU7EV (U1) Pin	Net Name	Level Shifter U114	
		Pin Name	Pin #
A33	MIO30_DP_AUX_IN	2A1	8
A32	MIO29_DP_OE	1A2	7
A31	MIO28_DP_HPD	2A2	9
A30	MIO27_DP_AUX_OUT	1A1	6



X16547-013018

Figure 3-15: **DisplayPort Circuit**

HDMI Video Output

[Figure 2-1, callouts 10 and 11]

The ZCU104 board provides an HDMI® video output using a TI SN65DP159RGZ re-timer at U94. The output is provided on a TE Connectivity 1888811-1 right-angle dual-stacked HDMI type-A receptacle at P7. The SN65DP159RGZ device is a dual mode DisplayPort to transition-minimized differential signal (TMDS) re-timer supporting digital video interface (DVI) 1.0, HDMI 1.4b, and 2.0 output signals.

The SN65DP159RGZ device supports the dual mode standard version 1.1 type 1 and type 2 through the digital down converter (DDC) link or AUX channel. The SN65DP159RGZ device supports data rates up to 6 Gb/s per data lane to support Ultra HD (4K x 2K/60 Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 x 1080/60 Hz). The SN65DP159RGZ device can automatically configure itself as a re-driver at data rates <1 Gb/s, or as a re-timer at more than this data rate. This feature can be turned off with I2C programming.

The HDMI block diagram, TX interface circuit, and RX interface circuit are shown in Figure 3-16, Figure 3-17, and Figure 3-18, respectively. The XCZU7EV MPSoC U1 to HDMI circuit connections are listed in Table 3-22.

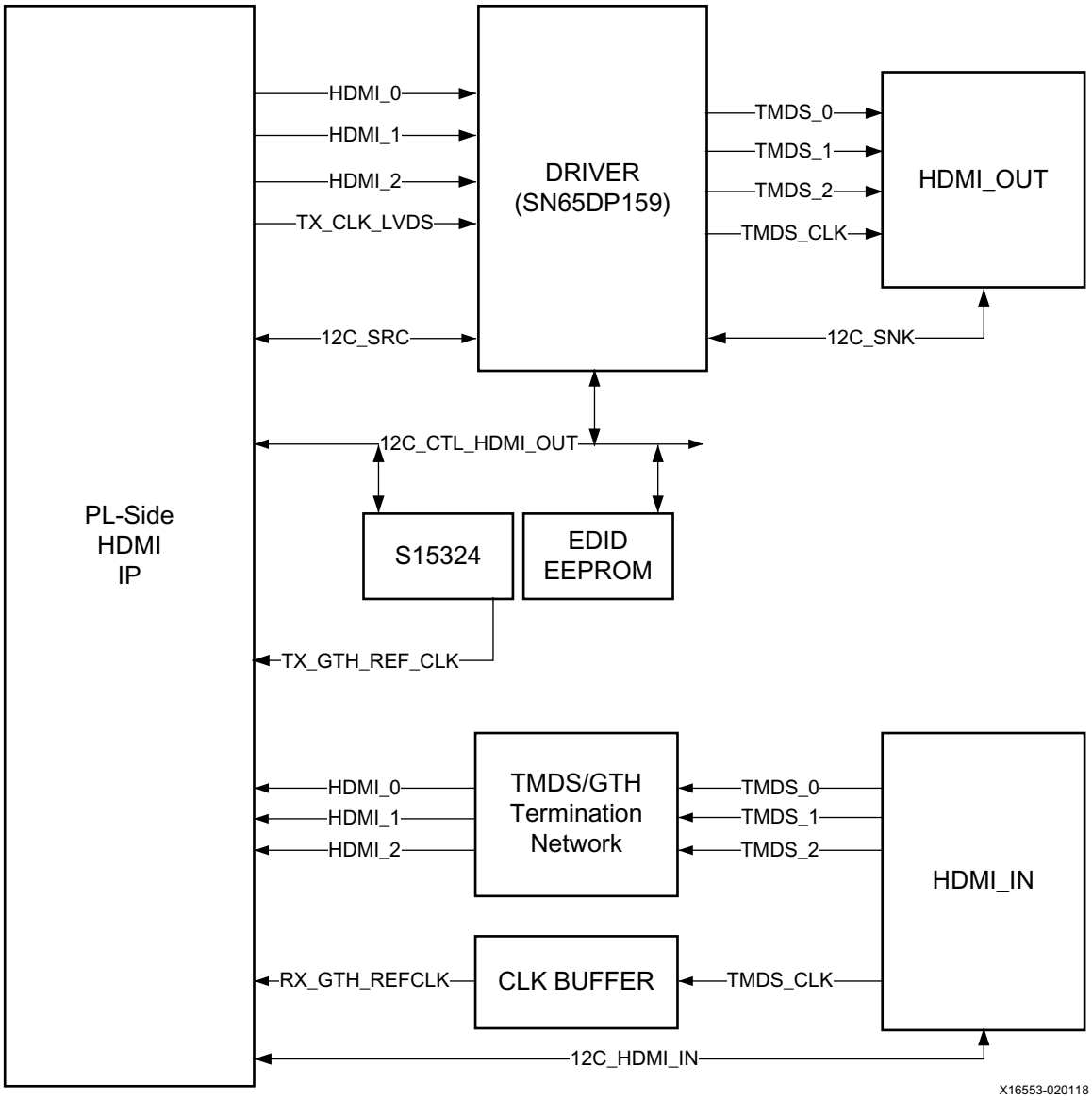


Figure 3-16: **HDMI Interface Block Diagram**

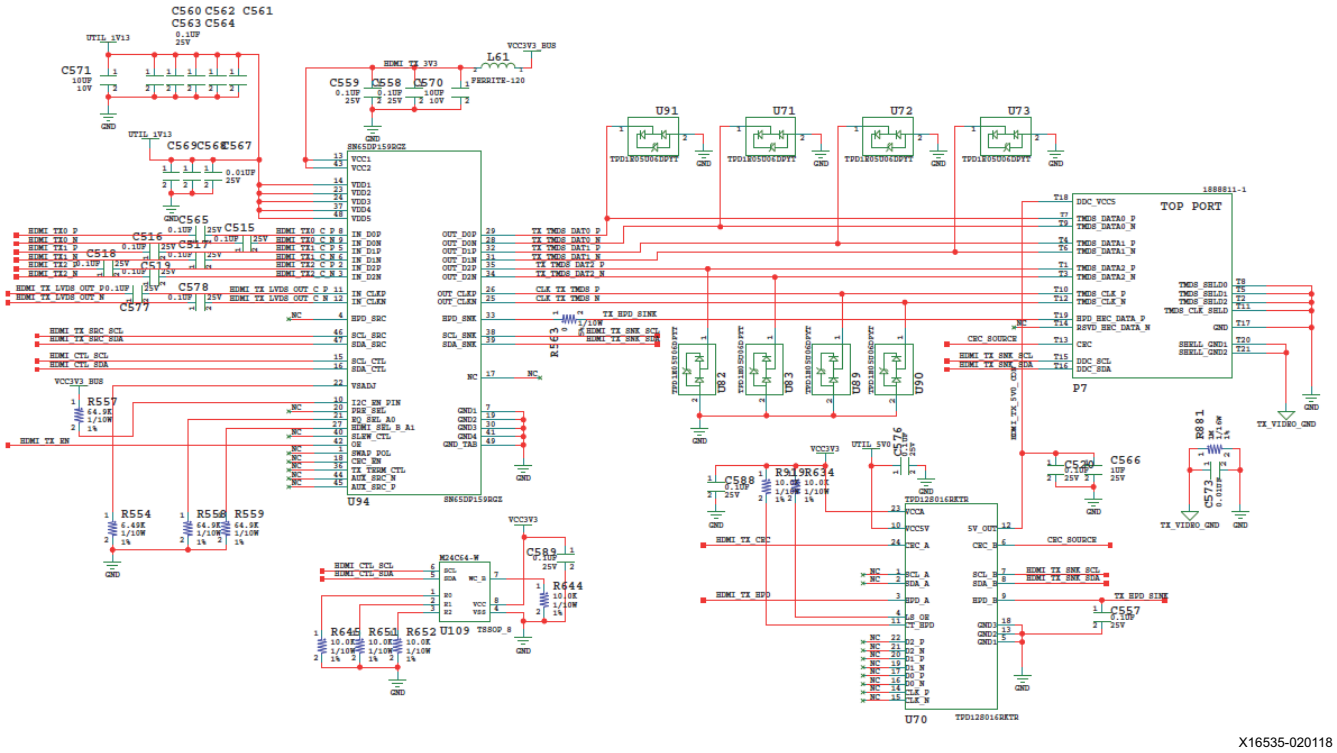


Figure 3-17: **HDMI TX Interface Circuit**

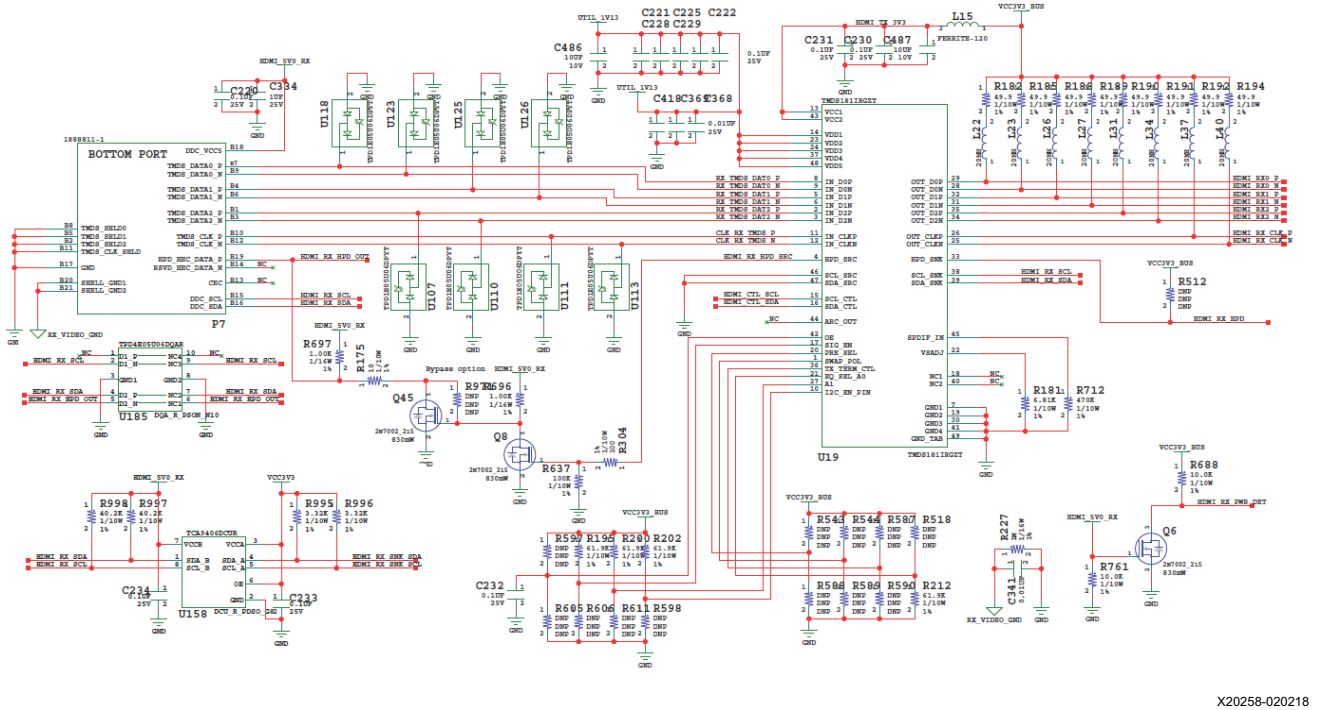


Figure 3-18: **HDMI RX Interface Circuit**

Table 3-22: **HDMI Connections to MPSoC U1**

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
M4	HDMI_TX0_P	(1)	8	IN_D0P	SN65DP159 (U94) Wired to top port (P7)
M3	HDMI_TX0_N	(1)	9	IN_D0N	
L6	HDMI_TX1_P	(1)	5	IN_D1P	
L5	HDMI_TX1_N	(1)	6	IN_D1N	
K4	HDMI_TX2_P	(1)	2	IN_D2P	
K3	HDMI_TX2_N	(1)	3	IN_D2N	
H9	HDMI_TX_LVDS_OUT_P	LVDS	11	IN_CLKP	
G9	HDMI_TX_LVDS_OUT_N	LVDS	12	IN_CLKN	
B1	HDMI_TX_SRC_SCL	LVCMOS33	46	SCL_SRC	
C1	HDMI_TX_SRC_SDA	LVCMOS33	47	SDA_SRC	
A2	HDMI_TX_EN	LVCMOS33	42	OE	
A3	HDMI_TX_CEC	LVCMOS33	24	CEC_A	TPD12S016RK (U70)
E3	HDMI_TX_HPD	LVCMOS33	3	HPD_A	
N11	HDMI_SI5324_LOL	LVCMOS33	18	LOL	SI5319C (U108)
M12	HDMI_SI5324_RST	LVCMOS33	1	RST_B	
G14	HDMI_REC_CLOCK_C_P	LVDS	16	CKIN1_P	
F13	HDMI_REC_CLOCK_C_N	LVDS	17	CKIN1_N	
T8	HDMI_SI5324_OUT_C_P	(1)	28	CKOUT1_P	
T7	HDMI_SI5324_OUT_C_N	(1)	29	CKOUT1_N	
N2	HDMI_RX0_C_P	(1)	29	OUT_D0P	TMDS181IRGZT (U19) Wired to HDMI bottom port(P7)
M3	HDMI_RX0_C_N	(1)	28	OUT_D0N	
L2	HDMI_RX1_C_P	(1)	32	OUT_D1P	
L1	HDMI_RX1_C_N	(1)	31	OUT_D1N	
J2	HDMI_RX2_C_P	(1)	35	OUT_D2P	
J1	HDMI_RX2_C_N	(1)	34	OUT_D2N	
R10	HDMI_RX_CLK_C_P	(1)	26	OUT_CLKP	
R9	HDMI_RX_CLK_C_N	(1)	25	OUT_CLKN	
F6	HDMI_RX_HPD	LVCMOS33	33	HPD_SNK	
E5	HDMI_RX_PWR_DET	LVCMOS33	3	D	Q6
D1	HDMI_CTL_SCL	LVCMOS33	15	SCL_CTL	(2)
E1	HDMI_CTL_SDA	LVCMOS33	16	SDA_CTL	

Table 3-22: **HDMI Connections to MPSoC U1 *(Cont'd)***

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
D2	HDMI_RX_SNK_SCL	LVCMOS33	1	SCL_A	TPD12S016RK (U102)
E2	HDMI_RX_SNK_SDA	LVCMOS33	1	SDA_A	

Notes:
1. U1 MGT (I/O standards do not apply).
2. TMDS181IRG (U19), SN65DP159 (U94), M24C64-W (U109), and SI5324C (U108).

HDMI Clock Recovery

[Figure 2-1, callout 29]

The ZCU104 board includes an IDT 8T49N241 jitter attenuator U181. The 8T49N241 has one fractional feedback phase-locked loop (PLL) that can be used as a jitter attenuator and frequency translator.

The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 67 (HDMI_REC_CLOCK_P, pin G14 and HDMI_REC_CLOCK_N, pin F13) for jitter attenuation. The jitter attenuated clock (HDMI_SI5324_OUT_C_P (U181 pin 22), HDMI_SI5324_OUT_C_N (U081 pin 39) is then routed as a series capacitor coupled reference clock to GTH Quad 227 inputs MGTREFCLK0P (U1 pin T8) and MGTREFCLK0N (U1 pin T7).

The 8T49N241 is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used in standalone mode, the 8T49N241 operates in free-running mode and uses an external oscillator as the reference. When the HDMI transmitter is used in pass-through mode, the 8T49N241 generates a jitter attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI Rx subsystem HMDI Rx TMDS clock, so that they are phase aligned. The 8T49N241 is controlled by an I2C interface connected to the FPGA. Enabling the jitter attenuation feature requires additional user programming through the FPGA connected HDMI_CTL I2C bus. The jitter attenuated clock circuit is shown in Figure 3-19.

IMPORTANT: *The IDT 8T49N241 pin 31 reset net HDMI_8T49N241_RST must be driven High to enable the device. U181 pin 31 net HDMI_8T49N241_RST is connected to FPGA U1 bank 87 pin M12.*

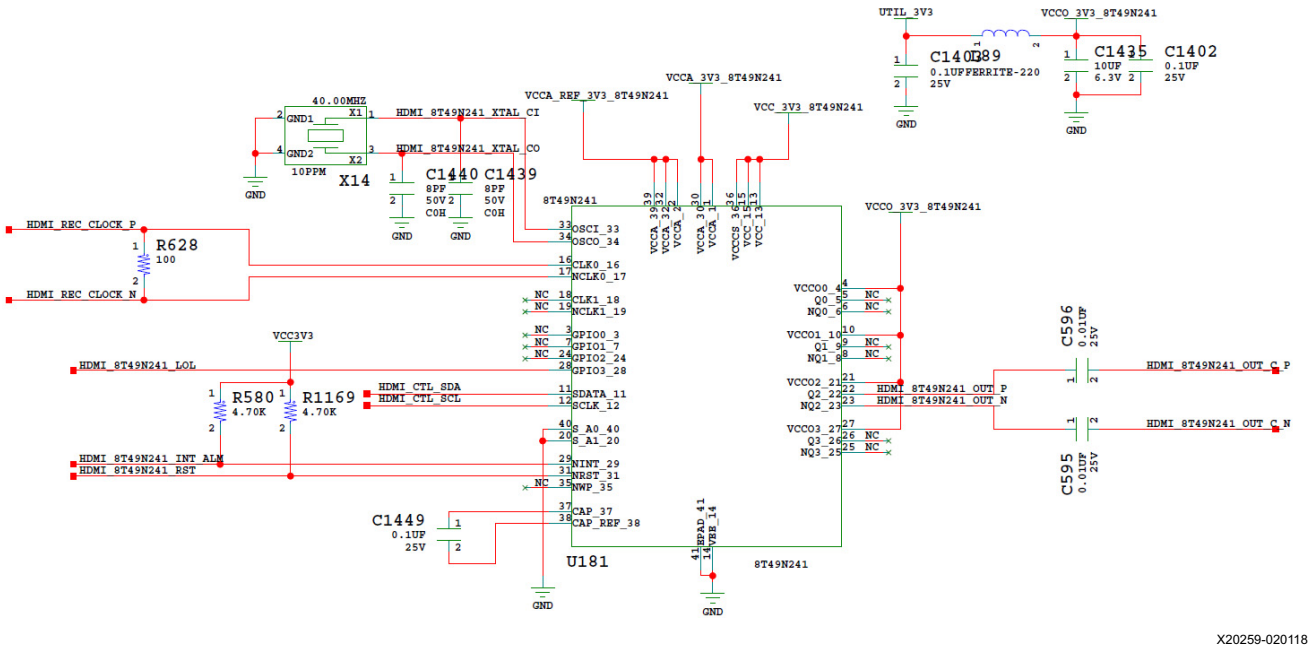


Figure 3-19: **HDMI Interface Clock Recovery**

User PMOD GPIO Connectors

[Figure 2-1, callout 14]

The ZCU104 evaluation board supports two PMOD GPIO headers J55 (right-angle female) and J87 (vertical male). The 3.3V PMOD nets are wired to the XCZU7EV device U1 bank 87. Figure 3-20 shows the GPIO PMOD headers J55 and J87. Table 3-23 lists the connections between the XCZU7EV MPSoC and the PMOD connectors.

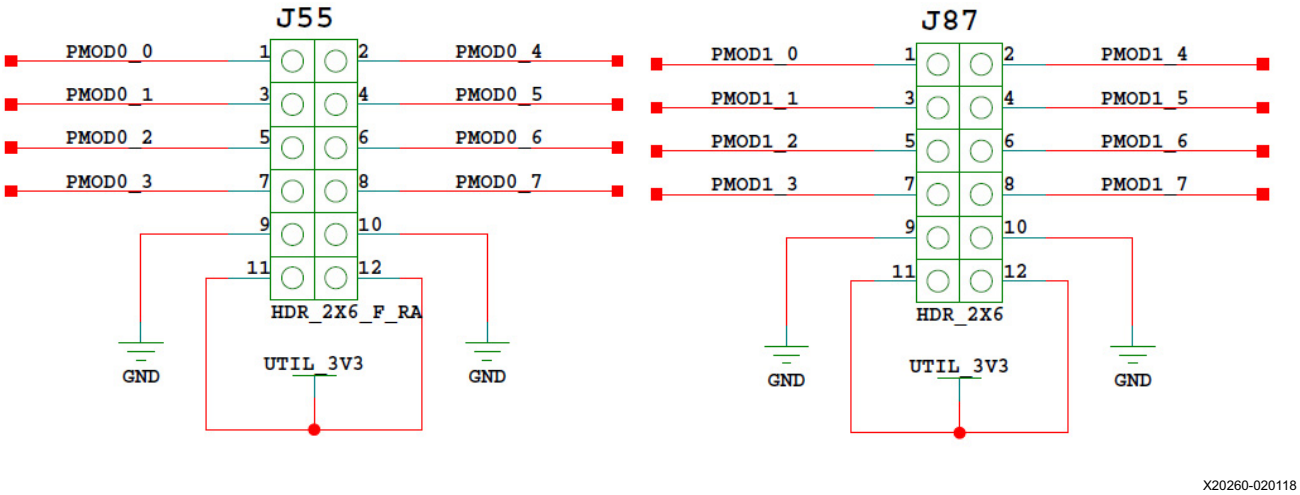


Figure 3-20: **PMOD Connectors**

Table 3-23: **XCZU7EV U1 to PMOD Connections**

XCZU7EV (U1) Pin	Net Name	I/O Standard	PMOD Pin
G8	PMOD0_0	LVCMOS33	J55.1
H8	PMOD0_1	LVCMOS33	J55.3
G7	PMOD0_2	LVCMOS33	J55.5
H7	PMOD0_3	LVCMOS33	J55.7
G6	PMOD0_4	LVCMOS33	J55.2
H6	PMOD0_5	LVCMOS33	J55.4
J6	PMOD0_6	LVCMOS33	J55.6
J7	PMOD0_7	LVCMOS33	J55.8
J9	PMOD1_0	LVCMOS33	J87.1
K9	PMOD1_1	LVCMOS33	J87.3
K8	PMOD1_2	LVCMOS33	J87.5
L8	PMOD1_3	LVCMOS33	J87.7
L10	PMOD1_4	LVCMOS33	J87.2
M10	PMOD1_5	LVCMOS33	J87.4
M8	PMOD1_6	LVCMOS33	J87.6
M9	PMOD1_7	LVCMOS33	J77.8

User I2C1 Receptacle

[Figure 2-1, callout 21]

The ZCU104 evaluation board supports a PMOD 2X6 receptacle (right-angle female) J160. Figure 3-21 shows the I2C1 PMOD receptacle J160. The I2C1 nets are a branch of the I2C1 main bus (see Figure 3-11, page 48). See the Digilent website [Ref 19] for more information about the PMOD.

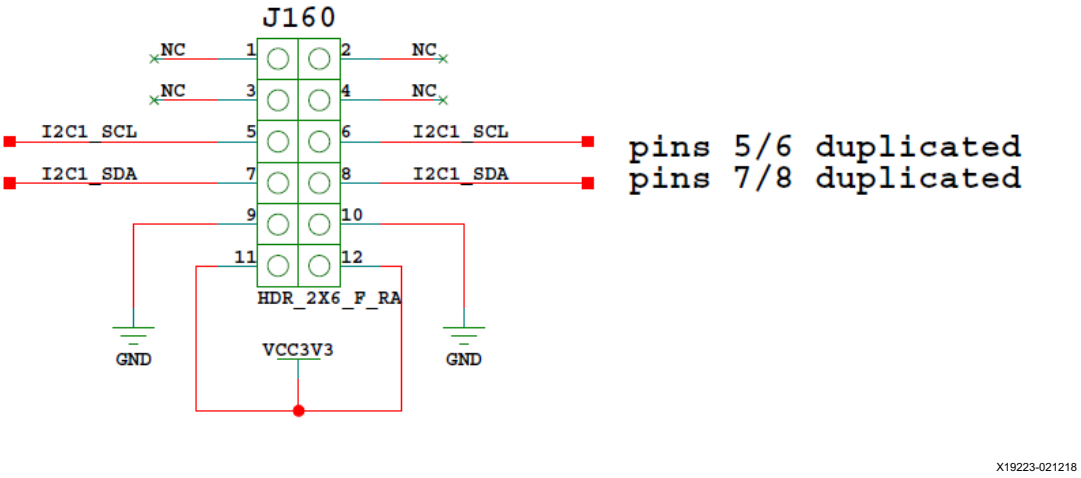


Figure 3-21: **J160 PMOD I2C1 Right-Angle Receptacle**

User I/O

[Figure 2-1, callouts 16-19]

The ZCU104 board provides these user and general purpose I/O capabilities:

- Four user LEDs (callout 16)
  - GPIO_LED[7-0]: DS38, DS37, DS39, DS40
- Four user pushbuttons and CPU reset switch (callouts 18 and 19)
  - GPIO_PB_SW[0:3]: SW18, SW17, SW16, SW14, SW15
  - CPU_RESET: SW20
- 4-position user DIP switch (callout 17)
  - GPIO_DIP_SW[7:0]: SW13

Figure 3-22 through Figure 3-24 show the GPIO circuits. Table 3-24 lists the GPIO connections to XCZU7EV U1 3.3V bank 88.

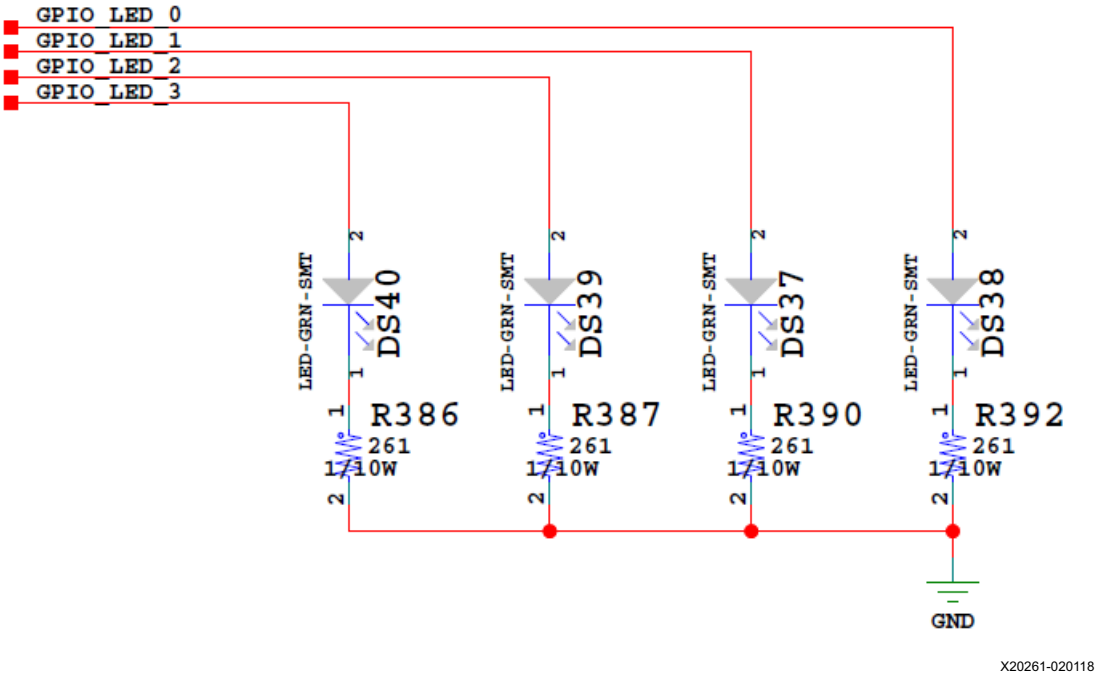


Figure 3-22: **GPIO LEDs**

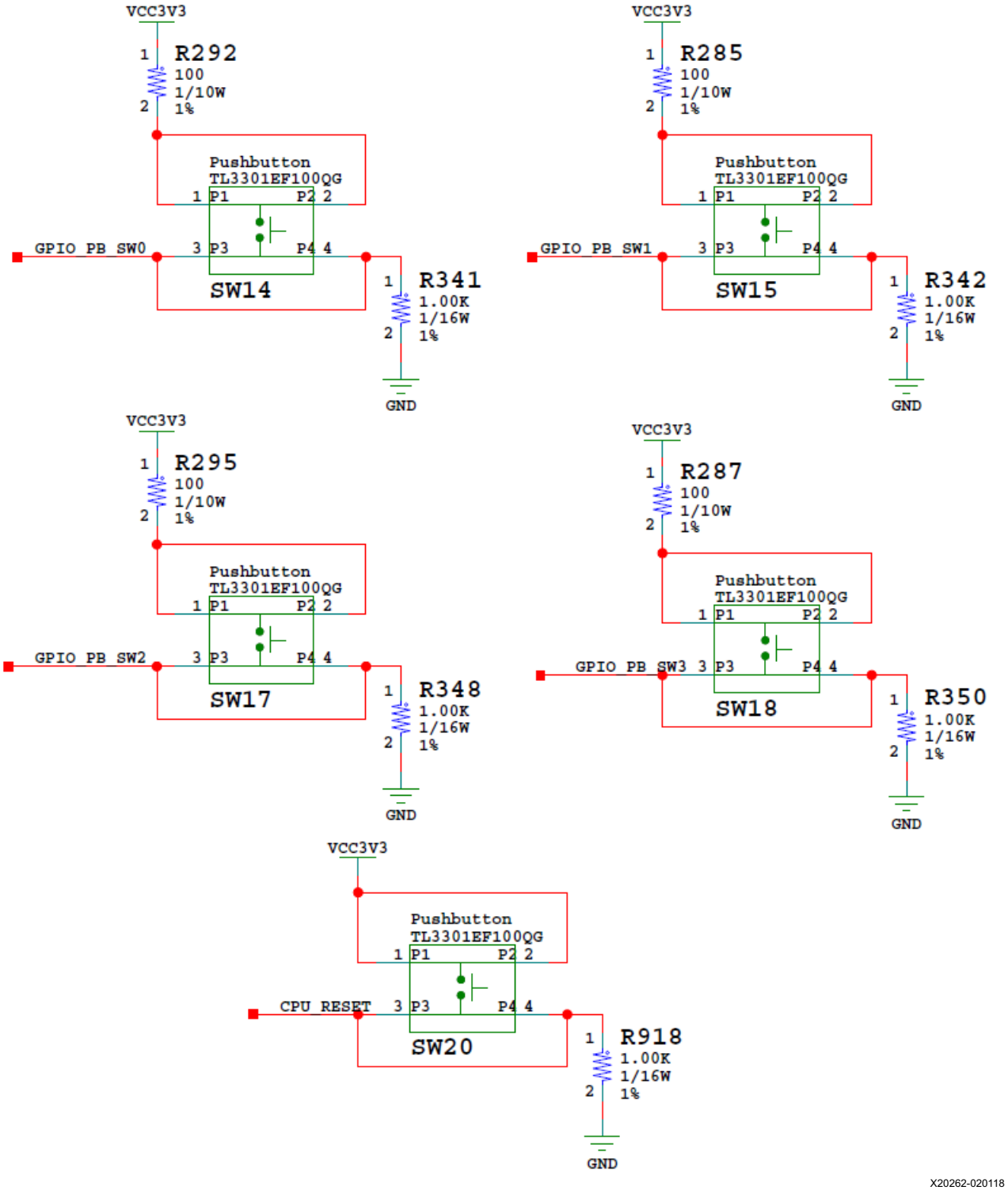


Figure 3-23: **GPIO Pushbutton Switches**

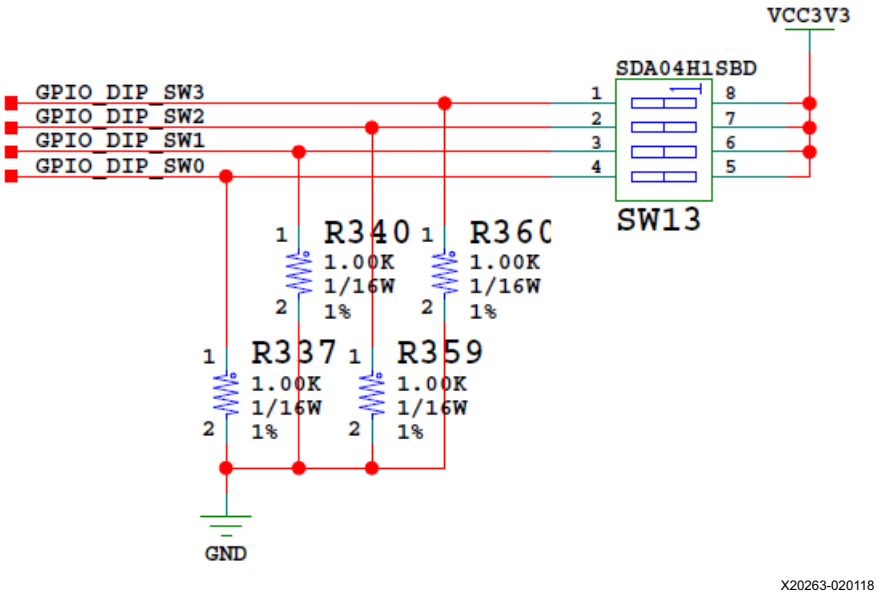


Figure 3-24: **GPIO 8-Pole DIP Switch**

Table 3-24: **XCZU7EV U1 to GPIO Connections**

XCZU7EV (U1) Pin	Net Name	I/O Standard	Device
GPIO LEDs (Active High)[1]			
D5	GPIO_LED_0	LVCMOS12	DS38.2
D6	GPIO_LED_1	LVCMOS12	DS37.2
A5	GPIO_LED_2	LVCMOS12	DS39.2
B5	GPIO_LED_3	LVCMOS12	DS40.2
Directional Pushbuttons (Active High)			
B4	GPIO_PB_SW0	LVCMOS12	SW14.3
C4	GPIO_PB_SW1	LVCMOS12	SW15.3
B3	GPIO_PB_SW2	LVCMOS12	SW17.3
C3	GPIO_PB_SW3	LVCMOS12	SW18.3
CPU Reset Pushbutton (Active High)			
M11	CPU_RESET	LVCMOS18	SW20.3
GPIO DIP SW (Active High)			
E4	GPIO_DIP_SW0	LVCMOS18	SW13.8
D4	GPIO_DIP_SW1	LVCMOS18	SW13.7
F5	GPIO_DIP_SW2	LVCMOS18	SW13.6
F4	GPIO_DIP_SW3	LVCMOS18	SW13.5

Notes:

1. LEDs are driven through the U163 SN74AVC4T245 buffer.

Power and Status LEDs

[Figure 2-1, area of callout 34]

Table 3-25 defines the power and status LEDs. For user controlled LEDs, see User I/O, page 63.

Table 3-25: **Power and Status LEDs**

Ref. Des.	Net Name	LED Color	Description
DS1	PS_INIT_B	Green/Red	Green: FPGA initialization was successful Red: FPGA initialization is in progress
DS2	VCC12_SW	Green	12 VDC power on
DS3	VCC1V8_PGOOD	Green	VCC1V8 1.8 VDC power on
DS4	MGTAVCC_PGOOD	Green	MGTAVCC 0.9 VDC power on
DS5	VCCINT_PGOOD	Green	VCCINT 0.85 VDC power on
DS6	VCC1V2_PGOOD	Green	VCC1V2 1.2 VDC power on
DS7	VCC3V3_PGOOD	Green	VCC3V3 3.3 VDC power on
DS8	VADJ_FMC_PGOOD	Green	VADJ_FMC 1.8 VDC (nominal) power on
DS9	MGT1V8_PGOOD	Green	MGTVCCAUX, PS_MGTRAVCC 1.81 VDC power on
DS10	MGT1V2_PGOOD	Green	MGTAVTT. VCC_PSPLL 1.2 VDC power on
DS21	PL_DDR4_VTERM_0V60_PGOOD	Green	PL_DDR4_VTERM 0.6 VDC power on
DS24	UTIL_2V5	Green	UTIL_2V5 2.5 VDC power on
DS25	UTIL_3V3_PGOOD	Green	UTIL_3V3 3.3 VDC power on
DS26	MGTRAVCC_PGOOD	Green	MGTRAVCC 0.85 VDC power on
DS27	ENET_LED_1	Green	EHPY U98 1000BASE-T link speed
DS32	PS_DONE	Green	MPSoC U1 bit file download is complete
DS33	PS_ERR_STATUS(1)	Green	PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
DS35	PS_ERR_OUT(1)	Red	PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU.
DS36	POR_RST_B	Red	POR U22 asserts RST_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or MR is asserted.
DS49	UTIL_1V13_PG	Green	UTIL_1V13 1.13 VDC power on
DS51	USB3 MIC2544 U121 FLG	Green	PS USB 3.0 ULPI VBUS power error
DS53	UTIL_5V0_PGOOD	Green	UTIL_5V0 5 VDC power on

Table 3-25: **Power and Status LEDs *(Cont'd)***

Ref. Des.	Net Name	LED Color	Description
DS54	PS_DDR4_VTERM_0V60_PGOOD	Green	PS_DDR4_VTERM 0.6 VDC power on

Notes:

1. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration pins.

Figure 3-25 shows the power and status LEDs area of the board.

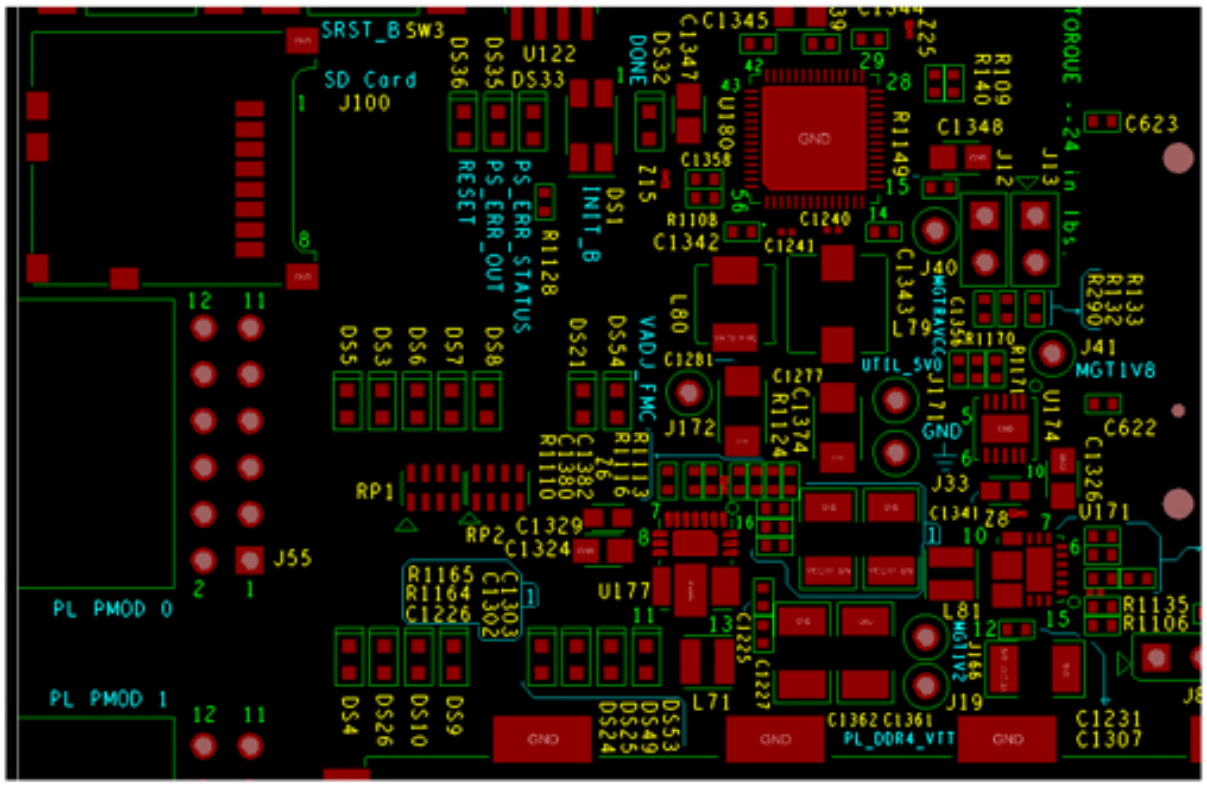


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Figure 3-25: **Power and Status LEDs**

GTH Transceivers

[Figure 2-1, callout 1]

The Zynq UltraScale+ XCZU7EV MPSoC has 20 GTH gigabit transceivers (16.3 Gb/s capable) on the PL-side. The GTH transceivers in the XCZU7EV device are grouped into four channels referred to as Quads. The reference clock for a Quad can be sourced from the Quad above or the Quad below the GTH Quad of interest. There are five GTH Quads on the ZCU104 board with connectivity as listed here:

Quad 223:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 224:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 225:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 226:

- MGTREFCLK0 - FMC_LPC_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - HDMI_DRU_CLOCK_C_P/N
- Contains one GTH transceiver allocated to FMC_LPC_DP0_C2M/M2C_P/N
- Four GTH transceivers not connected

Quad 227:

- MGTREFCLK0 - HDMI_8T49N241_OUT_C_P/N
- MGTREFCLK1 - HDMI_RX_CLK_C_P/N
- Contains three GTH transceivers allocated to HDMI_TX/RX[0:2]_P/N
- Contains one GTH transceiver allocated to FMC_LPC_DP0_C2M/M2C_P/N

GTH transceiver interface assignments on the ZCU104 are shown in Figure 3-26.

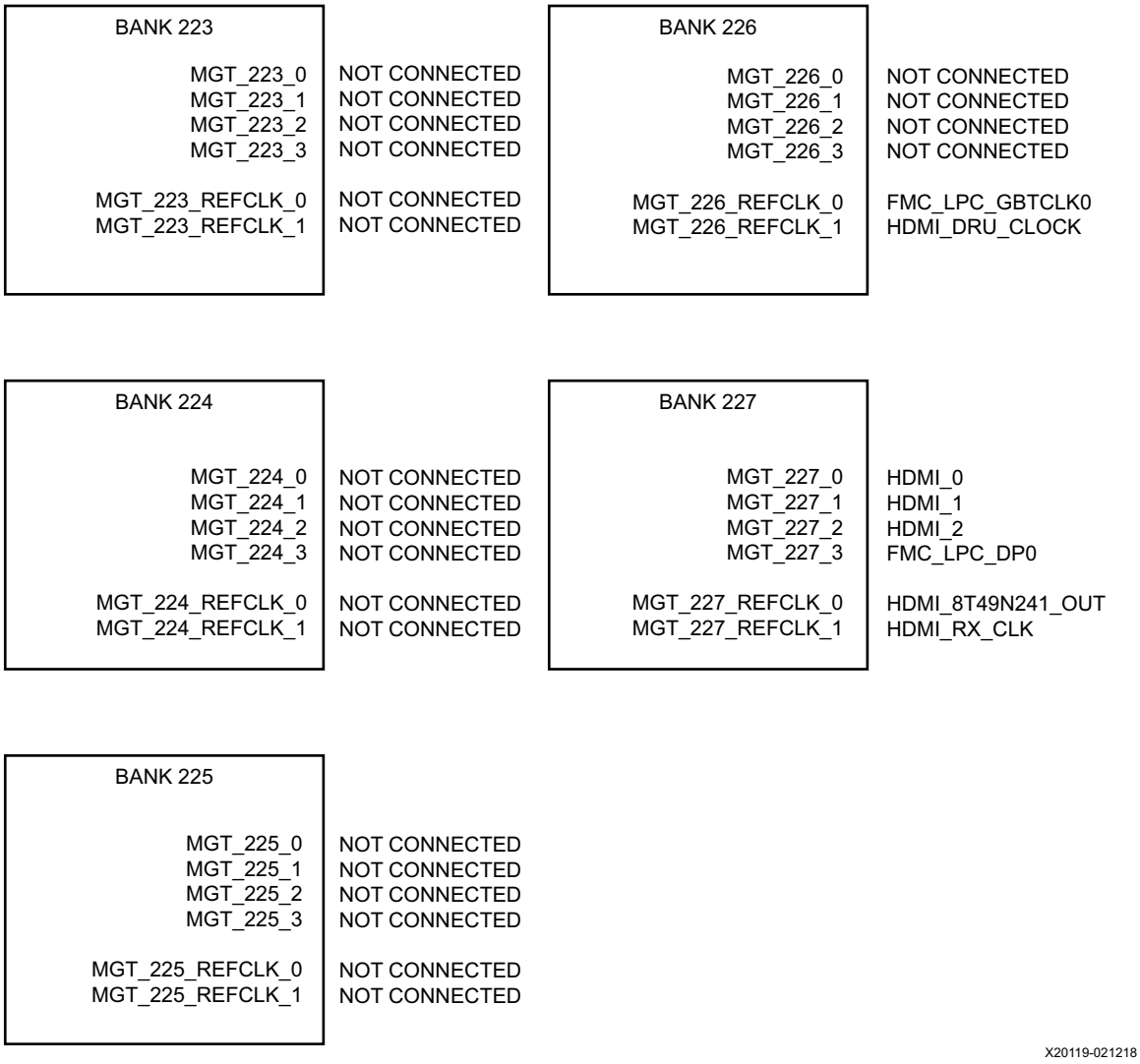

Figure 3-26: **GTH Transceiver Bank Assignments**

FMC LPC

The FMC low pin count (LPC) connector J5 has its full LA[00:33] bus connected across the XCZU7EV MPSoC PL banks 67 and 68.

The three FMC LPC clocks are connected as follows:

- FMC_LPC_GBTCLK0_M2C_C_P/N is connected to GTH bank 226 MGTREFCLK0
- FMC_LPC_CLK0_M2C_P/N is connected to PL bank 67 (LA[00:16]) GC pins E15/E14
- FMC_LPC_CLK1_M2C_P/N is connected to PL bank 68 (LA[17:33]) GC pins G10/F10

HDMI

Three PL-side GTH transceivers are dedicated for HDMI source and sink. Modes supported are 4K, 2K at 60 f/s, and 2160p60. External circuitry for interfacing TMDS signals with the GTH transceivers is required. Table 3-26 and Table 3-27 list MGTH banks 226 and 227 connections, respectively.

Table 3-26: **GTH Bank 226 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
U6	MGTHTXP0	Not connected	NA	NA	NA
U5	MGTHTXN0	Not connected	NA	NA	
V4	MGTHRXP0	Not connected	NA	NA	
V3	MGTHRXN0	Not connected	NA	NA	
T4	MGTHTXP1	Not connected	NA	NA	
T3	MGTHTXN1	Not connected	NA	NA	
U2	MGTHRXP1	Not connected	NA	NA	
U1	MGTHRXN1	Not connected	NA	NA	
R6	MGTHTXP2	Not connected	NA	NA	
R5	MGTHTXN2	Not connected	NA	NA	
R2	MGTHRXP2	Not connected	NA	NA	
R1	MGTHRXN2	Not connected	NA	NA	
N6	MGTHTXP3	Not Connected	NA	NA	NA
N5	MGTHTXN3	Not Connected	NA	NA	
P4	MGTHRXP3	Not Connected	NA	NA	
P3	MGTHRXN3	Not Connected	NA	NA	
V8	MGTREFCLK0P	FMC_LPC_GBTCLK0_M2C_C_P[1]	D4	GBTCLK0_M2C_P	FMC LPC J5
V7	MGTREFCLK0N	FMC_LPC_GBTCLK0_M2C_C_N[1]	D5	GBTCLK0_M2C_N	

Table 3-26: **GTH Bank 226 Interface Connections *(Cont'd)***

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
U10	MGTREFCLK1P	HDMI_DRU_CLOCK_C_N[1]	48	Q0	8T49N287 U182
U9	MGTREFCLK1N	HDMI_DRU_CLOCK_C_P[1]	47	NQ0	

Notes:
1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-27: **GTH Bank 227 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
M4	MGTHTXP0	HDMI_TX0_P[1]	8	IN_D0P	SN64DP159R U94
M3	MGTHTXN0	HDMI_TX0_N[1]	9	IN_D0N	
L6	MGTHTXP1	HDMI_TX1_P[1]	5	IN_D1P	
L5	MGTHTXN1	HDMI_TX1_N[1]	6	IN_D1N	
K4	MGTHTXP2	HDMI_TX2_P[1]	2	IN_D2P	
K3	MGTHTXN2	HDMI_TX2_N[1]	3	IN_D2N	
N2	MGTHRXP0	HDMI_RX0_C_P	29	OUT_D0P	TMDS181IR U19
N1	MGTHRXN0	HDMI_RX0_C_N	28	OUT_D0N	
L2	MGTHRXP1	HDMI_RX1_C_P	32	OUT_D1P	
L1	MGTHRXN1	HDMI_RX1_C_N	31	OUT_D1N	
J2	MGTHRXP2	HDMI_RX2_C_P	35	OUT_D2P	
J1	MGTHRXN2	HDMI_RX2_C_N	34	OUT_D2N	
H4	MGTHTXP3	FMC_LPC_DP0_C2M_N	A34	DP4_C2M_P	FMC LPC J5
H3	MGTHTXN3	FMC_LPC_DP0_C2M_P	A35	DP4_C2M_N	
G2	MGTHRXP3	FMC_LPC_DP0_M2C_P	A14	DP4_M2C_P	
G1	MGTHRXN3	FMC_LPC_DP0_M2C_N	A15	DP4_M2C_N	
T8	MGTREFCLK0P	HDMI_8T49N241_OUT_C_N[1]	22	Q2	8T49N241 U181
T7	MGTREFCLK0N	HDMI_8T49N241_OUT_C_P[1]	23	NQ2	
R10	MGTREFCLK1P	HDMI_RX_CLK_C_P[1]	26	OUT_CLKP	TMDS181IR U19
R9	MGTREFCLK1N	HDMI_RX_CLK_C_N[1]	25	OUT_CLKN	

Notes:
1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

PS-Side: GTR Transceivers

[Figure 2-1, callout 1]

The PS-side GTR transceiver bank 505 supports two DisplayPort transmit channels, USB (3.0) and SATA, as shown in Figure 3-27.

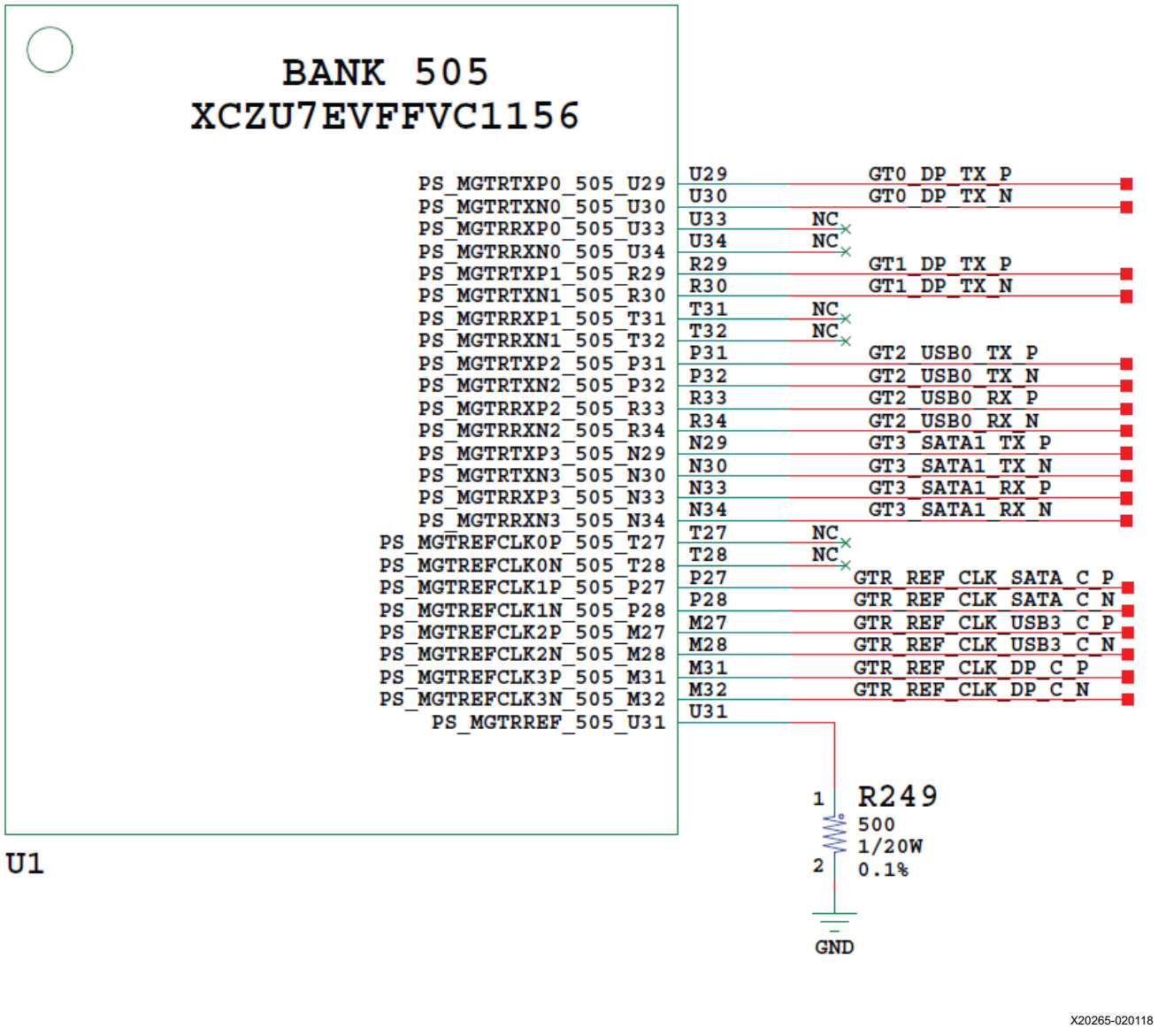

Figure 3-27: **PS-GTR Lane Assignments**

Bank 505 DP (DisplayPort) lanes 0 and 1 TX support the 2-channel source only PS-side DisplayPort circuitry described in DPAUX (MIO 27-30), page 54.

Bank 505 USB0 lane 2 supports the USB3.0 interface described in USB 3.0 Transceiver and USB 2.0 ULPI PHY, page 34.

Bank 505 SATA1 lane 3 supports the M.2 SATA connector U170 as shown in Figure 3-7.

Bank 505 reference clocks are connected to the U182 8T49N287 clock generator as described in Clock Generation, page 43.

Bank 505 connections are shown in Table 3-28.

Table 3-28: **PS-GTR Bank 505 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name(2)	Connected To		
			Pin No.	Pin Name	Device
U29	PS_MGTRTXP0	GT0_DP_TX_P(1)	4	ML_LANE1_P	DisplayPort connector P11
U30	PS_MGTRTXN0	GT0_DP_TX_N(1)	6	ML_LANE1_N	
R29	PS_MGTRTXP1	GT1_DP_TX_P(1)	1	ML_LANE0_P	
R30	PS_MGTRTXN1	GT1_DP_TX_N(1)	3	ML_LANE0_N	
U33	PS_MGTRRXP0	NC	NA	NA	NA
U34	PS_MGTRRXN0	NC	NA	NA	
T31	PS_MGTRRXP1	NC	NA	NA	
T32	PS_MGTRRXN1	NC	NA	NA	
P31	PS_MGTRTXP2	GT2_USB0_TX_P(1)	9	SSTXP	USB J96
P32	PS_MGTRTXN2	GT2_USB0_TX_N(1)	8	SSTXN	
R33	PS_MGTRRXP2	GT2_USB0_RX_P	6	SSRXP	
R34	PS_MGTRRXN2	GT2_USB0_RX_N	5	SSRXN	
N29	PS_MGTRTXP3	GT3_SATA1_TX_P(1)	2	SATA_A_P	M.2 U170
N30	PS_MGTRTXN3	GT3_SATA1_TX_N(1)	3	SATA_A_N	
N33	PS_MGTRRXP3	GT3_SATA1_RX_P(1)	6	SATA_B_P	
N34	PS_MGTRRXN3	GT3_SATA1_RX_N(1)	5	SATA_B_N	
T27	PS_MGTREFCLK0P	NC	NA	NA	NA
T28	PS_MGTREFCLK0N	NC	NA	NA	

Table 3-28: **PS-GTR Bank 505 Interface Connections *(Cont'd)***

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
P27	PS_MGTREFCLK1P	GTR_REF_CLK_SATA_C_P[1]	37	Q5	8T49N287 U182
P28	PS_MGTREFCLK1N	GTR_REF_CLK_SATA_C_N[1]	36	NQ5	
M27	PS_MGTREFCLK2P	GTR_REF_CLK_USB3_C_P[1]	27	Q2	
M28	PS_MGTREFCLK2N	GTR_REF_CLK_USB3_C_N[1]	28	NQ2	
M31	PS_MGTREFCLK3P	GTR_REF_CLK_DP_C_P[1]	23	Q3	
M32	PS_MGTREFCLK3N	GTR_REF_CLK_DP_C_N[1]	23	NQ3	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

FPGA Mezzanine Card Interface

[Figure 2-1, callout 25]

The ZCU104 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification [Ref 18] by implementing the LPC connector (J5). LPC connectors use a 10 x 40 form factor, partially populated with 160 pins. The connector is keyed so that a mezzanine card, when installed in the FMC LPC connector on the ZCU104 evaluation board, faces away from the board

FMC LPC Connector J5

[Figure 2-1, callout 25]

The FMC connector at J5 implements the full FMC LPC connectivity:

- 68 single-ended, or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- One GTH transceiver DP differential pair
- Two GBTCLK differential clocks
- 61 ground and 10 power connections

The ZCU104 board FMC VADJ voltage for LPC connector J5 is determined by the IRPS5401MTRPBF U180 voltage regulator described in Board Power System, page 82. Valid values for the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The LPC J5 connections to XCZU7EV U1 are shown in Table 3-29 and Table 3-30.

Table 3-29: **J5 LPC FMC Section C and D Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC_LPC_DP0_C2M_P	(2)	H4		D1	VADJ_FMC_PGOOD		
C3	FMC_LPC_DP0_C2M_N	(2)	H3		D4	FMC_LPC_GBTCLK0_M2C_P(1)	LVDS	V8
C6	FMC_LPC_DP0_M2C_P	(2)	G2		D5	FMC_LPC_GBTCLK0_M2C_N(1)	LVDS	V7
C7	FMC_LPC_DP0_M2C_N	(2)	G1		D8	FMC_LPC_LA01_CC_P	LVDS	H18
C10	FMC_LPC_LA06_P	LVDS	H19		D9	FMC_LPC_LA01_CC_N	LVDS	H17
C11	FMC_LPC_LA06_N	LVDS	G19		D11	FMC_LPC_LA05_P	LVDS	K17
C14	FMC_LPC_LA10_P	LVDS	L15		D12	FMC_LPC_LA05_N	LVDS	J17
C15	FMC_LPC_LA10_N	LVDS	K15		D14	FMC_LPC_LA09_P	LVDS	H16
C18	FMC_LPC_LA14_P	LVDS	C13		D15	FMC_LPC_LA09_N	LVDS	G16
C19	FMC_LPC_LA14_N	LVDS	C12		D17	FMC_LPC_LA13_P	LVDS	G15
C22	FMC_LPC_LA18_CC_P	LVDS	D11		D18	FMC_LPC_LA13_N	LVDS	F15
C23	FMC_LPC_LA18_CC_N	LVDS	D10		D20	FMC_LPC_LA17_CC_P	LVDS	F11
C26	FMC_LPC_LA27_P	LVDS	A8		D21	FMC_LPC_LA17_CC_N	LVDS	E10
C27	FMC_LPC_LA27_N	LVDS	A7		D23	FMC_LPC_LA23_P	LVDS	B11
C30	FMC_LPC_IIC_SCL				D24	FMC_LPC_LA23_N	LVDS	A11
C31	FMC_LPC_IIC_SDA				D26	FMC_LPC_LA26_P	LVDS	B9
C34	GND				D27	FMC_LPC_LA26_N	LVDS	B8
C35	VCC12_SW				D29	F4232_TCK		
C37	VCC12_SW				D30	FPGA_TDO_FMC_TDI_LS		
C39	UTIL_3V3				D31	FMC_TDO		
					D32	UTIL_3V3		
					D33	FT4232_TMS		
					D34	NC		
					D35	GA1=0=GND		
					D36	UTIL_3V3		
					D38	UTIL_3V3		
					D40	UTIL_3V3		

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-30: **J5 HPC0 FMC Section G and H Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	FMC_LPC_CLK1_M2C_P	LVDS	G10	H1	NC		
G3	FMC_LPC_CLK1_M2C_N	LVDS	F10	H2	FMC_LPC_PRSNT_M2C_B		
G6	FMC_LPC_LA00_CC_P	LVCMOS18	F17	H4	FMC_LPC_CLK0_M2C_P	LVDS	E15
G7	FMC_LPC_LA00_CC_N	LVCMOS18	F16	H5	FMC_LPC_CLK0_M2C_N	LVDS	E14
G9	FMC_LPC_LA03_P	LVDS	K19	H7	FMC_LPC_LA02_P	LVDS	L20
G10	FMC_LPC_LA03_N	LVDS	K18	H8	FMC_LPC_LA02_N	LVDS	K20
G12	FMC_LPC_LA08_P	LVDS	E18	H10	FMC_LPC_LA04_P	LVDS	L17
G13	FMC_LPC_LA08_N	LVDS	E17	H11	FMC_LPC_LA04_N	LVDS	L16
G15	FMC_LPC_LA12_P	LVDS	G18	H13	FMC_LPC_LA07_P	LVDS	J16
G16	FMC_LPC_LA12_N	LVDS	F18	H14	FMC_LPC_LA07_N	LVDS	J15
G18	FMC_LPC_LA16_P	LVDS	D17	H16	FMC_LPC_LA11_P	LVDS	A13
G19	FMC_LPC_LA16_N	LVDS	C17	H17	FMC_LPC_LA11_N	LVDS	A12
G21	FMC_LPC_LA20_P	LVDS	F12	H19	FMC_LPC_LA15_P	LVDS	D16
G22	FMC_LPC_LA20_N	LVDS	E12	H20	FMC_LPC_LA15_N	LVDS	C16
G24	FMC_LPC_LA22_P	LVDS	H13	H22	FMC_LPC_LA19_P	LVDS	D12
G25	FMC_LPC_LA22_N	LVDS	H12	H23	FMC_LPC_LA19_N	LVDS	C11
G27	FMC_LPC_LA25_P	LVDS	C7	H25	FMC_LPC_LA21_P	LVDS	B10
G28	FMC_LPC_LA25_N	LVDS	C6	H26	FMC_LPC_LA21_N	LVDS	A10
G30	FMC_LPC_LA29_P	LVDS	K10	H28	FMC_LPC_LA24_P	LVDS	B6
G31	FMC_LPC_LA29_N	LVDS	J10	H29	FMC_LPC_LA24_N	LVDS	A6
G33	FMC_LPC_LA31_P	LVDS	F7	H31	FMC_LPC_LA28_P	LVDS	M13
G34	FMC_LPC_LA31_N	LVDS	E7	H32	FMC_LPC_LA28_N	LVDS	L13
G36	FMC_LPC_LA33_P	LVDS	C9	H34	FMC_LPC_LA30_P	LVDS	E9
G37	FMC_LPC_LA33_N	LVDS	C8	H35	FMC_LPC_LA30_N	LVDS	D9
G39	VADJ			H37	FMC_LPC_LA32_P	LVDS	F8
				H38	FMC_LPC_LA32_N	LVDS	E8
				H40	VADJ		

Cooling Fan Connector

[Figure 2-1, near callout 17]

The ZCU104 cooling fan connector is shown in Figure 3-28.

The ZCU104 uses the Maxim MAX6643 fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the FPGA is cool and rotates faster as the FPGA heats up (acoustically noisy).

The fan speed (PWM) versus the FPGA die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device. The over temperature and fan failures alarms can be monitored by any available processor in the FPGA by polling the MAX6643_OT_B and MAX6643_FANFAIL_B signals wired to I2C expander U97 ports p02 and p03, U97 and pins 6 and 7, respectively. See the MAX6643 [Ref 17] data sheet for more information on the device circuit implementation on this board.

Note: At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

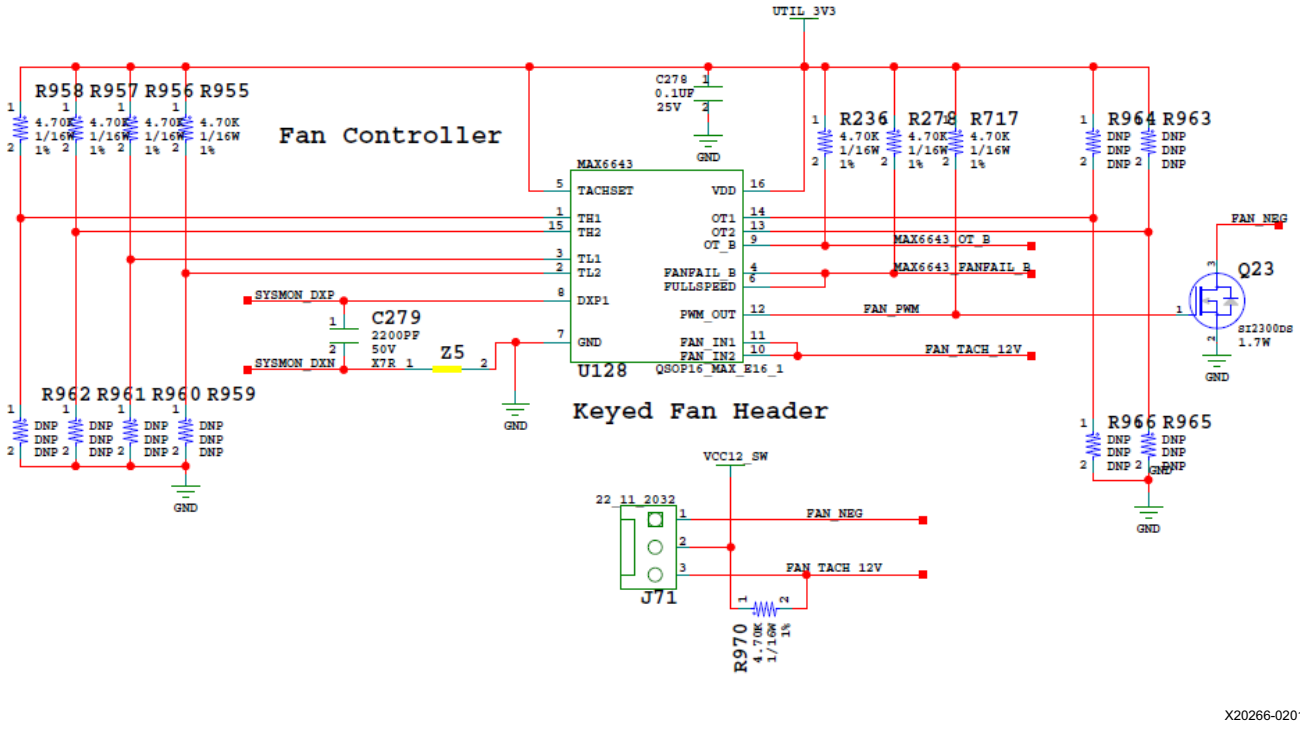

Figure 3-28: **12V Fan Header**

Switches

[Figure 2-1, callouts 20, 22, 24, and 30]

The ZCU104 board includes power, program, configuration, and reset switches:

- SW1 power on/off slide switch (callout 22)
- SW5 (PS_PROG_B), active-Low pushbutton (callout 24)
- SW3 (SRST_B), active-Low pushbutton (callout 20)
- SW4 (POR_B), active-Low pushbutton (callout 20)
- SW6 U1 MPSoC PS bank 503 4-pole mode DIP switch (callout 30)

Power On/Off Slide Switch

[Figure 2-1, callout 22]

The ZCU104 board power switch is SW1. Sliding the switch actuator from the off to the on position applies 12V power from J52, a 6-pin mini-fit connector. Green LED DS2 illuminates when the ZCU104 board power is on. See Board Power System, page 82 for details on the on-board power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU104 board power connector J52. The ATX 6-pin connector has a different pin-out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU104 board and voids the board warranty.*

Figure 3-29 shows the power connector J52, power switch SW1, and LED indicator DS2.

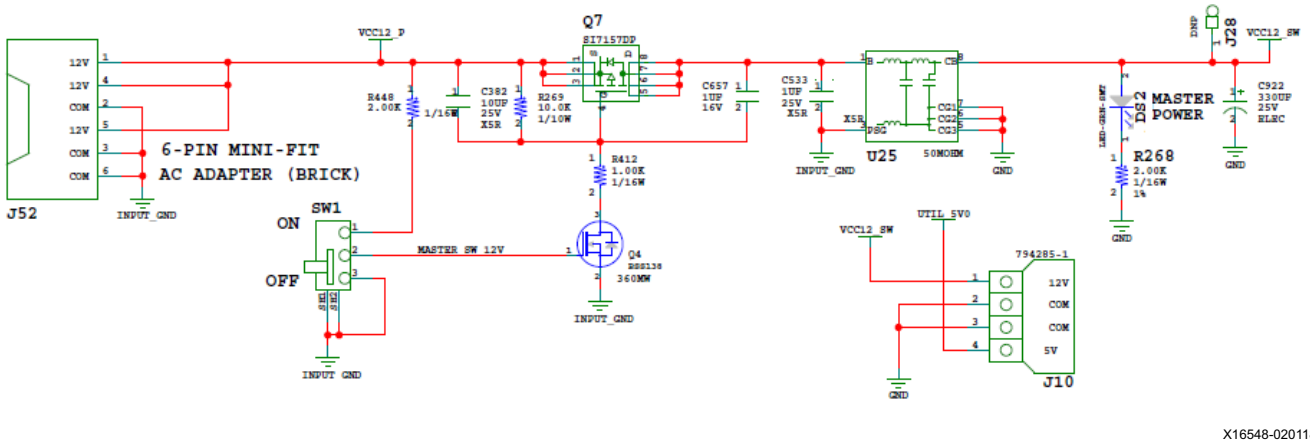

Figure 3-29: **Power Input**

Program_B Pushbutton

[Figure 2-1, callout 24]

PS_PROG_B pushbutton switch SW5 grounds the XCZU7EV MPSoC PS_PROG_B pin T24 when pressed (see Figure 3-30). This action clears the programmable logic configuration, which can then be acted on by the PS software. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for information about Zynq UltraScale+ MPSoC configuration.

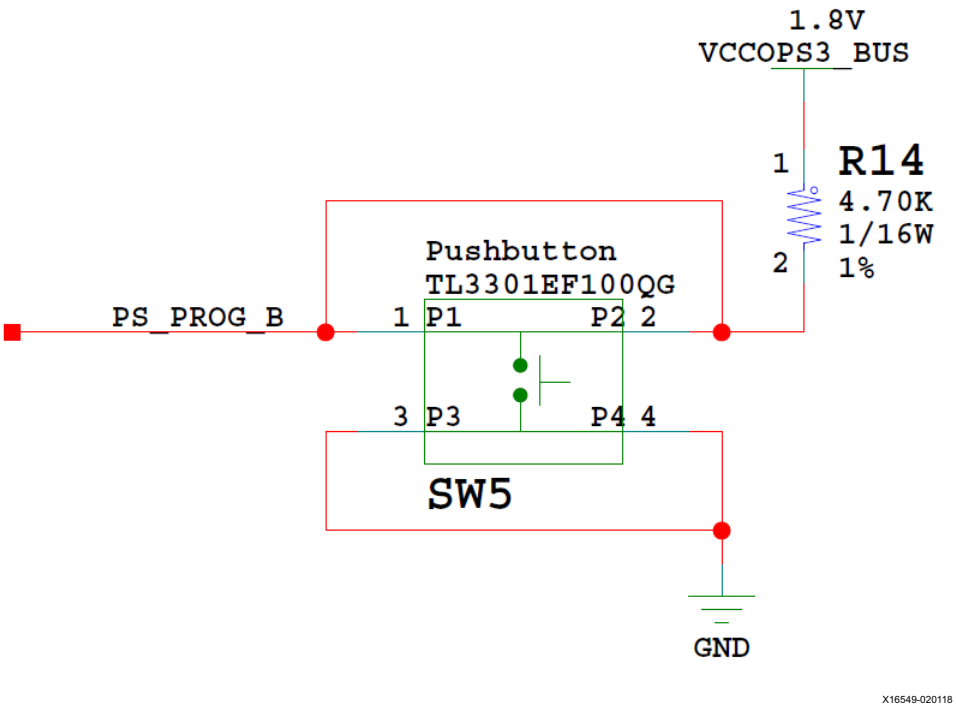

Figure 3-30: **PS_PROG_B Pushbutton Switch SW5**

System Reset Pushbuttons

[Figure 2-1, callout 20]

Figure 3-31 shows the reset circuitry for the PS.

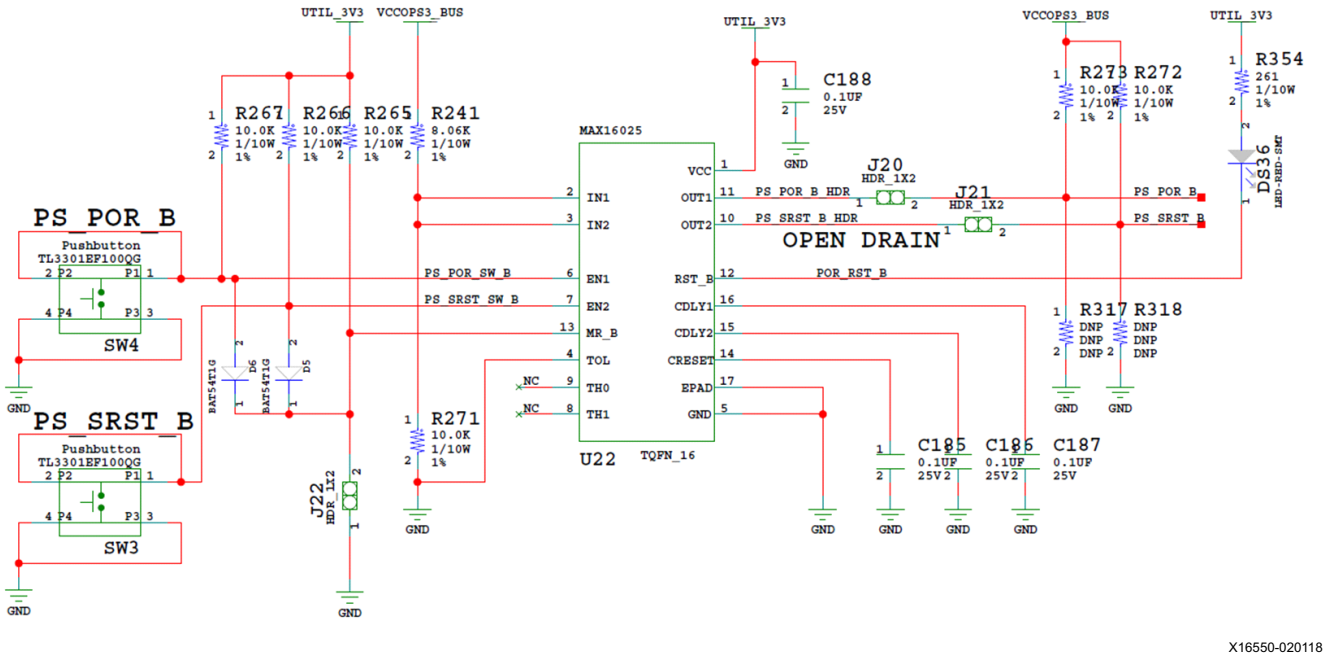

Figure 3-31: **PS SRST_B and POR_B Pushbutton Switches SW3 and SW4**

PS_POR_B Reset

Depressing and then releasing pushbutton SW4 causes net PS_POR_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal. When the voltage at U22 IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS_POR_B) goes Low.

PS_SRST_B Reset

Depressing and then releasing pushbutton SW3 causes net PS_SRST_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW3 is pressed) goes Low, OUT2 (PS_SRST_B) goes Low.

Active-Low reset output RST_B asserts when any of the monitored voltages (IN_) falls below the respective threshold, any EN_ goes Low, or MR is asserted. RST_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN_ are High, all OUT_ are High, and MR is deasserted. See the *Zynq*

UltraScale+ MPSoC Technical Reference Manual (UG1085) [Ref 2] for information on the resets.

Board Power System

[Figure 2-1, callout 26]

The ZCU104 hosts a Infineon PMBus based power system. Each individual Infineon IRPS5401MTRPBF voltage regulator has a PMBus interface.

Figure 3-32 shows the ZCU104 power system block diagram.

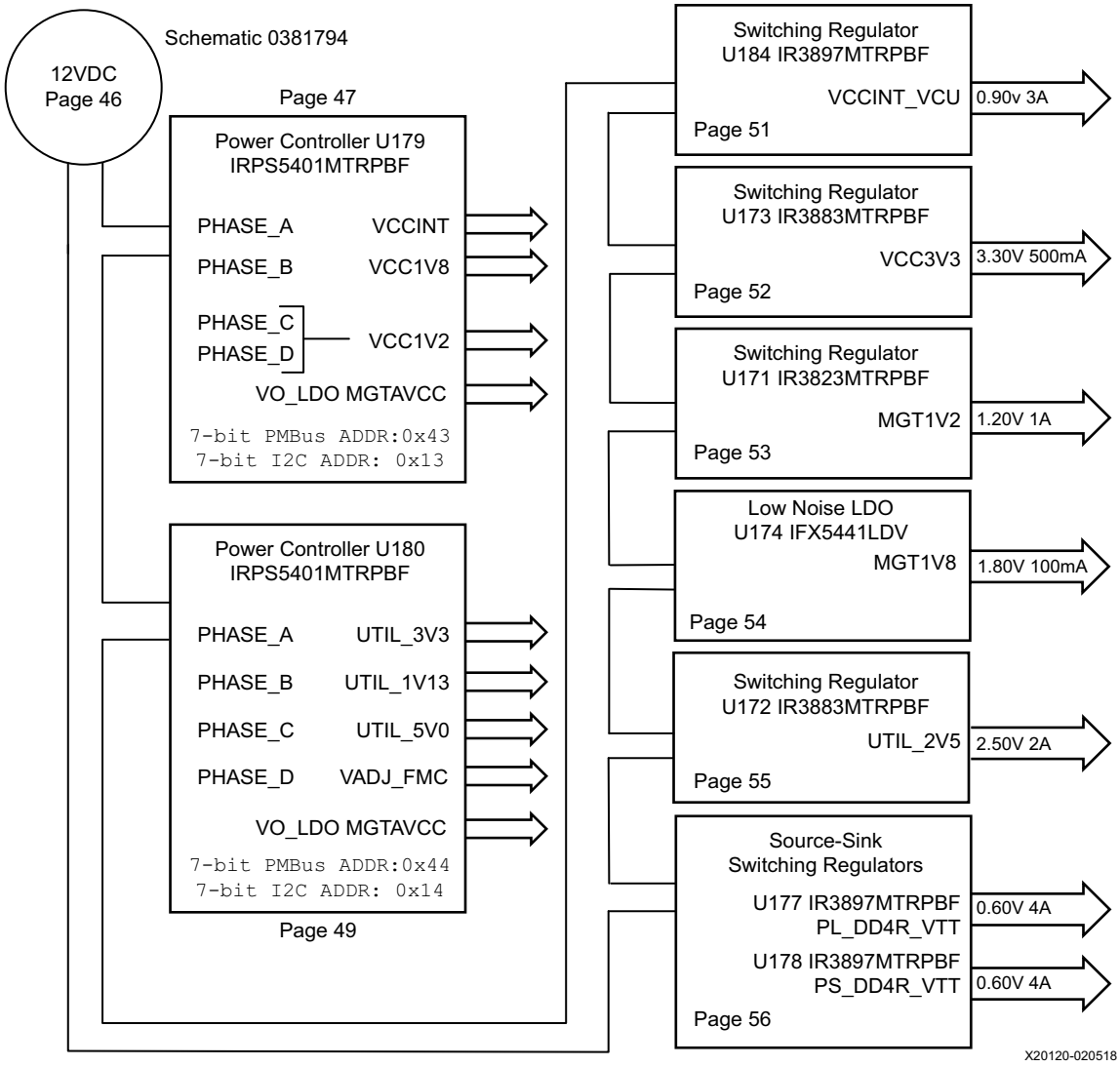

Figure 3-32: **Power System Block Diagram**

The ZCU104 evaluation board uses both PMBus compliant POL controllers and no-PMBus regulators from Infineon Technologies [Ref 21] to supply the core and auxiliary voltages listed in Table 3-31. The schematic page references are to 0381794.

Table 3-31: **Power System Devices**

Device Type	Ref. Des.	PMBus Addr.	I2C Addr.	Description	Output	Power Rail Net Name	Power Rail Voltage	Max. Current	Schem. Page
IRPS5401MTRPBF	U179	0x43	0x13	Infineon IRPS5401 multi-output PMIC	PHASE_A	VCCINT	0.85V		47
					PHASE_B	VCC1V8	1.80V		
					PHASE_C	VCC1V2	1.20V		
					PHASE_D				
					LDO	MGTAVCC	0.85V		
IRPS5401MTRPBF	U180	0x44	0x14	Infineon IRPS5401 multi-output PMIC	PHASE_A	UTIL_3V3	3.30V		49
					PHASE_B	VCC1V13	1.13V		
					PHASE_C	UTIL_5V0	5.00V		
					PHASE_D	VADJ_FMC	1.80V		
					LDO	MGTRAVCC	0.85V		
IR3883MTRPBF	U173	NA	NA	POL Switching regulator	SW	VCC3V3	3.30V	3A	51
IR3823MTRPBF	U171	NA	NA	Switching regulator	SW	MGT1V2	1.20V	3A	52
IFX54441LDV	U174	NA	NA	Low noise LDO	OUT	MGT1V8	1.81V	500 mA	53
IR3883MTRPBF	U172	NA	NA	POL switching regulator	SW	UTIL_2V5	2.50V	3A	54
IR3897MTRPBF	U177	NA	NA	Source-sink switching regulator	SW	PL_DDR4_VTT	0.60V	4A	55
IR3897MTRPBF	U178	NA	NA	Source-sink switching regulator	SW	PS_DDR4_VTT	0.60V	4A	55

The FMC LPC (J5) VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.80V by default. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The VADJ_FMC rail also powers the XCZU7EV HP banks 67 and 68 (see Table 3-2, page 23).

Documentation describing PMBus programming for the Infineon Technologies PMIC flexible power management unit power controllers is available at the Infineon Technologies website [Ref 21]. The PCB layout and power system design meets the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3].

Monitoring Voltage and Current

[Figure 2-1, callout 28]

Voltage and current monitoring and control are available on the power rails provided by the Infineon IRPS5401 power controllers through the Infineon IR PowERCenter graphical user interface. The onboard Infineon IRPS5401 power controllers listed in Table 3-31 are accessed through the I2C 1x3 male pin connector J175, which is included with the Infineon USB cable (Infineon part number USB005). The cable can be ordered from the Infineon website [Ref 21]). The associated Infineon IR PowERCenter GUI can be downloaded from the Infineon website. This is the most convenient way to monitor the voltage and current values for the Infineon PMBus programmed power rails listed in Table 3-31.

VITA 57.1 FMC Connector Pinouts

Overview

Figure A-1 shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZCU104 evaluation board implements the FMC specification, see FPGA Mezzanine Card Interface, page 75 and FMC LPC Connector J5, page 75.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

X20267-020118

Figure A-1: **FMC LPC Connector Pinouts**

Master Constraints File Listing

Overview

The master Xilinx design constraints (XDC) file template for the ZCU104 board provides for designs targeting the ZCU104 evaluation board. Net names in the constraints listed correlate with net names on the latest ZCU104 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 9] for more information.

For detailed I/O standards information required for a particular interface, see the constraint files generated by tools such as the memory interface generator (MIG) and base system builder (BSB).

The FMC connector J5 (LPC) is connected to MPSoC banks powered by the variable voltage V_{AJ_FMC}. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *The XDC file can be accessed on the TBD website.*

ZCU104 Board Constraints File

```
#CLOCKS


#PS_REF_CLK 33.33 MHz from U182 IDT 8T49N287A
#Other net   PACKAGE_PIN R24 - PS_REF_CLK Bank 503 - PS_REF_CLK


#CLK_125 125 MHz U69 SI5341B
# CLOCKS
# 125 MHz (PL BANK 68) from U182 IDT 8T49N287A Q6
set_property       PACKAGE_PIN    E23           [get_ports "CLK_125_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "CLK_125_N"] ;
```

```
set_property       PACKAGE_PIN    F23           [get_ports "CLK_125_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "CLK_125_P"] ;

# 300 MHz (PL BANK 64) from U182 IDT 8T49N287A Q4
set_property       PACKAGE_PIN    AH17          [get_ports "CLK_300_N"] ;
set_property       IOSTANDARD     DIFF_SSTL12   [get_ports "CLK_300_N"] ;
set_property       PACKAGE_PIN    AH18          [get_ports "CLK_300_P"] ;
set_property       IOSTANDARD     DIFF_SSTL12   [get_ports "CLK_300_P"] ;

#MEMORY
# DDR4 SODIMM SOCKET J1 (PL BANKS 64, 65, 66)
set_property       PACKAGE_PIN    AH16          [get_ports "DDR4_SODIMM_A0"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A0"] ;
set_property       PACKAGE_PIN    AG14          [get_ports "DDR4_SODIMM_A1"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A1"] ;
set_property       PACKAGE_PIN    AG15          [get_ports "DDR4_SODIMM_A2"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A2"] ;
set_property       PACKAGE_PIN    AF15          [get_ports "DDR4_SODIMM_A3"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A3"] ;
set_property       PACKAGE_PIN    AF16          [get_ports "DDR4_SODIMM_A4"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A4"] ;
set_property       PACKAGE_PIN    AJ14          [get_ports "DDR4_SODIMM_A5"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A5"] ;
set_property       PACKAGE_PIN    AH14          [get_ports "DDR4_SODIMM_A6"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A6"] ;
set_property       PACKAGE_PIN    AF17          [get_ports "DDR4_SODIMM_A7"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A7"] ;
set_property       PACKAGE_PIN    AK17          [get_ports "DDR4_SODIMM_A8"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A8"] ;
set_property       PACKAGE_PIN    AJ17          [get_ports "DDR4_SODIMM_A9"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A9"] ;
set_property       PACKAGE_PIN    AK14          [get_ports "DDR4_SODIMM_A10"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A10"] ;
set_property       PACKAGE_PIN    AK15          [get_ports "DDR4_SODIMM_A11"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A11"] ;
set_property       PACKAGE_PIN    AL18          [get_ports "DDR4_SODIMM_A12"] ;
set_property       IOSTANDARD     SSTL12        [get_ports "DDR4_SODIMM_A12"] ;
```

```
set_property      PACKAGE_PIN   AK18          [get_ports "DDR4_SODIMM_A13"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_A13"];
set_property      PACKAGE_PIN   AL15          [get_ports "DDR4_SODIMM_BA0"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_BA0"];
set_property      PACKAGE_PIN   AL16          [get_ports "DDR4_SODIMM_BA1"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_BA1"];
set_property      PACKAGE_PIN   AC16          [get_ports "DDR4_SODIMM_BG0"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_BG0"];
set_property      PACKAGE_PIN   AB16          [get_ports "DDR4_SODIMM_BG1"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_BG1"];
set_property      PACKAGE_PIN   AE24          [get_ports "DDR4_SODIMM_DQ0"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ0"];
set_property      PACKAGE_PIN   AE23          [get_ports "DDR4_SODIMM_DQ1"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ1"];
set_property      PACKAGE_PIN   AF22          [get_ports "DDR4_SODIMM_DQ2"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ2"];
set_property      PACKAGE_PIN   AF21          [get_ports "DDR4_SODIMM_DQ3"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ3"];
set_property      PACKAGE_PIN   AG20          [get_ports "DDR4_SODIMM_DQ4"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ4"];
set_property      PACKAGE_PIN   AG19          [get_ports "DDR4_SODIMM_DQ5"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ5"];
set_property      PACKAGE_PIN   AH21          [get_ports "DDR4_SODIMM_DQ6"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ6"];
set_property      PACKAGE_PIN   AG21          [get_ports "DDR4_SODIMM_DQ7"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ7"];
set_property      PACKAGE_PIN   AA20          [get_ports "DDR4_SODIMM_DQ8"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ8"];
set_property      PACKAGE_PIN   AA19          [get_ports "DDR4_SODIMM_DQ9"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ9"];
set_property      PACKAGE_PIN   AD19          [get_ports "DDR4_SODIMM_DQ10"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ10"];
set_property      PACKAGE_PIN   AC18          [get_ports "DDR4_SODIMM_DQ11"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ11"];
set_property      PACKAGE_PIN   AE20          [get_ports "DDR4_SODIMM_DQ12"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DQ12"];
set_property      PACKAGE_PIN   AD20          [get_ports "DDR4_SODIMM_DQ13"];
```

```
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ13"];
set_property      PACKAGE_PIN   AC19         [get_ports "DDR4_SODIMM_DQ14"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ14"];
set_property      PACKAGE_PIN   AB19         [get_ports "DDR4_SODIMM_DQ15"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ15"];
set_property      PACKAGE_PIN   AJ22         [get_ports "DDR4_SODIMM_DQ16"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ16"];
set_property      PACKAGE_PIN   AJ21         [get_ports "DDR4_SODIMM_DQ17"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ17"];
set_property      PACKAGE_PIN   AK20         [get_ports "DDR4_SODIMM_DQ18"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ18"];
set_property      PACKAGE_PIN   AJ20         [get_ports "DDR4_SODIMM_DQ19"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ19"];
set_property      PACKAGE_PIN   AK19         [get_ports "DDR4_SODIMM_DQ20"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ20"];
set_property      PACKAGE_PIN   AJ19         [get_ports "DDR4_SODIMM_DQ21"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ21"];
set_property      PACKAGE_PIN   AL23         [get_ports "DDR4_SODIMM_DQ22"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ22"];
set_property      PACKAGE_PIN   AL22         [get_ports "DDR4_SODIMM_DQ23"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ23"];
set_property      PACKAGE_PIN   AN23         [get_ports "DDR4_SODIMM_DQ24"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ24"];
set_property      PACKAGE_PIN   AM23         [get_ports "DDR4_SODIMM_DQ25"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ25"];
set_property      PACKAGE_PIN   AP23         [get_ports "DDR4_SODIMM_DQ26"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ26"];
set_property      PACKAGE_PIN   AN22         [get_ports "DDR4_SODIMM_DQ27"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ27"];
set_property      PACKAGE_PIN   AP22         [get_ports "DDR4_SODIMM_DQ28"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ28"];
set_property      PACKAGE_PIN   AP21         [get_ports "DDR4_SODIMM_DQ29"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ29"];
set_property      PACKAGE_PIN   AN19         [get_ports "DDR4_SODIMM_DQ30"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ30"];
set_property      PACKAGE_PIN   AM19         [get_ports "DDR4_SODIMM_DQ31"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ31"];
```

```
set_property    PACKAGE_PIN   AC13        [get_ports "DDR4_SODIMM_DQ32"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ32"];
set_property    PACKAGE_PIN   AB13        [get_ports "DDR4_SODIMM_DQ33"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ33"];
set_property    PACKAGE_PIN   AF12        [get_ports "DDR4_SODIMM_DQ34"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ34"];
set_property    PACKAGE_PIN   AE12        [get_ports "DDR4_SODIMM_DQ35"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ35"];
set_property    PACKAGE_PIN   AF13        [get_ports "DDR4_SODIMM_DQ36"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ36"];
set_property    PACKAGE_PIN   AE13        [get_ports "DDR4_SODIMM_DQ37"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ37"];
set_property    PACKAGE_PIN   AE14        [get_ports "DDR4_SODIMM_DQ38"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ38"];
set_property    PACKAGE_PIN   AD14        [get_ports "DDR4_SODIMM_DQ39"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ39"];
set_property    PACKAGE_PIN   AG8         [get_ports "DDR4_SODIMM_DQ40"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ40"];
set_property    PACKAGE_PIN   AF8         [get_ports "DDR4_SODIMM_DQ41"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ41"];
set_property    PACKAGE_PIN   AG10        [get_ports "DDR4_SODIMM_DQ42"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ42"];
set_property    PACKAGE_PIN   AG11        [get_ports "DDR4_SODIMM_DQ43"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ43"];
set_property    PACKAGE_PIN   AH13        [get_ports "DDR4_SODIMM_DQ44"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ44"];
set_property    PACKAGE_PIN   AG13        [get_ports "DDR4_SODIMM_DQ45"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ45"];
set_property    PACKAGE_PIN   AJ11        [get_ports "DDR4_SODIMM_DQ46"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ46"];
set_property    PACKAGE_PIN   AH11        [get_ports "DDR4_SODIMM_DQ47"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ47"];
set_property    PACKAGE_PIN   AK9         [get_ports "DDR4_SODIMM_DQ48"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ48"];
set_property    PACKAGE_PIN   AJ9         [get_ports "DDR4_SODIMM_DQ49"];
set_property    IOSTANDARD    POD12       [get_ports "DDR4_SODIMM_DQ49"];
set_property    PACKAGE_PIN   AK10        [get_ports "DDR4_SODIMM_DQ50"];
```

```
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ50"];
set_property      PACKAGE_PIN   AJ10         [get_ports "DDR4_SODIMM_DQ51"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ51"];
set_property      PACKAGE_PIN   AL12         [get_ports "DDR4_SODIMM_DQ52"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ52"];
set_property      PACKAGE_PIN   AK12         [get_ports "DDR4_SODIMM_DQ53"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ53"];
set_property      PACKAGE_PIN   AL10         [get_ports "DDR4_SODIMM_DQ54"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ54"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ55"];
set_property      PACKAGE_PIN   AL11         [get_ports "DDR4_SODIMM_DQ55"];
set_property      PACKAGE_PIN   AM8          [get_ports "DDR4_SODIMM_DQ56"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ56"];
set_property      PACKAGE_PIN   AM9          [get_ports "DDR4_SODIMM_DQ57"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ57"];
set_property      PACKAGE_PIN   AM10         [get_ports "DDR4_SODIMM_DQ58"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ58"];
set_property      PACKAGE_PIN   AM11         [get_ports "DDR4_SODIMM_DQ59"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ59"];
set_property      PACKAGE_PIN   AP11         [get_ports "DDR4_SODIMM_DQ60"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ60"];
set_property      PACKAGE_PIN   AN11         [get_ports "DDR4_SODIMM_DQ61"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ61"];
set_property      PACKAGE_PIN   AP9          [get_ports "DDR4_SODIMM_DQ62"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ62"];
set_property      PACKAGE_PIN   AP10         [get_ports "DDR4_SODIMM_DQ63"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DQ63"];
set_property      PACKAGE_PIN   AH22         [get_ports "DDR4_SODIMM_DM0_B"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DM0_B"];
set_property      PACKAGE_PIN   AE18         [get_ports "DDR4_SODIMM_DM1_B"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DM1_B"];
set_property      PACKAGE_PIN   AL20         [get_ports "DDR4_SODIMM_DM2_B"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DM2_B"];
set_property      PACKAGE_PIN   AP19         [get_ports "DDR4_SODIMM_DM3_B"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DM3_B"];
set_property      PACKAGE_PIN   AF11         [get_ports "DDR4_SODIMM_DM4_B"];
set_property      IOSTANDARD    POD12        [get_ports "DDR4_SODIMM_DM4_B"];
```

```
set_property      PACKAGE_PIN   AH12          [get_ports "DDR4_SODIMM_DM5_B"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DM5_B"];
set_property      PACKAGE_PIN   AK13          [get_ports "DDR4_SODIMM_DM6_B"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DM6_B"];
set_property      PACKAGE_PIN   AN12          [get_ports "DDR4_SODIMM_DM7_B"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_DM7_B"];
set_property      PACKAGE_PIN   AG23          [get_ports "DDR4_SODIMM_DQS0_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS0_C"];
set_property      PACKAGE_PIN   AF23          [get_ports "DDR4_SODIMM_DQS0_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS0_T"];
set_property      PACKAGE_PIN   AB18          [get_ports "DDR4_SODIMM_DQS1_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS1_C"];
set_property      PACKAGE_PIN   AA18          [get_ports "DDR4_SODIMM_DQS1_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS1_T"];
set_property      PACKAGE_PIN   AK23          [get_ports "DDR4_SODIMM_DQS2_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS2_C"];
set_property      PACKAGE_PIN   AK22          [get_ports "DDR4_SODIMM_DQS2_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS2_T"];
set_property      PACKAGE_PIN   AN21          [get_ports "DDR4_SODIMM_DQS3_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS3_C"];
set_property      PACKAGE_PIN   AM21          [get_ports "DDR4_SODIMM_DQS3_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS3_T"];
set_property      PACKAGE_PIN   AD12          [get_ports "DDR4_SODIMM_DQS4_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS4_C"];
set_property      PACKAGE_PIN   AC12          [get_ports "DDR4_SODIMM_DQS4_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS4_T"];
set_property      PACKAGE_PIN   AH9           [get_ports "DDR4_SODIMM_DQS5_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS5_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS5_T"];
set_property      PACKAGE_PIN   AG9           [get_ports "DDR4_SODIMM_DQS5_T"];
set_property      PACKAGE_PIN   AL8           [get_ports "DDR4_SODIMM_DQS6_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS6_C"];
set_property      PACKAGE_PIN   AK8           [get_ports "DDR4_SODIMM_DQS6_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS6_T"];
set_property      PACKAGE_PIN   AN8           [get_ports "DDR4_SODIMM_DQS7_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS7_C"];
set_property      PACKAGE_PIN   AN9           [get_ports "DDR4_SODIMM_DQS7_T"];
```

```
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_DQS7_T"];
set_property      PACKAGE_PIN   AG18          [get_ports "DDR4_SODIMM_CK0_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_CK0_C"];
set_property      PACKAGE_PIN   AF18          [get_ports "DDR4_SODIMM_CK0_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_CK0_T"];
set_property      PACKAGE_PIN   AD17          [get_ports "DDR4_SODIMM_CKE0"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CKE0"];
set_property      PACKAGE_PIN   AJ15          [get_ports "DDR4_SODIMM_CK1_C"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_CK1_C"];
set_property      PACKAGE_PIN   AJ16          [get_ports "DDR4_SODIMM_CK1_T"];
set_property      IOSTANDARD    DIFF_POD12    [get_ports "DDR4_SODIMM_CK1_T"];
set_property      PACKAGE_PIN   AM15          [get_ports "DDR4_SODIMM_CKE1"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CKE1"];
set_property      PACKAGE_PIN   AA14          [get_ports "DDR4_SODIMM_CAS_B"];
set_property      IOSTANDARD    SSTL21        [get_ports "DDR4_SODIMM_CAS_B"];
set_property      PACKAGE_PIN   AD15          [get_ports "DDR4_SODIMM_RAS_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_RAS_B"];
set_property      PACKAGE_PIN   AA16          [get_ports "DDR4_SODIMM_WE_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_WE_B"];
set_property      PACKAGE_PIN   AC17          [get_ports "DDR4_SODIMM_ACT_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_ACT_B"];
set_property      PACKAGE_PIN   AB15          [get_ports "DDR4_SODIMM_ALERT_B"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_ALERT_B"];
set_property      PACKAGE_PIN   AD16          [get_ports "DDR4_SODIMM_PARITY"];
set_property      IOSTANDARD    POD12         [get_ports "DDR4_SODIMM_PARITY"];
set_property      PACKAGE_PIN   AE15          [get_ports "DDR4_SODIMM_ODT0"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_ODT0"];
set_property      PACKAGE_PIN   AM16          [get_ports "DDR4_SODIMM_ODT1"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_ODT1"];
set_property      PACKAGE_PIN   AA15          [get_ports "DDR4_SODIMM_CS0_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CS0_B"];
set_property      PACKAGE_PIN   AL17          [get_ports "DDR4_SODIMM_CS1_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CS1_B"];
set_property      PACKAGE_PIN   AN17          [get_ports "DDR4_SODIMM_CS2_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CS2_B"];
set_property      PACKAGE_PIN   AN16          [get_ports "DDR4_SODIMM_CS3_B"];
set_property      IOSTANDARD    SSTL12        [get_ports "DDR4_SODIMM_CS3_B"];
```

```
set_property        PACKAGE_PIN    AB14          [get_ports"DDR4_SODIMM_RESET_B"];
set_property        IOSTANDARD     LVCMOS12      [get_ports"DDR4_SODIMM_RESET_B"];

#DDR4 COMPONENT 64-BIT PS DDR Bank 504 Interface
#Other net          PACKAGE_PIN    AN34          DDR4_A0
#Other net          PACKAGE_PIN    AM34          DDR4_A1
#Other net          PACKAGE_PIN    AM33          DDR4_A2
#Other net          PACKAGE_PIN    AL34          DDR4_A3
#Other net          PACKAGE_PIN    AL33          DDR4_A4
#Other net          PACKAGE_PIN    AK33          DDR4_A5
#Other net          PACKAGE_PIN    AK30          DDR4_A6
#Other net          PACKAGE_PIN    AJ30          DDR4_A7
#Other net          PACKAGE_PIN    AJ31          DDR4_A8
#Other net          PACKAGE_PIN    AH31          DDR4_A9
#Other net          PACKAGE_PIN    AG31          DDR4_A10
#Other net          PACKAGE_PIN    AF31          DDR4_A11
#Other net          PACKAGE_PIN    AG30          DDR4_A12
#Other net          PACKAGE_PIN    AF30          DDR4_A13
#Other net          PACKAGE_PIN    AG29          DDR4_A14_WE_B
#Other net          PACKAGE_PIN    AG28          DDR4_A15_CAS_B
#Other net          PACKAGE_PIN    AF28          DDR4_A16_RAS_B
#Other net          PACKAGE_PIN    AE27          DDR4_BA0
#Other net          PACKAGE_PIN    AE28          DDR4_BA1
#Other net          PACKAGE_PIN    AD27          DDR4_BG0
#Other net          PACKAGE_PIN    AN24          DDR4_DM0
#Other net          PACKAGE_PIN    AM29          DDR4_DM1
#Other net          PACKAGE_PIN    AH24          DDR4_DM2
#Other net          PACKAGE_PIN    AJ29          DDR4_DM3
#Other net          PACKAGE_PIN    AD29          DDR4_DM4
#Other net          PACKAGE_PIN    Y29           DDR4_DM5
#Other net          PACKAGE_PIN    AC32          DDR4_DM6
#Other net          PACKAGE_PIN    Y32           DDR4_DM7
#Other net          PACKAGE_PIN    AP27          DDR4_DQ0
#Other net          PACKAGE_PIN    AP25          DDR4_DQ1
#Other net          PACKAGE_PIN    AP26          DDR4_DQ2
#Other net          PACKAGE_PIN    AM26          DDR4_DQ3
#Other net          PACKAGE_PIN    AP24          DDR4_DQ4
```

```
#Other net        PACKAGE_PIN    AL25          DDR4_DQ5
#Other net        PACKAGE_PIN    AM25          DDR4_DQ6
#Other net        PACKAGE_PIN    AM24          DDR4_DQ7
#Other net        PACKAGE_PIN    AM28          DDR4_DQ8
#Other net        PACKAGE_PIN    AN28          DDR4_DQ9
#Other net        PACKAGE_PIN    AP29          DDR4_DQ10
#Other net        PACKAGE_PIN    AP28          DDR4_DQ11
#Other net        PACKAGE_PIN    AM31          DDR4_DQ12
#Other net        PACKAGE_PIN    AP31          DDR4_DQ13
#Other net        PACKAGE_PIN    AN31          DDR4_DQ14
#Other net        PACKAGE_PIN    AM30          DDR4_DQ15
#Other net        PACKAGE_PIN    AF25          DDR4_DQ16
#Other net        PACKAGE_PIN    AG25          DDR4_DQ17
#Other net        PACKAGE_PIN    AG26          DDR4_DQ18
#Other net        PACKAGE_PIN    AJ25          DDR4_DQ19
#Other net        PACKAGE_PIN    AG24          DDR4_DQ20
#Other net        PACKAGE_PIN    AK25          DDR4_DQ21
#Other net        PACKAGE_PIN    AJ24          DDR4_DQ22
#Other net        PACKAGE_PIN    AK24          DDR4_DQ23
#Other net        PACKAGE_PIN    AH28          DDR4_DQ24
#Other net        PACKAGE_PIN    AH27          DDR4_DQ25
#Other net        PACKAGE_PIN    AJ27          DDR4_DQ26
#Other net        PACKAGE_PIN    AK27          DDR4_DQ27
#Other net        PACKAGE_PIN    AL26          DDR4_DQ28
#Other net        PACKAGE_PIN    AL27          DDR4_DQ29
#Other net        PACKAGE_PIN    AH29          DDR4_DQ30
#Other net        PACKAGE_PIN    AL28          DDR4_DQ31
#Other net        PACKAGE_PIN    AB29          DDR4_DQ32
#Other net        PACKAGE_PIN    AB30          DDR4_DQ33
#Other net        PACKAGE_PIN    AC29          DDR4_DQ34
#Other net        PACKAGE_PIN    AD32          DDR4_DQ35
#Other net        PACKAGE_PIN    AC31          DDR4_DQ36
#Other net        PACKAGE_PIN    AE30          DDR4_DQ37
#Other net        PACKAGE_PIN    AC28          DDR4_DQ38
#Other net        PACKAGE_PIN    AE29          DDR4_DQ39
#Other net        PACKAGE_PIN    AC27          DDR4_DQ40
#Other net        PACKAGE_PIN    AA27          DDR4_DQ41
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#Other net        PACKAGE_PIN   AA28          DDR4_DQ42
#Other net        PACKAGE_PIN   AB28          DDR4_DQ43
#Other net        PACKAGE_PIN   W27           DDR4_DQ44
#Other net        PACKAGE_PIN   W29           DDR4_DQ45
#Other net        PACKAGE_PIN   W28           DDR4_DQ46
#Other net        PACKAGE_PIN   V27           DDR4_DQ47
#Other net        PACKAGE_PIN   AA32          DDR4_DQ48
#Other net        PACKAGE_PIN   AA33          DDR4_DQ49
#Other net        PACKAGE_PIN   AA34          DDR4_DQ50
#Other net        PACKAGE_PIN   AE34          DDR4_DQ51
#Other net        PACKAGE_PIN   AD34          DDR4_DQ52
#Other net        PACKAGE_PIN   AB31          DDR4_DQ53
#Other net        PACKAGE_PIN   AC34          DDR4_DQ54
#Other net        PACKAGE_PIN   AC33          DDR4_DQ55
#Other net        PACKAGE_PIN   AA30          DDR4_DQ56
#Other net        PACKAGE_PIN   Y30           DDR4_DQ57
#Other net        PACKAGE_PIN   AA31          DDR4_DQ58
#Other net        PACKAGE_PIN   W30           DDR4_DQ59
#Other net        PACKAGE_PIN   Y33           DDR4_DQ60
#Other net        PACKAGE_PIN   W33           DDR4_DQ61
#Other net        PACKAGE_PIN   W34           DDR4_DQ62
#Other net        PACKAGE_PIN   Y34           DDR4_DQ63
#Other net        PACKAGE_PIN   AN26          DDR4_DQS0_T
#Other net        PACKAGE_PIN   AN27          DDR4_DQS0_C
#Other net        PACKAGE_PIN   AN29          DDR4_DQS1_T
#Other net        PACKAGE_PIN   AP30          DDR4_DQS1_C
#Other net        PACKAGE_PIN   AH26          DDR4_DQS2_T
#Other net        PACKAGE_PIN   AJ26          DDR4_DQS2_C
#Other net        PACKAGE_PIN   AK28          DDR4_DQS3_T
#Other net        PACKAGE_PIN   AK29          DDR4_DQS3_C
#Other net        PACKAGE_PIN   AD30          DDR4_DQS4_T
#Other net        PACKAGE_PIN   AD31          DDR4_DQS4_C
#Other net        PACKAGE_PIN   Y27           DDR4_DQS5_T
#Other net        PACKAGE_PIN   Y28           DDR4_DQS5_C
#Other net        PACKAGE_PIN   AB33          DDR4_DQS6_T
#Other net        PACKAGE_PIN   AB34          DDR4_DQS6_C
#Other net        PACKAGE_PIN   W31           DDR4_DQS7_T
```

```
#Other net         PACKAGE_PIN    W32            DDR4_DQS7_C
#Other net         PACKAGE_PIN    AL31           DDR4_CK_T
#Other net         PACKAGE_PIN    AN32           DDR4_CK_C
#Other net         PACKAGE_PIN    AN33           DDR4_CKE
#Other net         PACKAGE_PIN    AP33           DDR4_CS_B
#Other net         PACKAGE_PIN    AE25           DDR4_ACT_B
#Other net         PACKAGE_PIN    AB26           DDR4_ALERT_B
#Other net         PACKAGE_PIN    AP32           DDR4_ODT
#Other net         PACKAGE_PIN    AA26           DDR4_PAR
#Other net         PACKAGE_PIN    AD26           DDR4_RESET_B
#Other net         PACKAGE_PIN    AC26           SODIMM_ZQ

#QSPI
#QSPI_LWR U119 is connected to PS MIO Bank 500
#Other net         PACKAGE_PIN    A24            MIO0_QSPI_LWR_CLK
#Other net         PACKAGE_PIN    C24            MIO1_QSPI_LWR_DQ1
#Other net         PACKAGE_PIN    B24            MIO2_QSPI_LWR_DQ2
#Other net         PACKAGE_PIN    E25            MIO3_QSPI_LWR_DQ3
#Other net         PACKAGE_PIN    A25            MIO4_QSPI_LWR_DQ0
#Other net         PACKAGE_PIN    D25            MIO5_QSPI_LWR_CS_B

#FMC
# FMC LPC J5  (PL BANKS 67, 68)
set_property       PACKAGE_PIN    E14            [get_ports "FMC_LPC_CLK0_M2C_N"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_CLK0_M2C_N"] ;
set_property       PACKAGE_PIN    E15            [get_ports "FMC_LPC_CLK0_M2C_P"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_CLK0_M2C_P"] ;
set_property       PACKAGE_PIN    F10            [get_ports "FMC_LPC_CLK1_M2C_N"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_CLK1_M2C_N"] ;
set_property       PACKAGE_PIN    G10            [get_ports "FMC_LPC_CLK1_M2C_P"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_CLK1_M2C_P"] ;
set_property       PACKAGE_PIN    F16            [get_ports "FMC_LPC_LA00_CC_N"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_LA00_CC_N"] ;
set_property       PACKAGE_PIN    F17            [get_ports "FMC_LPC_LA00_CC_P"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_LA00_CC_P"] ;
set_property       PACKAGE_PIN    H17            [get_ports "FMC_LPC_LA01_CC_N"] ;
set_property       IOSTANDARD     LVDS           [get_ports "FMC_LPC_LA01_CC_N"] ;
```

```
set_property      PACKAGE_PIN   H18          [get_ports "FMC_LPC_LA01_CC_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA01_CC_P"] ;
set_property      PACKAGE_PIN   K20          [get_ports "FMC_LPC_LA02_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA02_N"] ;
set_property      PACKAGE_PIN   L20          [get_ports "FMC_LPC_LA02_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA02_P"] ;
set_property      PACKAGE_PIN   K18          [get_ports "FMC_LPC_LA03_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA03_N"] ;
set_property      PACKAGE_PIN   K19          [get_ports "FMC_LPC_LA03_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA03_P"] ;
set_property      PACKAGE_PIN   L16          [get_ports "FMC_LPC_LA04_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA04_N"] ;
set_property      PACKAGE_PIN   L17          [get_ports "FMC_LPC_LA04_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA04_P"] ;
set_property      PACKAGE_PIN   J17          [get_ports "FMC_LPC_LA05_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA05_N"] ;
set_property      PACKAGE_PIN   K17          [get_ports "FMC_LPC_LA05_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA05_P"] ;
set_property      PACKAGE_PIN   G19          [get_ports "FMC_LPC_LA06_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA06_N"] ;
set_property      PACKAGE_PIN   H19          [get_ports "FMC_LPC_LA06_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA06_P"] ;
set_property      PACKAGE_PIN   J15          [get_ports "FMC_LPC_LA07_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA07_N"] ;
set_property      PACKAGE_PIN   J16          [get_ports "FMC_LPC_LA07_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA07_P"] ;
set_property      PACKAGE_PIN   E17          [get_ports "FMC_LPC_LA08_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA08_N"] ;
set_property      PACKAGE_PIN   E18          [get_ports "FMC_LPC_LA08_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA08_P"] ;
set_property      PACKAGE_PIN   G16          [get_ports "FMC_LPC_LA09_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA09_N"] ;
set_property      PACKAGE_PIN   H16          [get_ports "FMC_LPC_LA09_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA09_P"] ;
set_property      PACKAGE_PIN   K15          [get_ports "FMC_LPC_LA10_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA10_N"] ;
set_property      PACKAGE_PIN   L15          [get_ports "FMC_LPC_LA10_P"] ;
```

```
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA10_P"] ;
set_property       PACKAGE_PIN    A12           [get_ports "FMC_LPC_LA11_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA11_N"] ;
set_property       PACKAGE_PIN    A13           [get_ports "FMC_LPC_LA11_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA11_P"] ;
set_property       PACKAGE_PIN    F18           [get_ports "FMC_LPC_LA12_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA12_N"] ;
set_property       PACKAGE_PIN    G18           [get_ports "FMC_LPC_LA12_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA12_P"] ;
set_property       PACKAGE_PIN    F15           [get_ports "FMC_LPC_LA13_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA13_N"] ;
set_property       PACKAGE_PIN    G15           [get_ports "FMC_LPC_LA13_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA13_P"] ;
set_property       PACKAGE_PIN    C12           [get_ports "FMC_LPC_LA14_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA14_N"] ;
set_property       PACKAGE_PIN    C13           [get_ports "FMC_LPC_LA14_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA14_P"] ;
set_property       PACKAGE_PIN    C16           [get_ports "FMC_LPC_LA15_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA15_N"] ;
set_property       PACKAGE_PIN    D16           [get_ports "FMC_LPC_LA15_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA15_P"] ;
set_property       PACKAGE_PIN    C17           [get_ports "FMC_LPC_LA16_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA16_N"] ;
set_property       PACKAGE_PIN    D17           [get_ports "FMC_LPC_LA16_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA16_P"] ;
set_property       PACKAGE_PIN    E10           [get_ports "FMC_LPC_LA17_CC_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA17_CC_N"] ;
set_property       PACKAGE_PIN    F11           [get_ports "FMC_LPC_LA17_CC_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA17_CC_P"] ;
set_property       PACKAGE_PIN    D10           [get_ports "FMC_LPC_LA18_CC_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA18_CC_N"] ;
set_property       PACKAGE_PIN    D11           [get_ports "FMC_LPC_LA18_CC_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA18_CC_P"] ;
set_property       PACKAGE_PIN    C11           [get_ports "FMC_LPC_LA19_N"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA19_N"] ;
set_property       PACKAGE_PIN    D12           [get_ports "FMC_LPC_LA19_P"] ;
set_property       IOSTANDARD     LVDS          [get_ports "FMC_LPC_LA19_P"] ;
```

```
set_property      PACKAGE_PIN   E12          [get_ports "FMC_LPC_LA20_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA20_N"] ;
set_property      PACKAGE_PIN   F12          [get_ports "FMC_LPC_LA20_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA20_P"] ;
set_property      PACKAGE_PIN   A10          [get_ports "FMC_LPC_LA21_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA21_N"] ;
set_property      PACKAGE_PIN   B10          [get_ports "FMC_LPC_LA21_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA21_P"] ;
set_property      PACKAGE_PIN   H12          [get_ports "FMC_LPC_LA22_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA22_N"] ;
set_property      PACKAGE_PIN   H13          [get_ports "FMC_LPC_LA22_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA22_P"] ;
set_property      PACKAGE_PIN   A11          [get_ports "FMC_LPC_LA23_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA23_N"] ;
set_property      PACKAGE_PIN   B11          [get_ports "FMC_LPC_LA23_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA23_P"] ;
set_property      PACKAGE_PIN   A6           [get_ports "FMC_LPC_LA24_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA24_N"] ;
set_property      PACKAGE_PIN   B6           [get_ports "FMC_LPC_LA24_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA24_P"] ;
set_property      PACKAGE_PIN   C6           [get_ports "FMC_LPC_LA25_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA25_N"] ;
set_property      PACKAGE_PIN   C7           [get_ports "FMC_LPC_LA25_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA25_P"] ;
set_property      PACKAGE_PIN   B8           [get_ports "FMC_LPC_LA26_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA26_N"] ;
set_property      PACKAGE_PIN   B9           [get_ports "FMC_LPC_LA26_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA26_P"] ;
set_property      PACKAGE_PIN   A7           [get_ports "FMC_LPC_LA27_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA27_N"] ;
set_property      PACKAGE_PIN   A8           [get_ports "FMC_LPC_LA27_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA27_P"] ;
set_property      PACKAGE_PIN   L13          [get_ports "FMC_LPC_LA28_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA28_N"] ;
set_property      PACKAGE_PIN   M13          [get_ports "FMC_LPC_LA28_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "FMC_LPC_LA28_P"] ;
set_property      PACKAGE_PIN   J10          [get_ports "FMC_LPC_LA29_N"] ;
```

```
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA29_N"] ;
set_property      PACKAGE_PIN   K10           [get_ports "FMC_LPC_LA29_P"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA29_P"] ;
set_property      PACKAGE_PIN   D9            [get_ports "FMC_LPC_LA30_N"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA30_N"] ;
set_property      PACKAGE_PIN   E9            [get_ports "FMC_LPC_LA30_P"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA30_P"] ;
set_property      PACKAGE_PIN   E7            [get_ports "FMC_LPC_LA31_N"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA31_N"] ;
set_property      PACKAGE_PIN   F7            [get_ports "FMC_LPC_LA31_P"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA31_P"] ;
set_property      PACKAGE_PIN   E8            [get_ports "FMC_LPC_LA32_N"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA32_N"] ;
set_property      PACKAGE_PIN   F8            [get_ports "FMC_LPC_LA32_P"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA32_P"] ;
set_property      PACKAGE_PIN   C8            [get_ports "FMC_LPC_LA33_N"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA33_N"] ;
set_property      PACKAGE_PIN   C9            [get_ports "FMC_LPC_LA33_P"] ;
set_property      IOSTANDARD    LVDS          [get_ports "FMC_LPC_LA33_P"] ;

#HDMI
set_property      PACKAGE_PIN   AP3           [get_ports "HDMI_RX0_C_N"] ;
set_property      PACKAGE_PIN   AP4           [get_ports "HDMI_RX0_C_P"] ;
set_property      PACKAGE_PIN   AN1           [get_ports "HDMI_RX1_C_N"] ;
set_property      PACKAGE_PIN   AN2           [get_ports "HDMI_RX1_C_P"] ;
set_property      PACKAGE_PIN   AL1           [get_ports "HDMI_RX2_C_N"] ;
set_property      PACKAGE_PIN   AL2           [get_ports "HDMI_RX2_C_P"] ;
set_property      PACKAGE_PIN   AN5           [get_ports "HDMI_TX0_N"] ;
set_property      PACKAGE_PIN   AN6           [get_ports "HDMI_TX0_P"] ;
set_property      PACKAGE_PIN   AM3           [get_ports "HDMI_TX1_N"] ;
set_property      PACKAGE_PIN   AM4           [get_ports "HDMI_TX1_P"] ;
set_property      PACKAGE_PIN   AL5           [get_ports "HDMI_TX2_N"] ;
set_property      PACKAGE_PIN   AL6           [get_ports "HDMI_TX2_P"] ;
set_property      PACKAGE_PIN   AD7           [get_ports "HDMI_SI5324_OUT_C_N"];
set_property      PACKAGE_PIN   AD8           [get_ports "HDMI_SI5324_OUT_C_P"];
set_property      PACKAGE_PIN   F13           [get_ports "HDMI_REC_CLOCK_C_N"];
set_property      IOSTANDARD    LVDS          [get_ports "HDMI_REC_CLOCK_C_N"];
```

```
set_property      PACKAGE_PIN   G14          [get_ports "HDMI_REC_CLOCK_C_P"];
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_REC_CLOCK_C_P"];
set_property      PACKAGE_PIN   F21          [get_ports "HDMI_TX_LVDS_OUT_N"];
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_TX_LVDS_OUT_N"];
set_property      PACKAGE_PIN   G21          [get_ports "HDMI_TX_LVDS_OUT_P"];
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_TX_LVDS_OUT_P"];
set_property      PACKAGE_PIN    AC9         [get_ports "HDMI_RX_CLK_C_N"];
set_property      IOSTANDARD    AC10         [get_ports "HDMI_RX_CLK_C_P"];
set_property      PACKAGE_PIN   M8           [get_ports "HDMI_RX_PWR_DET"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_PWR_DET"];
set_property      PACKAGE_PIN   M10          [get_ports "HDMI_RX_HPD"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_HPD"];
set_property      PACKAGE_PIN   M9           [get_ports "HDMI_RX_SNK_SCL"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_SNK_SCL"];
set_property      PACKAGE_PIN   M11          [get_ports "HDMI_RX_SNK_SDA"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_SNK_SDA"];
set_property      PACKAGE_PIN   N11          [get_ports "HDMI_TX_EN"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_EN"];
set_property      PACKAGE_PIN   M12          [get_ports "HDMI_TX_CEC"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_CEC"];
set_property      PACKAGE_PIN   N13          [get_ports "HDMI_TX_HPD"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_HPD"];
set_property      PACKAGE_PIN   N8           [get_ports "HDMI_TX_SRC_SCL"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_SRC_SCL"];
set_property      PACKAGE_PIN   N9           [get_ports "HDMI_TX_SRC_SDA"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_SRC_SDA"];
set_property      PACKAGE_PIN   N12          [get_ports "HDMI_CTL_SCL"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_CTL_SCL"];
set_property      PACKAGE_PIN   P12          [get_ports "HDMI_CTL_SDA"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_CTL_SDA"];
set_property      PACKAGE_PIN   G8           [get_ports "HDMI_SI5324_LOL"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_SI5324_LOL"];
set_property      PACKAGE_PIN   H8           [get_ports "HDMI_SI5324_RST"];
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_SI5324_RST"];
```

```
# HDMI I/F (PL BANK 88 CONTROL, MGTH BANK 227 TX/RX + RX_CLK)
set_property      PACKAGE_PIN   F21          [get_ports "HDMI_TX_LVDS_OUT_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_TX_LVDS_OUT_N"] ;
set_property      PACKAGE_PIN   G21          [get_ports "HDMI_TX_LVDS_OUT_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_TX_LVDS_OUT_P"] ;
set_property      PACKAGE_PIN   E22          [get_ports "HDMI_REC_CLOCK_N"] ;
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_REC_CLOCK_N"] ;
set_property      PACKAGE_PIN   F22          [get_ports "HDMI_REC_CLOCK_P"] ;
set_property      IOSTANDARD    LVDS         [get_ports "HDMI_REC_CLOCK_P"] ;
set_property      PACKAGE_PIN   E5           [get_ports "HDMI_RX_PWR_DET"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_PWR_DET"] ;
set_property      PACKAGE_PIN   F6           [get_ports "HDMI_RX_HPD"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_HPD"] ;
set_property      PACKAGE_PIN   C2           [get_ports "HDMI_RX_LS_OE"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_LS_OE"] ;
set_property      PACKAGE_PIN   D2           [get_ports "HDMI_RX_SNK_SCL"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_SNK_SCL"] ;
set_property      PACKAGE_PIN   E2           [get_ports "HDMI_RX_SNK_SDA"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_RX_SNK_SDA"] ;
set_property      PACKAGE_PIN   E3           [get_ports "HDMI_TX_HPD"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_HPD"] ;
set_property      PACKAGE_PIN   A2           [get_ports "HDMI_TX_EN"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_EN"] ;
set_property      PACKAGE_PIN   A3           [get_ports "HDMI_TX_CEC"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_CEC"] ;
set_property      PACKAGE_PIN   B1           [get_ports "HDMI_TX_SRC_SCL"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_SRC_SCL"] ;
set_property      PACKAGE_PIN   C1           [get_ports "HDMI_TX_SRC_SDA"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_TX_SRC_SDA"] ;
set_property      PACKAGE_PIN   D1           [get_ports "HDMI_CTL_SCL"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_CTL_SCL"] ;
set_property      PACKAGE_PIN   E1           [get_ports "HDMI_CTL_SDA"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_CTL_SDA"] ;
set_property      PACKAGE_PIN   N11          [get_ports "HDMI_8T49N241_LOL"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_8T49N241_LOL"] ;
set_property      PACKAGE_PIN   M12          [get_ports "HDMI_8T49N241_RST"] ;
set_property      IOSTANDARD    LVCMOS33     [get_ports "HDMI_8T49N241_RST"] ;
```

```
set_property       PACKAGE_PIN    N13            [get_ports "HDMI_TX_LS_OE"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "HDMI_TX_LS_OE"] ;
set_property       PACKAGE_PIN    N8             [get_ports "HDMI_TX_CT_HPD"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "HDMI_TX_CT_HPD"] ;

# GPIO
# GPIO LED DS38/37/39/40 (ACTIVE HIGH) (PL BANK 88)
set_property       PACKAGE_PIN    D5             [get_ports "GPIO_LED_0_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_LED_0_LS"] ;
set_property       PACKAGE_PIN    D6             [get_ports "GPIO_LED_1_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_LED_1_LS"] ;
set_property       PACKAGE_PIN    A5             [get_ports "GPIO_LED_2_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_LED_2_LS"] ;
set_property       PACKAGE_PIN    B5             [get_ports "GPIO_LED_3_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_LED_3_LS"] ;

# GPIO 4-POLE DIP SW13 (ACTIVE HIGH) (PL BANK 88)
set_property       PACKAGE_PIN    F4             [get_ports "GPIO_DIP_SW3"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_DIP_SW3"] ;
set_property       PACKAGE_PIN    F5             [get_ports "GPIO_DIP_SW2"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_DIP_SW2"] ;
set_property       PACKAGE_PIN    D4             [get_ports "GPIO_DIP_SW1"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_DIP_SW1"] ;
set_property       PACKAGE_PIN    E4             [get_ports "GPIO_DIP_SW0"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_DIP_SW0"] ;

# GPIO PB SW14/15/17/18 (ACTIVE HIGH) (PL BANK 88)
set_property       PACKAGE_PIN    B4             [get_ports "GPIO_PB_SW0"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_PB_SW0"] ;
set_property       PACKAGE_PIN    C4             [get_ports "GPIO_PB_SW1"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_PB_SW1"] ;
set_property       PACKAGE_PIN    B3             [get_ports "GPIO_PB_SW2"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_PB_SW2"] ;
set_property       PACKAGE_PIN    C3             [get_ports "GPIO_PB_SW3"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "GPIO_PB_SW3"] ;
```

```
# GPIO PB SW20 ASSIGNED TO CPU_RESET (ACTIVE HIGH) (PL BANK 87)
set_property       PACKAGE_PIN    M11            [get_ports "CPU_RESET"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "CPU_RESET"] ;

# PMOD
# PMOD0 RT. ANGLE RECEPTACLE J55 2X6 (PL BANK 87)
set_property       PACKAGE_PIN    G8             [get_ports "PMOD0_0"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_0"] ;
set_property       PACKAGE_PIN    H8             [get_ports "PMOD0_1"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_1"] ;
set_property       PACKAGE_PIN    G7             [get_ports "PMOD0_2"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_2"] ;
set_property       PACKAGE_PIN    H7             [get_ports "PMOD0_3"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_3"] ;
set_property       PACKAGE_PIN    G6             [get_ports "PMOD0_4"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_4"] ;
set_property       PACKAGE_PIN    H6             [get_ports "PMOD0_5"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_5"] ;
set_property       PACKAGE_PIN    J6             [get_ports "PMOD0_6"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_6"] ;
set_property       PACKAGE_PIN    J7             [get_ports "PMOD0_7"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PMOD0_7"] ;

#I2CBUS
# PL I2C
set_property       PACKAGE_PIN    N12            [get_ports "PL_I2C1_SCL_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PL_I2C1_SCL_LS"] ;
set_property       PACKAGE_PIN    P12            [get_ports "PL_I2C1_SDA_LS"] ;
set_property       IOSTANDARD     LVCMOS33       [get_ports "PL_I2C1_SDA_LS"] ;

#USBUART
set_property       PACKAGE_PIN    A20            [get_ports "UART2_TXD_FPGA_RXD"] ;
set_property       IOSTANDARD     LVCMOS18       [get_ports "UART2_TXD_FPGA_RXD"] ;
set_property       PACKAGE_PIN    C19            [get_ports "UART2_RXD_FPGA_TXD"] ;
set_property       IOSTANDARD     LVCMOS18       [get_ports "UART2_RXD_FPGA_TXD"] ;
set_property       PACKAGE_PIN    C18            [get_ports "UART2_RTS_B"] ;
set_property       IOSTANDARD     LVCMOS18       [get_ports "UART2_RTS_B"] ;
```

```
set_property       PACKAGE_PIN    A19           [get_ports "UART2_CTS_B"] ;
set_property       IOSTANDARD     LVCMOS18      [get_ports "UART2_CTS_B"] ;

#PS GTR BANK 505
#Other net         PACKAGE_PIN    U29           GT0_DP_TX_P
#Other net         PACKAGE_PIN    U30           GT0_DP_TX_N
#Other net         PACKAGE_PIN    R29           GT1_DP_TX_P
#Other net         PACKAGE_PIN    R30           GT1_DP_TX_N
#Other net         PACKAGE_PIN    P31           GT2_USB0_TX_P
#Other net         PACKAGE_PIN    P32           GT2_USB0_TX_N
#Other net         PACKAGE_PIN    R33           GT2_USB0_RX_P
#Other net         PACKAGE_PIN    R34           GT2_USB0_RX_N
#Other net         PACKAGE_PIN    N29           GT3_SATA1_TX_P
#Other net         PACKAGE_PIN    N30           GT3_SATA1_TX_N
#Other net         PACKAGE_PIN    N33           GT3_SATA1_RX_P
#Other net         PACKAGE_PIN    N34           GT3_SATA1_RX_N
#Other net         PACKAGE_PIN    P27           GTR_REF_CLK_SATA_C_P
#Other net         PACKAGE_PIN    P28           GTR_REF_CLK_SATA_C_N
#Other net         PACKAGE_PIN    M27           GTR_REF_CLK_USB3_C_P
#Other net         PACKAGE_PIN    M28           GTR_REF_CLK_USB3_C_N
#Other net         PACKAGE_PIN    M31           GTR_REF_CLK_DP_C_P
#Other net         PACKAGE_PIN    M32           GTR_REF_CLK_DP_C_N
```

Appendix C

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the ZCU104 board and its documentation is available on the ZCU104 Evaluation Kit website.

These Xilinx documents provide supplemental material useful with this guide:

1. *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891)
2. *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085)
3. *UltraScale Architecture PCB Design User Guide* (UG583)
4. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
5. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
6. *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
7. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
8. *Tera Term Terminal Emulator Installation Guide* (UG1036)
9. *Vivado Design Suite User Guide: Using Constraints* (UG903)

The following websites provide supplemental material useful with this guide:

10. Micron Technology: www.micron.com

    (MT40A256M16GE-075E, MT25QU512ABB8ESF-0SIT data sheets)

11. Standard Microsystems Corporation (SMSC): www.microchip.com

    (USB3320 data sheet)

12. SanDisk Corporation: www.sandisk.com
13. SD Association: www.sdcard.org
14. Silicon Labs: www.silabs.com/Pages/default.aspx

    (SI5341B, Si570, Si5319C, Si53340, CP2108 data sheets)

15. Texas Instruments: www.ti.com/product/DP83867IR

    (TI DP83867 data sheet)

16. PCI: https://pcisig.com/specifications/pciexpress/M.2_Specification/
17. Maxim Integrated Circuits: https://www.maximintegrated.com
18. VITA FMC Marketing Alliance: www.vita.com/fmc

19. Digilent: www.digilentinc.com
(Pmod peripheral modules)

20. Integrated Device Technology (IDT): www.idt.com
(8T49N241, 8T49N287 data sheets)

21. Infineon Technologies: https://www.infineon.com/
(IRPS5401 data sheet)

22. Future Technology Devices International Ltd.: www.ftdichip.com
(FT2232H data sheet)

Please Read: Important Legal Notices