FEATURES

- **Differential D, clock and Q**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **V_{BB} output for single-ended use**
- **1100MHz min. toggle frequency**
- **Edge-triggered asynchronous set and reset**
- **Fully compatible with Motorola MC10E/100E431**
- **Available in 28-pin PLCC package**

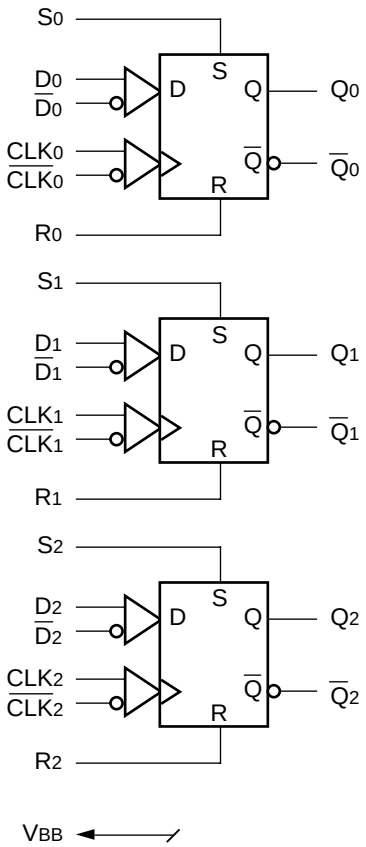
DESCRIPTION

The SY10/100E431 are 3-bit flip-flops with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduces the metastability susceptibility window.

BLOCK DIAGRAM



PIN NAMES

Pin	Function
D[0:2], $\overline{D}$[0:2]	Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0:2]	Differential Clock Inputs
S[0:2]	Edge Triggered Set Inputs
R[0:2]	Edge Triggered Reset Inputs
V_{BB}	V_{BB} Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs
V_{CCO}	V_{CC} to Output

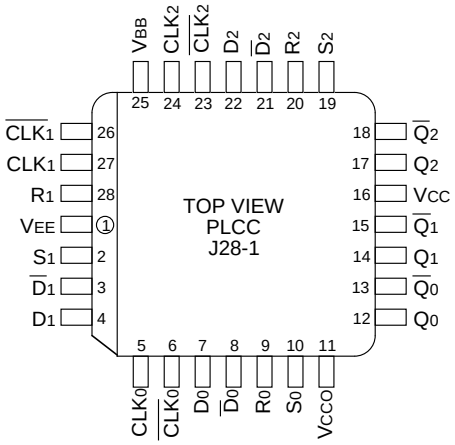
TRUTH TABLE(1)

D_n	CLK_n	R_n	S_n	Q_n
L	Z	L	L	L
H	Z	L	L	H
X	L	Z	L	L
X	L	L	Z	H

NOTE:

1. Z = LOW-to-HIGH transition.

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E431JC	J28-1	Commercial	SY10E431JC	Sn-Pb
SY10E431JCTR[2]	J28-1	Commercial	SY10E431JC	Sn-Pb
SY100E431JC	J28-1	Commercial	SY100E431JC	Sn-Pb
SY100E431JCTR[2]	J28-1	Commercial	SY100E431JC	Sn-Pb
SY10E431JZ[3]	J28-1	Commercial	SY10E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E431JZTR[2, 3]	J28-1	Commercial	SY10E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E431JZ[3]	J28-1	Commercial	SY100E431JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E431JZTR[2, 3]	J28-1	Commercial	SY100E431JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		
V_{CMR}	Common Mode Range	–1.5	—	0	–1.5	—	0	–1.5	—	0	V	1

Notes:

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

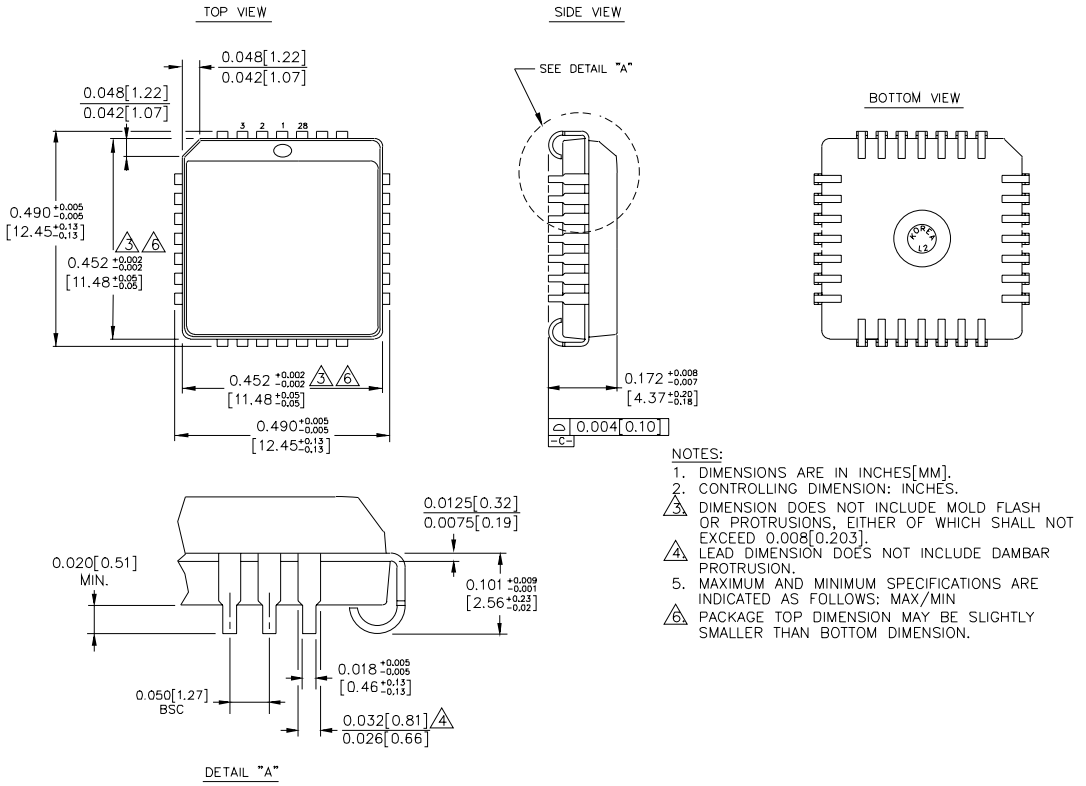
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PD}	Propagation Delay to Output										ps	—
	CLK (Diff)	450	600	750	450	600	750	450	600	750		
	CLK (SE)	400	600	800	400	600	800	400	600	800		
	R	550	725	925	550	725	925	550	725	925		
	S	550	725	925	550	725	925	550	725	925		
t_S	Set-up Time										ps	
	D	200	0	—	200	0	—	200	0	—		
	R	1000	700	—	1000	700	—	1000	700	—		1
	S	1000	700	—	1000	700	—	1000	700	—		1
t_H	Hold Time, D	200	0	—	200	0	—	200	0	—	ps	—
t_{PW}	Minimum Pulse Width, CLK	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	2
$V_{PP\ (AC)}$	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	3
t_r t_f	Rise/Fall Time 20% to 80%	275	450	650	275	450	650	275	450	650	ps	—

Notes:

1. These set-up times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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