# Si8250/1/2

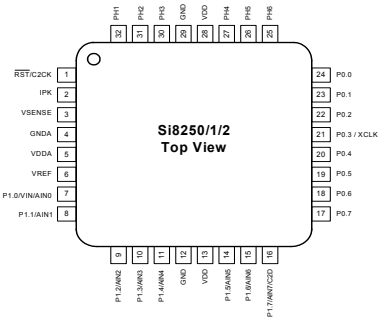
# DIGITAL POWER CONTROLLER

## Features

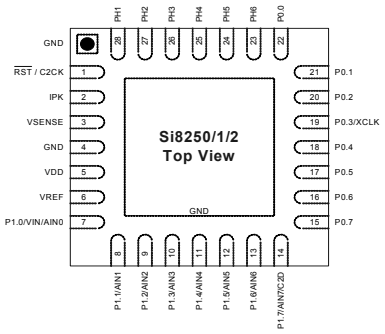
- Single-chip, Flash-based digital power controller
  - Supports isolated and non-isolated applications
  - Enables new system capabilities such as:
    - Adaptive dead-time control for higher efficiency
    - Nonlinear control for faster transient response
    - Self diagnostics for higher reliability
    - SMBus port
- Highly-integrated control solution:
  - High-speed digital hardware control loop
  - In-system programmable supervisory processor
  - Programmable system protection functions
  - Hardware cycle-by-cycle current limiting and OCP
  - External clock and frame synchronization inputs
  - Performs system management functions, such as external power supply sequencing and fan control/monitoring
- In-system Flash programmable
  - Flash can also be used as NV memory for data storage
- Low-cost, comprehensive development tool kit includes:
  - Graphical, easy-to-use system design tools
  - Integrated development environment
  - In-system, on-line debugger
  - Turnkey isolated 35 W digital half-bridge target board
- Typical Applications
  - Isolated and non-isolated DC/DC converters
  - AC/DC converters
- Fully Pb-free and ROHS compliant packages
  - 32-pin LQFP
  - 28-pin 5x5 mm QFN
- Temp Range: –40 to +125 °C

**Pin Assignments:**
**See page 23**

**32-pin LQFP**




**28-pin QFN**




Patents pending

## Description

The Si8250/1/2 provides all control and protection functions necessary to implement highly-intelligent, fast-response power delivery and management control systems for isolated and non-isolated power supplies. Onboard processing capability enables intelligent control optimization for improved system performance and new capabilities, such as serial connectivity via the SMBus or onboard UART. The Si8250/1/2 family is in-system Flash programmable, enabling control and protection parameters, such as system regulation and protection settings, startup and shutdown modes, loop response, and modulation timing, to be readily modified. The built-in, high-speed control path provides loop updates every 100 ns and provides pulse-by-pulse current limiting and overcurrent protection, even while the internal CPU is disabled.

The Si825x family is supported by the Si8250DK development kit, which contains everything required to develop and program power supply applications with the Si825x family of digital controllers.

# TABLE OF CONTENTS

# 1. Electrical Specifications

**Table 1. Absolute Maximum Ratings***

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Ambient temperature under bias | | –55 | — | +135 | °C |
| Storage temperature | | –65 | — | +150 | °C |
| Voltage on any Port0 Pin with respect to GND | | –0.3 | — | 5.5 | V |
| Voltage on all other pins with respect to GND | | –0.3 | — | 4.0 | V |
| Voltage on $V_{DD}$ with respect to GND | | –0.3 | — | 4.0 | V |
| Maximum total current through $V_{DD}$ or GND | | — | — | 400 | mA |
| Maximum output current sunk by $\overline{RST}$ or any port pin | | — | — | 80 | mA |

***Note:** Stresses above those listed in this table may cause permanent device damage. This is a stress rating only, and functional operation of the devices at those or any conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 2. DC Electrical Specifications**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply voltage | | 2.25 | — | 2.75 | V |
| Supply current (all peripherals enabled) | Analog + Digital Supply Current. | — | 26 | — | mA |
| Lockout mode supply current | Analog + Digital Supply Current. (See Table 1) | — | 300 | — | µA |
| Digital supply current (shutdown) | Oscillator not running, $V_{DD}$ monitor disabled | — | — | 500 | µA |
| Digital supply RAM data retention voltage | | — | 1.5 | — | V |

**Table 3. Reference DAC Electrical Specifications**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Resolution | | — | — | 9 | Bits |
| LSB size | | — | 2.44 | — | mV |
| Integral nonlinearity (INL) | | –2 | — | +2 | LSB |
| Differential nonlinearity (DNL) | | –1.0 | — | +1.0 | LSB |
| Settling time | 1/2 LSB change from 0 to full scale | — | 2 | — | µs |
| Turn-on time | | — | 20 | — | µs |
| Noise | 2 MHz BW | — | 1 | — | $mV_{PP}$ |
| Power supply rejection | | — | 70 | — | db |
| Supply current | | — | 220 | — | µA |
| Shutdown supply current | | — | 0.1 | — | µA |

### Table 4. ADC0 (12-Bit ADC) Specifications

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **DC Accuracy** | | | | | |
| Resolution | | — | 12 | — | bits |
| Integral nonlinearity | | — | — | ±2 | LSB |
| Differential nonlinearity | Guaranteed Monotonic | — | — | ±1 | LSB |
| Offset error | | — | ±3 | — | LSB |
| Full scale error | Differential Mode | — | 3 | — | LSB |
| Offset temperature coefficient | | — | 13600 | — | ppm/°C |
| **Dynamic Performance (10 kHz sine-wave Single-ended input, 0 to 1 dB below Full Scale, 200 ksps)** | | | | | |
| Signal-to-noise plus distortion | | — | 64 | — | dB |
| Total harmonic distortion | Up to the 5th harmonic | — | 83 | — | dB |
| Spurious-free dynamic range | | — | –73 | — | dB |
| **Conversion Rate** | | | | | |
| Conversion time in SAR clocks | Note 1 | — | 13 | — | clocks |
| Track/Hold acquisition time | Note 2 | 1 | — | — | µs |
| Throughput rate | | — | — | 200 | ksps |
| **Analog Inputs** | | | | | |
| Input voltage range | | 0 | — | $V_{REF}$ | V |
| Input capacitance | | — | 15 | — | pF |
| **Temperature Sensor** | | | | | |
| Linearity | Notes 3, 4 | — | ±0.2 | — | °C |
| Gain | Notes 3, 4 | — | 1353 | — | µV/°C |
| Offset | Notes 3, 4 (Temp = 0 °C) | — | 488 | — | mV |
| **Power Specifications** | | | | | |
| Power supply current ($V_{DD}$ supplied to ADC0) | Operating Mode, 200 ksps | — | 780 | — | µA |
| Power-on time | After $V_{REF}$ settle, before tracking begins | — | 5 | — | µs |
| Power supply rejection | | — | 0.7 | — | mV/V |

**Notes:**
1. An additional two $F_{CLK}$ cycles are required to start and complete a conversion.
2. Additional tracking time may be required depending on the output impedance connected to the ADC input.
3. Represents one standard deviation from the mean.
4. Includes ADC offset, gain, and linearity variations.

### Table 5. ADC1 Specifications

TA = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Sampling frequency | ADCSP1 = 0<br>ADCSP2 = 0 | — | 10 | — | Msps |
| | ADCSP1 = 1<br>ADCSP2 = 0 | — | 5 | — | |
| | ADCSP1 = 0<br>ADCSP2 = 1 | — | 2.5 | — | |
| | ADCSP1 = 1<br>ADCSP2 = 1 | — | 1.25 | — | |
| Resolution | | — | — | 6 | Bits |
| LSB size | | 4 | — | 20 | mV |
| Differential input voltage range | * | –32 | — | +31 | LSB |
| Common-mode input voltage range | | 0.8 | — | 1.3 | V |
| Integral nonlinearity | | –2 | — | +2 | LSB |
| Differential nonlinearity | | –1 | — | +1 | LSB |
| Gain error | | — | 5 | — | % |
| Offset error | | — | 3 | — | mV |
| Input bias current | | — | 5 | — | µA |
| Standby mode supply current | Disabled | — | 0.1 | — | µA |
| Operating mode supply current | | — | — | 3 | mA |

***Note:** LSB size (mV) is programmable using the RES[3:0] bits in the ADC1CN register.

### Table 6. DSP Filter Engine Electrical Specifications

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Resolution[1] | | — | — | 9 | Bits |
| Dithering[2] | | — | — | 6 | Bits |
| Standby mode supply current | Disabled | — | 0.1 | — | µA |

**Notes:**
1. Internal word length = 22 bits.
2. Up to a total 15 bits of resolution when dithering is enabled.

**Table 7. Peak Current Limit Detector Electrical Specifications**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| IPK input to DPWM output latency | 10 mV Overdrive | — | 45 | — | ns |
| Threshold detector voltage | VT[3:0] = 0000 | 35 | 50 | 65 | mV |
| | VT[3:0] = 0001 | 85 | 100 | 115 | |
| | VT[3:0] = 0010 | 135 | 150 | 165 | |
| | VT[3:0] = 0011 | 185 | 200 | 215 | |
| | VT[3:0] = 0100 | 235 | 250 | 265 | |
| | VT[3:0] = 0101 | 285 | 300 | 315 | |
| | VT[3:0] = 0110 | 335 | 350 | 365 | |
| | VT[3:0] = 0111 | 485 | 400 | 415 | |
| | VT[3:0] = 1000 | 435 | 450 | 465 | |
| | VT[3:0] = 1001 | 485 | 500 | 515 | |
| | VT[3:0] = 1010 | 535 | 550 | 565 | |
| | VT[3:0] = 1011 | 585 | 600 | 615 | |
| | VT[3:0] = 1100 | 635 | 650 | 665 | |
| | VT[3:0] = 1101 | 685 | 700 | 715 | |
| | VT[3:0] = 1110 | 735 | 750 | 765 | |
| | VT[3:0] = 1111 | 785 | 800 | 815 | |
| Hysteresis | HYST[1:0] = 00 | — | 0 | — | mV |
| | HYST[1:0] = 01 | — | 5 | — | |
| | HYST[1:0] = 10 | — | 10 | — | |
| | HYST[1:0] = 11 | — | 20 | — | |
| Blanking time | LEB[1:0] = 00, $f_{PLL}$ = 200 MHz | — | 0 | — | ns |
| | LEB[1:0] = 01, $f_{PLL}$ = 200 MHz | — | 20 | — | |
| | LEB[1:0] = 10, $f_{PLL}$ = 200 MHz | — | 40 | — | |
| | LEB[1:0] = 11, $f_{PLL}$ = 200 MHz | — | 80 | — | |
| Input capacitance | | — | 4.5 | — | pF |
| Input bias current | | — | 0.1 | — | µA |
| Shutdown supply current | Enable bit = 0 | — | 0.1 | — | µA |
| Active supply current | IIN = (Vt + 100 mVpp), 1.5 MHz square wave | — | 100 | — | µA |

**Table 8. DPWM Specifications**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Clock frequency | DPWMSP[4:3] = 00 | — | — | 200 | MHz |
| | DPWMSP[4:3] = 01 | — | — | 50 | |
| | DPWMSP[4:3] = 1x | — | — | 25 | |
| Resolution | No dithering | — | — | 9 | Bits |
| | Dithering enabled | — | — | 15 | |
| Time resolution | DPWMSP[4:3] = 00 | 5 | — | — | ns |
| | DPWMSP[4:3] = 01 | 20 | — | — | |
| | DPWMSP[4:3] = 1x | 40 | — | — | |
| SYNC pulse set-up time | SYNC signal minimum LOW time before positive transition | 3 | — | — | DPWM Clock Cycles |
| PH rise, fall time | 50 pF on pin | — | — | 5 | ns |
| Output resistance high | $I_{OUT}$ = –5 mA | — | 75 | — | Ω |
| Output resistance low | $I_{OUT}$ = 8 mA | — | 40 | — | Ω |
| Shutdown supply current | | — | — | 0.1 | µA |

**Table 9. Bandgap Voltage Reference Specs**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output voltage | | — | 1.20 | — | V |
| Temperature stability | | –1 | — | +1 | % |
| Turn-on response | (0.01%, 4.7 µF) | — | 6.5 | — | ms |
| | no load | — | 2 | — | µs |
| Noise | 4.7 µF | — | 2 | — | µV (RMS) |
| Bandgap current | | — | 60 | — | µA |
| Reference buffer current | | — | 30 | — | µA |
| Power supply rejection | | — | 50 | — | dB |

**Table 10. Comparator0 Specifications**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IN}$ | | 0 | — | $V_{DD}$ | V |
| Low-speed supply current | | — | 8 | — | µA |
| Full-speed supply current | | — | 225 | — | µA |
| Hysteresis | CP0HYP[1:0] = 00 | — | 0 | — | mV |
| | CP0HYP[1:0] = 01 | — | 7 | — | |
| | CP0HYP[1:0] = 10 | — | 14 | — | |
| | CP0HYP[1:0] = 11 | — | 28 | — | |
| | CP0HYN[1:0] = 00 | — | 0 | — | |
| | CP0HYN[1:0] = 01 | — | –7 | — | |
| | CP0HYN[1:0] = 10 | — | –14 | — | |
| | CP0HYN[1:0] = 11 | — | –28 | — | |
| Response time | Low power mode, 25 mv overdrive | — | 180 | — | ns |
| | High-speed mode, 25 mv overdrive | — | 25 | — | |
| Input capacitance | | — | 5 | — | pF |
| CMRR | | — | 50 | — | db |
| Input offset | | — | 5 | — | mV |

**Table 11. Reset Electrical Characteristics**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $\overline{RST}$ output low voltage | $I_{OL}$ = 8.5 mA, $V_{DD}$ = 2.5 V | — | — | 0.7 | V |
| $\overline{RST}$ input high voltage | | 0.7 x $V_{DD}$ | — | — | V |
| $\overline{RST}$ input low voltage | | — | — | 0.3 x $V_{DD}$ | V |
| $\overline{RST}$ input pull-up current | $\overline{RST}$ = 0.0 | — | 25 | 45 | µA |
| $V_{DD}$ POR threshold | | 2.0 | 2.1 | 2.2 | V |
| Missing clock detector timeout | Time from last system clock rising edge to start of reset | — | 250 | 650 | µs |
| Reset time delay | Delay between release of any reset source and code execution at location 0x0000 | 5.0 | — | — | µs |
| Minimum $\overline{RST}$ low time to generate a System Reset | | 6.5 | — | — | µs |
| $V_{DD}$ monitor turn-on time | | 100 | — | — | µs |
| $V_{DD}$ monitor supply current | | — | 40 | — | µA |

**Table 12. Flash Electrical Characteristics**

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.25 to 2.75 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Flash size | Si8250 | 32768* | — | — | bytes |
| | Si8251, Si8252 | 16384* | — | — | |
| Endurance | | 10 k | 100 k | — | Erase/Write |
| Read cycle time | | 40 | — | — | ns |
| Erase cycle time | 50 MHz system clock | 32 | — | 48 | ms |
| Write cycle time | 50 MHz system clock | 76 | — | 114 | µs |

***Note:** The last 512 bytes of memory are reserved.

### Table 13. Port I/O DC Electrical Characteristics

$T_A$ = –40 to +125 °C, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Port0 input voltage tolerance | push-pull | — | — | $V_{DD}$ + 0.7 | V |
| | open-drain | — | — | 5.5 | |
| Port1 input voltage tolerance | | — | — | $V_{DD}$ + 0.7 | |
| Output high voltage | $I_{OH}$ = –3 mA, Port I/O push-pull | $V_{DD}$ – 0.4 | — | — | V |
| | $I_{OH}$ = –10 µA, Port I/O push-pull | $V_{DD}$ – 0.1 | — | — | |
| | $I_{OH}$ = –10 mA, Port I/O push-pull | — | $V_{DD}$ – 0.8 | — | |
| Output low voltage | $I_{OL}$ = 8.5 mA | — | — | 0.6 | V |
| | $I_{OL}$ = 10 µA | — | — | 0.1 | |
| | $I_{OL}$ = 25 mA | — | 1.25 | — | |
| Input high voltage | | (0.7) $V_{DD}$ | — | — | V |
| Input low voltage | | — | — | (0.3) $V_{DD}$ | V |
| Input leakage current | Weak Pullup Off | — | — | ±10 | µA |
| | Weak Pullup On, $V_{IN}$ = 0 V | — | 20 | 50 | |

### Table 14. PLL Specifications

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Stabilization time | | — | 30 | — | µs |
| Input frequency range | | 15 | — | 25 | MHz |
| PLL frequency | | — | 200 | — | MHz |
| Cycle-to-cycle jitter | | — | 250 | — | ps |
| Supply current | | — | 15 | — | mA |
| Shutdown current | | — | 0.1 | — | µA |

### Table 15. 25MHz Oscillator Specifications

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Frequency | | 24 | 24.5 | 25 | MHz |
| Start-up time | | — | 100 | — | µs |
| Power supply sensitivity | | — | 0.3 | — | %/V |
| Temperature coefficient | | — | 50 | — | PPM/°C |
| Supply current | | — | 450 | — | µA |
| Shutdown current | | — | 0.1 | — | µA |

### Table 16. Low Frequency Oscillator (LFO) Specifications

$T_A$ = –40 to +125 °C, $V_{DD}$ = 2.5 V, SYSCLK = 25 MHz, PLLCLK = 200 MHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Frequency | | — | 80 | — | kHz |
| Start-up time | | — | 100 | — | µs |
| Power supply sensitivity | | — | 1.7 | — | %/V |
| Temperature coefficient | | — | 1000 | — | PPM/°C |
| Supply current | | — | 4 | — | µA |
| Shutdown current | | — | 0.1 | — | µA |

## 2. Benefits of Digital Power Control

Digitally-controlled power systems have the following key advantages over analog implementations:

- In-system programmability: Virtually all aspects of digital controller behavior can be changed in software locally or remotely and without hardware modification. This benefits the system in several ways:
  - Hardware designs can be segregated into base platforms (for example, by form factor or output power), and optimized to the end application in software. This lowers development costs by reducing the total number of hardware designs required to address a given application segment.
  - The controller's ability to readily accept changes enables low-cost, custom power supply versions with relatively short lead-times.
  - The cost and risk of field configuration and/or updating is greatly reduced, lowering the overhead associated with customer support.
- More advanced control algorithms: Power supply design with fixed-function analog components leads to many performance trade-offs. For example, analog compensator design routinely trades stability for higher loop bandwidth and places the required poles and zeros using passive components. The "if-then-else" decision-making capability of digital control can change loop bandwidth as needed for optimum control response. For example, the controller can operate the compensator at a relatively low bandwidth during steady-state operation, but significantly extend bandwidth during a transient. This adaptive response concept can be applied to improve other operating parameters, such as efficiency.
- Power Efficiency Optimization: In a switched mode power supply, it is desirable to maintain high power efficiency over a wide range of loads. Software algorithms can optimize efficiency at every point of line and load. For example, the software can adjust dead time with changing load, disable synchronous rectification at low loads, or take other measures to maximize efficiency.
- Higher operating precision: Switch timing, control response, and protection setting thresholds in analog systems are typically determined by the values of external passive components. These components typically have a wide tolerance and vary with temperature and time. Designers must allow for these tolerances when considering worst-case operating conditions. Digital control offers tighter parameter tolerances with greatly reduced temperature/time variations, resulting in improved worst-case operating specifications.
- Power management and power delivery functions in a single package: Power management functions, such as external supply sequencing and fan control can be performed by the digital controller, eliminating dedicated external components.
- System connectivity: Communication protocols enable system processors to communicate with the power supply to obtain data and command action. For example, the system processor may request the power supply operating history, perform self-diagnostics, or change system settings without taking the supply off-line. Communication with the system controller enables notification of a pending power supply failure, enhancing system reliability. This attribute also reduces the cost and complexity of field configurations and upgrades.
- Higher integration/smaller size/lower cost: Many discrete circuits can be transformed to lines of software code, eliminating components and lowering cost. The digital controller can be used to execute self-diagnostic routines during production test, thereby reducing test time and lowering cost. The small physical size of the Si8250 in particular (5 x 5 mm) saves board space.

# 3. Product Description

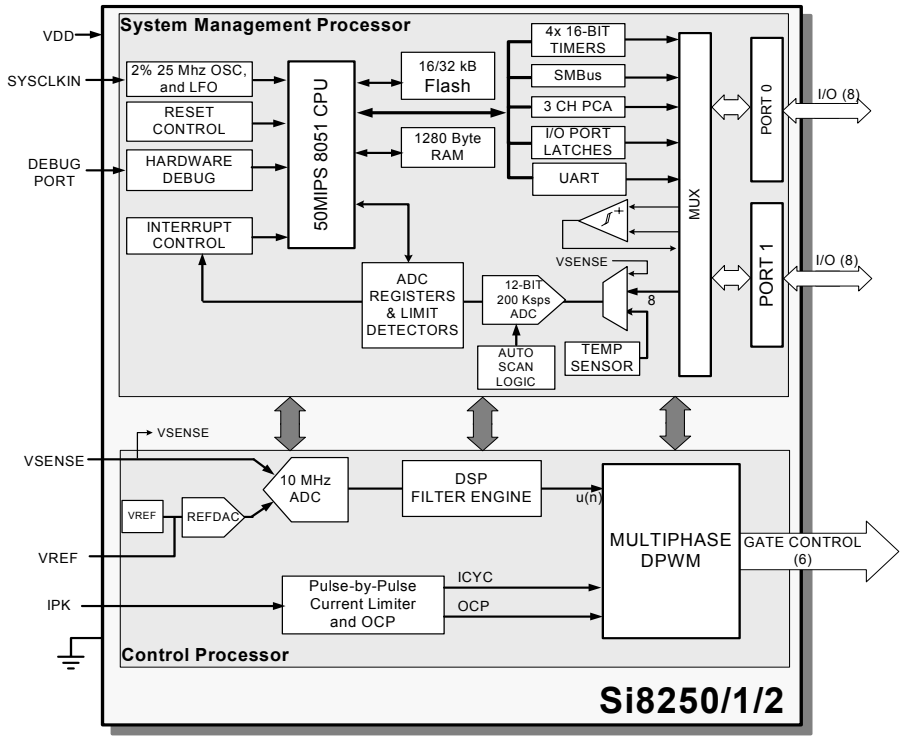



**Figure 1. Functional Block Diagram**

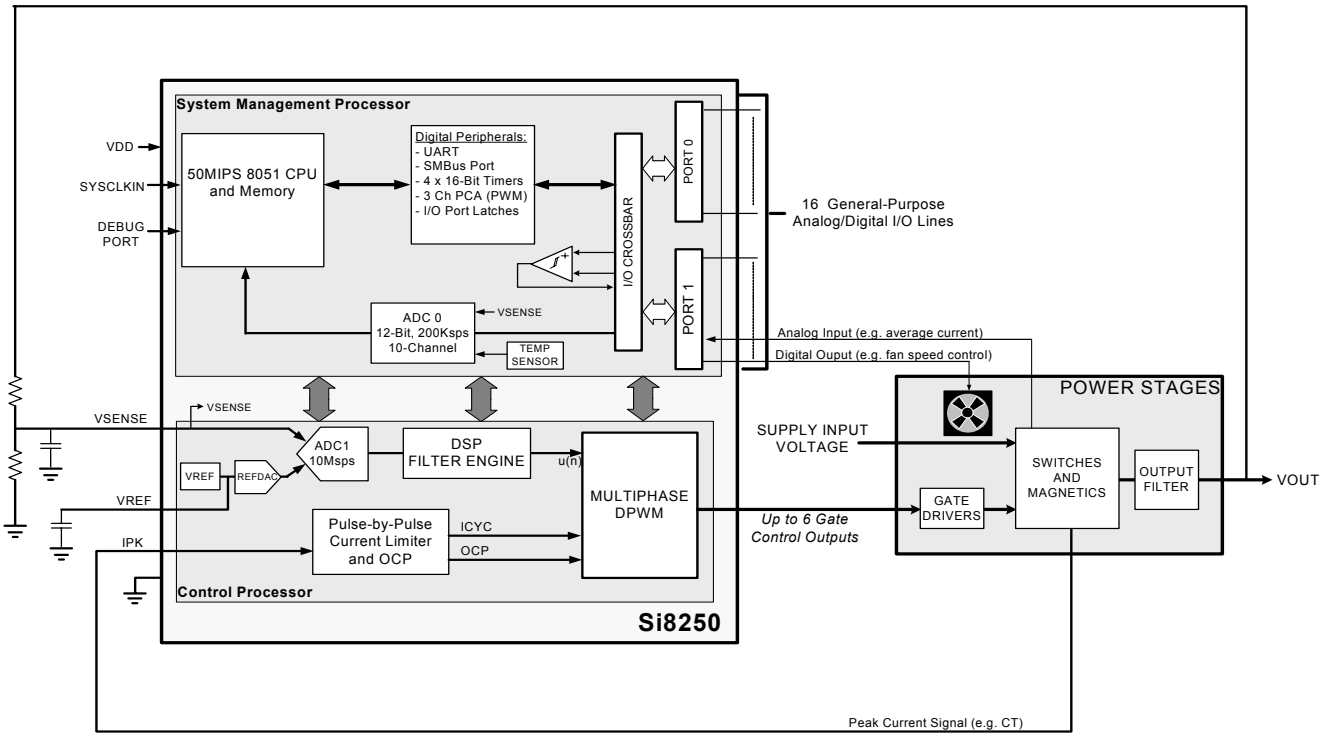



**Figure 2. Si8250 Top-Level Block Diagram**

## 3.1. System Operation

Figure 2 shows the Si8250/1/2 controlling a non-isolated dc/dc converter operating in digital voltage mode control. The output voltage signal connects to the $V_{SENSE}$ input through a resistive divider, limiting the common-mode voltage range applied to ADC1 to a maximum of $V_{REF}$. The equivalent resistance of the divider and the capacitor form an anti-aliasing filter with a cutoff frequency equal to ADC1 sampling frequency divided by 2 (the amplitudes of frequencies above fS/2 must be minimized to prevent aliasing).

Differential ADC1 and the DSP Filter Engine together perform the same function as an analog error amplifier and associated RC compensation network. ADC1 digitizes the difference between the scaled output voltage and a programmable reference voltage provided by the REFDAC. The ADC1 output signal is frequency-compensated (in the digital domain) by the DSP Filter Engine. The resulting output from the DSP Filter Engine is a digital code that represents the compensated duty cycle ratio, u(n). The digital PWM generator (DPWM) directly varies output timing to the external gate drivers based on the value of u(n) until the difference between $V_{SENSE}$ and the ADC1 reference level is driven to zero.

Sensing circuitry within the power stages (current transformer, sense amp, etc.) provides a signal representative of inductor or transformer current. This signal connects to the pulse-by-pulse current-limiting hardware in the Si8250/1/2 via the IPK input pin. This current-limiting circuitry is similar to that found in a voltage mode analog PWM. It contains a fast analog comparator and a programmable leading-edge blanking circuit to prevent unwanted tripping of the current-sensing circuitry on the leading edge of the current pulse. Current limiting occurs when the sensed current exceeds the programmed threshold. When this occurs, the ongoing active portions of the PWM outputs are terminated. A programmable OCP counter keeps track of the number of consecutive current limit cycles and automatically shuts the supply down when the accumulated number of limit cycles exceeds the programmed maximum.

The System Management Processor is based on a 50 million instruction per second (MIPS) 8051 CPU and dedicated A/D converter (ADC0). ADC0 digitizes key analog parameters that are used by the MCU to provide protection and manage and control other aspects of the power system. Onboard digital peripherals include timers, an SMBus interface port, and a universal asynchronous receiver/transmitter (UART) for serial communications (useful for communicating across an isolation boundary).

The System Management Processor serves several purposes:

1. Continuously optimizes Control Processor operation (e.g. efficient optimization)
2. Executes user-specific algorithms (e.g. support for proprietary system interfaces)
3. Provides regulation for low-bandwidth system variables (e.g. $V_{IN}$ feed-forward)
4. Performs system fault detection and recovery
5. Provides system housekeeping functions, such as SMBus communication support
6. Manages external device functions (e.g. external supply sequencing, fan control/monitoring)

Si8250/1/2 system development requires using the Si8250DK, a comprehensive development kit providing all required hardware and software for control system design. It comes complete with prewritten and verified application software and a set of tools that enable the user to adapt this software to the end application. It also includes a turnkey isolated half-bridge dc/dc converter based on the Si8250/1/2 for evaluation and experimentation.

## 3.2. Control Processor Functional Block Descriptions (Figure 1)

### 3.2.1. ADC 1

Differential input, 10 Msps control loop analog-to-digital converter. ADC1 digitizes the difference between the $V_{SENSE}$ input and the programmable voltage reference level from the REFDAC. ADC1 can be operated at 1.25, 2.5, 5, or 10 Msps and has a programmable LSB size to prevent limit cycle oscillation (Limit cycle oscillation can also be avoided using dithering to increase DPWM resolution). ADC1 has programmable conversion rates of 1.25, 2.5, 5, or 10 Msps to accommodate a wide loop gain range. ADC1 also contains a hardware transient detector that interrupts the CPU at the onset of an output load or unload transient. The CPU responds by executing specific algorithms to accelerate output recovery. These algorithms may include increasing loop bandwidth or other measures.

### 3.2.2. REFDAC

9-bit digital-to-analog converter provides the output voltage reference setting. The REFDAC uses the onboard band gap as its voltage reference, or it can be referenced to an external voltage reference source. REFDAC is used for output voltage calibration, margining, and positioning. The CPU continuously manages the REFDAC during soft-start and soft-stop.

### 3.2.3. DSP Filter Engine

This two-stage loop compensation filter is the functional equivalent of an active RC compensation in an analog

control scheme. The first filter stage is a PID filter providing one pole and two zeros. The second stage is selectable: a two-pole, low-pass filter (LPF) for the fastest possible response, or a SINC (multiple zero) decimation filter for quieter operation. The PID plus the LPF result in a three-pole, two-zero composite filter, while the PID plus the SINC results in a single-pole, multiple-zero composite filter. The SINC filter provides zeros at intervals equal to $f_S/(2*DEC)$ where DEC is the decimation ratio (i.e. ratio of input to output sampling rate). DEC is a software-programmable parameter and can be programmed such that zero placement occurs at the PWM frequency and its harmonics. This creates more than 100 dB attenuation at these frequencies providing lower system noise levels. The end-to-end response of the filter is defined using only six software parameters and can be reprogrammed during converter operation to implement nonlinear control response for improved transient resolution.

As described in the ADC1 section above, limit cycle oscillation can be avoided by increasing ADC1 LSB size to allow the DPWM LSB to fit within a single ADC1 output code (i.e. zero-error bin). However in some applications, it may not be desirable to lower ADC1 sensitivity. For such applications, limit cycle oscillation can be avoided by dithering the DPWM output. The DSP Filter Engine contains a pseudo-random, broadband noise generator - mixing this noise into the filter output randomly moves the gate control output(s) over a range of 1 LSB, such that the time-averaged resolution of the DPWM is increased.

The filter response is programmed using S-domain design tools included in the Si8250DK development kit, greatly minimizing software writing tasks.

#### 3.2.4. Pulse-by-pulse Current Limiter/OCP

High-speed comparator with 4-bit DAC threshold generator and 2-bit programmable leading-edge blanking delay generator. The comparator output causes the DPWM to terminate the on-going portions of the active outputs when the peak current signal applied to the IPK input exceeds the threshold setting. Hardware performs an OCP supply shutdown when the number of consecutive current limit events equals a programmed maximum.

#### 3.2.5. DPWM

Output generator may be programmed for pulse width (PWM) or phase-shift modulation using design tools contained in the Si8250DK design kit. The DPWM may be modulated by the front-end of the Control Processor (ADC1 and DSP Filter Engine); or by the CPU. The DPWM has individually programmable stop states for supply off (disable) and OCP. Software bypass mode allows the CPU to force selected outputs high or low while the remaining outputs continue normal operation. The DPWM includes an external SYNC input and ENABLE input, both of which can be connected to the I/O pins. The Enable is a logic input used to turn the power supply on and off. It can be configured to be active high or active low. The SYNC input allows the start of each switching cycle to be synchronized to an external clock source, including another Si8250/1/2.

## 3.3. System Management Processor Functional Block Descriptions

#### 3.3.1. ADC0

Self-sequencing, 10-input, 200 Ksps analog-to-digital converter. This general-purpose ADC acquires other analog system parameters for supplemental control by the CPU (e.g. dead time control using average input current as the control variable). ADC0 also converts the output of the on-board temperature sensor. Eight of the ten analog inputs may be connected to the I/O pins for external interface. The remaining two analog inputs ($V_{SENSE}$ and Temp Sensor) are internally connected. When placed in Auto Sequencing mode, ADC0 automatically converts, stores and limit-checks each analog input, and interrupts the CPU when a converted result is outside of its programmed range. This feature greatly facilitates protection functions because all measurement and comparison operations are automated.

#### 3.3.2. Temperature Sensor

This sensor measures the die temperature of the Si8250/1/2. It can achieve 3 °C accuracy with a single-point calibration and 1 °C with a two-point calibration. The temperature output signal is digitized by ADC0.

#### 3.3.3. 8051 CPU

50 MIPS CPU core with 1 kB of SRAM and up to 32 kB of Flash memory. This processor has its own onboard oscillator and PLL, reset sources, and real-time in-system hardware debug interface eliminating the need for external processor supervisors, timebases, and "emulators". The CPU has an external interrupt (INT0/) that can be connected to an external device via the I/O pins. When interrupted, the CPU suspends execution of the current task and immediately vectors to an interrupt service routine specifically designed to handle the interrupting device.

#### 3.3.4. Digital Peripherals

Peripherals include four 16-bit timers, a three-channel programmable counter array (PCA, with each channel useful as a PWM), an SMBus port, a UART (useful as a serial data port for isolated applications), and two 8-bit I/O port latches for logic control outputs.

## 4. Design Tools

The Si8250DK development kit (Figure 3) contains everything required to develop applications with the Si825x family of digital power controllers. This kit supports all phases of power supply development from controller design through real-time system debugging. It also includes a turnkey, 35 W isolated dc/dc target board for evaluation and experimentation.


**Figure 3. Si8250DK Development Kit**

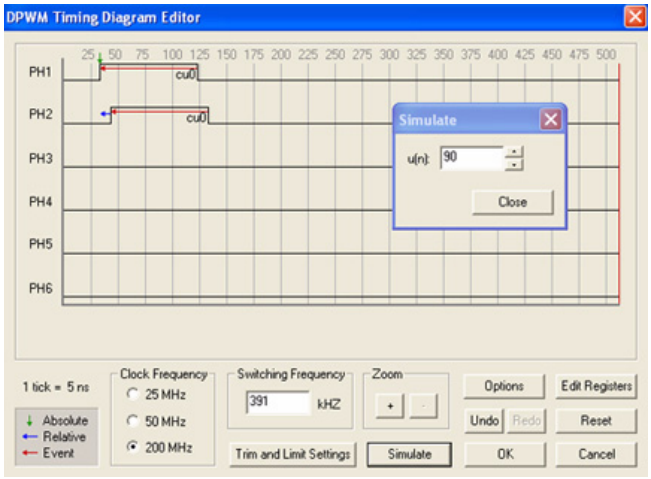



**Figure 4. Timing Design Tool**

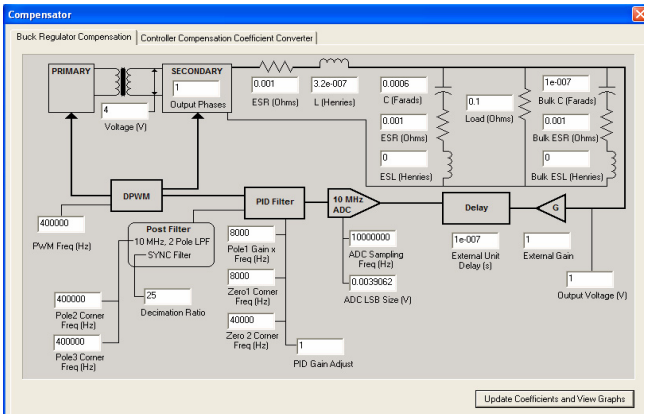



**Figure 5. Buck Regulator Compensation Tool**

The tool set enables users to configure pre-written application software included in the kit to their application using a set of PC-based graphical user interface (GUIs). These GUIs (Figures 4 and 5) allow the user to quickly and easily specify and verify system timing, loop compensation, and protection settings and compile and download the resulting code into the Si8250/1/2 (Figure 6).

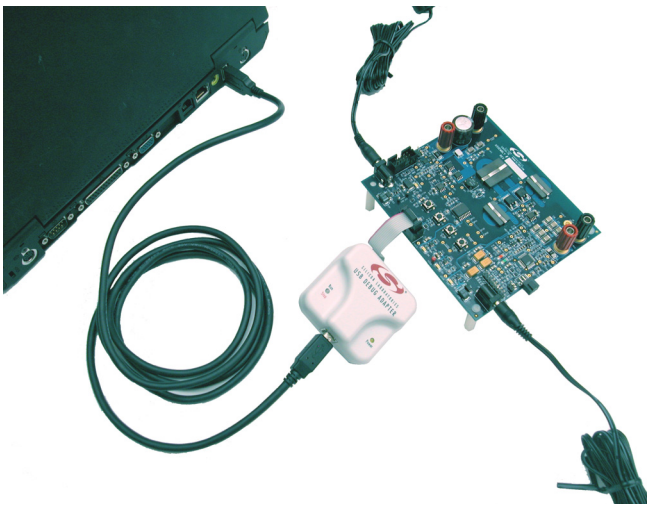


**Figure 6. Software Download to Si8250 Mounted in Power Supply**

# 5. Example Applications

The Si825x is the ideal choice for digitally-controlled switched mode power supplies. This section provides a quick overview of the Si825x in an isolated half-bridge dc/dc converter and a single-phase point-of-load converter. Reference designs are available for both of these. For more details, visit our web site at www.silabs.com.

## 5.1. Isolated DC/DC Converter

A 35 W, 400 kHz, Si8250-based half bridge converter is shown in Figure 7. This circuit is the same as that of the target (evaluation) board shipped in the Si8250DK development kit.

The Si8250/1/2 is located on the secondary-side of the power supply for optimum transient response. DPWM outputs PH3 and PH4 control gates of the synchronous rectifiers via a dual driver I.C. DPWM outputs PH1 and PH2 control the gates of the primary-side switching transistors with isolation provided by a Silicon Laboratories isolator. A current transformer circuit provides peak current sensing. Primary side analog parameters (input voltage and current and the filter node voltage) are digitized by a Silicon Laboratories C8051F300 microcontroller and passed to the Si8250/1/2 using the onboard UART through additional channels of the isolator IC to the Si8250/1/2.

The Si8250/1/2 uses the application software included with the Si8250DK development kit after being configured for the half-bridge application using the tools supplied in the kit.

When power is applied, the CPU executes an internal reset followed by initialization of all parameters. The Si8250/1/2 remains in a low-power state, monitoring digitized $V_{IN}$ data from the primary-side MCU until $V_{IN}$ is within specified limits. At this time, the controller is fully enabled and executes soft-start by monitoring $V_{OUT}$ while sequentially incrementing the loop voltage reference (REFDAC) until the supply output voltage is within the specified range, at which time steady-state operation begins.

During steady-state operation, the MCU operates in interrupt mode where hardware events divert program execution to specific routines in priority order.

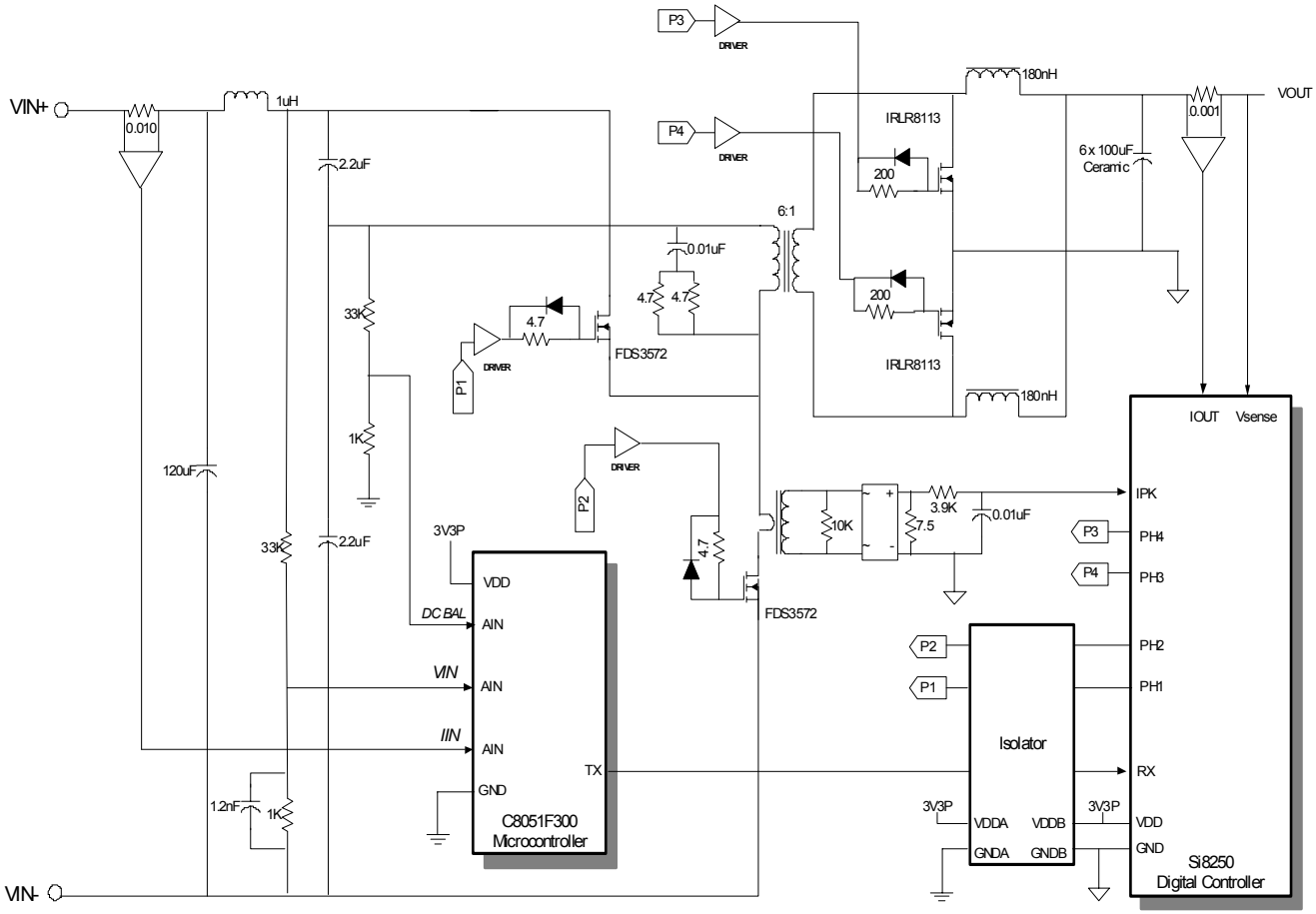



**Figure 7. Isolated Half-Bridge DC/DC Converter**

## 5.2. Single-Phase Point of Load (POL) Converter

A 65 W, 400 KHz Si8252 based single phase POL converter block diagram is shown in Figure 8. DPWM outputs PH1 and PH2 control the gates of the buck and synchronous switching transistors. A lossless current sensing method that relies on the resistor and inductance of the inductor is used to measure the current for overcurrent protection. The input voltage is measured using the resistor divider network and analog input port AIN0 of 12bit, 200 kHz ADC0.

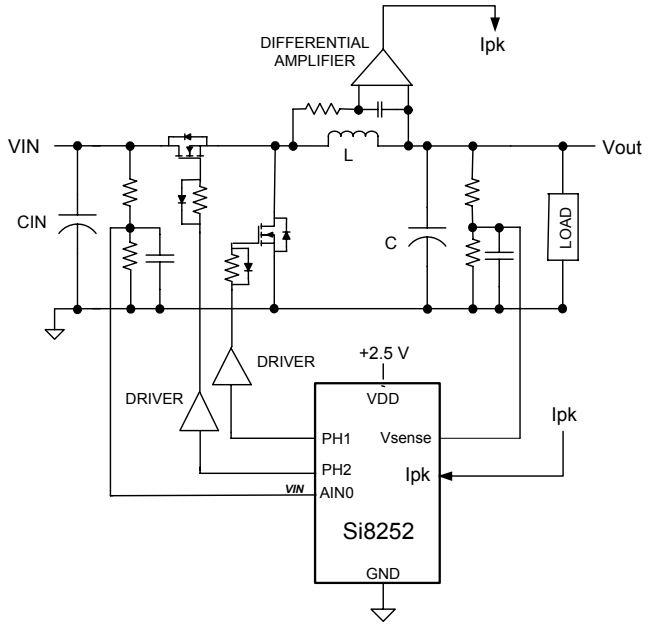



**Figure 8. Single-Phase POL Block Diagram**

When power is applied, the CPU executes an internal reset followed by initialization of all parameters. The Si8252 remains in a low-power state, monitoring digitized $V_{IN}$ data until $V_{IN}$ is within specified limits. At this time, the controller is fully enabled and executes soft-start by monitoring output voltage while sequentially incrementing the loop voltage reference (REFDAC) until the supply output voltage is within the specified range, at which time steady-state operation begins. As in the previous half-bridge example, transient response is improved by adjusting loop gain at the onset of a transient (i.e. nonlinear control). The efficiency of the POL converter can be optimized over the complete load range by dynamically adjusting the dead-times. Typical efficiency simulation results for the POL are shown in Figure 9. In this case, the single-phase POL operates at a PWM frequency of 400 kHz with an output voltage of 3.3 V and an input voltage range of 10 to 15 V. The curve shows the efficiency with an input voltage of 12.0 V.

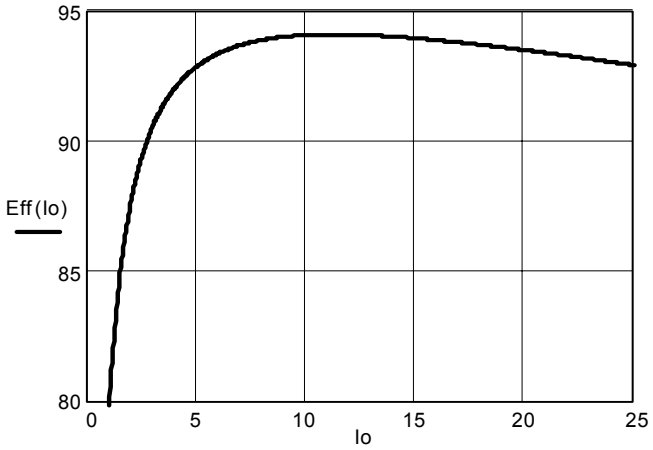



**Figure 9. POL Efficiency**

## 6. Layout Considerations

The mixed-signal nature of the Si8250/1/2 mandates clean bias supplies and ground returns. It is best to provide separate ground planes for analog, digital, and power switch returns. These planes should tie together at only one point to eliminate the possibility of circulating ground currents. For best performance, the $V_{DD}$ supply should be decoupled from the main supply. The LQFP-32 package provides the best noise performance because it has separate analog and digital $V_{DD}$ and ground inputs ($V_{DDA}$, GNDA).

As shown in Figure 10, the $V_{DDA}$ is decoupled by a filter consisting of a 1 Ω resistor in series with a 500 mA, 40 Ω ferrite bead and a parallel combination of a 10 µF with a 0.1 µF high-frequency bypass capacitor. All connections should be kept as short as possible. $V_{DDA}$ and GNDA should be connected into their respective ground planes. The QFN-28 package shares analog and digital power with ground on the same pins. Power supply decoupling is shown in Figure 11. Again, all connections should be kept as short as possible.

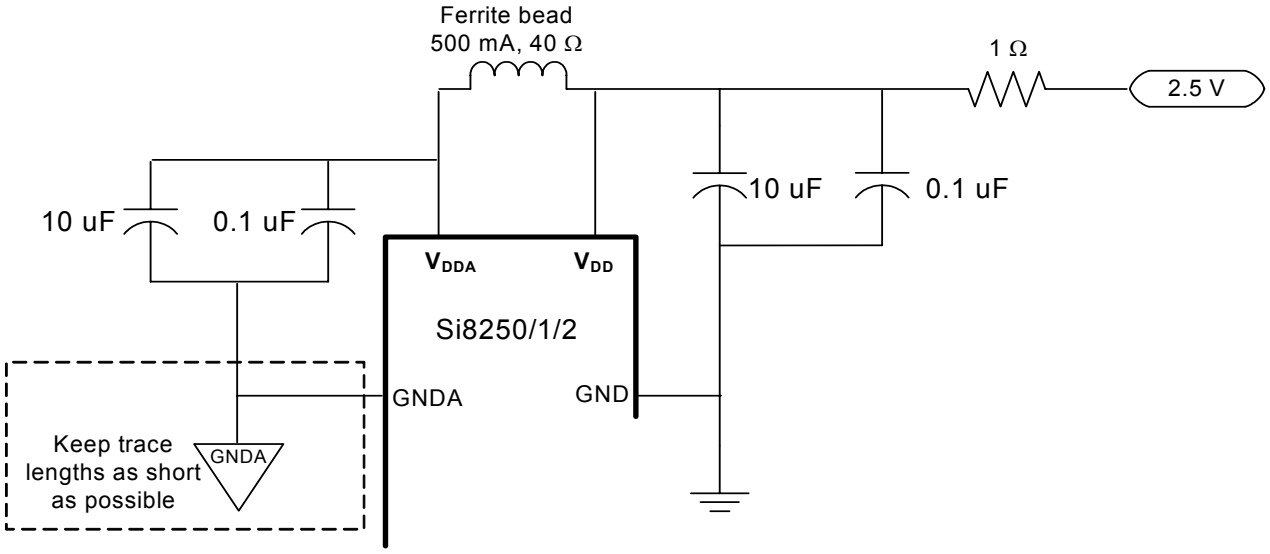



**Figure 10. Power Supply Connections for LQFP-32 Package**

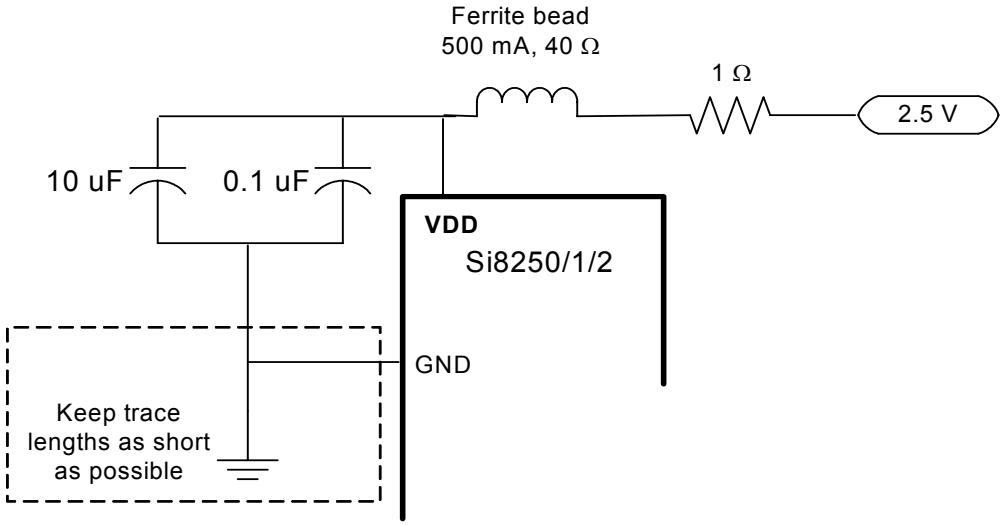



**Figure 11. Power Supply Connections for QFN-28 Package**

In both cases, the bias supplies must be filtered using low ESR/ESL capacitors placed close to the IC pins. Thick copper traces should be connected to the bias pins ($V_{DD}$, $V_{DDA}$) and the ground pins (GND, GNDA) to reduce resistance and inductance. The copper routings from the drivers to the FETs should be kept short and wide, especially in very high frequency applications, to reduce inductance of the traces so that the drive signals can be kept clean. Connections between $V_{SENSE}$ and the output voltage must be kept as short as possible to minimize inductance and parasitic ringing effects.

It is best to locate the Si8250/1/2 as close to the output voltage terminal as possible and use a Kelvin connection to reduce the difference in ground potential between the Si8250/1/2 and the output voltage ground return. Most applications will require access to the debug pins. These pins are susceptible to damage from electrostatic discharge (ESD). It is, therefore, recommended that the debug circuit interface use the input protection circuitry shown in Figure 12.

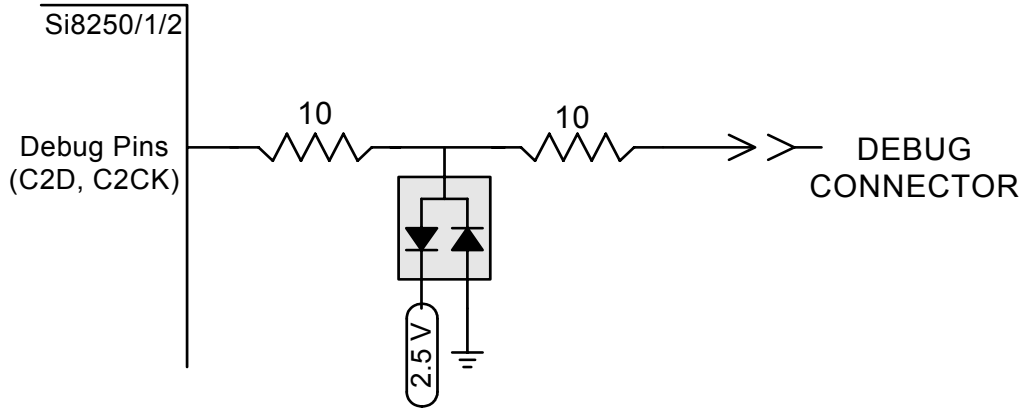



**Figure 12. Debug Interface Pin Protection Circuit**

# 7. Pin Descriptions: Si8250/1/2

**32-pin LQFP** **28-pin QFN**

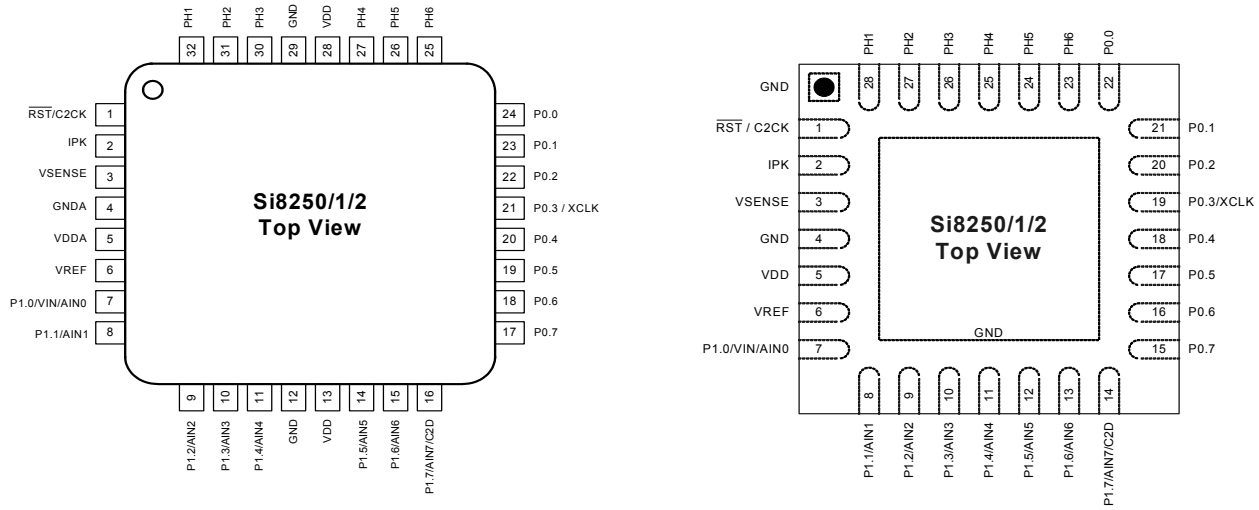



**Figure 13. Example Pin Configurations**

**Table 17. Pin Descriptions**

| Name | QFN-28 Pin # | LQFP-32 Pin# | Type | Description |
|---|---|---|---|---|
| $\overline{\text{RST}}$/C2CK | 1 | 1 | D I/O | Reset input or bidirect debug clock |
| IPK | 2 | 2 | AIN | Inductor current input |
| $V_{SENSE}$ | 3 | 3 | AIN | Output voltage feedback input |
| GND | 4 | — | AIN | Ground |
| GNDA | — | 4 | AIN | Ground |
| $V_{DD}$ | 5 | — | AIN | Power supply input |
| $V_{DDA}$ | — | 5 | AIN | Power supply input |
| $V_{REF}$ | 6 | 6 | AIN | External voltage reference input |
| P1.0/$V_{IN}$ or AIN0 | 7 | 7 | D I/O or AIN | Port 1 I/O or scaled power supply input voltage or ADC input 0 |
| P1.1/AIN1 | 8 | 8 | D I/O or AIN | Port 1 I/O or ADC input 1 |
| P1.2/AIN2 | 9 | 9 | D I/O or AIN | Port 1 I/O or ADC input 2 |
| P1.3/AIN3 | 10 | 10 | D I/O or AIN | Port 1 I/O or ADC input 3 |
| P1.4/AIN4 | 11 | 11 | D I/O or AIN | Port 1 I/O or ADC input 4 |
| GND | — | 12 | AIN | Ground |
| $V_{DD}$ | — | 13 | AIN | Power supply input |
| P1.5/AIN5 | 12 | 14 | D I/O or AIN | Port 1 I/O or ADC input 5 |
| P1.6/AIN6 | 13 | 15 | D I/O or AIN | Port 1 I/O or ADC input 6 |
| P1.7/ AIN7/C2D | 14 | 16 | D I/O, DIN or AIN | Port 1 I/O or ADC input 7 or C2 Data |
| P0.7 | 15 | 17 | D I/O | Port 0 I/O |
| P0.6 | 16 | 18 | D I/O | Port 0 I/O |

**Table 17. Pin Descriptions (Continued)**

| Name | QFN-28 Pin # | LQFP-32 Pin# | Type | Description |
|---|---|---|---|---|
| P0.5 | 17 | 19 | D I/O | Port 0 I/O |
| P0.4 | 18 | 20 | D I/O | Port 0 I/O |
| P0.3/XCLK | 19 | 21 | D I/O | Port 0 I/O |
| P0.2 | 20 | 22 | D I/O | Port 0 I/O |
| P0.1 | 21 | 23 | D I/O | Port 0 I/O |
| P0.0 | 22 | 24 | D I/O | Port 0 I/O or bidirectional debug data |
| PH6 | 23 | 25 | DOUT | Phase 6 switch control output |
| PH5 | 24 | 26 | DOUT | Phase 5 switch control output |
| PH4 | 25 | 27 | DOUT | Phase 4 switch control output |
| $V_{DD}$ | — | 28 | AIN | Power supply input |
| GND | — | 29 | AIN | Ground |
| PH3 | 26 | 30 | DOUT | Phase 3 switch control output |
| PH2 | 27 | 31 | DOUT | Phase 2 switch control output |
| PH1 | 28 | 32 | DOUT | Phase 1 switch control output |

## 7.1. Pin Functions

### 7.1.1. RST/C2CK

CPU reset or debug tool clock. Driving this pin low resets the CPU. This pin is also clocked by the USB debug adaptor during debug.

### 7.1.2. $I_{PK}$

Input to the peak current detector for pulse-by-pulse current limiting and overcurrent protection shutdown control.

### 7.1.3. $V_{SENSE}$

ADC1 inverting input. This is the voltage feedback input for the Si8250. The maximum allowable signal is $V_{REF}$.

### 7.1.4. GND

Digital ground for the 32LQFP package and the main ground for the 28MLP package.

### 7.1.5. GNDA

Analog ground for 32LQFP only.

### 7.1.6. $V_{DD}$

Digital supply voltage for the 32LQFP package and main supply voltage for the 28MLP package.

### 7.1.7. $V_{DDA}$

Analog supply for 32LQFP only.

### 7.1.8. P1.0/$V_{IN}$ or AIN0

Programmable multifunction I/O pin. This pin can be software-configured to be either a Port 1 digital input or output, or an ADC0 input at AMUX address 0. If used in a non-isolated application, positive input supply voltage must be tied to this input through a resistor divider and anti-aliasing capacitor to minimize the frequencies above fS/2 (100 kHz) to prevent aliasing. Isolated applications may use this input as general-purpose digital I/O or analog input.

### 7.1.9. P1.1 or AIN1–P1.7 or AIN7

Programmable multifunction I/O pins. These pins can be software-configured to be a Port 1 digital input or output, or an ADC0 input. P1.7 also serves as the debug data input (C2D) and is used during debug by the USB debug adaptor. P1.7 may be used as general-purpose digital I/O when not in debug mode. Any of the digital peripherals may be programmed to connect to these pins.

### 7.1.10. P0.0–P0.7

Programmable multifunction I/O pins. These pins can be software-configured to be either a Port 1 digital input or output, or an ADC0 input. Any of the digital peripherals (including the ENABLE input) may be programmed to connect to these pins. P0.3 may be programmed to serve as an external (25 MHz nominal) clock input.

### 7.1.11. PH1–PH6

DPWM gate control (complementary drive) outputs. These signals connect to the MOSFET gates through an external gate driver. The output levels swing between ground and $V_{DD}$.

## 8. Ordering Guide

| Ordering Number | Flash Memory | # of PWM Outputs | UART | Package |
|---|---|---|---|---|
| Si8250-IQ | 32 kB | 6 | Yes | LQFP-32 |
| Si8250-IM | 32 kB | 6 | Yes | QFN-28 |
| Si8251-IQ | 16 kB | 6 | Yes | LQFP-32 |
| Si8251-IM | 16 kB | 6 | Yes | QFN-28 |
| Si8252-IQ | 16 kB | 3 | No | LQFP-32 |
| Si8252-IM | 16 kB | 3 | No | QFN-28 |

## 9. Package Outline: 32LQFP

Figure 14 illustrates the package details for the 32-pin LQFP version of the Si8250/1/2. Table 18 lists the values for the dimensions shown in the illustration.

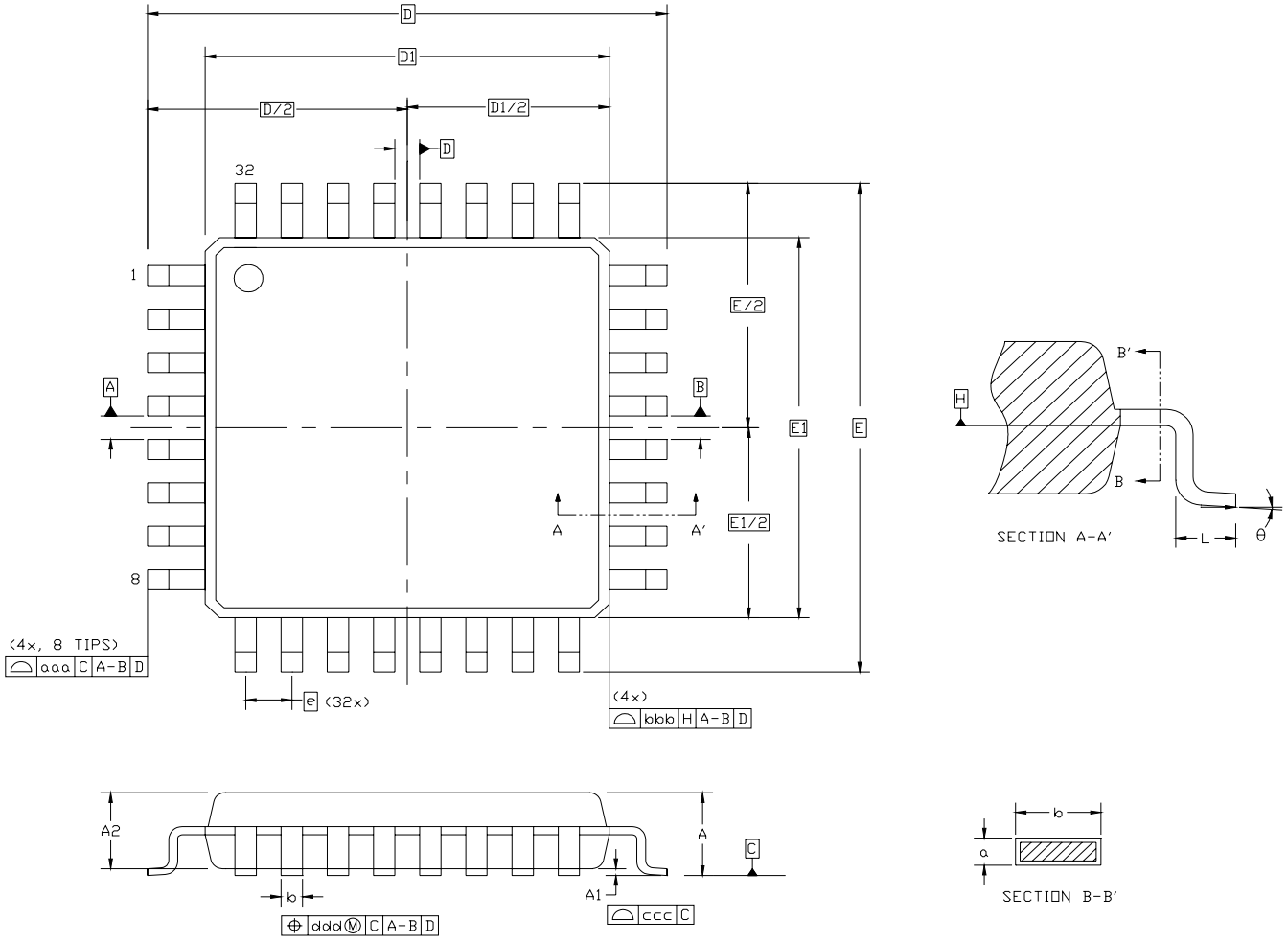



**Figure 14. 32-pin LQFP Package Diagram**

**Table 18. LQFP-32 Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | — | 0.20 |
| D | 9.00 BSC. | | |
| D1 | 7.00 BSC. | | |
| e | 0.80 BSC. | | |
| E | 9.00 BSC. | | |
| E1 | 7.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.20 | | |
| Θ | 0° | 3.5° | 7° |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

## 10. Package Outline: 28QFN

Figure 15 illustrates the package details for the 28-lead QFN version of the Si8250/1/2. Table 19 lists the values for the dimensions shown in the illustration.

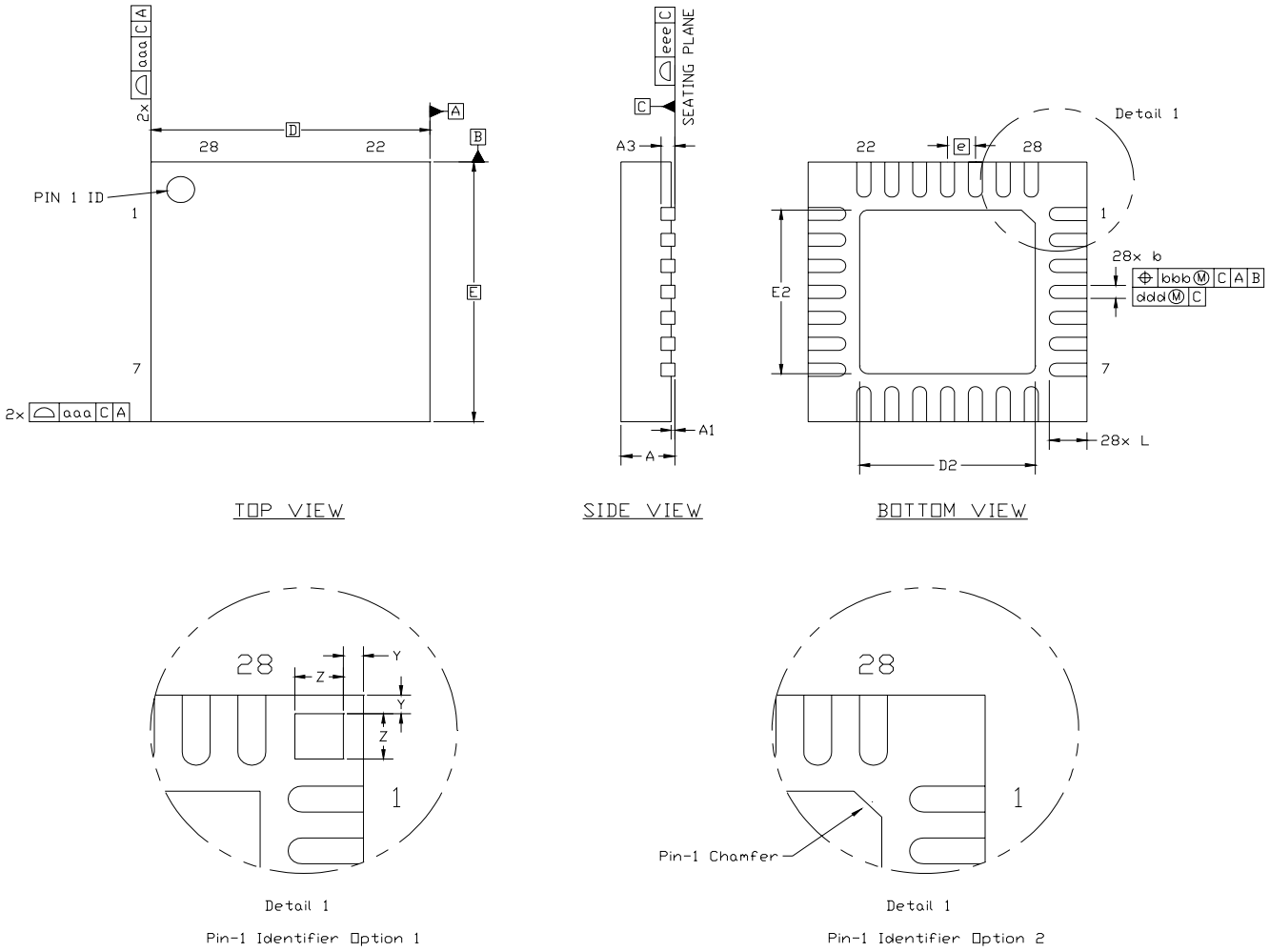



**Figure 15. 28-lead Quad Flat No-lead (QFN) Package Diagram**

**Table 19. QFN-28 Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.03 | 0.07 | 0.11 |
| A3 | | 0.25 REF | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC. | |
| D2 | 2.90 | 3.15 | 3.35 |
| e | | 0.50 BSC. | |
| E | | 5.00 BSC. | |
| E2 | 2.90 | 3.15 | 3.35 |
| L | 0.45 | 0.55 | 0.65 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| Z | | 0.435 | |
| Y | | 0.18 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-243, variation VHHD except for custom features D2, E2, L, Z, and Y, which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

# DOCUMENT CHANGE LIST

## Revision 0.7 to Revision 0.8

- Updated DPWM phase output drive-high and drive-low resistance in Table 8, “DPWM Specifications,” on page 9.

## Revision 0.8 to Revision 0.9

- Updated Table 5, “ADC1 Specifications,” on page 7.
  - Updated common-mode input voltage range spec.
- Updated "Contact Information" on page 32.
  - Updated disclaimer.

## Revision 0.9 to Revision 1.0

- Updated Figure 8, “Single-Phase POL Block Diagram,” on page 20.
- Removed all TBDs.
- Updated package drawings.

## NOTES:

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