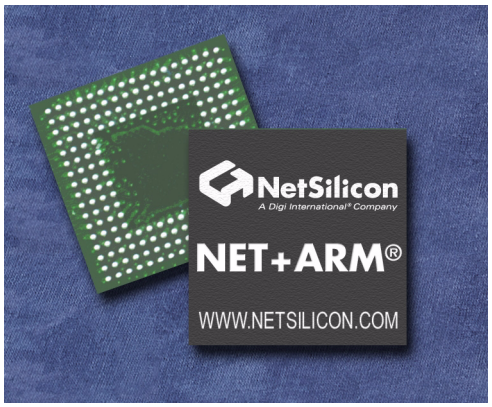
NET+50 Data Sheet

The Digi **NET+50** is a high-performance, highly integrated, 32-bit, system-on-a-chip ASIC, designed for use in intelligent networked devices and Internet appliances. The NET+50 is based on the standard architecture in the NET+ARM™ family of devices.



To support a variety of networking scenarios, the NET+50 includes a 10/100 BaseT Ethernet MAC with MII interface and two independent serial ports, each of which can run in UART, HDLC, or SPI mode.

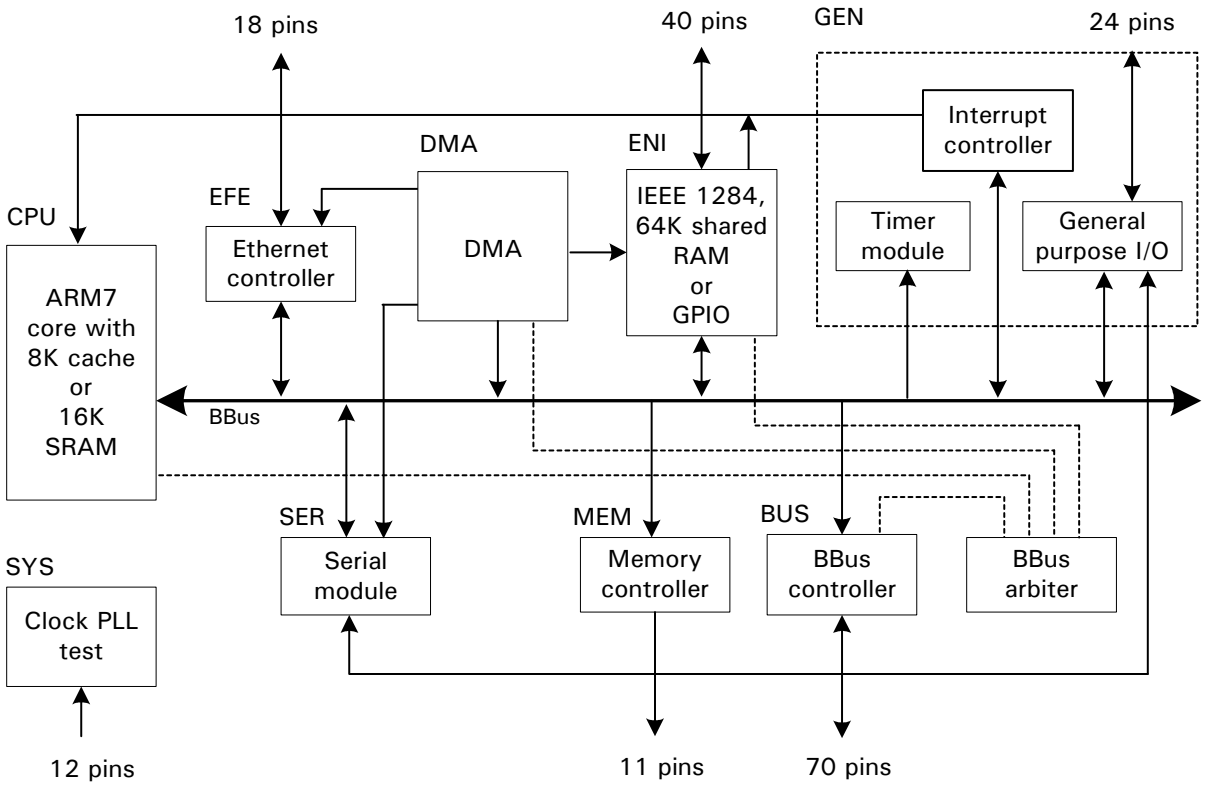
The NET+50 CPU is an ARM7TDMI 32-bit RISC processor with a rich complement of support peripherals and memory controllers for various types of memory (including flash, SDRAM, EEPROM, and others), programmable timers, a 10-channel DMA controller, a P1284/ENI interface, an external bus expansion module, and up to 40 general-purpose I/O pins and 16 general-purpose input pins.

NET+ARM is the hardware foundation for the **NET+Works**™ family of integrated hardware and software solutions for device networking. The NET+Works solution includes drivers, operating systems, networking software, development tools, APIs, and complete development boards.

Contents

NET+50 block diagram

The following diagram provides an overview of the modules that make up the NET+50 device:



Key features

CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 8 KB cache, configurable as 16 KB RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- Supports TP-PMD and fiber-PMD devices
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 128-byte transmit FIFO, 2 KB receive FIFO
- Intelligent receive-side buffer selection

Operating frequency

- 44-MHz maximum system clock, requiring only a simple external 18.432-MHz crystal
- Supports external oscillators

ENI/P1284 Interface

- ENI host interface
- Four IEEE 1284 parallel ports
- 64 KB shared RAM ENI interface — 8- or 16-bit
- Full-duplex FIFO mode interface — 8- or 16-bit
- 32-byte transmit/receive FIFO mode FIFOs

Programmable timers

- Two independent, 27-bit timers (2 μs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Bus timer

Serial port

- Two fully independent serial ports (UART, HDLC, SPI)
- Digital phase locked loop (DPLL) for receive clock extractions
- 32 byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode, 1200 bps – 4 Mbps in 1X mode. (Higher rates may be possible depending on the board design.)

10-channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to serial transmit and receive
- Four channels (two at a time) configurable for external peripherals
- Flexible buffer management

Bus interface

- Five independent, programmable chip selects with 256 Mb addressing per chip select
- All chip selects support SRAM, EDO DRAM, SDRAM, and devices such as flash and EEPROM with SRAM interfaces
- Supports 8-, 16-, and 32-bit peripherals
- Dynamic bus sizing support
- Supports ASYNC and SYNC peripheral timing
- Internal DRAM address multiplexing
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–15 wait states per chip select
- Bootstrap support

Power and operating voltages

- 552 mW maximum (typically, 484 mW), outputs switching
- 3.3 V — I/O
- 2.5 V — core

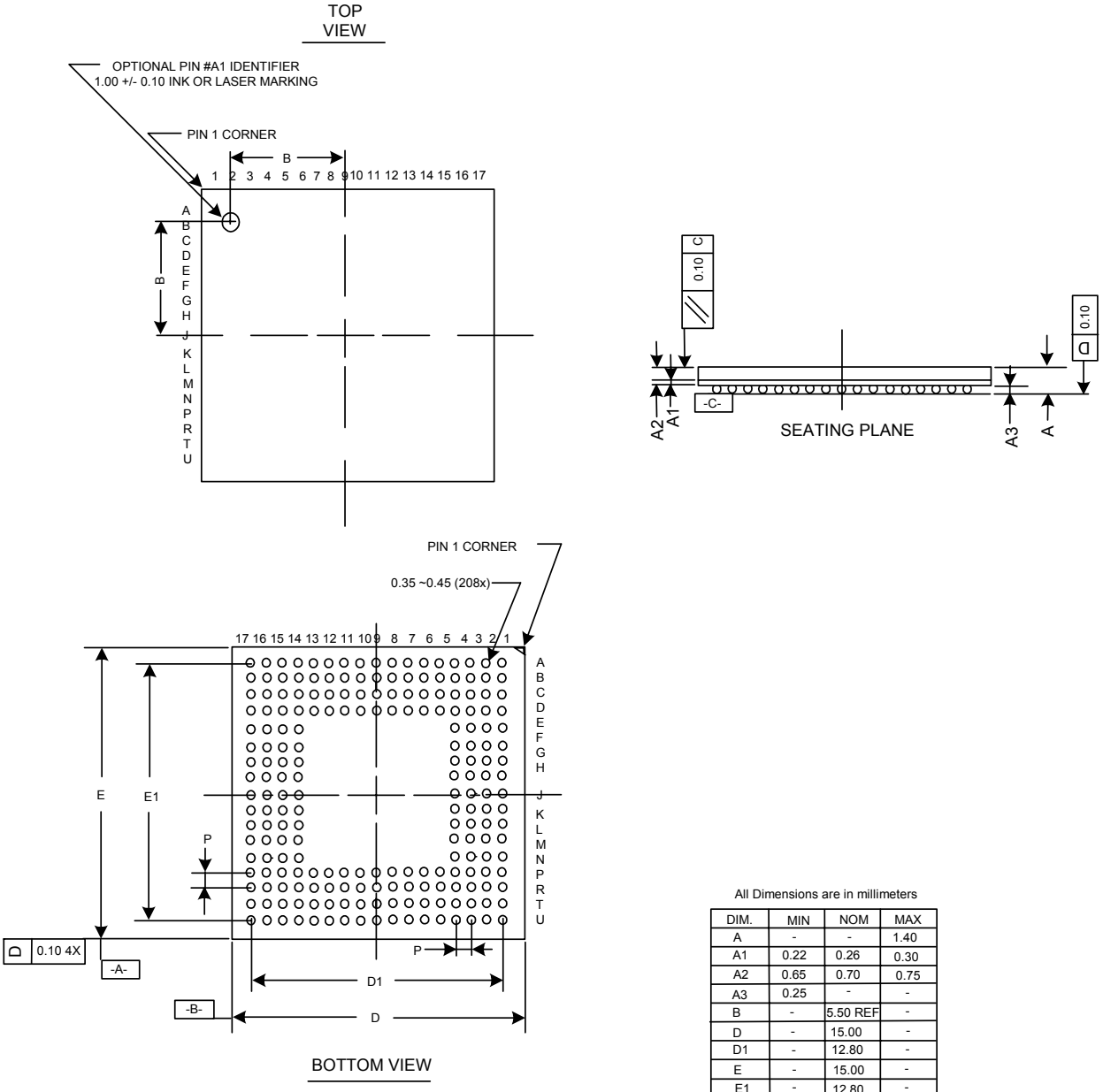
Serial port (cont)

- Odd, even, or no parity
- 5, 6, 7, or 8 bits
- 1 or 2 stop bits
- Internal and external clock support
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram

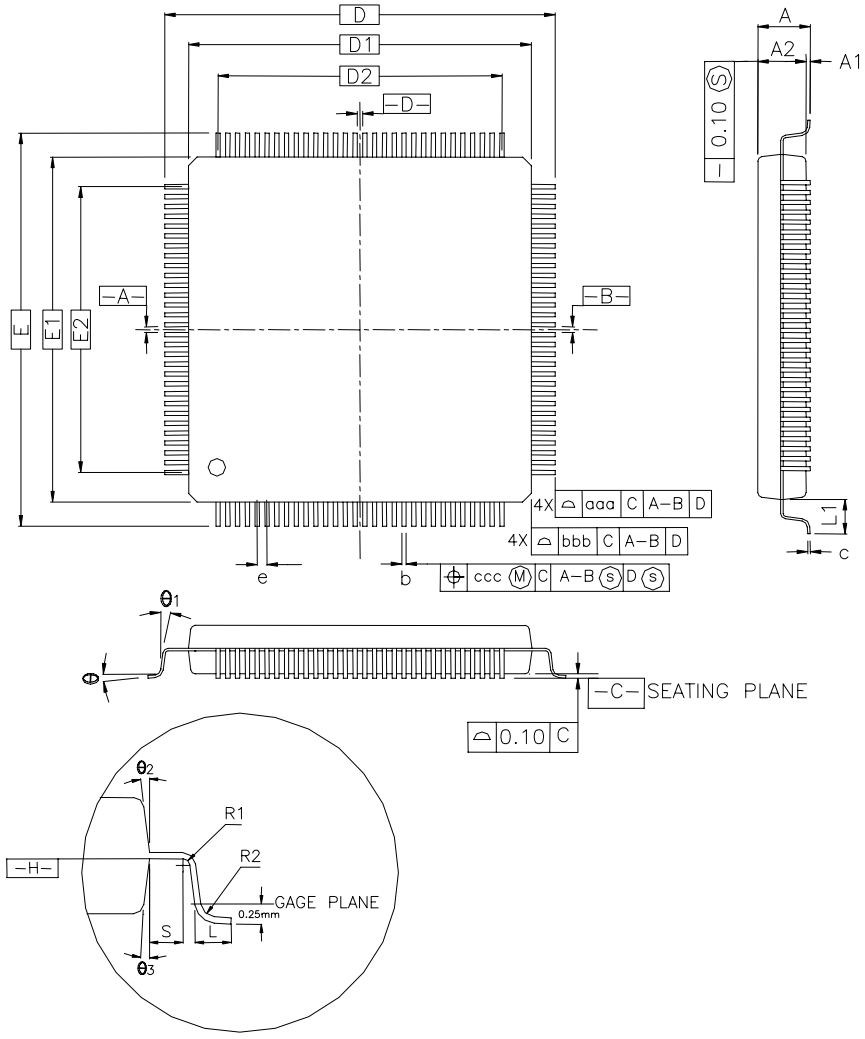


All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

PQFP packaging and pinout diagrams

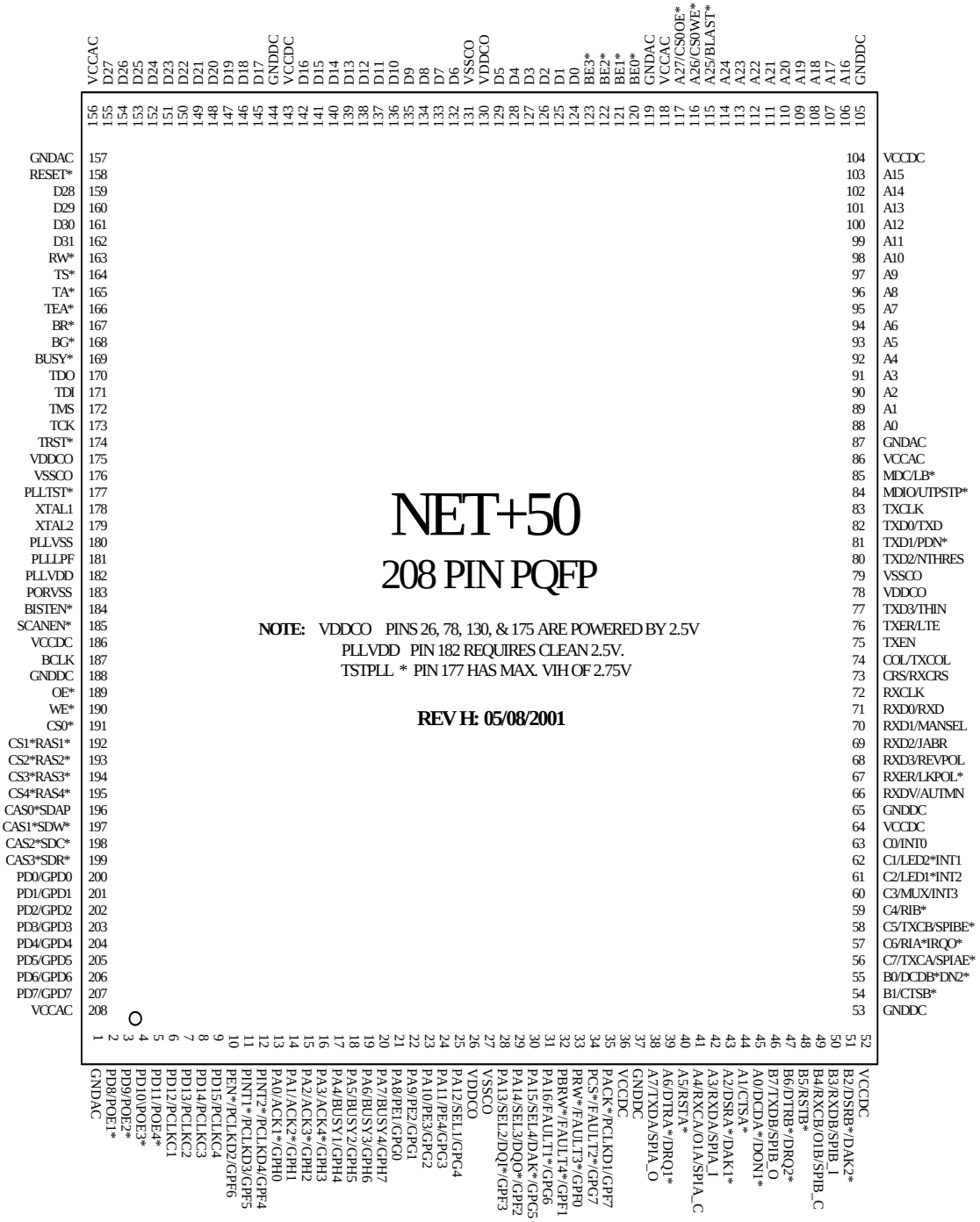
PQFP packaging



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

PQFP pinout


NET+50
208 PIN PQFP
NOTE: VDDCO PINS 26, 78, 130, & 175 ARE POWERED BY 2.5V
PLLVDD PIN 182 REQUIRES CLEAN 2.5V.
TSTPLL * PIN 177 HAS MAX. VIH OF 2.75V
REV H: 05/08/2001
1 GNDAC
2 PD8/POE1*
3 PD9/POE2*
4 PD10/POE3*
5 PD11/POF4*
6 PD12/PCLKC1
7 PD13/PCLKC2
8 PD14/PCLKC3
9 PD15/PCLKC4
10 PEN*/PCLKD2/GPF6
11 PINT1*/PCLKD3/GPF5
12 PINT2*/PCLKD4/GPF4
13 PA0/ACK1*/GPH0
14 PA1/ACK2*/GPH1
15 PA2/ACK3*/GPH2
16 PA3/ACK4*/GPH3
17 PA4/BUSY1/GPH4
18 PA5/BUSY2/GPH5
19 PA6/BUSY3/GPH6
20 PA7/BUSY4/GPH7
21 PA8/PE1/GPG0
22 PA9/PE2/GPG1
23 PA10/PE3/GPG2
24 PA11/PE4/GPG3
25 PA12/SEL1/GPG4
26 VDDCO
27 VSSCO
28 PA13/SEL2/DQI*/GPF3
29 PA14/SEL3/DQO*/GPF2
30 PA15/SEL4/DAK*/GPG5
31 PA16/FAULT1*/GPG6
32 PBRW*/FAULT4*/GPF1
33 PRW*/FAULT3*/GPF0
34 PCS*/FAULT2*/GPG7
35 PACK*/PCLKD1/GPF7
36 VCCDC
37 GNDDC
38 A7/TXDA/SPIA_O
39 A6/DTRA*/DRQ1*
40 A5/RSTA*
41 A4/RXCA/O1A/SPIA_C
42 A3/RXDA/SPIA_I
43 A2/DSRA*/DAK1*
44 A1/CTSA*
45 A0/DCDA*/DDN1*
46 B7/TXDB/SPIB_O
47 B6/DTRB*/DRQ2*
48 B5/RSTB*
49 B4/RXCB/O1B/SPIB_C
50 B3/RXDB/SPIB_I
51 B2/DSRB*/DAK2*
52 VCCDC
53 GNDDC
54 B1/CTSB*
55 B0/DCDB*DN2*
56 C7/TXCA/SPIAE*
57 C6/RIA*IRQO*
58 C5/TXCB/SPIBE*
59 C4/RIB*
60 C3/MUX/INT3
61 C2/LED1*INT2
62 C1/LED2*INT1
63 C0/INT0
64 VCCDC
65 GNDDC
66 RXDV/AUTMN
67 RXER/LKPOL*
68 RXD3/REVPOL
69 RXD2/JABR
70 RXD1/MANSEL
71 RXD0/RXD
72 RXCLK
73 CRS/RXCRS
74 COL/TXCOL
75 TXEN
76 TXER/LTE
77 TXD3/THIN
78 VDDCO
79 VSSCO
80 TXD2/NTHRES
81 TXD1/PDN*
82 TXD0/TXD
83 TXCLK
84 MDIO/UTPSTP*
85 MDC/LB*
86 VCCAC
87 GNDAC
88 A0
89 A1
90 A2
91 A3
92 A4
93 A5
94 A6
95 A7
96 A8
97 A9
98 A10
99 A11
100 A12
101 A13
102 A14
103 A15
104 VCCDC
105 GNDDC
106 A16
107 A17
108 A18
109 A19
110 A20
111 A21
112 A22
113 A23
114 A24
115 A25/BLAST*
116 A26/CS0WE*
117 A27/CS0OE*
118 VCCAC
119 GNDAC
120 BE0*
121 BE1*
122 BE2*
123 BE3*
124 D0
125 D1
126 D2
127 D3
128 D4
129 D5
130 VDDCO
131 VSSCO
132 D6
133 D7
134 D8
135 D9
136 D10
137 D11
138 D12
139 D13
140 D14
141 D15
142 D16
143 VCCDC
144 GNDDC
145 D17
146 D18
147 D19
148 D20
149 D21
150 D22
151 D23
152 D24
153 D25
154 D26
155 D27
156 VCCAC
157 GNDAC
158 RESET*
159 D28
160 D29
161 D30
162 D31
163 RW*
164 TS*
165 TA*
166 TEA*
167 BR*
168 BG*
169 BUSY*
170 TDO
171 TDI
172 TMS
173 TCK
174 TRST*
175 VDDCO
176 VSSCO
177 PLLTST*
178 XTAL1
179 XTAL2
180 PLLVSS
181 PLLLPF
182 PLLVDD
183 PORVSS
184 BISTEN*
185 SCANEN*
186 VCCDC
187 BCLK
188 GNDDC
189 OE*
190 WE*
191 CS0*
192 CS1*RAS1*
193 CS2*RAS2*
194 CS3*RAS3*
195 CS4*RAS4*
196 CAS0*SDAP
197 CAS1*SDW*
198 CAS2*SDC*
199 CAS3*SDR*
200 PD0/GPD0
201 PD1/GPD1
202 PD2/GPD2
203 PD3/GPD3
204 PD4/GPD4
205 PD5/GPD5
206 PD6/GPD6
207 PD7/GPD7
208 VCCAC

Pinout detail tables

The pinout tables in the following sections have the following columns:

Signal	The pin name for each I/O signal.Some signals have dual modes and are identified accordingly. The mode is configured through firmware using a configuration register. Some modes may require hardware configuration during a RESET condition
BGA	The BGA pin number for specific I/O signals.
PQFP	The PQFP pin number for specific I/O signals.
†	A dagger indicates a pin that is an input current source. (The daggers appear in the BGA column, but this applies in PQFP layout as well.)
*	An asterisk indicates a pin that is *active low*.
I/O	The type of signal — input, output, or input/output (I/O).
OD	The output drive strength of an output buffer. The NET+50 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

System bus interface

Signal		BGA	PQFP	I/O	OD	Description	
BCLK		T10	187	O	8	Synchronous bus clock	
ADDR27	CS0OE*	F4 †	117	I/O	4	Address bus	Chip select 0 output enable
ADDR26	CS0WE*	F3 †	116	I/O	4	Address bus	Chip select 0 write enable
ADDR25	BLAST*	E2 †	115	I/O	4	Address bus	Burst-terminated input
ADDR24		D2 †	114	I/O	4		
ADDR23		E3 †	113	I/O	4		
ADDR22		E4 †	112	I/O	4		
ADDR21		D1 †	111	I/O	4		
ADDR20		C2 †	110	I/O	4		
ADDR19		D3 †	109	I/O	4		
ADDR18		C1 †	108	I/O	4		
ADDR17		B1 †	107	I/O	4		
ADDR16		B2 †	106	I/O	4		
ADDR15		B3 †	103	I/O	4		
ADDR14		A3 †	102	I/O	4		
ADDR13		A4 †	101	I/O	4		
ADDR12		B4 †	100	I/O	4		

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
ADDR11	C3 †	99	I/O	4	
ADDR10	A5 †	98	I/O	4	
ADDR9	D4 †	97	I/O	4	
ADDR8	C4 †	96	I/O	4	
ADDR7	B5 †	95	I/O	4	
ADDR6	A6 †	94	I/O	4	
ADDR5	D5 †	93	I/O	4	
ADDR4	C5 †	92	I/O	4	
ADDR3	B6 †	91	I/O	4	
ADDR2	A7 †	90	I/O	4	
ADDR1	D6 †	89	I/O	4	
ADDR0	C6 †	88	I/O	4	
DATA31	T3	162	I/O	4	Data bus
DATA30	R4	161	I/O	4	
DATA29	U3	160	I/O	4	
DATA28	U2	159	I/O	4	
DATA27	R2	155	I/O	4	
DATA26	R1	154	I/O	4	
DATA25	P1	153	I/O	4	
DATA24	P2	152	I/O	4	
DATA23	R3	151	I/O	4	
DATA22	N1	150	I/O	4	
DATA21	P4	149	I/O	4	
DATA20	P3	148	I/O	4	
DATA19	N2	147	I/O	4	
DATA18	M1	146	I/O	4	
DATA17	N4	145	I/O	4	
DATA16	L1	142	I/O	4	
DATA15	M4	141	I/O	4	
DATA14	M3	140	I/O	4	
DATA13	L2	139	I/O	4	
DATA12	K1	138	I/O	4	

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
DATA11	L4	137	I/O	4	
DATA10	L3	136	I/O	4	
DATA9	K2	135	I/O	4	
DATA8	J1	134	I/O	4	
DATA7	K4	133	I/O	4	
DATA6	K3	132	I/O	4	
DATA5	J4	129	I/O	4	
DATA4	J3	128	I/O	4	
DATA3	H2	127	I/O	4	
DATA2	G1	126	I/O	4	
DATA1	H4	125	I/O	4	
DATA0	H3	124	I/O	4	
TS*	no connect				
BE3*	G2	123	I/O	2	Byte enable D31:D24
BE2*	F1	122	I/O	2	Byte enable D23:D16
BE1*	G4	121	I/O	2	Byte enable D15:D08
BE0*	G3	120	I/O	2	Byte enable D07:D00
RW*	U4	163	I/O	2	Transfer direction
TA*	R5 †	165	I/O	8	Data transfer acknowledge
TEA*	T4 †	166	I/O	8	Transfer error/last acknowledge
BR*	no connect				
BG*	no connect				
BUSY*	no connect				

Chip select controller

Signal		BGA	PQFP	I/O	OD	Description	
CS0*		T11	191	O	4	Chip select (boot select)	
CS1*	RAS1*	R12	192	O	4	Chip select	DRAM RAS*
CS2*	RAS2*	P12	193	O	4	Chip select	DRAM RAS*
CS3*	RAS3*	U11	194	O	4	Chip select	DRAM RAS*
CS4*	RAS4*	T12	195	O	4	Chip select	DRAM RAS*
CAS3*	SDRAS*	T13	199	O	4	DRAM column strobe D31:24	SDRAM RAS*
CAS2*	SDCAS*	U12	198	O	4	DRAM column strobe D23:16	SDRAM CAS*
CAS1*	SDWE*	P13	197	O	4	DRAM column strobe D15:08	SDRAM WE*
CAS0*	SD(AP)	R13	196	O	4	DRAM column strobe D07:00	SDRAM (AP)
WE*		R11	190	O	4	Write enable	
OE*		P11	189	O	4	Output enable	

Ethernet interface

MII	10BaseT	BGA	PQFP	I/O	OD	MII	10BaseT
MDC	LB*	D7	85	O	2	MII clock	Loopback enable
MDIO	UTPSTP*	C7 †	84	I/O	2	MII data	Cable type
TXCLK	TXCLK	B8	83	I		TX clock	
TXD0	TXD	A9	82	O	2	TX data 0	TX data
TXD1	PDN* (OD)	D8	81	O	2	TX data 1	Power down
TXD2	NTHRES	C8	80	O	2	TX data 2	Normal threshold
TXD3	THIN	D9	77	O	2	TX data 3	Enable Thinnet
TXER	LTE	C9	76	O	2	TX code error	Link test enable
TXEN	TXEN	B10	75	O	2	TX enable	
COL	TXCOL	A11	74	I		Collision	
CRS	RXCRS	D10	73	I		Carrier sense	
RXCLK	RXCLK	C10	72	I		RX clock	
RXD0	RXD	B11	71	I		RX data 0	RX data
RXD1	MANSENSE	A12	70	I		RX data 1	Sense jumper
RXD2	JABBER	D11	69	I		RX data 2	Jabber
RXD3	REVPOL	C11	68	I		RX data 3	Reverse polarity
RXER	LINKPUL*	B12	67	I		RX error	Link pulse detection
RXDV	AUTOMAN	A13	66	I		RX data valid	10B2 selected

UARTs, SPI, and GPIO

GPIO	UART / HDLC	Special / DMA mode	BGA	PQFP	I/O	OD	SPI slave mode	SPI master mode
PORTA7	TXDA		G17 †	38	I/O	2	SPI-S-TXD-O-A	SPI-M-TXD-O-A
PORTA6	DTRA*	DRQ1*	F16 †	39	I/O	2		
PORTA5	RTSA*		E15 †	40	I/O	2		
PORTA4		RXCA	E14 †	41	I/O	2	SPI-S-CLK-I-A	SPI-M-CLK-O-A
PORTA3	RXDA		F17 †	42	I/O	2	SPI-S-RXD-I-A	SPI-M-RXD-I-A
PORTA2	DSRA*	DAK1*	E16 †	43	I/O	2		
PORTA1	CTSA*		D15 †	44	I/O	2		
PORTA0	DCDA*	DON1*	D14 †	45	I/O	2		
PORTB7	TXDB		E17 †	46	I/O	2	SPI-S-TXD-O-B	SPI-M-TXD-O-B
PORTB6	DTRB*	DRQ2*	C15 †	47	I/O	2		
PORTB5	RTSB*		D16 †	48	I/O	2	Reject* Ethernet packet	
PORTB4		RXCB	D17 †	49	I/O	2	SPI-S-CLK-I-B	SPI-M-CLK-O-B
PORTB3	RXDB		C17 †	50	I/O	2	SPI-S-RXD-I-B	SPI-M-RXD-O-B
PORTB2	DSRB*	DAK2*	C16 †	51	I/O	2		
PORTB1	CTSB*		B16 †	54	I/O	2	RPSF* Ethernet frame boundary	
PORTB0	DCDB*	DON2*	A16 †	55	I/O	2		
PORTC7		TXCA	A15 †	56	I/O	2	SPI-S-EN-I-A	SPI-M-EN-O-A
PORTC6	RIA*	IRQO*	C14 †	57	I/O	2		
PORTC5		TXCB	B15 †	58	I/O	2	SPI-S-EN-I-B	SPI-M-EN-O-B
PORTC4	RIB*		A14 †	59	I/O	2		
PORTC3		AMUX	D13 †	60	I/O	8	Interrupt 3	
PORTC2			C13 †	61	I/O	8	Interrupt 2	
PORTC1			B14 †	62	I/O	8	Interrupt 1	
PORTC0			B13 †	63	I/O	8	Interrupt 0	

ENI/Parallel 1284 Interface

IEEE1284	ENI	GPIO	BGA	PQFP	I/O	OD	Description
PDATA0	PDATA0	GPIOD0	R14 †	200	I/O	2	
PDATA1	PDATA1	GPIOD1	P14 †	201	I/O	2	
PDATA2	PDATA2	GPIOD2	U13 †	202	I/O	2	
PDATA3	PDATA3	GPIOD3	R15 †	203	I/O	2	
PDATA4	PDATA4	GPIOD4	T14 †	204	I/O	2	
PDATA5	PDATA5	GPIOD5	U14 †	205 †	I/O	2	
PDATA6	PDATA6	GPIOD6	U15 †	206	I/O	2	
PDATA7	PDATA7	GPIOD7	T15 †	207	I/O	2	
POE1*	PDATA8		T16 †	2	I/O	2	
POE2*	PDATA9		T17 †	3	I/O	2	
POE3*	PDATA10		R17 †	4	I/O	2	
POE4*	PDATA11		P15 †	5	I/O	2	
PCLKC1	PDATA12		R16 †	6	I/O	2	
PCLKC2	PDATA13		P17 †	7	I/O	2	
PCLKC3	PDATA14		N14 †	8	I/O	2	
PCLKC4	PDATA15		N15 †	9	I/O	2	
PCLKD1	PACK*	GPIOF7	G16	35	I/O	8	
PCLKD2	PEN*	GPIOF6	P16 †	10	I/O	2	
PCLKD3	PINT1*	GPIOF5	N16	11	I/O	2	
PCLKD4	PINT2*	GPIOF4	M15	12	I/O	2	Or ENI DMA output PDRQIO
ACK1*	PA0	GPIH0	M14	13	I		
ACK2*	PA1	GPIH1	N17	14	I		
ACK3*	PA2	GPIH2	M16	15	I		
ACK4*	PA3	GPIH3	L15	16	I		
BUSY1	PA4	GPIH4	L14	17	I		
BUSY2	PA5	GPIOH5	M17	18	I		
BUSY3	PA6	GPIH6	L16	19	I		
BUSY4	PA7	GPIH7	K15	20	I		
PE1	PA8	GPIG0	K14	21	I		
PE2	PA9	GPIG1	L17	22	I		
PE3	PA10	GPIG2	K16	23	I		
PE4	PA11	GPIG3	J15	24	I		

ENI/Parallel 1284 Interface (cont.)

IEEE1284	ENI	GPIO	BGA	PFQP	I/O	OD	Description
PSELECT1	PA12	GPIG4	J14	25	I		
PSELECT2	PA13	GPIOF3	H15	28	I/O	2	Or ENI DMA output PDRQI*
PSELECT3	PA14	GPIOF2	H14	29	I/O	2	Or ENI DMA output PDRQO*
PSELECT4	PA15	GPIG5	J17	30	I		Or ENI DMA input PDACK*
FAULT1*	PA16	GPIG6	H16	31	I		
FAULT2*	PCS*	GPIG7	H17	34	I		
FAULT3*	PRW*	GPIOF0	G14	33	I/O	2	
FAULT4*	PBRW*	GPIOF1	G15	32	I/O	2	

Clock generation

Signal	BGA	PQFP	I/O	OD	Description
XTAL1	U7	178	I		2.5 V crystal oscillator circuit
XTAL2	T8	179	O		
PLLVDD	U8	182			2.5 V PLL clean power
PLLLPF	P9	181			PLL loop filter capacitor
PLLVSS	R9	180			PLL clean ground
PLLTST*	P8 †	177	I		2.5 V PLL test mode
BISTEN*	R10 †	184	I		Enable internal BIST operation
SCANEN*	P10 †	185	I		Enable internal SCAN testing

System reset

Signal	BGA	PQFP	I/O	OD	Description
RESET*	T2 †	158	I		System reset *

Debug support for ARM core

Signal	BGA	PQFP	I/O	OD	Description
TDI	T6 †	171	I		Test data in
TDO	U5	170	O	2	Test data out
TMS	R7 †	172	I		Test mode select
TRST*	R8	174	I		Test mode reset (input current sink)
TCK	P7	173	I		Test mode clock

Power supply

Signal	BGA	PQFP	Description
V_{CC} DC 3.3 V DC	F15, B17, C12, A2, M2, U9	36, 52, 64, 104, 143, 186	I/O steady state (6 pairs)
V_{SS} DC Gnd Returns	F14, A17, D12, A1, N3, U10	37, 53, 65, 105, 144, 188	
V_{CC} AC 3.3 V	A8, E1, T1, U16	86, 118, 156, 208	I/O switching (4 pairs — see note below on 3.3 V power and GND pads)
V_{SS} AC Gnd Return	B7, F2, U1, U17	87, 119, 157, 1	
V_{DD} CO 2.5 V	K17, A10, H1, T7	26, 78, 130, 175	Core power (4 pairs)
V_{SS} CO Gnd Returns	J16, B9, J2, U6	27, 79, 131, 176	
PLL V_{DD} 2.5 V	U8	182	PLL bead filtered clean power
PLL V_{SS} Gnd Return	R9	180	Power-up reset ground reference
POR V_{SS} Gnd	T9	183	

Additional information about NET+50 pins

- All outputs drive TTL levels. Outputs drive to 0.4 V maximum on low, 2.4 V minimum on high.
- The following pins require a 2.5 V input level:

Signal	BGA	PQFP
XTAL1	U7	178
PLLTST	P8	177
PLLVDD	U8	182

- TRST* (R8, 174) is the only pin that is an input current sink.
- Remaining inputs are TTL levels and are 3.3 V tolerant, allowing integration with 3.3 V devices.
- Regarding 3.3 V power and GND pads: In general, you should use separate power pairs for AC and DC power to prevent the noise in the AC power buses from reaching the DC power buses. Digi recommends (and uses) a ferrite bead to filter the AC power pins.

Registers and addresses

General control module

Address	Register	Address	Register
0xFFB0 0000	System control register	0xFFB0 0024	Port B register
0xFFB0 0004	System status register	0xFFB0 0028	Port C register
0xFFB0 0008	PLL control register	0xFFB0 0030	Interrupt enable register
0xFFB0 000C	Software service register	0xFFB0 0034	Interrupt enable register — Set
0xFFB0 0010	Timer 1 control register	0xFFB0 0038	Interrupt enable register — Clear
0xFFB0 0014	Timer 1 status register	0xFFB0 0034	Interrupt status register — Enabled
0xFFB0 0018	Timer 2 control register	0xFFB0 0038	Interrupt status register — Raw
0xFFB0 001C	Timer 2 status register	0xFFB0 0040	Cache control register 0
0xFFB0 0020	Port A register	0xFFB0 0044	Cache control register 1

Memory module controller

Address	Register	Address	Register
0xFFC0 0000	Memory module configuration register (MMCR)	0xFFC0 0034	Chip select 2 option register (OR2)
0xFFC0 0010	Chip select 0 base address register (BAR0)	0xFFC0 0038	Chip select 2 option register B (OR2B)
0xFFC0 0014	Chip select 0 option register (OR0)	0xFFC0 0040	Chip select 3 base address register (BAR3)
0xFFC0 0018	Chip select 0 option register B (OR0B)	0xFFC0 0044	Chip select 3 option register (OR3)
0xFFC0 0020	Chip select 1 base address register (BAR1)	0xFFC0 0048	Chip select 3 option register B (OR3B)
0xFFC0 0024	Chip select 1 option register (OR1)	0xFFC0 0050	Chip select 4 base address register (BAR4)
0xFFC0 0028	Chip select 1 option register B (OR1B)	0xFFC0 0054	Chip select 4 option register (OR4)
0xFFC0 0030	Chip select 2 base address register (BAR2)	0xFFC0 0058	Chip select 4 option register B (OR4B)

DMA controller module

DMA register key: 0xFF90*nnnn* where *nnnn* = DMAx + Offset							
DMA*x*:						**Offset:**	
1A:	00	2:	80	6:	100	00	Buffer descriptor pointer
1B:	20	3:	A0	7:	120	10	Buffer control register
1C:	40	4:	C0	8:	140	14	Buffer status register
1D:	60	5:	E0	9:	160		
				10:	180		

Examples:	
0xFF90 0000	DMA 1A buffer descriptor pointer
0xFF90 0010	DMA 1A buffer control register
0xFF90 0014	DMA 1A buffer status register

Ethernet controller module

Address	Register	Address	Register
0xFF80 0000	General control register	0xFF80 0440 – 0478	Transmit control registers
0xFF80 0004	General status register	0xFF80 0480 – 0488	Receive control registers
0xFF80 0008	FIFO data register	0xFF80 040C0	Link fail counter
0xFF80 000C	FIFO last word data register	0xFFB0 0500	10 Mbit jabber counter
0xFF80 0010	TX status register	0xFFB0 0504	10 Mbit loss of carrier counter
0xFF80 0014	RX status register	0xFFB0 0540 – 0550	MII control registers
0xFF80 0400 – 0404	MAC configuration and test registers	0xFFB0 0580 – 059C	Status registers
0xFF80 0408 – 040C	PCS configuration and test registers	0xFFB0 05C0	SAL address filter register
0xFF80 0410 – 0414	STL configuration and test registers	0xFFB0 05C4 – 05DC	SAL hash table registers

Serial controller module

Address	Register	Address	Register
0xFFD0 0000 – 0030	Channel 1 registers	0xFFD0 0040 – 0070	Channel 2 registers

ENI controller module

Address	Register	Address	Register
0xFFA0 0000	General control register	0xFFA0 0030	ENI control register
0xFFA0 0004	General status register	0xFFA0 0034	ENI pulsed interrupt register
0xFFA0 0008	FIFO mode data register	0xFFA0 0038	ENI shared RAM address register
0xFFA0 0010 – 001C	IEEE1284 ports 1–4 control registers	0xFFA0 003C	ENI shared register
0xFFA0 0020 – 002C	IEEE 1284 ports 1–4 data registers	0xFFA0 0040 – 0050	GPIO ports D, F, G, H, and F registers

Test modes and PLL usage

The PLLTST*, BISTEN*, and SCANEN* primary inputs control test modes for test operations (in manufacturing) and for using an external oscillator instead of a crystal, as follows:

PLLTST*	BISTEN*	SCANEN*	Mode
1	1	1	Normal with PLL operational
0	1	1	Normal with PLL bypass
1	1	0	HiZ / Tri-state (manufacturing testing)

Note: All other combinations of these inputs are reserved.

PLL

When the PLLTST* signal is active low, the PLL is isolated, and the internal system clock is provided by the XTAL1 input (XTAL1 = SYSCLK). The PLL is not programmable. If you want to use the PLL (crystal) and get a system clock of 44.236 MHz, you must use an 18.432 MHz crystal.

HiZ/Tri-state

The NET+50 chip supports a way to tri-state all outputs. When both PLLTST* and BISTEN* are inactive (high) and SCANNEN* is active (low), all outputs are placed in a low current tri-state mode.

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

DC inputs

Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

DC outputs

Symbol	Characteristic	Conditions	Min.	Max.	Unit
V_{OL}	Output low voltage		0	0.4	V
V_{OH}	Output high voltage		2.4	V_{CC}	V
I_{OZ}	High-Z leakage current	$V_O = V_{SS}$	-10	10	µA
I_{OS}	Output short circuit current	V_{CC} = 3.6V, V_O (low) = V_{CC}		55	µA
		V_{CC} = 3.6V, V_O (high) = V_{SS}	-55		
C_{IO}	Input/output capacitance	Any input, output, or I/O		7	pF

DC absolute maximum voltages

Characteristic	Min.	Max.
Supply voltage 2.5 V — core	-0.3	3.15
Supply voltage 3.3 V — I/O	-0.3	4.00
Input voltage	-0.3	4.50
Output voltage	-0.3	4.50

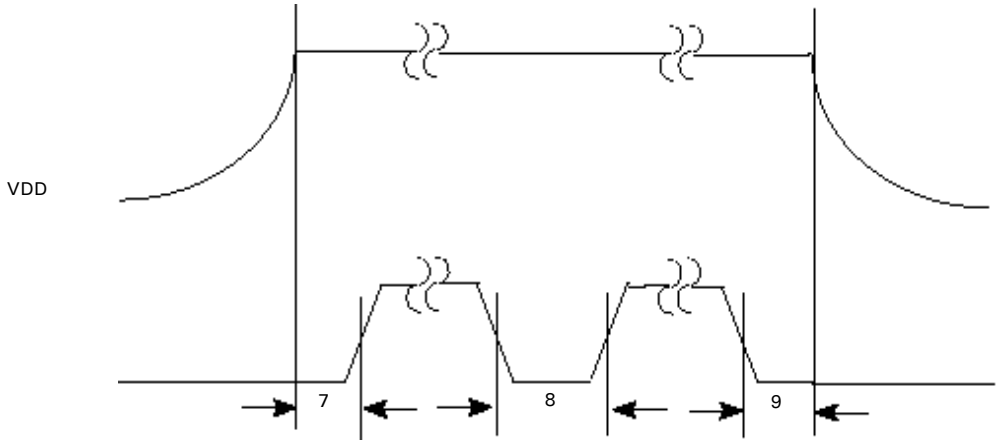
Temperature considerations

Characteristic	Min.	Max.
Thermal resistance — junction to ambient	37°C/W	
Operating junction temperature (°C)	-40°	100°
Operating ambient temperature (°C)	-40°	85°
Storage temperature (°C)	-60°	150°

Timing data and diagrams

Reset timing

Number	Characteristic	Min.	Max.	Unit
7	V_{DD} at 3.0 V to RESET* high	40		ms
8	RESET* pulse width low	$10/F_{SYSCLK}$		µs
9	RESET* low to V_{DD} below 3.0 V	$8/F_{SYSCLK}$		µs

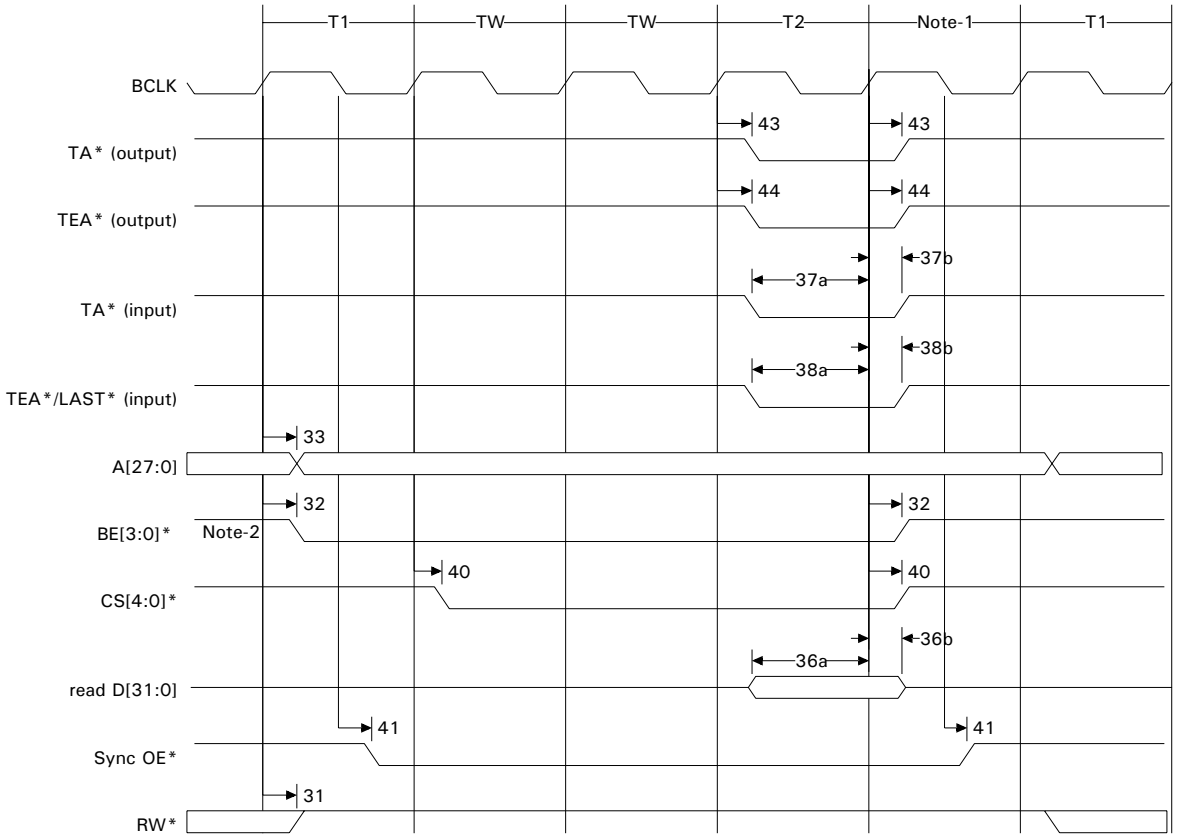


SRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
40	BCLK high to CS* valid		16
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14

Minimum and maximum are in nanoseconds (ns).

SRAM Sync Read (Wait = 2)



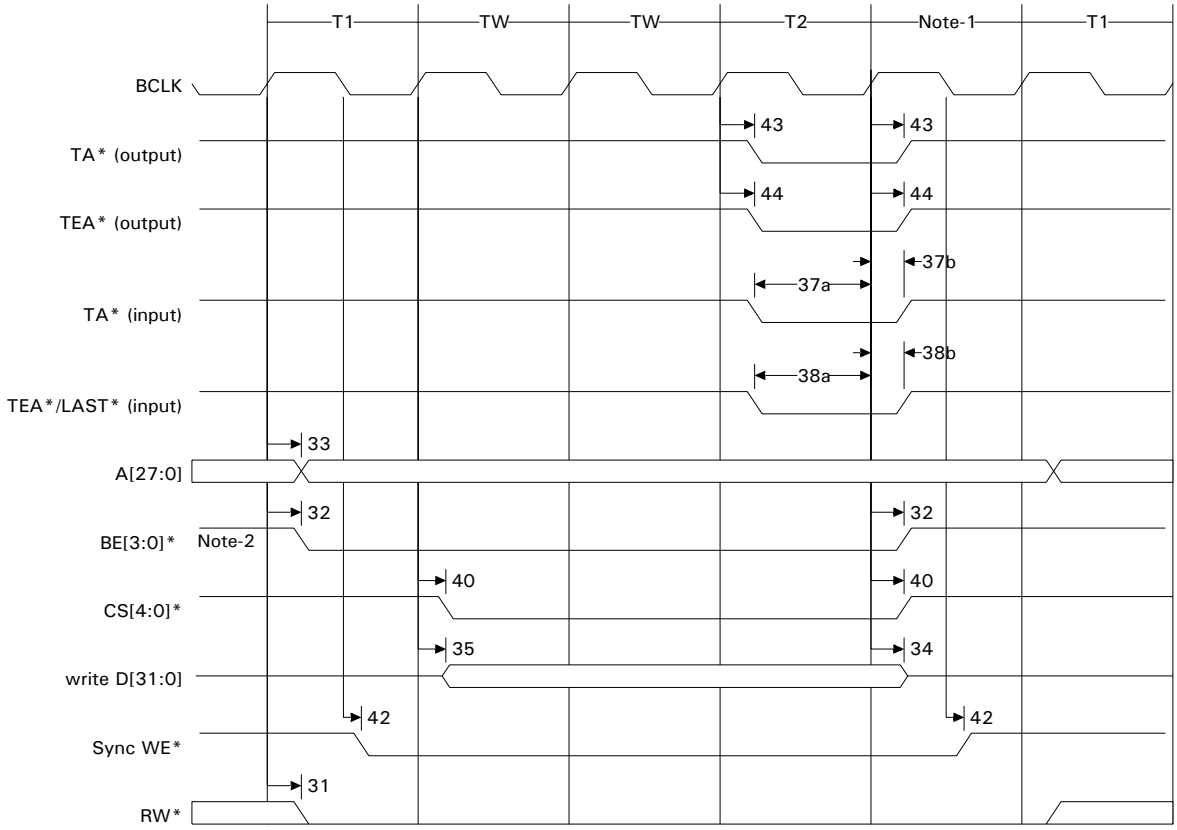
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Write (Wait = 2)



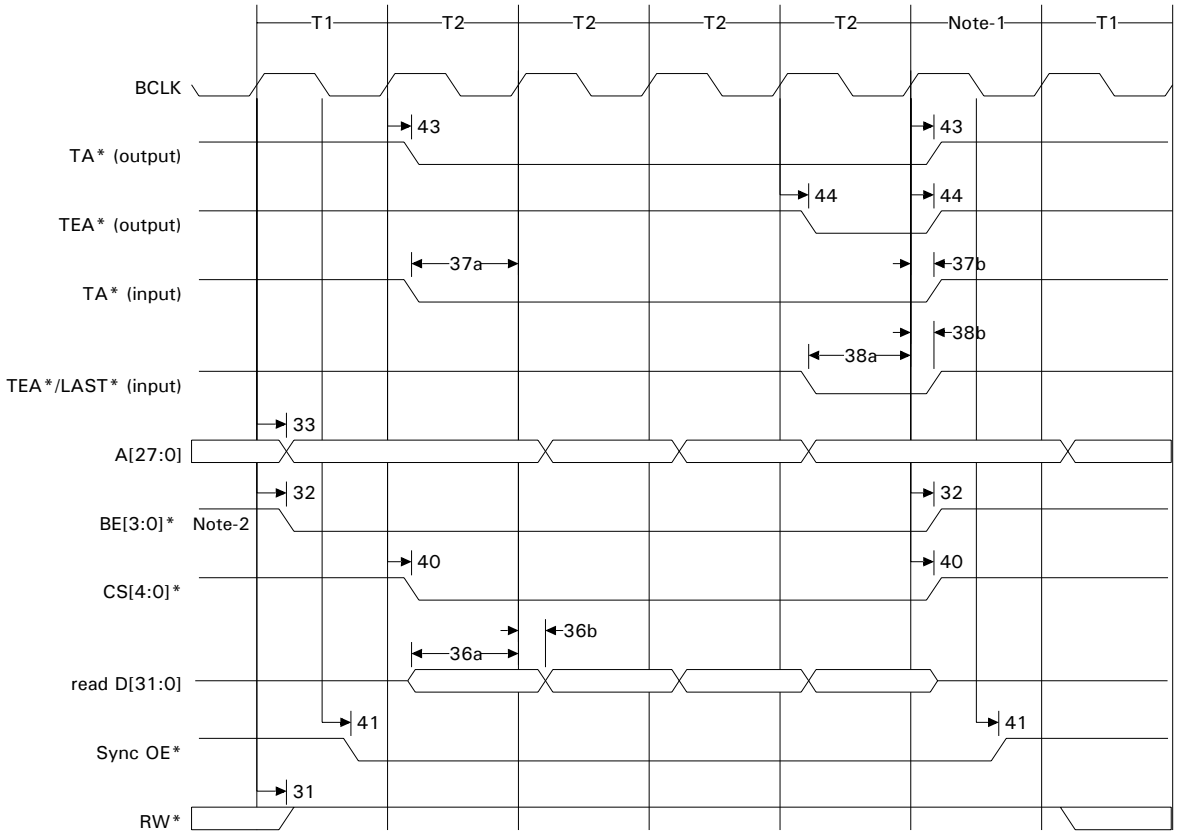
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)



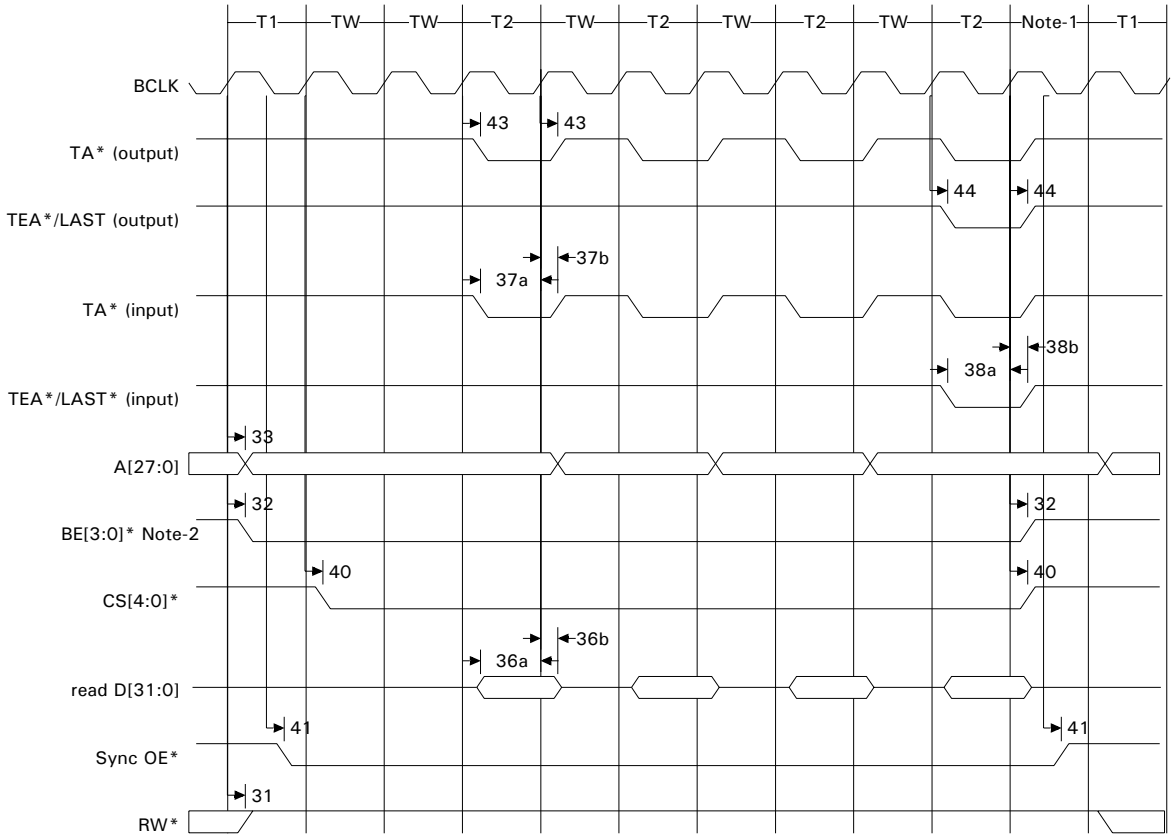
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Read (4-222, Wait = 2, BCYC = 01)



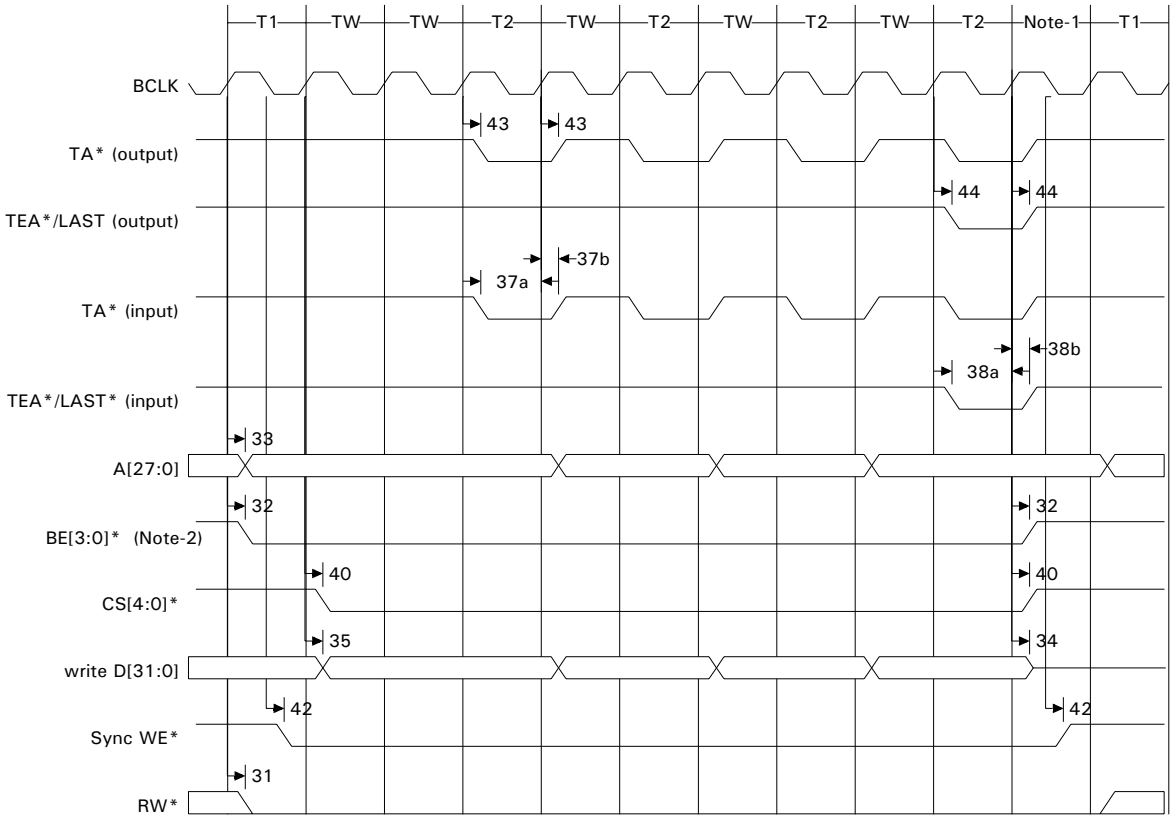
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Write (4-222, Wait = 2, BCYC = 01)



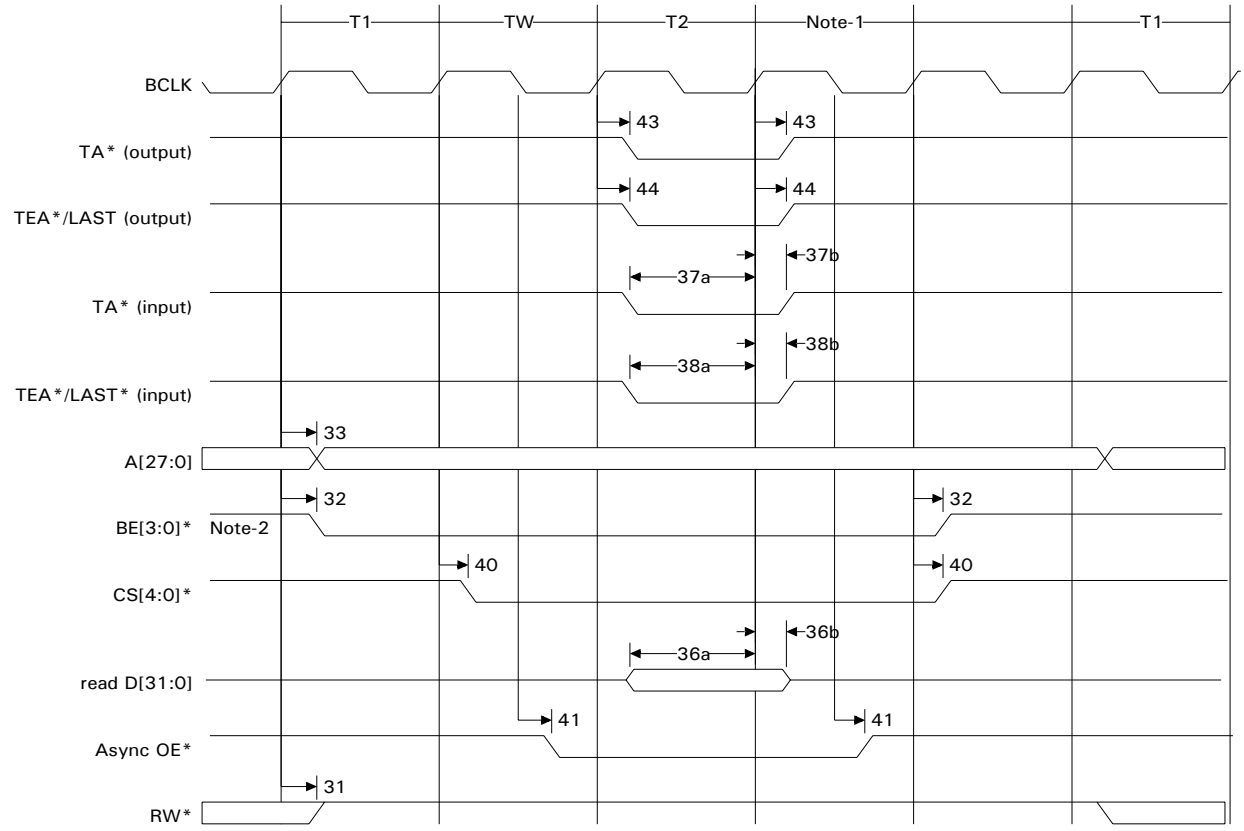
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Read (Wait = 2)



Notes:

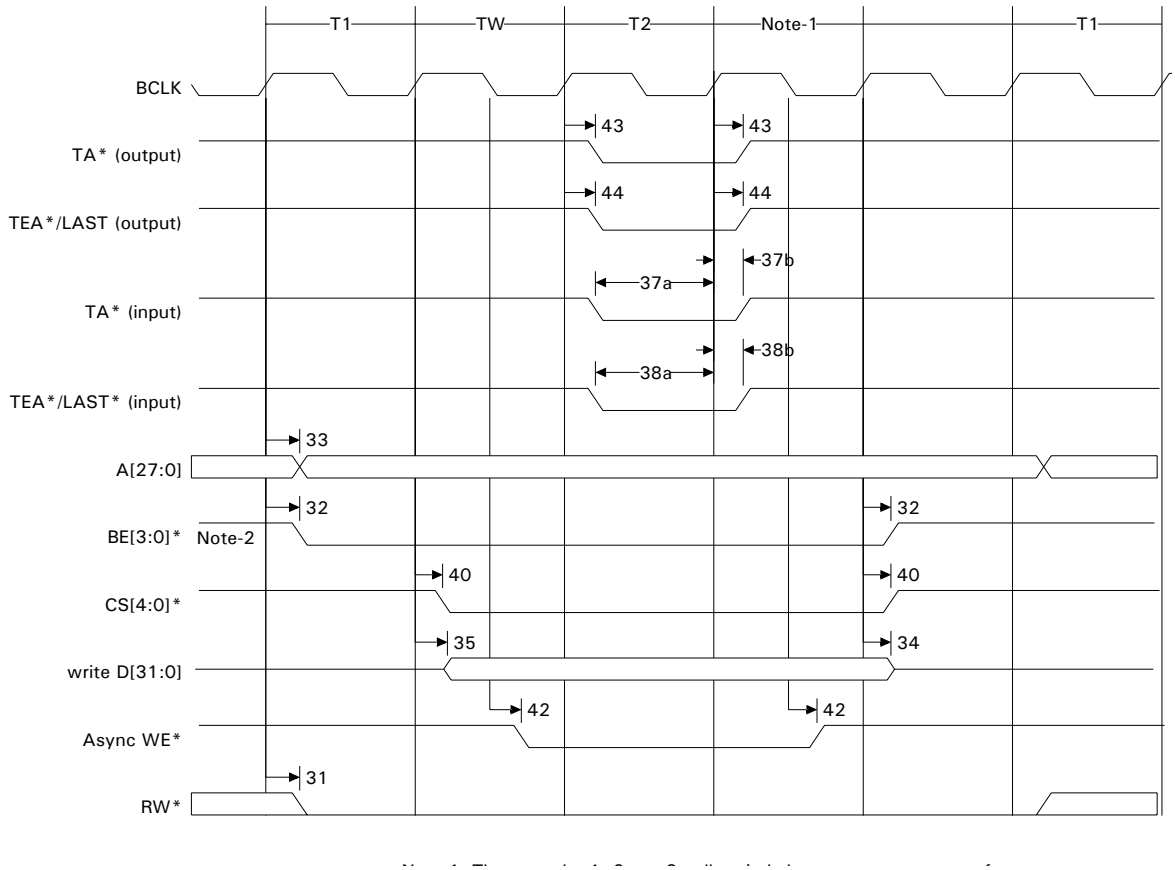
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Write (Wait = 2)



Notes:

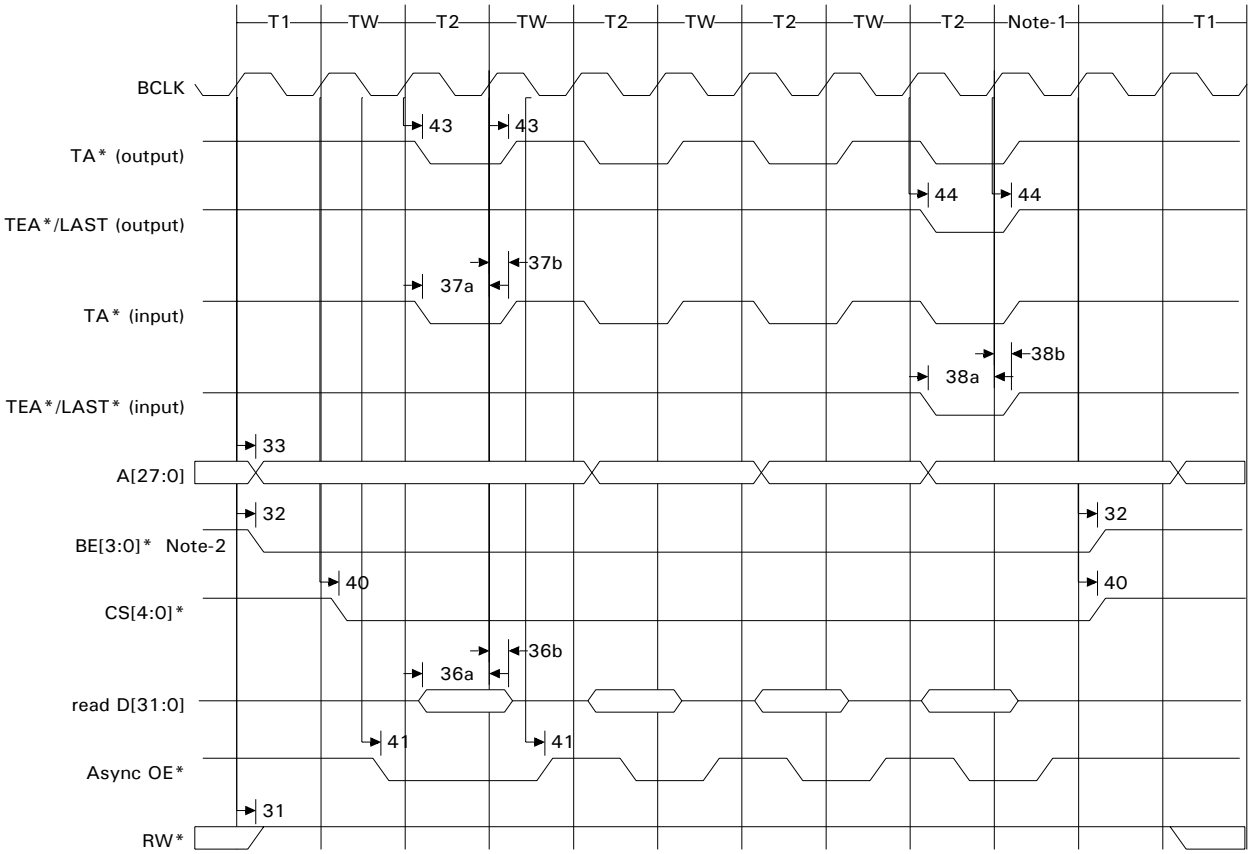
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Burst Read (Wait = 2, BCYC = 01)



Notes:

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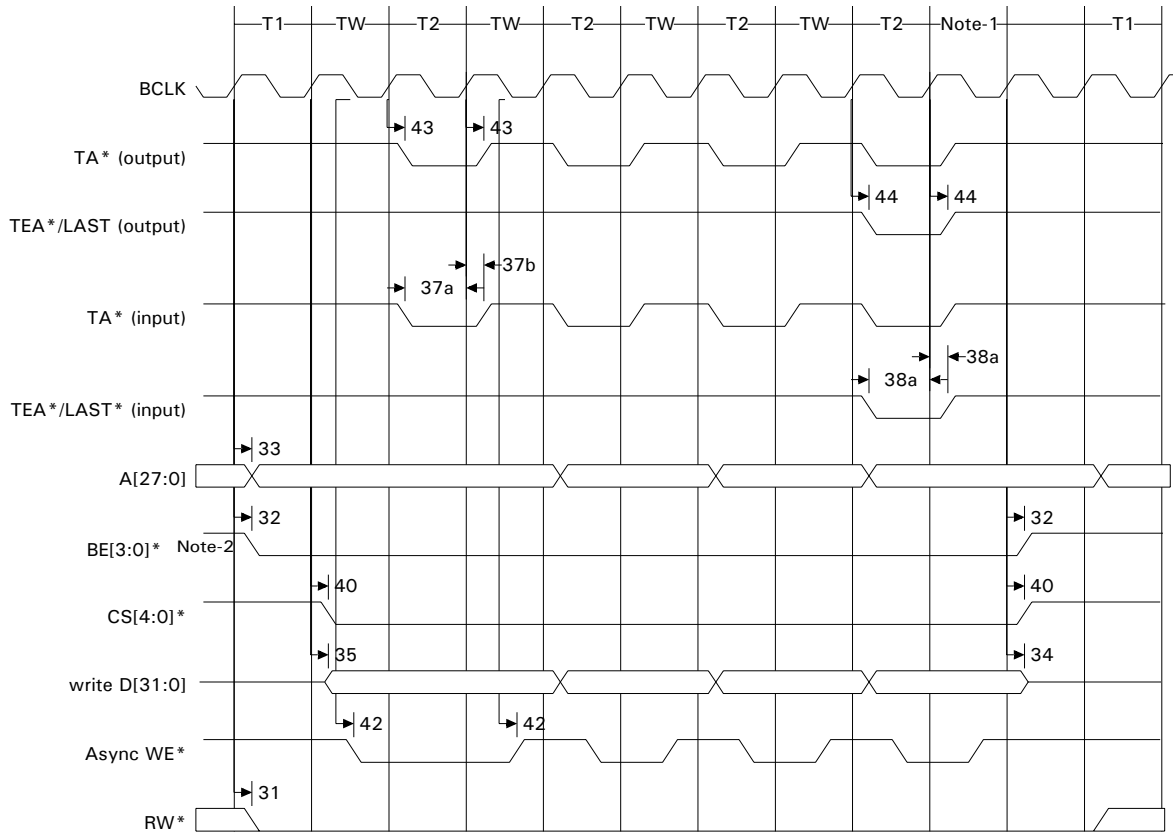
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Burst Write (Wait = 2, BCYC = 01)



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

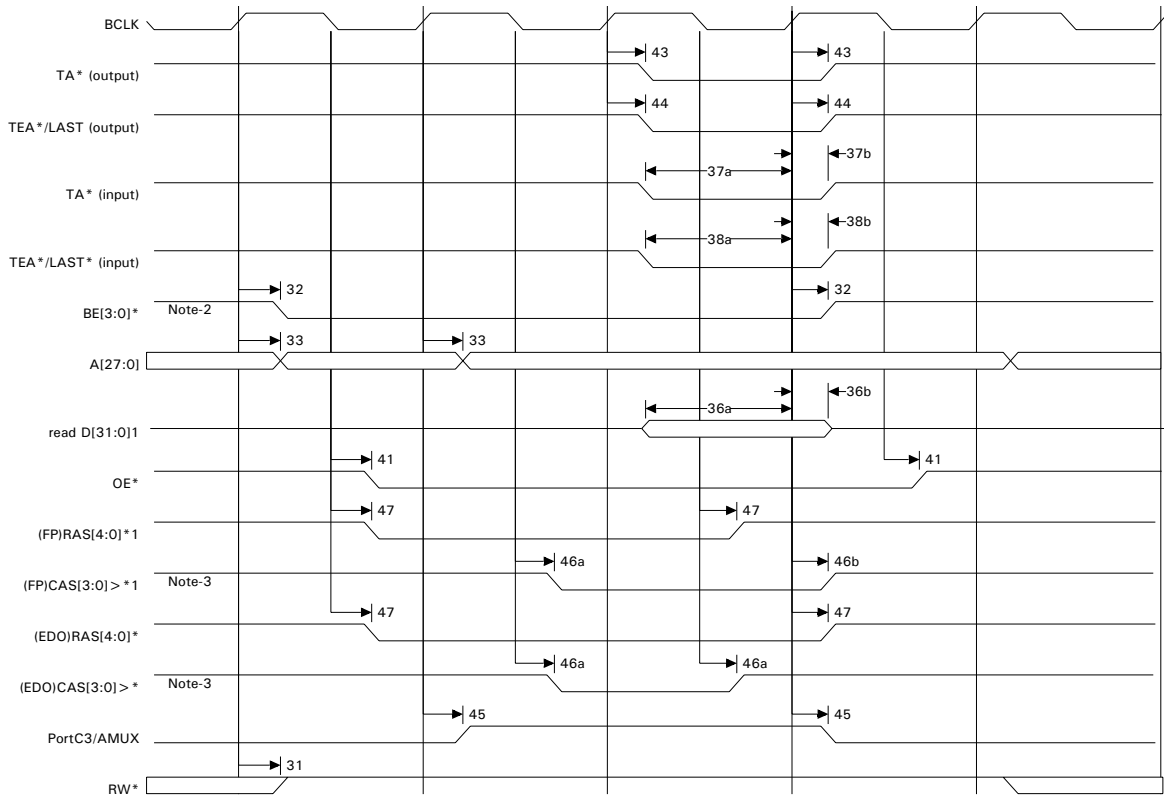
3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14
45	BCLK high to PORTC3/AMUX valid		8
46a	BCLK low to CAS* valid		13
46b	BCLK high to CAS* valid		13
47	BCLK low to RAS* valid		16

Minimum and maximum are in nanoseconds (ns).

Fast Page and EDO DRAM Read



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

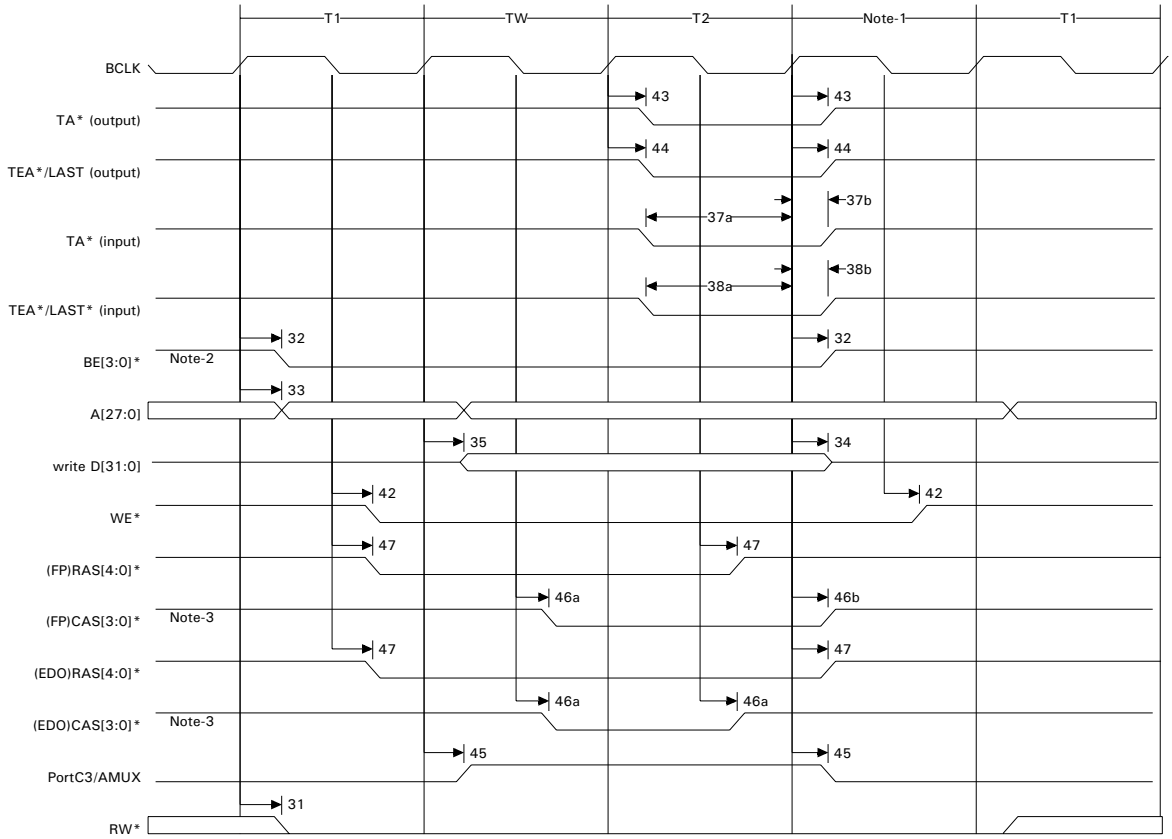
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

Fast Page and EDO DRAM Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

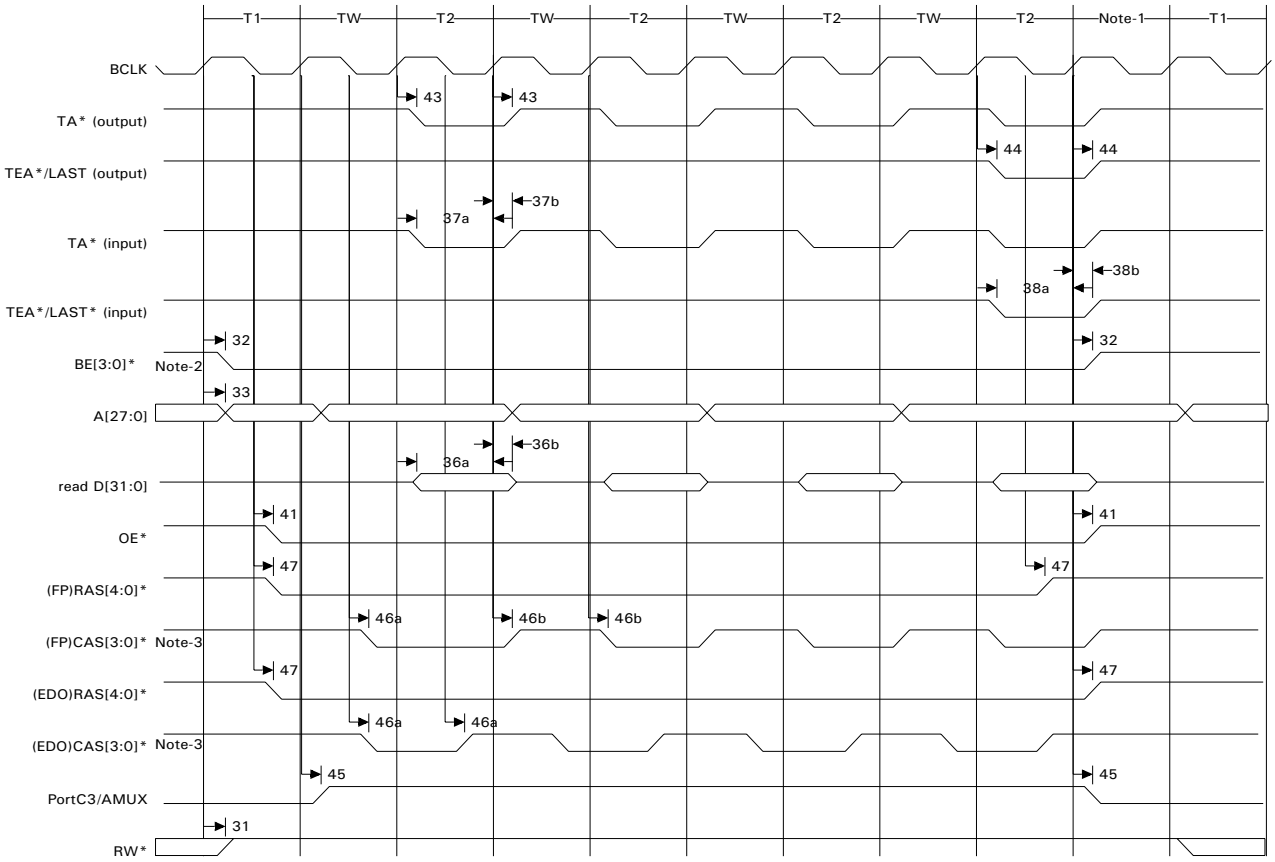
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

Fast Page and EDO DRAM Burst Read



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

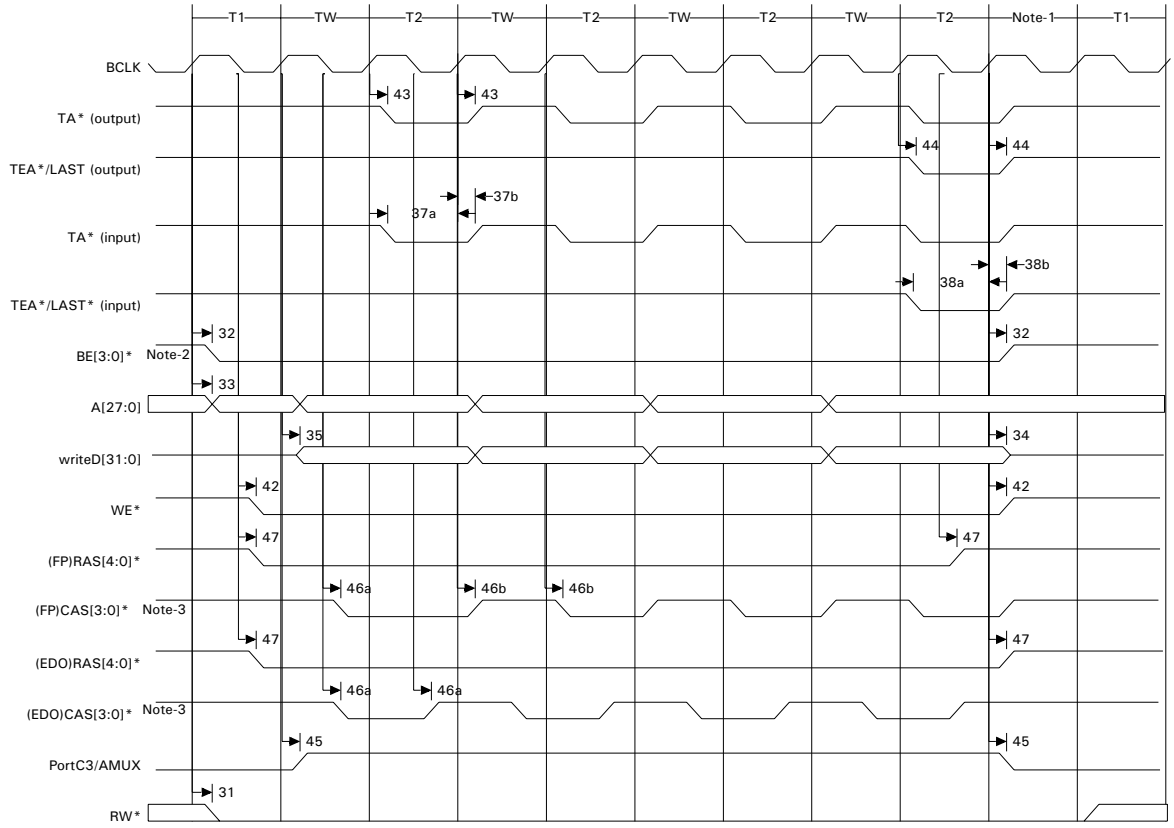
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

Fast Page and EDO DRAM Burst Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

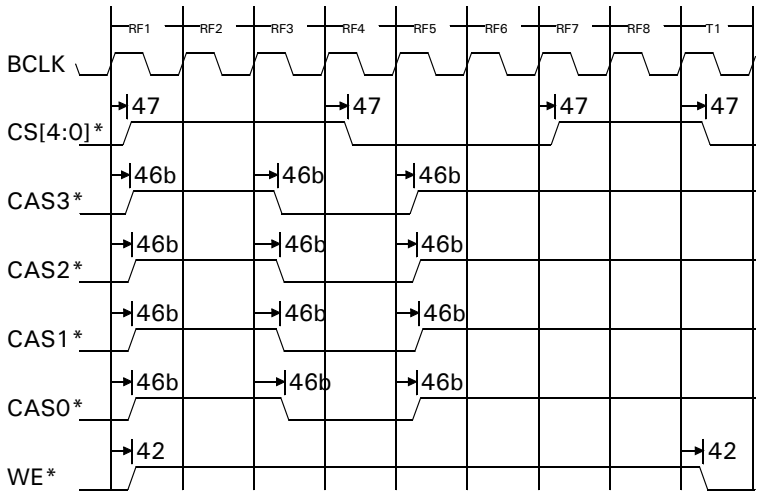
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

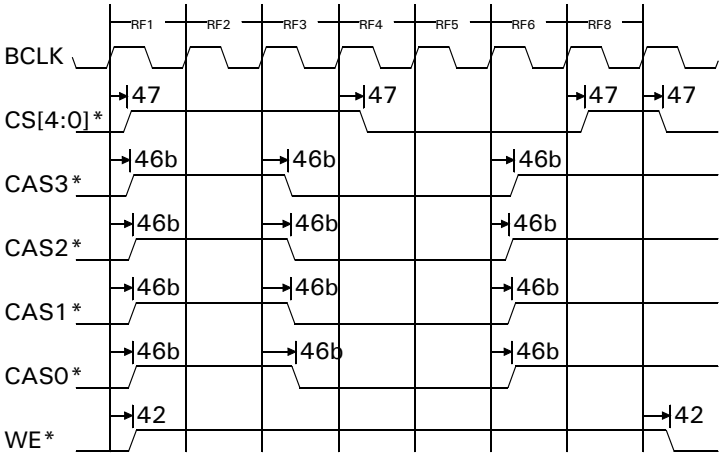
8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

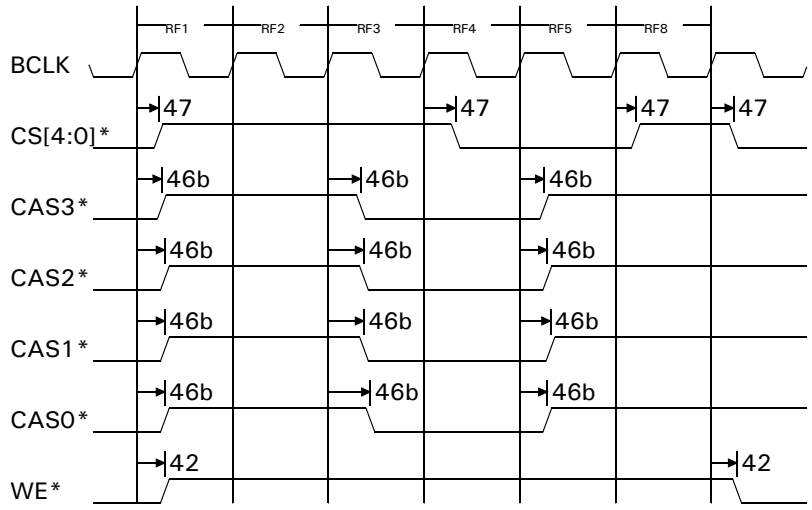
Fast Page and EDO DRAM Refresh (RCYC = 0)



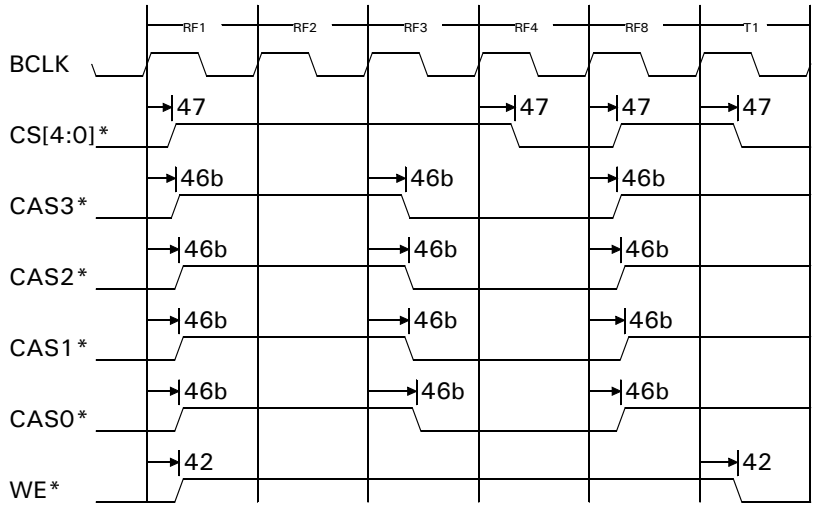
Fast Page and EDO DRAM Refresh (RCYC = 1)



Fast Page and EDO DRAM Refresh (RCYC = 2)



Fast Page and EDO DRAM Refresh (RCYC = 3)

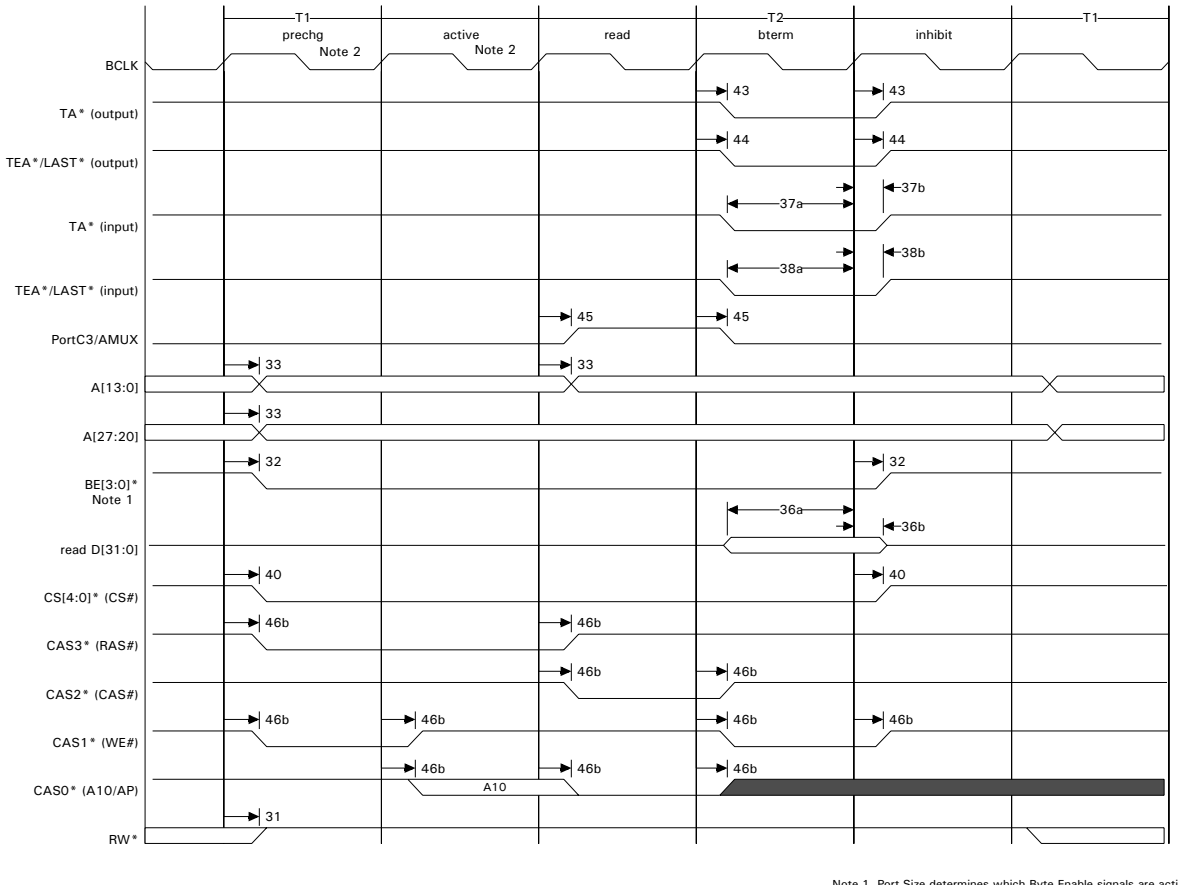


SDRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
40	BCLK high to CS* valid		16
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14

Minimum and maximum are in nanoseconds (ns).

SDRAM Read (CAS Latency = 1)



Note 1. Port Size determines which Byte Enable signals are active

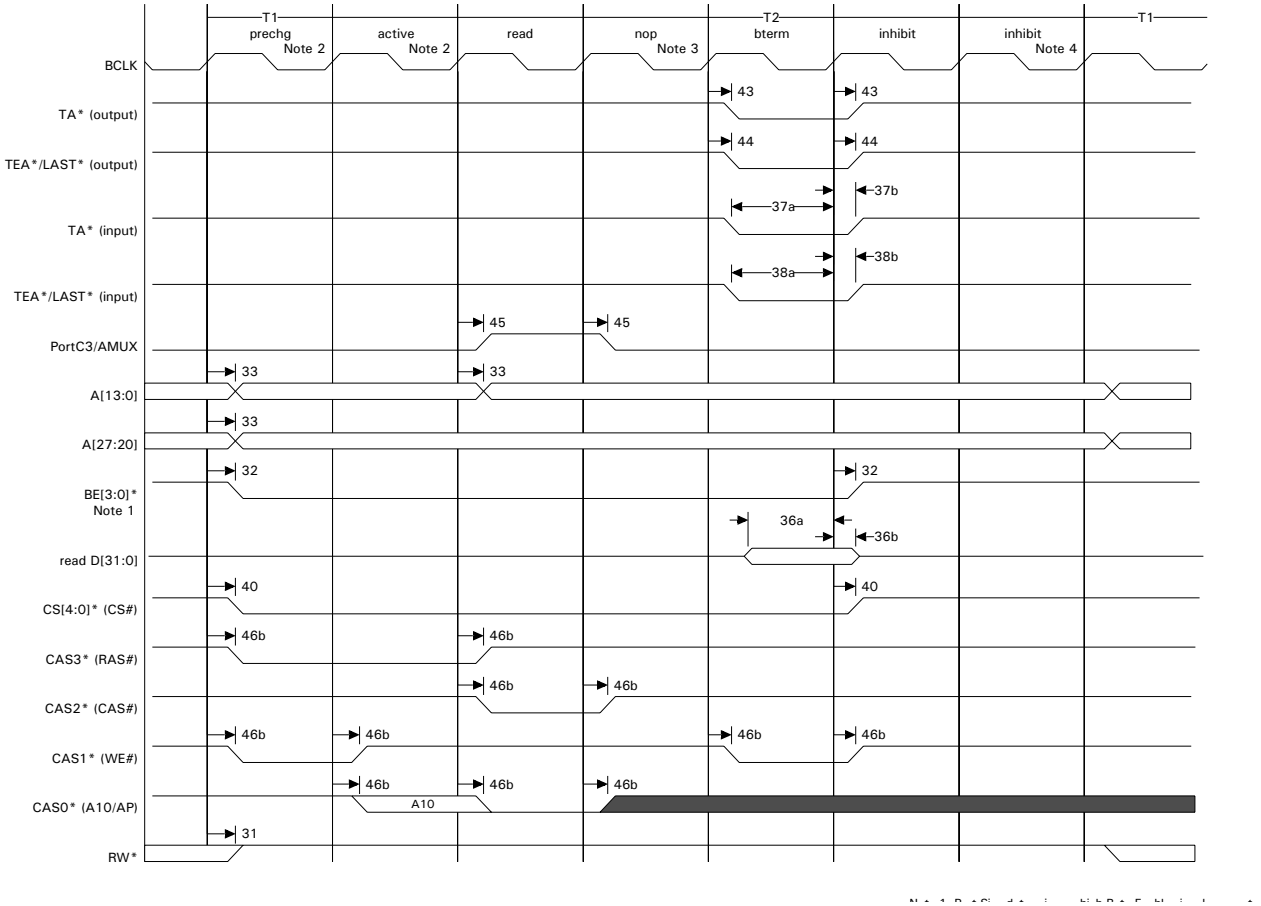
Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

SDRAM Read (CAS Latency = 2)



Notes:

1 Port size determines which byte enable signals are active:

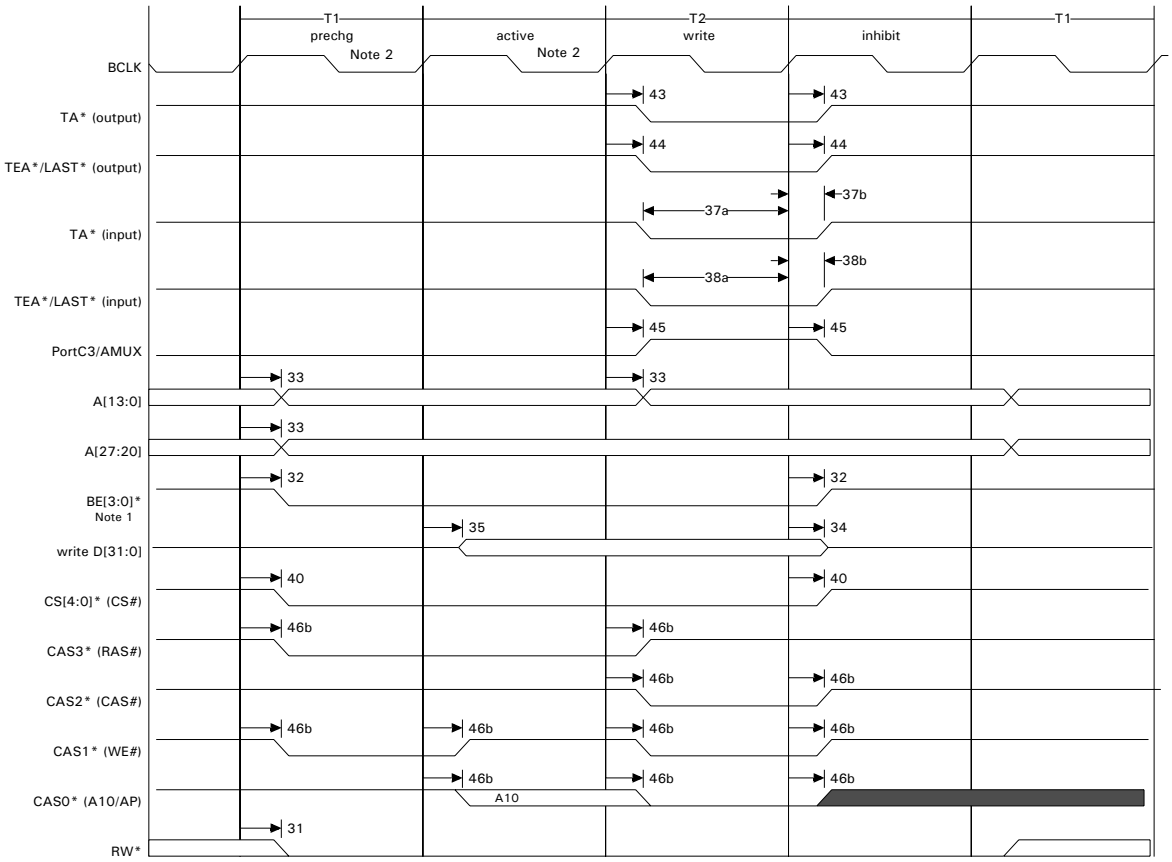
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

3 If CAS latency = 3, there are:

- Two NOPs between the Read and Burst Terminate commands
- Three Inhibit commands after the Burst Terminate command

SDRAM Write



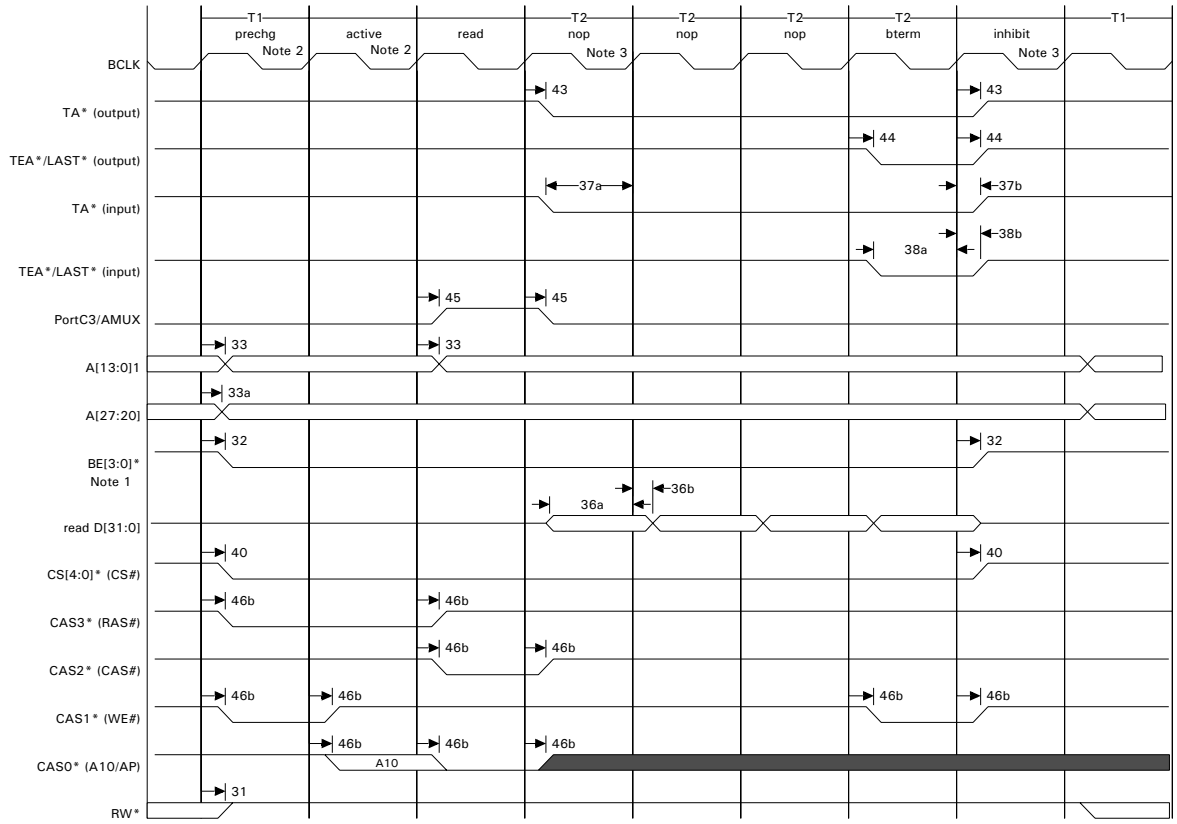
Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

SDRAM Burst Read (CAS Latency = 1)



Notes:

1 Port size determines which byte enable signals are active:

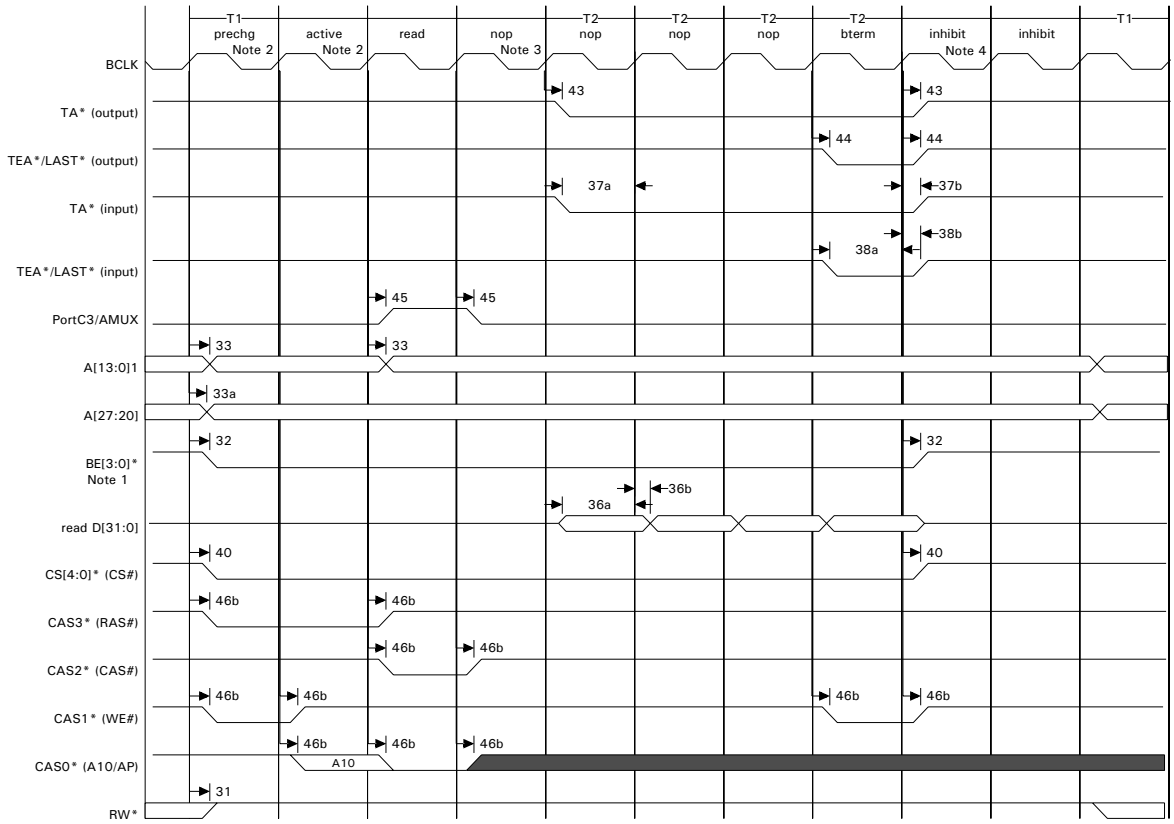
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

3 If CAS latency = 3, there are:

- Two NOPs between the Read and Burst Terminate commands
- Three Inhibit commands after the Burst Terminate command

SDRAM Burst Read (CAS Latency = 2)



Notes:

1 Port size determines which byte enable signals are active:

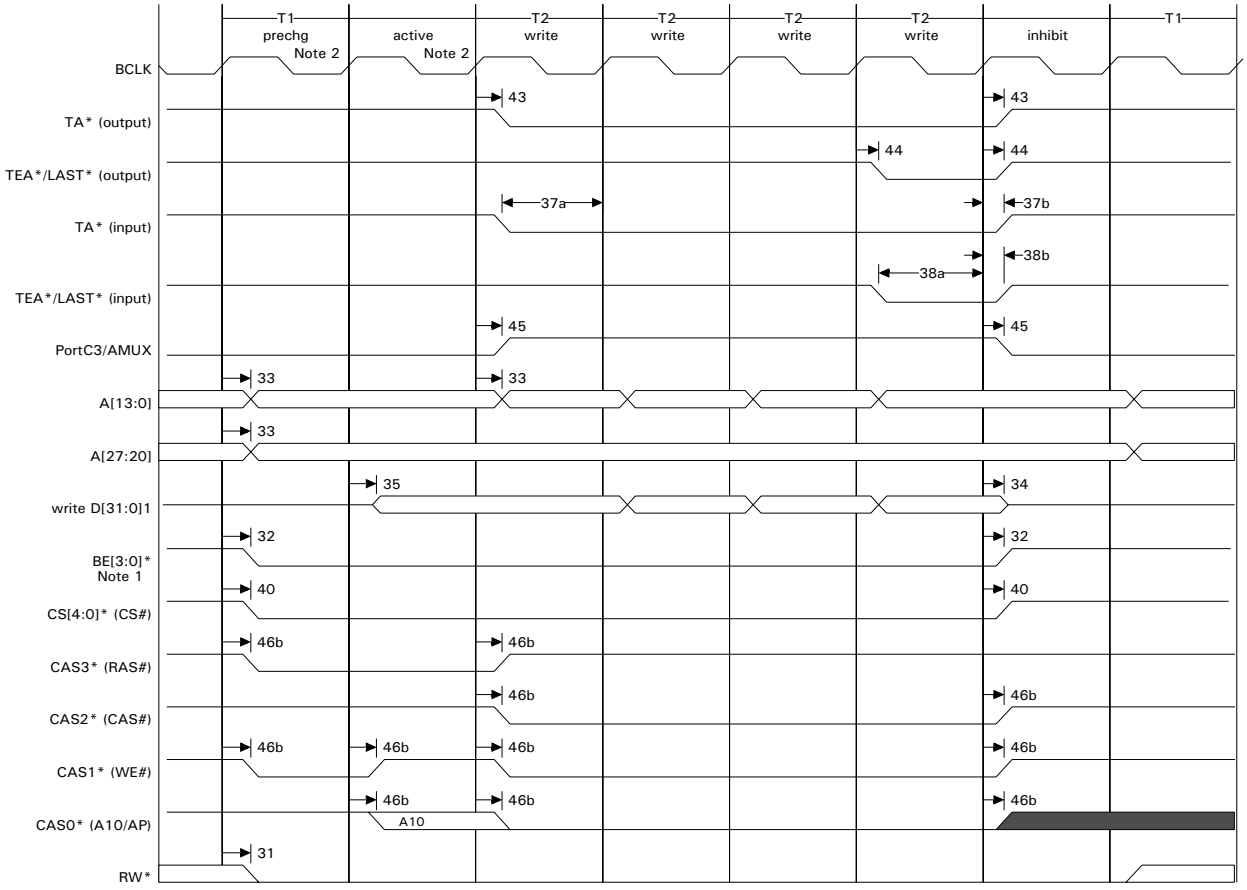
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

3 If CAS latency = 3, there are:

- 5 NOPs between the Read and Burst Terminate commands
- 3 Inhibit commands after the Burst Terminate command

SDRAM Burst Write



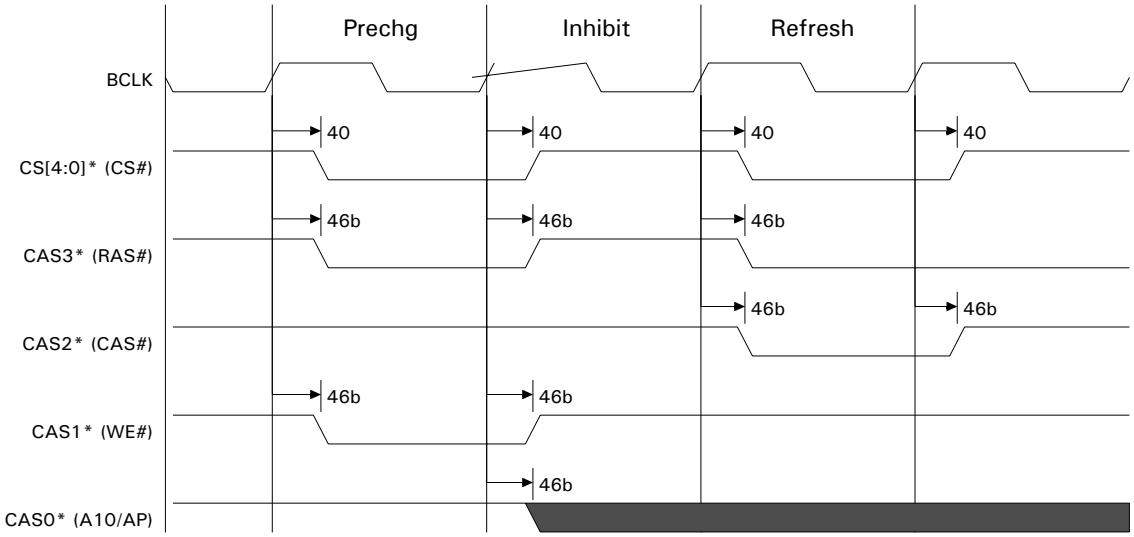
Notes:

1 Port size determines which byte enable signals are active:

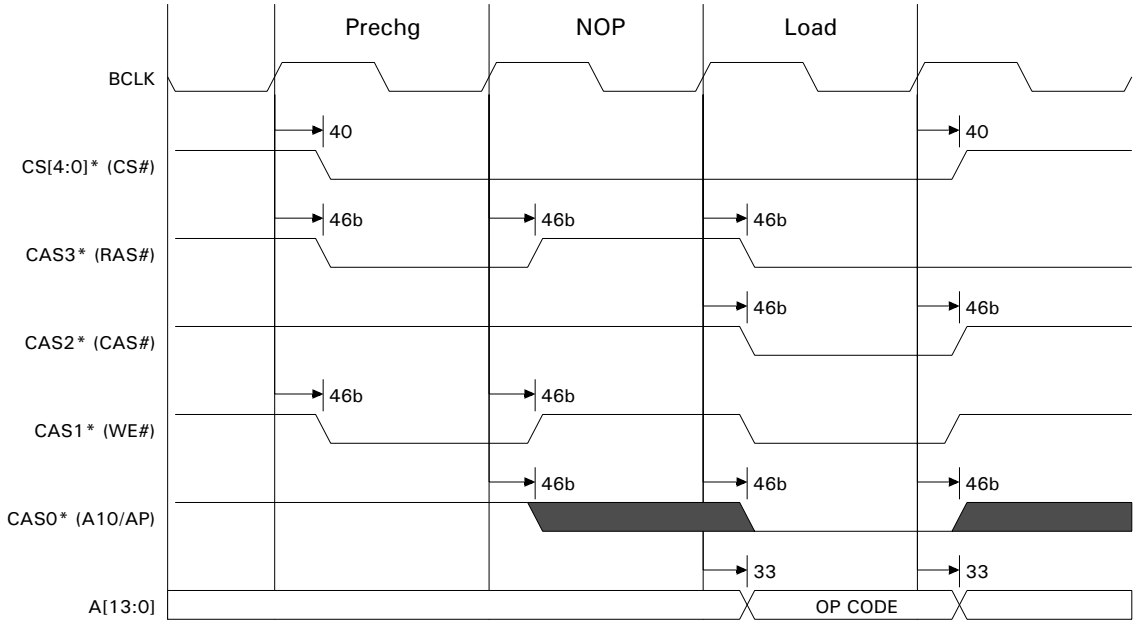
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

SDRAM Refresh Command



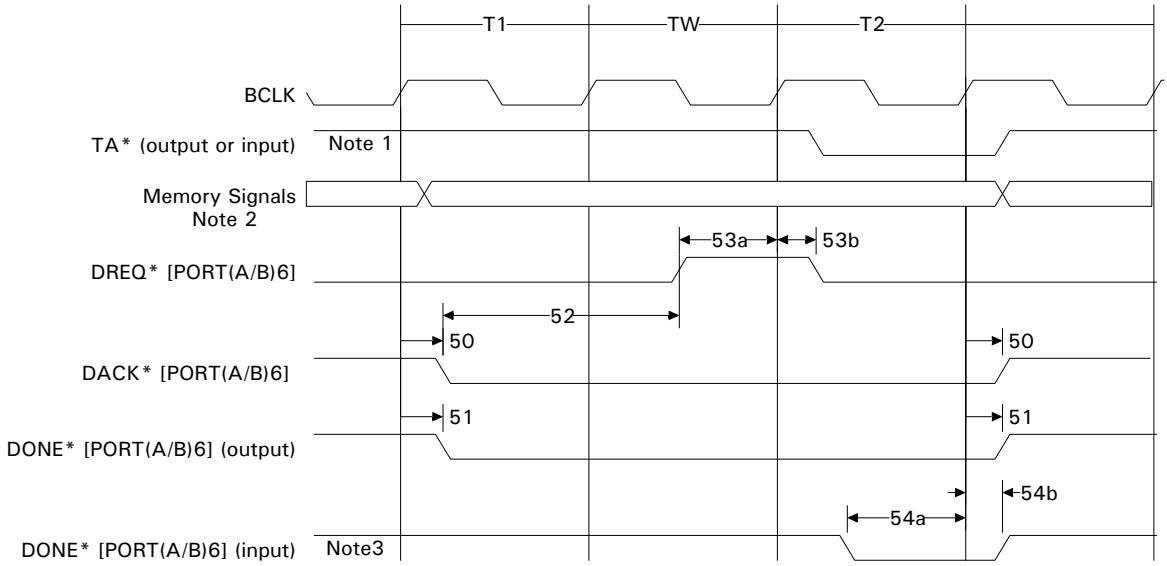
SDRAM Load Mode Command



External DMA timing

Number	Characteristic	Min.	Max.
50	BCLK High to DACK* valid		26
51	BCLK High to DONE* (output) valid		27
52	DACK* low to DREQ* high	0	
53a	DREQ* valid to BCLK high (setup)	11	
53b	BCLK high to DREQ* valid (hold)	0	
54a	DONE* (input) valid to BCLK high (setup)	14	
54b	BCLK high to DONE* (input) valid (hold)	0	
	Minimum and maximum are in nanoseconds (ns).		

External Fly-By DMA



Notes:

1 TA* is shown here for reference. Its timing is available on the diagrams referenced on page 46.

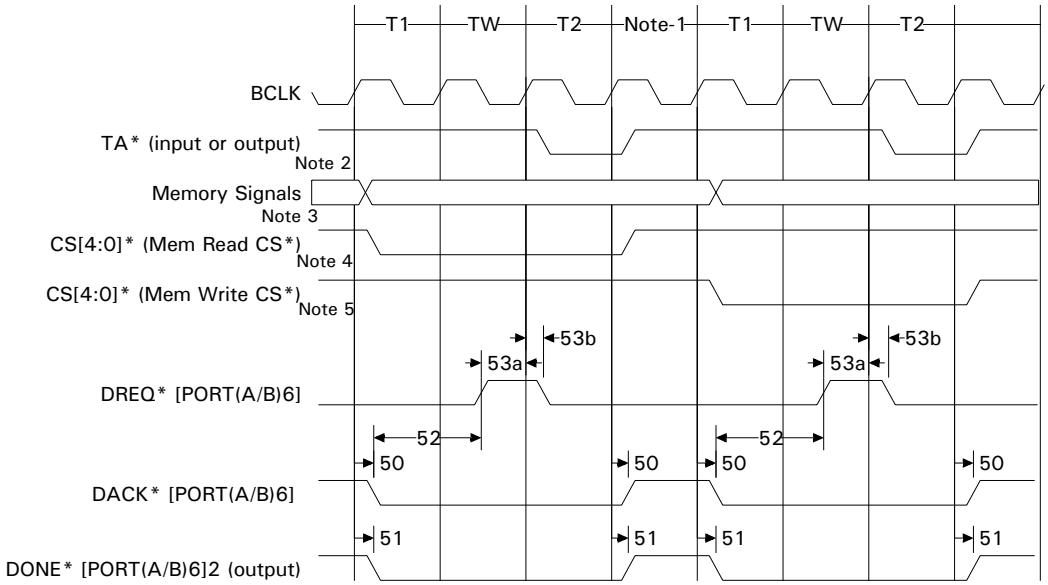
2 The memory signals consist of:

DATA[31:0]	CS/RAS[4:0]*	OE*
ADDR[27:0]	CAS[3:0]*	WE*
BE[3:0]*	RW*	PORTC3/AMUX

The timing of these signals depends on how the memory is configured. See the timing diagrams referenced on page 46.

3 The DONE* signal works as an input only when the DMA channel is configured as Fly-By Write.

External Memory to Memory DMA



Notes:

1 Between memory cycles, 0, 1, or 2 null periods can occur. Contact the factory for details.

2 TA* is shown here for reference. Its timing is available on the diagrams in the sections referenced below.

3 The memory signals consist of:

DATA[31:0]	CS/RAS[4:0]*	OE*
ADDR[27:0]	CAS[3:0]*	WE*
BE[3:0]*	RW*	PORTC3/AMUX

The timing of these signals depends on how the memory is configured. See the timing diagrams in the sections referenced below.

4 The timing of the chip select associated with the buffer descriptor's source address depends on how that chip select is configured.

5 The timing of the chip select associated with the buffer descriptor's destination address depends on how that chip select is configured.

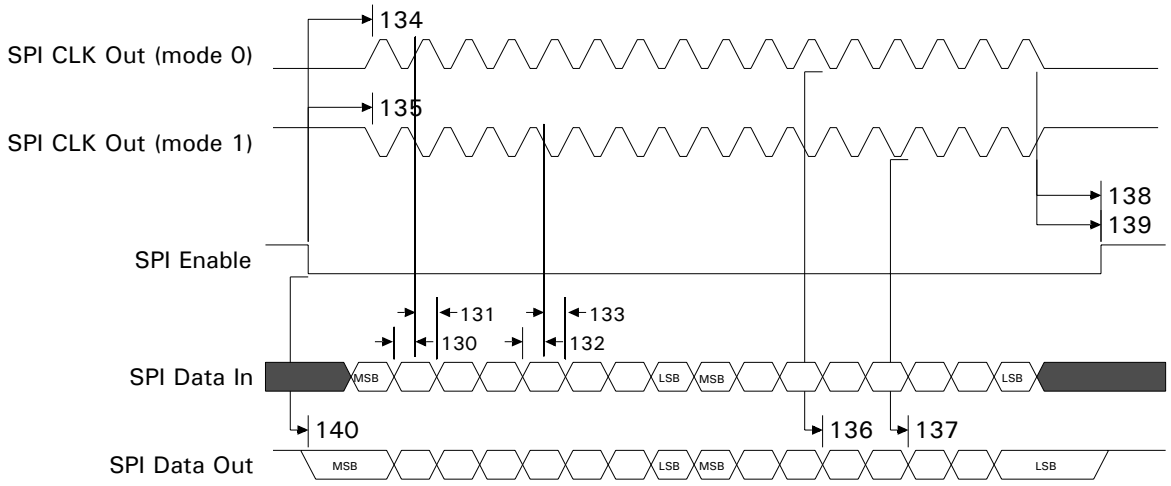
See also

- "SRAM timing" on page 20
- "Fast Page and EDO DRAM timing" on page 30
- "SDRAM timing" on page 37

SPI master and slave timing

SPI Master Mode 0 and 1 (Two-Byte Transfer)

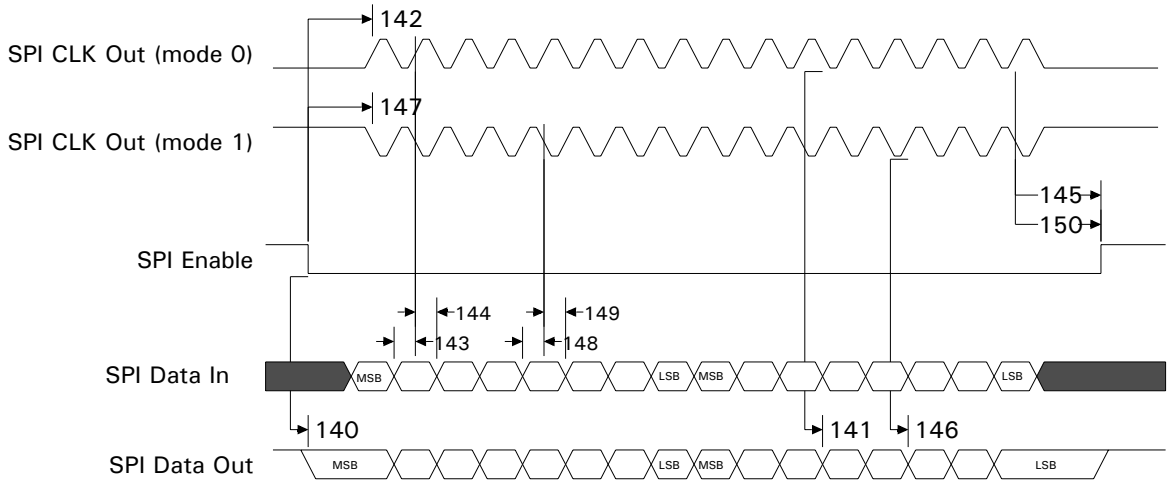
Number	Characteristic	Min.	Max.	Unit
130	Data In valid to mode 0 rising clock (setup)	20		ns
131	Mode 0 rising clock to Data In valid (hold)	0		ns
132	Data In valid to mode 1 falling clock (setup)	20		ns
133	Mode 1 falling clock to Data In valid (hold)	0		ns
134	Enable low to mode 0 first rising clock		1.5	Bit-Time
135	Enable low to mode 1 first falling clock		1.5	Bit-Time
136	Mode 0 falling edge to Data Out valid	-Tsys	Tsys	ns
137	Mode 1 rising edge to Data Out valid	-Tsys	Tsys	ns
138	Mode 0 last falling clock to Enable high		1.5	Bit-Time
139	Mode 1 last rising clock to Enable high		1.5	Bit-Time
140	Enable low to Data Out valid	-Tsys	Tsys	ns



SPI Slave Mode 0 and 1 (Two-Byte Transfer)

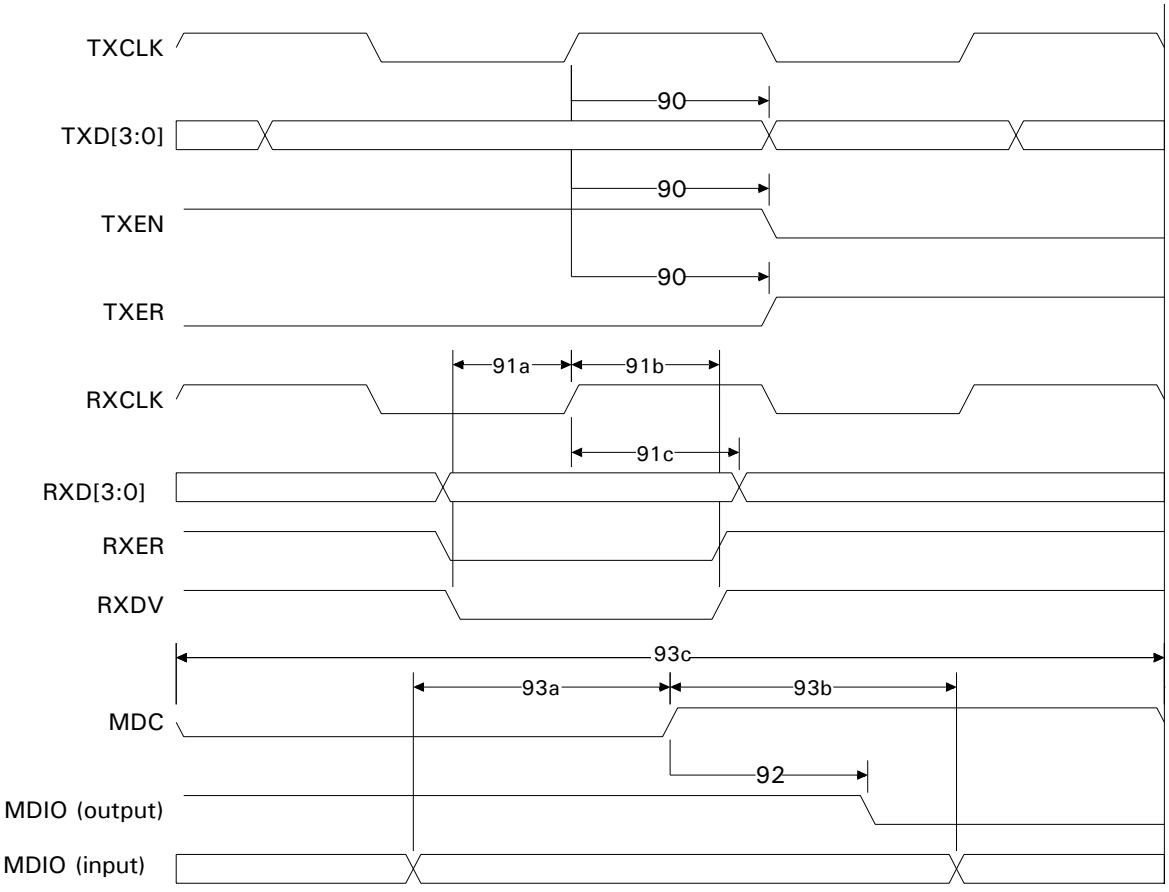
Number	Characteristic	Min.	Max.
141	Mode 0 SPI Clock high to TXD valid	3 * T_{SYS}	4 * T_{SYS}
142	Mode 0 SPI Enable low to SPI Clock high (setup)	0	
143	Mode 0 RXD Input valid to SPI Clock high (setup)	3.4	
144	Mode 0 SPI Clock high to RXD input change (hold)	4 * T_{SYS}	
145	Mode 0 SPI Clock high to SPI Enable high (hold)	4 * T_{SYS}	
146	Mode 1 SPI Clock low to TXD valid	3 * T_{SYS}	4 * T_{SYS}
147	Mode 1 SPI Enable low to SPI Clock low (setup)	0	
148	Mode 1 RXD Input valid to SPI Clock low (setup)	3.4	
149	Mode 1 SPI Clock low to RXD input change (hold)	4 * T_{SYS}	
150	Mode 1 SPI Clock low to SPI Enable high (hold)	4 * T_{SYS}	

Minimum and maximum are in nanoseconds (ns).

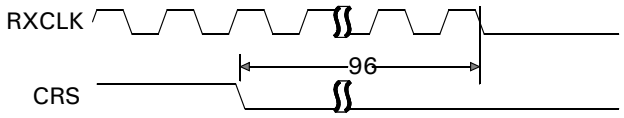


Ethernet timing

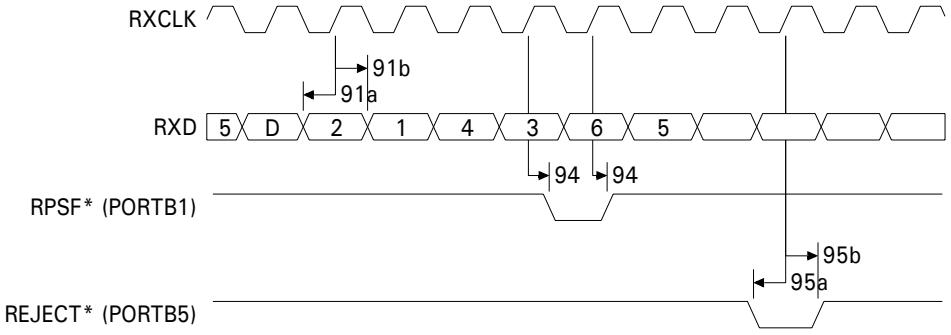
Number	Characteristic	Min.	Max.	Unit
90	TXCLK high to TXD, TXEN, TXER valid	5	17	ns
91a	RXD, RXER, RXDV valid to RXCLK high (setup)	8		ns
91b	RXCLK high to RXD, RXER, RXDV hold time	0		ns
91c	RXCLK high to RXD hold time	0		ns
92	MDC high to MDIO change	40	50	ns
93a	MDIO valid to MDC high (setup)	10		ns
93b	MDC high to MDIO hold time	0		ns
93c	MDC cycle time		SYSCLK/10	
94	RXCLK high to RPSF* change		6.5	ns
95a	REJECT* valid to RXCLK high (setup)	2.6		ns
95b	REJECT* valid from RXCLK high (hold)	0		ns
96	CRS low to RXCLK idle	27		Bit-Time



Ethernet Receive Clock Idle



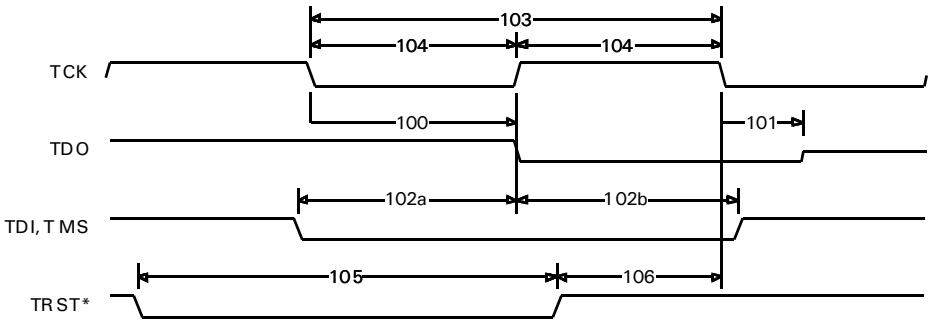
External Ethernet CAM Filtering



ARM core debug timing

Number	Characteristic	Min.	Max.
100	TCK low to TDO valid	0	33.5
101	TCK low to TDO high impedance	0	32.3
102a	TDI, TMS valid to TCK high (setup)	0.72	
102b	TCK high to TDI, TMS hold time	1.3	
103	TCK cycle time	31.2	
104	TCK pulse width	15.6	
105	TRST* low time	27	
	Minimum and maximum are in nanoseconds (ns).		

Note: TRST* has an internal current sink. On production units, do not leave TRST* pulled low. The noise margin on inputs at a logic 0 is only a few tenths of a volt. Digi recommends tying TRST* to RESET* on production units.



ENI timing

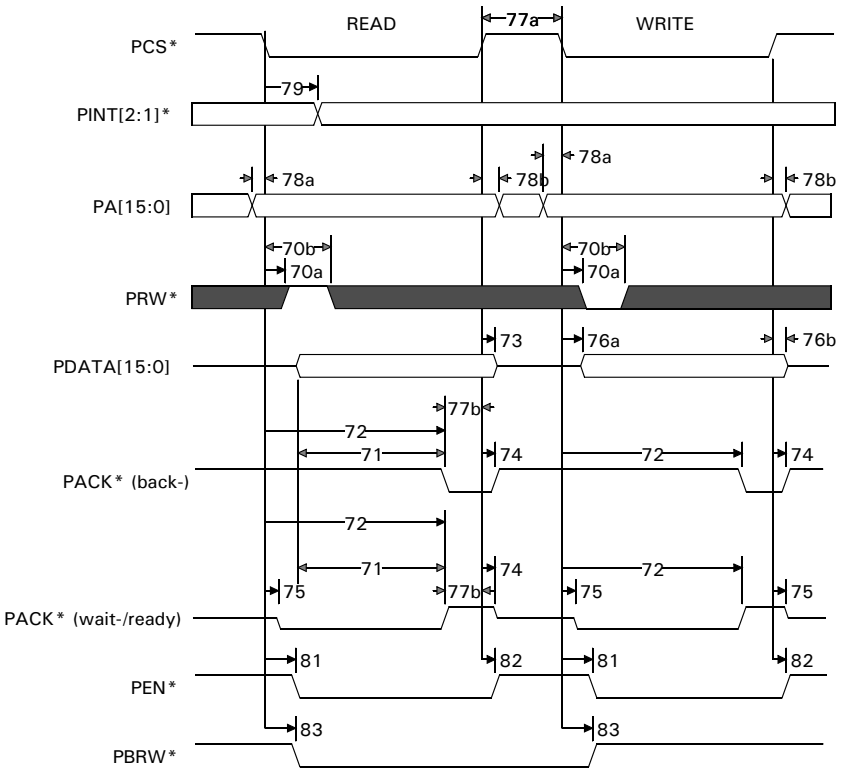
The data shown is independent of SYS_CLK and BCLK settings. Units are nanoseconds (ns).

Num	Characteristic	Note	Min	Max
70a	PCS*/PDACK* low to PRW* sampled	1		T_{SYS} - 2.5
70b	PCS*/PDACK* low to PRW* hold time	1	$4*T_{SYS}$	
71	Read Data Valid to PACK* valid		T_{SYS}	
72	PCS*/PDACK* low to PACK* low	3	T_{SYS}	$6*T_{SYS}$
72a	PCS* low to PACK* low	4	$7*T_{SYS}$	Determined by shared RAM access time
72b	PCS*/PACK* low to PACK* low	5	$2*T_{SYS}$	$4*T_{SYS}$
72c	PCS* low to PACK* valid (shared RAM only)	6	$7*T_{SYS}$	Determined by shared RAM access time
73	PCS*/PDACK* high to PDATA high impedance		0	7.84
74	PCS*/PDACK* high to PACK* high		0	13
75	PCS*/PDACK* low to PACK* (wait-) low		0	14
76a	PCS*/PDACK* low to Write Data valid			$2*T_{SYS}$
76b	PCS*/PDACK* high to Write Data hold time		0	
77a	PCS*/PDACK* width high (recovery)		16	
77b	PACK* low to PCS*/PDACK* high (hold)	8	0	
77c	PDACK* minimum low		120	
78a	Address valid to PCS* low		0	
78b	PCS* high to Address hold time		0	
79	PCS* low to PINT1/2 change (write)		$3*T_{SYS}$	$5*T_{SYS}$
80a	PDACK* low to PDRQI*, PDRQO* high			$5*T_{SYS}$
80b	PDRQO* high width		$5*T_{SYS}$	
80c	PDRQI* high width		$4*T_{SYS}$	
80d	PDACK* low to PINT2 low			14
80e	PDACK* high to PINT2 high		15	
81	PCS*/PDACK* low to PEN* low	2	$1*T_{SYS}$	$3*T_{SYS}$
82	PCS*/PDACK* high to PEN* high	2	0	13
83	PCS*/PDACK* low to PBRW* low	2	$1*T_{SYS}$	$2*T_{SYS}$
84a	PRW* valid to PDACK* low (setup)	1	0	
84b	PDACK* high to PRW* hold time	1	0	
85	PDACK* low to PDATA valid	7	$3*T_{SYS}$	$5*T_{SYS}$
85a	PDACK* low to PDATA valid	7	$1*T_{SYS}$	$2*T_{SYS}$

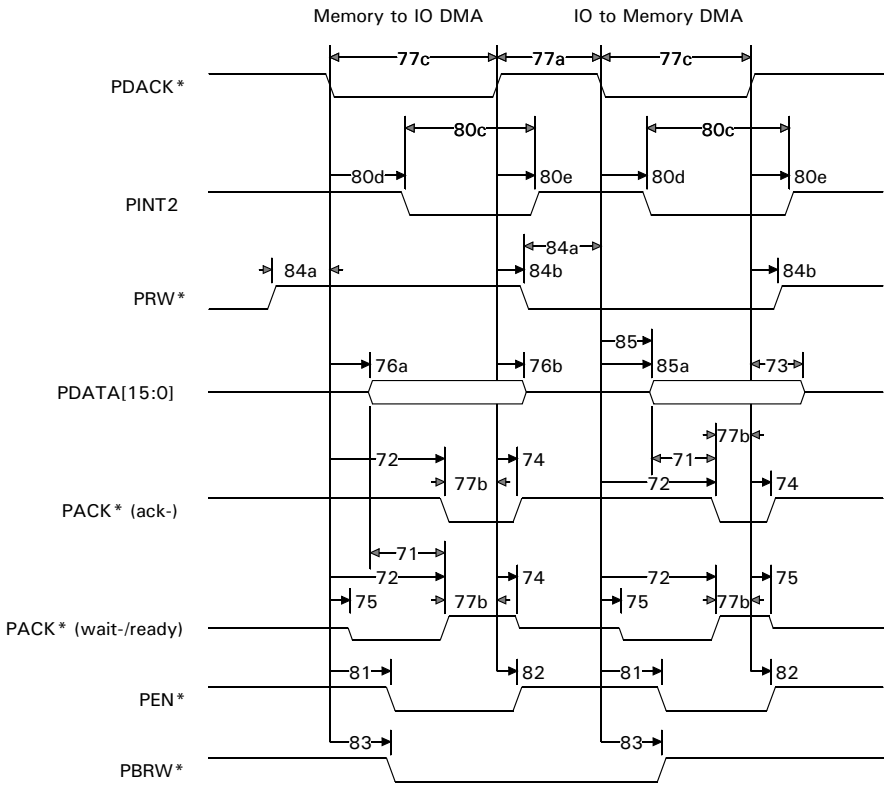
Notes:

1. Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
2. The PEN* and PBRW* signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
3. Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
4. Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
5. Parameter 72b applies to ENI register accesses when FAST is set to 1.
6. Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
7. Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
8. Parameter 77c can be reduced to $3*T_{SYS}$ when FAST is set to 1.

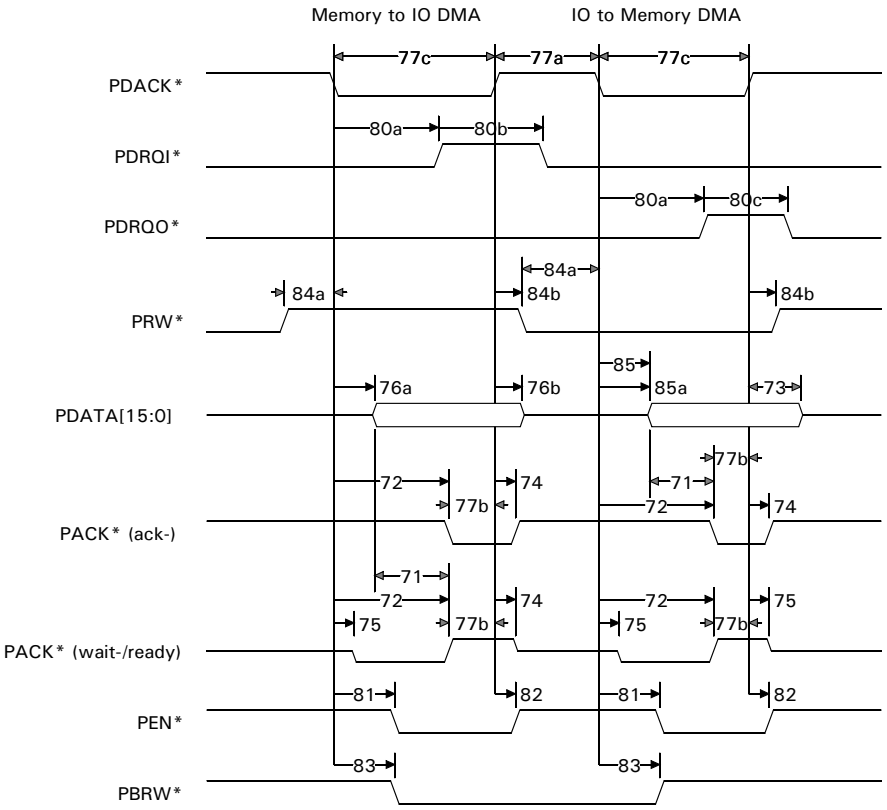
ENI Shared RAM and Register Cycle timing



ENI Single Direction DMA timing



ENI Dual Direction DMA timing



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