OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ISL95810, ISL95811

Single Digitally-Controlled (XDCP™) Potentiometer

The X9279 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

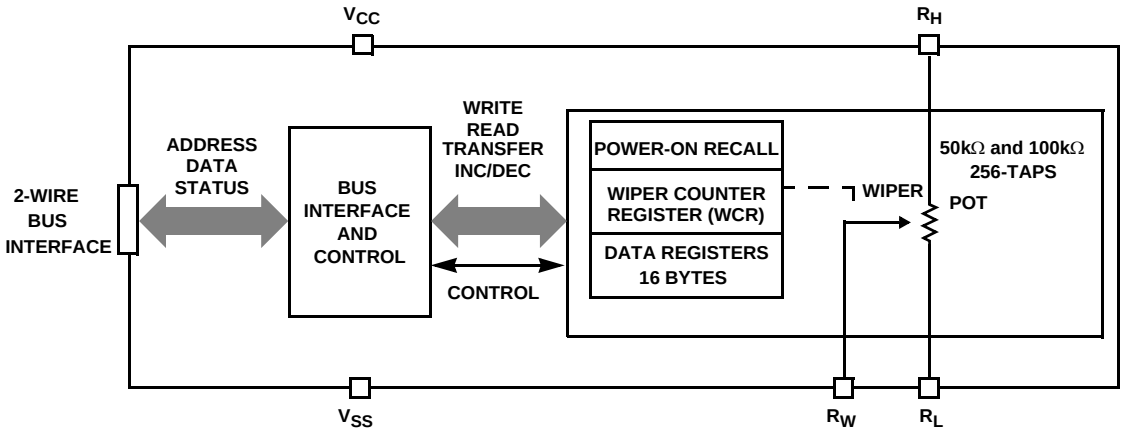
The digital controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-Wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 256 Resistor Taps
- 2-Wire Serial Interface for Write, Read, and Transfer Operations of the Potentiometer
- Wiper Resistance, 100Ω Typical @ 5V
- 16 Non-volatile Data Registers for Each Potentiometer
- Non-volatile Storage of Multiple Wiper Positions
- Power-on Recall. Loads Saved Wiper Position on Power-up.
- Standby Current < 5µA Max
- V_{CC}: 2.7V to 5.5V Operation
- 50kΩ, 100kΩ Versions of End-to-End Resistance
- Endurance: 100,000 Data Changes per Bit per Register
- 100 yr. Data Retention
- 14 Ld TSSOP
- Low Power CMOS
- Pb-Free Available (RoHS Compliant)

Functional Diagram



Ordering Information

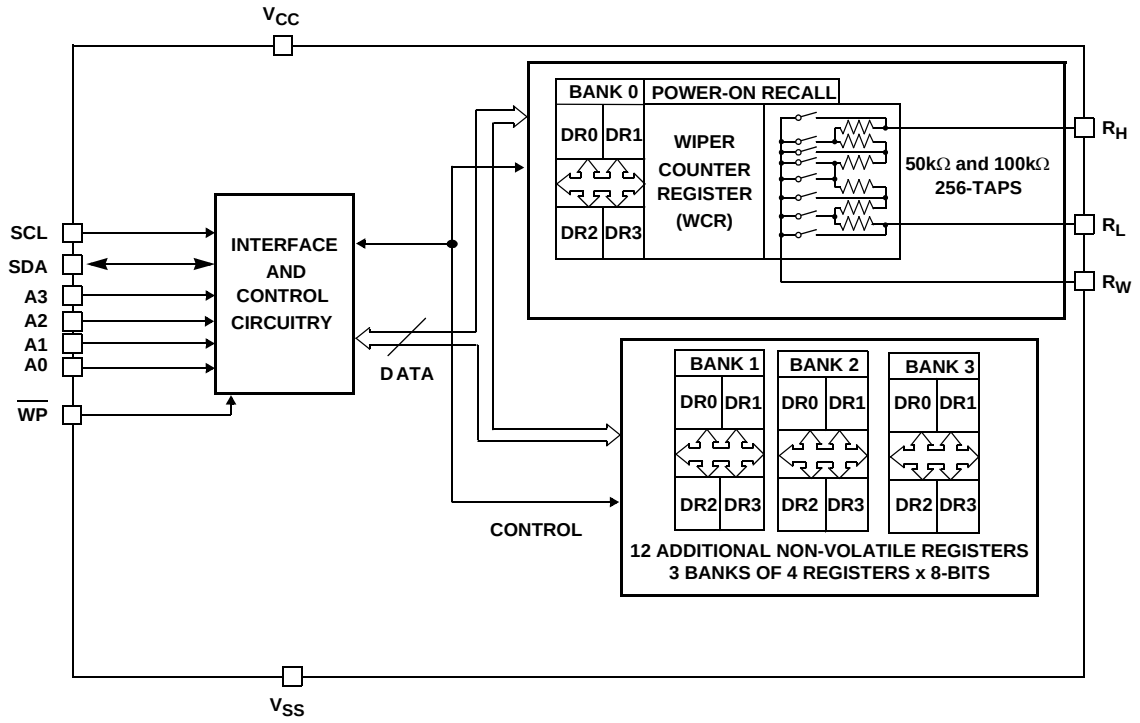
PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X9279TV14* (Note 2)	X9279 TV	5 ±10%	100	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9279TV14Z* (Note 1)	X9279 TVZ			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279TV14I* (Note 2)	X9279 TVI			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9279TV14IZ* (Note 1)	X9279 TVZI			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279UV14* (Note 2)	X9279 UV		50	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9279UV14Z* (Note 1)	X9279 UVZ			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279UV14I* (Note 2)	X9279 UVI			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9279UV14IZ* (Note 1)	X9279 UVZI			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279TV14-2.7* (Note 2)	X9279 TVF	2.7 to 5.5	100	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9279TV14Z-2.7* (Note 1)	X9279 TVZF			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279TV14I-2.7* (Note 2)	X9279 TVG			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9279TV14IZ-2.7* (Note 1)	X9279 TVZG			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279UV14-2.7* (Note 2)	X9279 UVF		50	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9279UV14Z-2.7* (Note 1)	X9279 UVZF			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X9279UV14I-2.7* (Note 2)	X9279 UVG			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9279UV14IZ-2.7* (Note 1)	X9279 UVZG			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Not recommended for new designs.

Detailed Functional Diagram



Circuit Level Applications

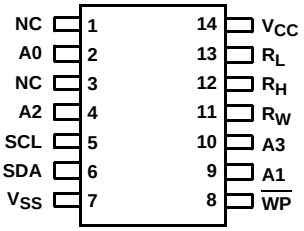
- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

Pinout

X9279
(14 LD TSSOP)
TOP VIEW



Pin Functions

PIN TSSOP	SYMBOL	FUNCTION
1	NC	No Connect
2	A0	Device Address for 2-Wire bus
3	NC	No Connect
4	A2	Device Address for 2-Wire bus
5	SCL	Serial Clock for 2-Wire bus
6	SDA	Serial Data Input/Output for 2-Wire bus
7	V_{SS}	System Ground
8	WP	Hardware Write Protect
9	A1	Device Address for 2-Wire bus
10	A3	Device Address for 2 wire-bus. Must be connected to Ground
11	R_W	Wiper Terminal of the Potentiometer
12	R_H	High Terminal of the Potentiometer
13	R_L	Low Terminal of the Potentiometer
14	V_{CC}	System Supply Voltage

Pin Descriptions

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for a 2-Wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from an 2-Wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

SERIAL CLOCK (SCL)

This input is used by 2-Wire master to supply 2-Wire serial clock to the X9279.

DEVICE ADDRESS (A3 - A0)

The Address inputs A2 - A0 are used to set the least significant 3 bits of the 8-bit slave address, address pin A3 must be connected to ground for proper operation. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9279. A maximum of 8 devices may occupy the 2-Wire serial bus.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

Bias Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT

No connect pins should be left open. This pins are used for Intersil manufacturing and testing purposes.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents non-volatile writes to the Data Registers.

Principles Of Operation

The X9279 is a integrated microcircuit incorporating a resistor array and associated registers and counter and the serial interface logic providing direct communication between the host and the digitally controlled potentiometers. This section provides detail description of the following:

- Resistor Array Description
- Serial Interface Description
- Instruction and Register Description

Array Description

The X9279 is comprised of a resistor array (see Figure 1). The array contains, in effect, 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (see Table 1).

The WCR may be written directly. These Data Registers can the WCR can be read and written by the host system.

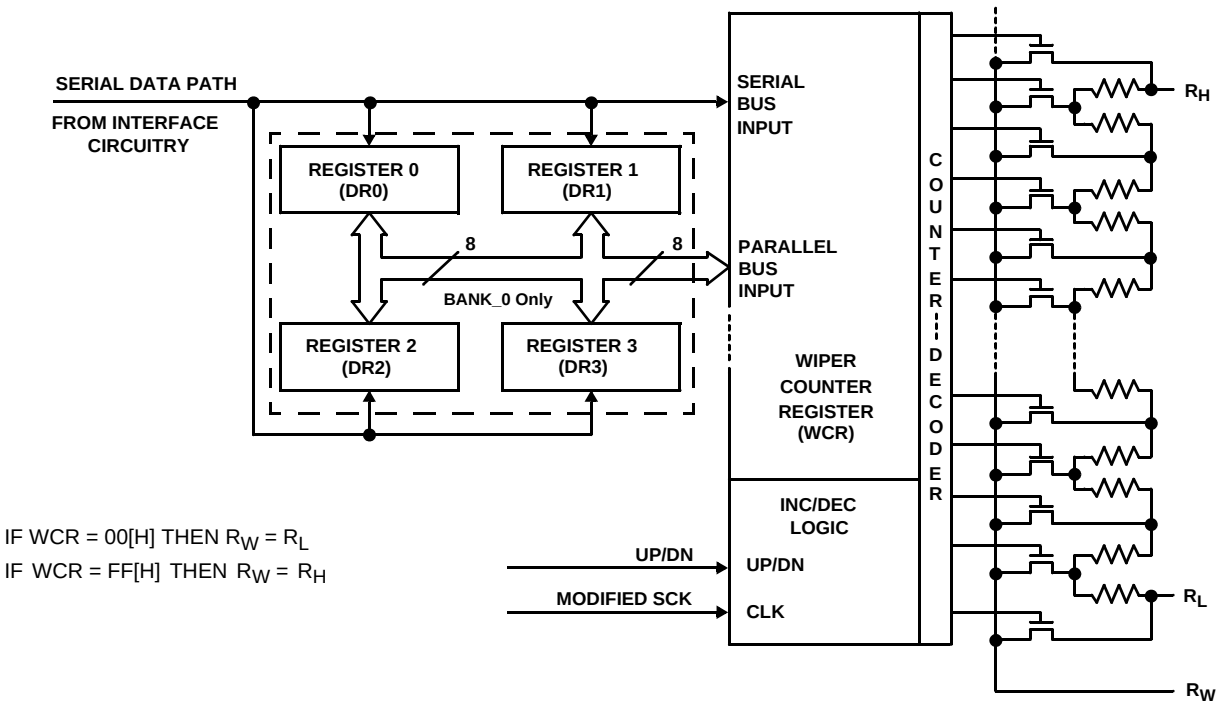


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

Power-up and Down Recommendations.

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H$, V_L, V_W. The V_{CC} ramp rate specification is always in effect.

Serial Interface Description

Serial Interface

The X9279 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9279 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (see Figure 2.

Start Condition

All commands to the X9279 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9279 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met (see Figure 2).

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 2).

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9279 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9279 will respond with a final acknowledge (see Figure 2).

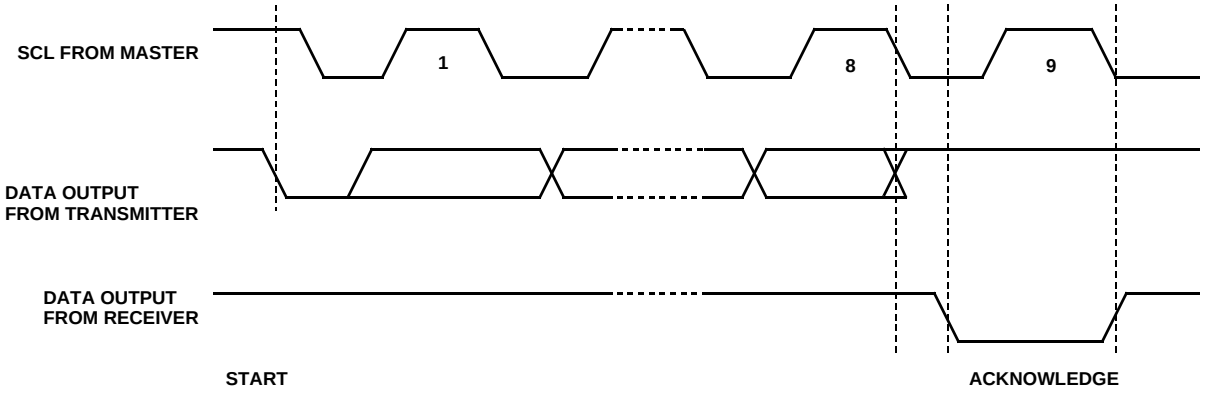
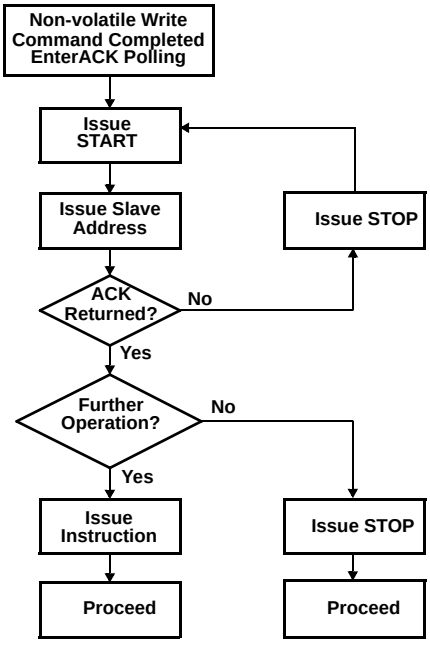


FIGURE 2. ACKNOWLEGE RESPONSE FROM RECEIVER

Acknowledge Polling

The disabling of the inputs, during the internal non-volatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the non-volatile write command the X9279 initiates the internal write cycle. ACK Polling Sequence, Flow 1, can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9279 is still busy with the write operation no ACK will be returned. If the X9279 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

Flow 1: ACK Polling Sequence



Instruction and Register Description

Device Addressing: Identification Byte (ID and A)

The first byte sent to the X9279 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device ID for the X9279; this is fixed as 0101[B] (refer to Table 3).

The A[2:0] bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A2 - A0 input pins. The slave address is externally specified by the user. The X9279 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9279 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A2 - A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Instruction Byte (I)

The next byte sent to the X9279 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode I [2:0]. The RB and RA bits point to one of the four Data Registers. P0 is the POT selection; since the X9279 is single POT, the P0 = 0. The format is shown in Table 4.

Register Bank Selection (RB, RA, P1, P0)

There are 16 registers organized into four banks. Bank 0 is the default bank of registers. Only Bank 0 registers can be used for Data Register to Wiper Counter Register operations.

Banks 1, 2, and 3 are additional banks of registers (12 total) that can be used for 2-Wire write and read operations. The Data Registers in Banks 1, 2, and 3 cannot be used for direct read/write operations between the Wiper Counter Register.

TABLE 1. REGISTER SELECTION (R0 TO R3)

RB	RA	REGISTER SELECTION	OPERATIONS
0	0	0	Data Register Read and Write; Wiper Counter Register Operations
0	1	1	Data Register Read and Write; Wiper Counter Register Operations
1	0	2	Data Register Read and Write; Wiper Counter Register Operations
1	1	3	Data Register Read and Write; Wiper Counter Register Operations

TABLE 2. REGISTER BANK SELECTION (BANK 0 TO BANK 3)

P1	P0	BANK SELECTION	OPERATIONS
0	0	0	Data Register Read and Write; Wiper Counter Register Operations
0	1	1	Data Register Read and Write Only
1	0	2	Data Register Read and Write Only
1	1	3	Data Register Read and Write Only

TABLE 3. IDENTIFICATION BYTE FORMAT

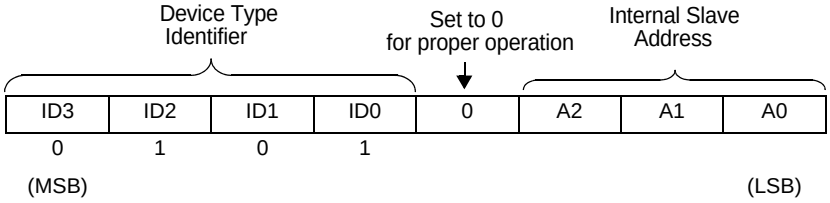
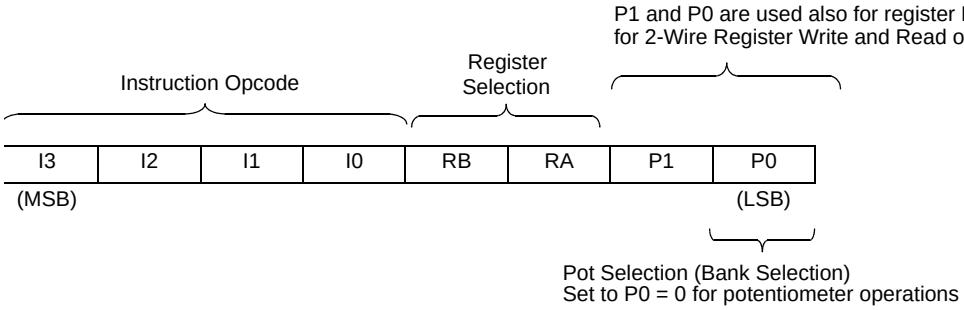


TABLE 4. INSTRUCTION BYTE FORMAT



Register Selection

Register Selected	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

TABLE 5. INSTRUCTION SET

INSTRUCTION	INSTRUCTION Set								OPERATION
	I3	I2	I1	I0	RB	RA	P_1	P_0	
Read Wiper Counter Register	1	0	0	1	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1 - P0 and RB - RA
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1 - P0 and RB - RA
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by RB-RA (Bank 0 only) to the Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Register pointed to by RB-RA (Bank 0 only)
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	0	Enable Increment/decrement of the Wiper Counter Register

NOTE:

3. 1/0 = data is one or zero

TABLE 6. WIPER COUNTER REGISTER, WCR (8-bit), WCR[7:0]: (Used to store the current wiper position (Volatile, V)

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V
(MSB)							(LSB)

TABLE 7. DATA REGISTER, DR (8-BIT), BIT [7:0]: Used to store wiper positions or data (Non-volatile, NV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NV	NV	NV	NV	NV	NV	NV	NV
MSB							LSB

Device Description

Wiper Counter Register (WCR)

The X9279 contains a Wiper Counter Register, for the DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see “Instruction Format” on page 10 for more details). Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9279 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR. The DR0 value of Bank 0 is the default value.

Data Registers (DR)

The potentiometer has four 8-bit non-volatile Data Registers (DR3-DR0). These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a non-volatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit [7:0] are used to store one of the 256 wiper positions (0~255).

Instructions

Four of the seven instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the potentiometer,
- **Read Data Register** – read the contents of the selected Data Register;
- **Write Data Register** – write a new value to the selected Data Register.

The basic sequence of the three byte instructions is illustrated in Figure 4. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between the potentiometer and one of its four associated registers (Bank 0).

Two instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9279; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the Wiper Counter Register to the specified Data Register.

The final command is Increment/Decrement (Figures 5 and 6). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9279 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal. See “Instruction Format” on page 10 for more details.

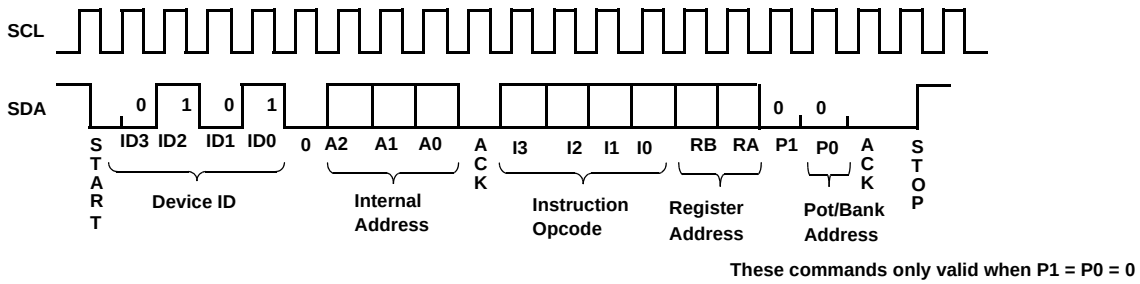


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

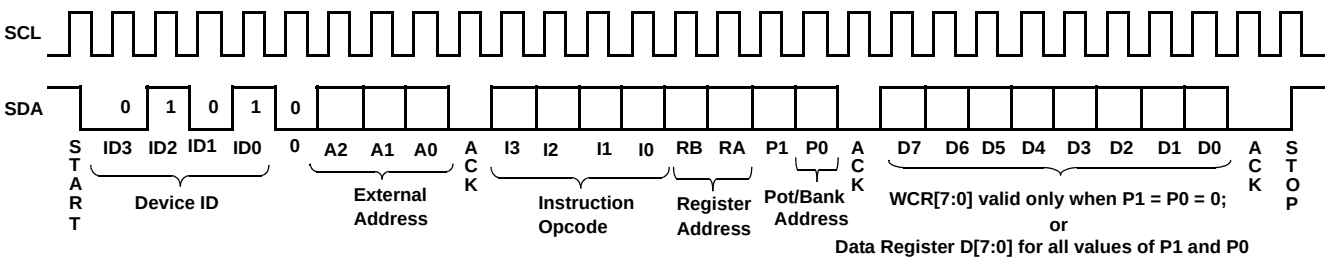


FIGURE 4. THREE-BYTE INSTRUCTION SEQUENCE

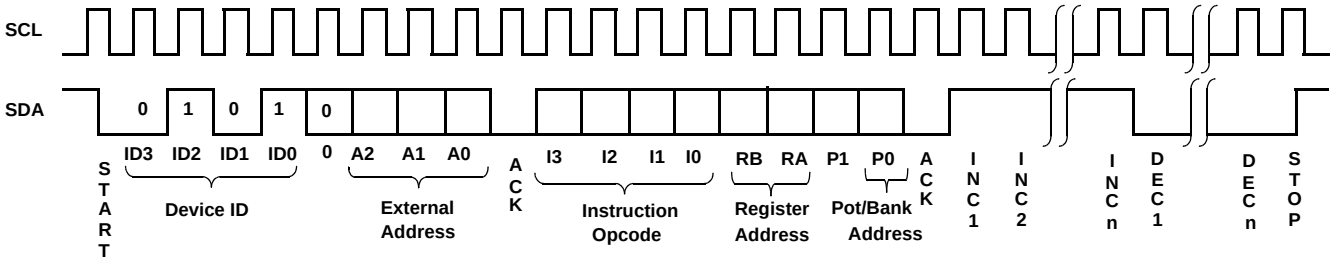


FIGURE 5. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

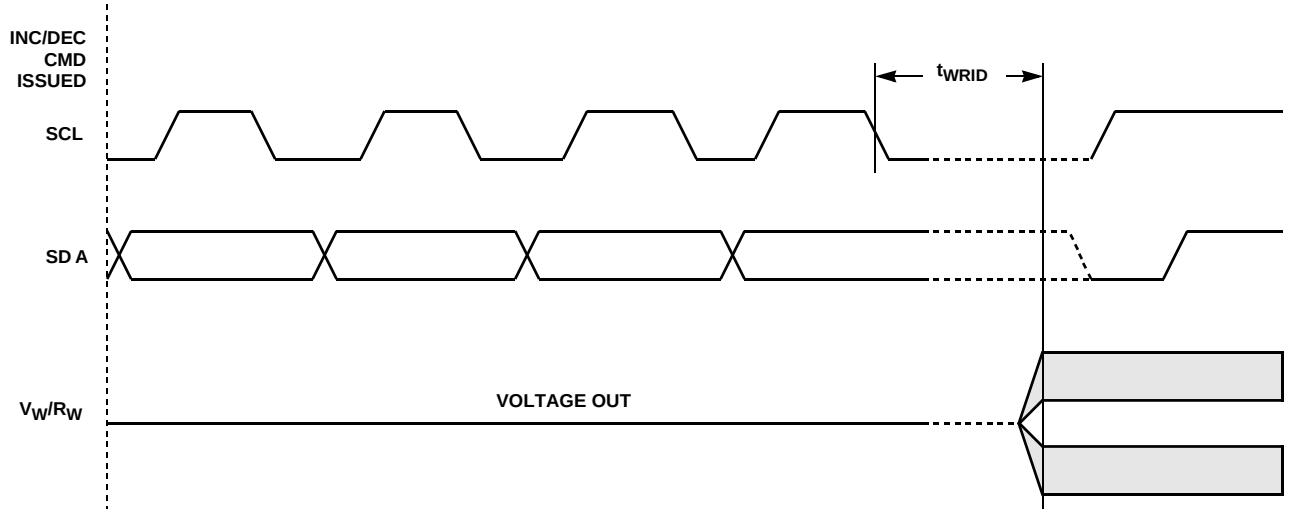


FIGURE 6. INCREMENT/DECREMENT TIMING LIMITS

Instruction Format

Read Wiper Counter Register (WCR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	Wiper Position (Sent by X9279 on SDA)								M A C K	S T O P
	0	1	0	1	0	A 2	A 1	A 0		1	0	0	1	0	0	0	0		WC R7	WC R6	WC R5	WC R4	WC R3	WC R2	WC R1	WC R0		

Write Wiper Counter Register (WCR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	Wiper Position (Sent by Master on SDA)								S A C K	S T O P
	0	1	0	1	0	A 2	A 1	A 0		1	0	1	0	0	0	0	0		WC R7	WC R6	WC R5	WC R4	WC R3	WC R2	WC R1	WC R0		

Read Data Register (DR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	Wiper Position (Sent by X9279 on SDA)								M A C K	S T O P
	0	1	0	1	0	A 2	A 1	A 0		1	0	1	1	RB	RA	P1	P0		WC R7	WC R6	WC R5	WC R4	WC R3	WC R2	WC R1	WC R0		

Write Data Register (DR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	Wiper Position (Sent by Master on SDA)								S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	A 2	A 1	A 0		1	1	0	0	RB	RA	P1	P0		WC R7	WC R6	WC R5	WC R4	WC R3	WC R2	WC R1	WC R0			

Transfer Wiper Counter Register (WCR) to Data Register (DR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	S T O P	High-Voltage Write Cycle
	0	1	0	1	0	A 2	A 1	A 0		1	1	1	0	RB	RA	0	0			

Transfer Data Register (DR) to Wiper Counter Register (WCR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	S T O P
	0	1	0	1	0	A 2	A 1	A 0		1	1	0	1	RB	RA	0	0			

Increment/Decrement Wiper Counter Register (WCR)

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				DR/Bank Addresses				S A C K	Increment/Decrement (Sent by Master on SDA)								S T O P
	0	1	0	1	0	A 2	A 1	A 0		0	0	1	0	0	0	0	0		I/D	I/D	.	.	.	.	I/D	I/D	

NOTES:

4. “MACK”/”SACK”: stands for the acknowledge sent by the master/slave.
5. “A3 ~ A0”: stands for the device addresses sent by the master.
6. “X”: indicates that it is a “0” for testing purpose but physically it is a “don’t care” condition.
7. “I”: stands for the increment operation, SDA held high during active SCL phase (high).
8. “D”: stands for the decrement operation, SDA held low during active SCL phase (high).

Absolute Maximum Ratings

Voltage on SCL, SDA any Address Input
with respect to VSS . . . . . -1V to +7V
DV = | (VH - VL) | 5.5V
I_W (10s) . . . . . ±6mA

Operating Conditions

Temperature Range
Commercial . . . . . 0 to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage VCC Limits (Note 13)
X9279 . . . . . 5V ± 10%
X9279-2.7 . . . . . 2.7V to 5.5V
Wiper Max Current (I_W) . . . . . ±3mA
Power Rating @ +25°C, each pot 50mW

Thermal Information

Thermal Resistance (Typical, Note 9) θ_{JA} (°C/W)
14 Lead TSSOP 90
Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

9. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Characteristics

Operating Conditions over recommended industrial (2.7V) unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
R_{TOTAL}	End-to-End Resistance	T version		100		kΩ
R_{TOTAL}	End-to-End Resistance	U version		50		kΩ
	End-to-End Resistance Tolerance				±20	%
R_W	Wiper Resistance @ V = 3V	$I_W = (V_{RH} - V_{RL})/R_{TOTAL}$			300	Ω
R_W	Wiper Resistance @ V = 5V	$I_W = (V_{RH} - V_{RL})/R_{TOTAL}$			150	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Noise	Ref: 1V		-120		dBV/$\sqrt{Hz}$
	Resolution			0.4		%
	Absolute Linearity (Note 10)	$R_{w(n)(actual)} - R_{w(n)(expected)}$ (Note 14)			±1	MI (Note 12)
	Relative Linearity (Note 11)	$R_{w(n+1)} - [R_{w(n)} + MI]$ (Note 14)			±0.2	MI (Note 12)
	Temperature Coefficient of R_{TOTAL}			±300		ppm/°C
	Ratiometric Temp. Coefficient			±20		ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See Macro model		10/10/25		pF

NOTES:

10. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
11. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
12. MI = RTOT / 255 or (R_H - R_L)/255, single pot
13. During power-up $V_{CC} > V_H$, V_L, and V_W.
14. n = 0, 1, 2,....,255; m = 0, 1, 2,...., 254.

DC Electrical Specifications

Over the recommended Operating Conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC1}	V_{CC} Supply Current (Active)	f_{SCL} = 400kHz; V_{CC} = +6V; SDA = Open; (for 2-Wire, Active, Read and Volatile Write States only)			3	mA
I_{CC2}	V_{CC} Supply Current (Non-volatile Write)	f_{SCL} = 400kHz; V_{CC} = +6V; SDA = Open (for 2-Wire, Active, Non-volatile Write State only)			5	mA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +6V; V_{IN} = V_{SS} or V_{CC}; SDA = V_{CC} (for 2-Wire, Standby State only)			5	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 1	V
V_{IL}	Input LOW Voltage		-1		V_{CC} x 0.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V

Endurance and Data Retention

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

Capacitance

SYMBOL	TEST	TYP	UNITS	TEST CONDITIONS
$C_{IN/OUT}$	Input /Output capacitance (SDA)	8	pF	V_{OUT} = 0V
C_{IN}	Input capacitance (SCL, $\overline{WP}$, A2, A1 and A0)	6	pF	V_{IN} = 0V

Power-Up Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_r V_{CC} (Note 15)	V_{CC} Power-up rate	0.2	50	V/ms
t_{PUR} (Note 16)	Power-up to initiation of read operation		1	ms
t_{PUW} (Note 16)	Power-up to initiation of write operation		50	ms

NOTES:

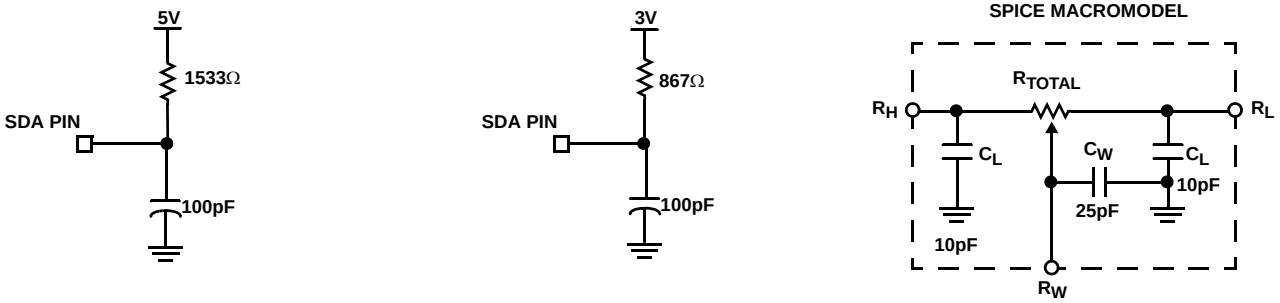
15. This parameter is not 100% tested.

16. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Equivalent AC Load Circuit



AC Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	Clock Frequency		400	kHz
t_{CYC}	Clock Cycle Time	2500		ns
t_{HIGH}	Clock High Time	600		ns
t_{LOW}	Clock Low Time	1300		ns
$t_{SU:STA}$	Start Setup Time	600		ns
$t_{HD:STA}$	Start Hold Time	600		ns
$t_{SU:STO}$	Stop Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	100		ns
$t_{HD:DAT}$	SDA Data Input Hold Time	30		ns
t_R	SCL and SDA Rise Time		300	ns
t_F	SCL and SDA Fall Time		300	ns
t_{AA}	SCL Low to SDA Data Output Valid Time		0.9	µs
t_{DH}	SDA Data Output Hold Time	0		ns
t_I	Noise Suppression Time Constant at SCL and SDA inputs	50		ns
t_{BUF}	Bus Free Time (Prior to Any Transmission)	1200		ns
$t_{SU:WPA}$	A0, A1 Setup Time	0		ns
$t_{HD:WPA}$	A0, A1 Hold Time	0		ns

High Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP	MAX	UNITS
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

XDCP Timing

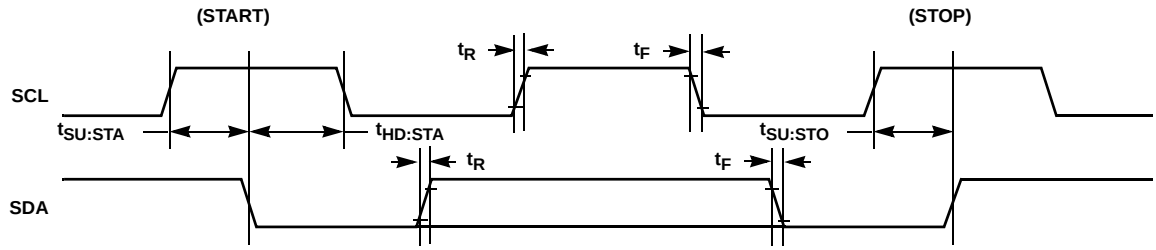
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{WRPO}	Wiper response time after the third (last) power supply is stable	5	10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)	5	10	µs

Symbol Table

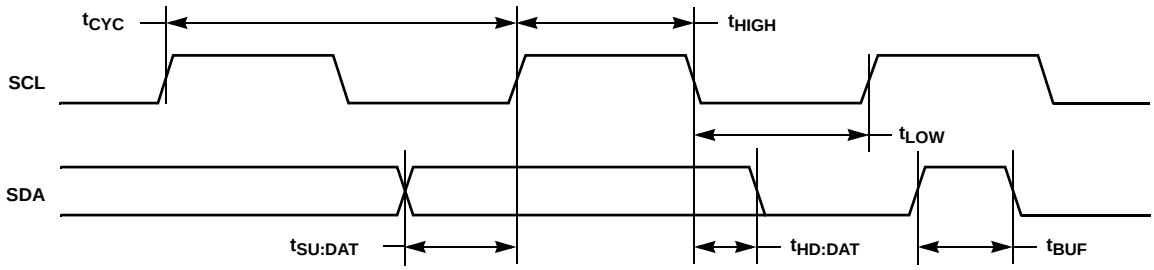
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Timing Diagrams

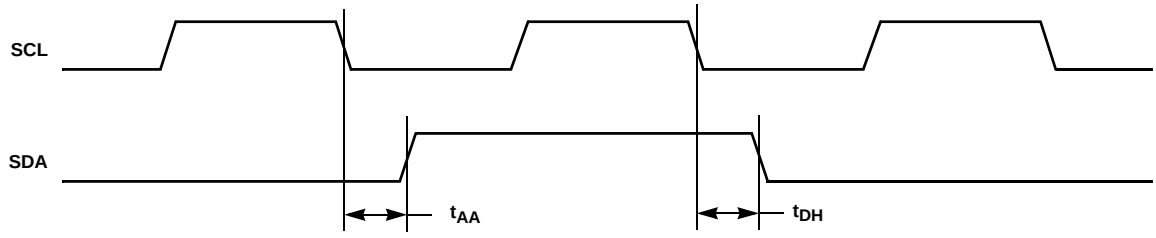
Start and Stop Timing



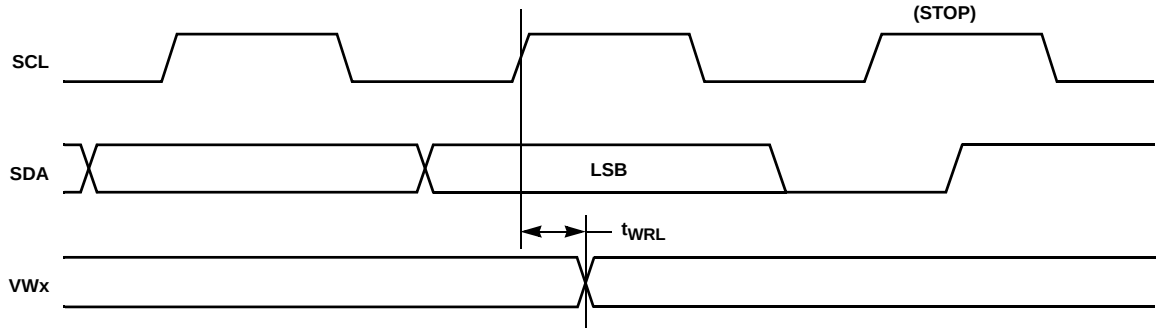
Input Timing



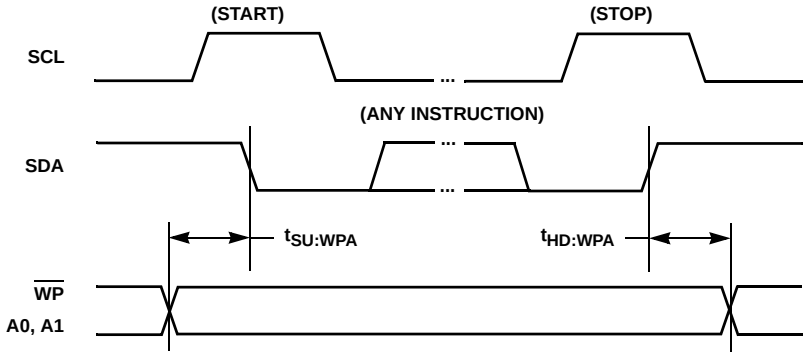
Output Timing



XDCP Timing (for All Load Instructions)

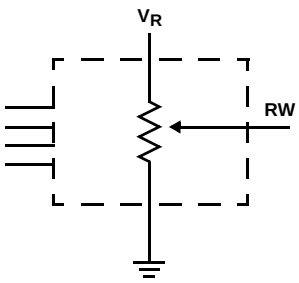


Write Protect and Device Address Pins Timing

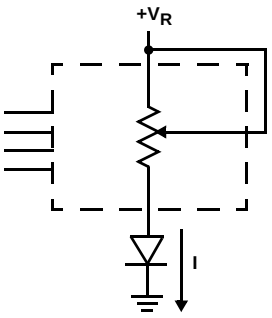


Applications information

Basic Configurations of Electronic Potentiometers

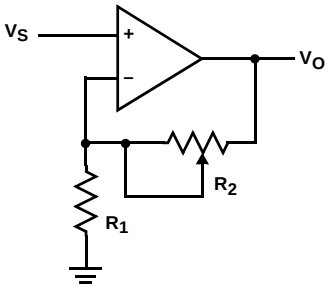


Three terminal Potentiometer;
Variable voltage divider



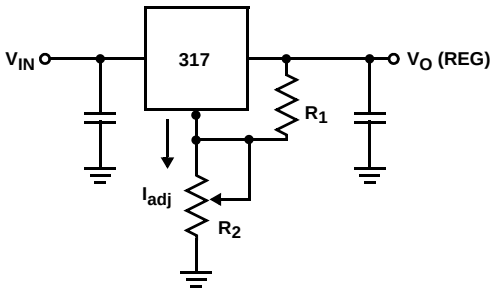
Two terminal Variable Resistor;
Variable current

Application Circuits



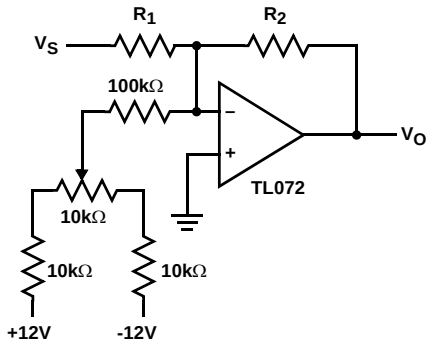
$V_O = (1+R_2/R_1)V_S$

NON-INVERTING AMPLIFIER

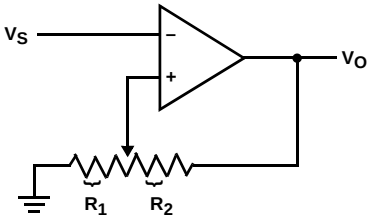


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

VOLTAGE REGULATOR

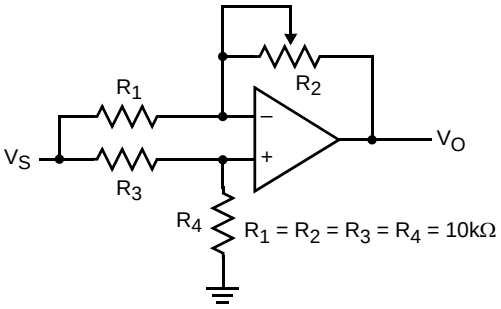


OFFSET VOLTAGE ADJUSTMENT



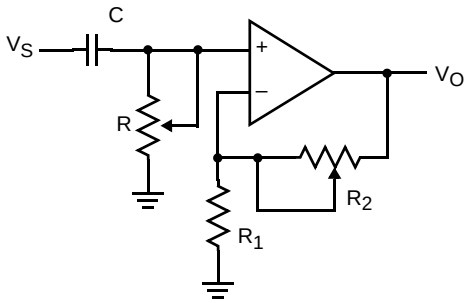
$V_{UL} = \{R_1/(R_1+R_2)\}$ $V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}$ $V_O(min)$

COMPARATOR WITH HYSTERISIS



$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

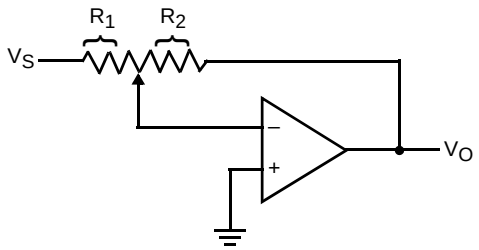
ATTENUATOR



$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

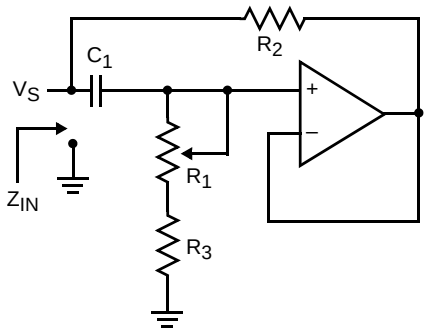
FILTER

Application Circuits (Continued)



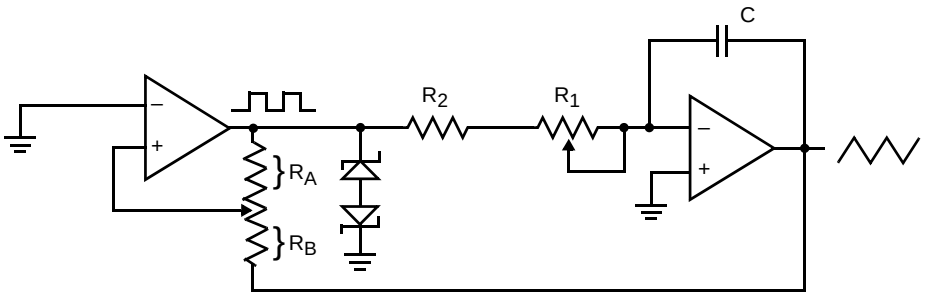
$V_O = G\ V_S$
$G = - R_2/R_1$

INVERTING AMPLIFIER



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

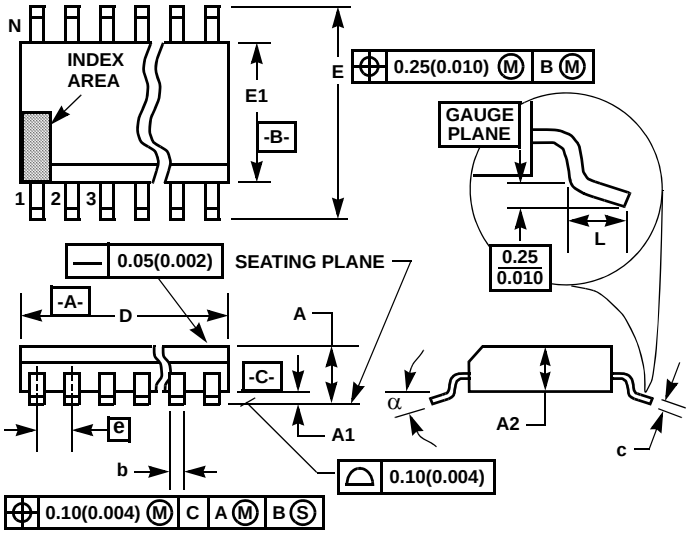
EQUIVALENT L-R CIRCUIT



Frequency $\propto R_1, R_2, C$
Amplitude $\propto R_A, R_B$

FUNCTION GENERATOR

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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