

SCOPE: MICROPROCESSOR SUPERVISORY CIRCUITS

<u>Device Type</u>	<u>Generic Number</u>
01	MAX696(x)/883B
02	MAX697(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>		<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM	SMD			
JE	E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP	2	CQCC1-N20	20 Pin Leadless Chip	L20

Absolute Maximum Ratings

Terminal Voltage

V_{CC} for 01	-0.3V to +6.0V
V_{CC} for 02	+0.3V
V_{BATT} for 01	-0.3V to +6.0V
GND for 02	-0.3V
All other Inputs I_1	-0.3V to ($V_{OUT}+0.5V$)

Input Current

V_{CC}	200mA
V_{BATT}	50mA
GND	20mA

Output Current

V_{OUT}	Short-circuit protected
All other outputs	20mA

Rate of Rise, V_{CC} , V_{BATT} 100V/ μ s

Lead Temperature (soldering, 10 seconds) +300°C

Storage Temperature -65°C to +160°C

Continuous Power Dissipation $T_A=+70^\circ\text{C}$

16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW

20 lead LCC(derate 9.1mW/°C above +70°C) 727mW

Junction Temperature T_J +150°C

Thermal Resistance, Junction to Case, θ_{JC} :

Case Outline 16 lead CERDIP..... 50°C/W

Case Outline 20 leadless Chip carrier 20°C/W

Thermal Resistance, Junction to Ambient, θ_{JA} :

Case Outline 16 lead CERDIP..... 100°C/W

Case Outline 20 leadless Chip carrier 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) -55°C to +125°C

Supply Voltage Range (V_{CC}) +3.0V to 5.5V

NOTE 1: The input voltage limits on PFI and WDI may be exceeded if the input current is limited to less than 10mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125 °C 2/ Unless otherwise specified						
Operating Voltage Range	V _{CC}			1,2,3	01	3.2	5.5	V
					02	3.0	5.5	
	V _{BATT}				01	2.0	V _{CC} -0.3	
Supply Current	I _{CC}			1,2,3	02		400	μA
BATTERY-BACKUP SWITCHING								
Output Voltage	V _{OUT}	I _{OUT} =1mA		1,2,3	01	V _{CC} -0.3		V
		I _{OUT} =50mA				V _{CC} -0.5		
Output Voltage-Battery-Backup Mode	BATT _{OUT}	I _{OUT} =250μA, V _{CC} <V _{BATT} -0.2V		1,2,3	01	V _{BATT} -0.1		V
Supply Current (Excludes I _{OUT})	I _{CC}	I _{OUT} =1mA		1,2,3	01		4,7	mA
		I _{OUT} =50mA		1,2,3			7,10	
Supply Current in Battery-Backup Mode	I _{BATT}	V _{CC} =0V, V _{BATT} =2.8V		1,2,3	01		1,10	μA
Battery Standby Leakage Current	BATT _{SLKG}	5.5V > V _{CC} > V _{BATT} + 1V		1,2,3	01	-0.10, -1.00	0.02, 0.02	μA
Battery-Switchover Threshold, V _{CC} to V _{BATT}	BATT _{SWTH}	Power-Up or Power-Down		1,2,3	All	-200	+200	mV
BATT ON Output Voltage	BATT _{ONOUT}	I _{SINK} =1.6mA		1,2,3	01		0.4	V
BATT ON Output Short-Circuit Current	BATT _{ONIOS}	BATT ON = V _{OUT}		1,2,3	01		60	mA
		BATT ON = 0V, V _{CC} =0V					0.5	
RESET AND WATCHDOG TIMING								
Low-Line Threshold	LL _{IN}	V _{CC} =5V, 3V		1,2,3	All	1.25	1.35	V
Reset Timeout Delay	R _{DEL}	OSC SEL High, V _{CC} =5V		9,10,11	All	35,31	70,78	ms
Watchdog Timeout Period, Internal Oscillator	WD _{INT}	Long period, V _{CC} =5V		9,10,11	All	1.00, 0.90	2.25, 2.42	sec
		Short period, V _{CC} =5V		9,10,11		70,62	140,154	
Watchdog Timeout Period, External Clock	WD _{EXT}	Long period		9,10,11	All	3840	4097	Clock Cycles
		Short period				768	1025	
Minimum WDI Input Pulse Width	WDI _{PW}	V _{IL} =0.4V, V _{IH} =4.0V, V _{CC} =5V		9,10,11	All	200,300		ns
RESET Output Voltage	R _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		9,10,11	All	3.5		V

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125 °C 2/ Unless otherwise specified						
RESET Output Voltage	$\overline{R_{VOL}}$	I _{SINK} =1.6mA		1,2,3	All		0.4	V
		I _{SINK} =400μA, V _{CC} =0V				01	0.4	
LOWLINE Output Voltage	$\overline{LL_{VOH}}$	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
	$\overline{LL_{VOL}}$	I _{SINK} =800μA					0.4	
RESET Output Voltage	R _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
	R _{VOL}	I _{SINK} =1.6mA					0.4	
WDO Output Voltage High	$\overline{WDO_{VOH}}$	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
WDO Output Voltage Low	$\overline{WDO_{VOL}}$	I _{SINK} =800μA		2,3			0.4	V
Output Short-Circuit Current	I _{OS}	RESET, \overline{WDO} , \overline{WDO} , $\overline{LOWLINE}$		1,2,3	All	1.0	25	μA
WDI Input Threshold Logic Low	WDI _{VIL}	V _{CC} =5V	NOTE 3	1 2,3	All		0.8 0.4	V
WDI Input Threshold Logic High	WDI _{VIH}	V _{CC} =5V	NOTE 3	1	01 02	3.5 3.8		V
				2,3	All	4.0		
WDI Input Current	WDI _{IN}	WDI=V _{OUT} WDI=V _{CC} WDI=0V		1	01 02 All		50 50	μA
		WDI=V _{OUT} WDI=V _{CC} WDI=0V		2,3	01 02 All		80 80	
POWER-FAIL DETECTOR								
PFI Input Threshold	PFI _{VIN}	V _{CC} =3V, 5V		1,2,3	All	1.2	1.4	V
PFI-LLIN Threshold Difference	PFI _{LIN}	V _{CC} =3V, 5V		1	All	-50	50	mV
PFI Input Current	PFI _{IN}			1,2,3	All	-25	25	nA
LLIN Input Current	LL _{IN1}			1,2,3	All	-500 -25	25 25	nA
\overline{PFO} Output Voltage	$\overline{PFO_{VOH}}$	I _{SOURCE} =1μA, V _{CC} =5V		1	All	3.5		V
	$\overline{PFO_{VOL}}$	I _{SINK} =1.6mA		2,3		0.4		
\overline{PFO} Short-Circuit Source Current	$\overline{PFO_{IOS}}$	PFI=V _{IH} , \overline{PFO} =0V		1,2,3	All	1.0	25	μA

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units	
		-55 °C ≤ T _A ≤ +125°C 2/ Unless otherwise specified							
CHIP-ENABLE GATING									
CE IN Threshold Logic Low	CE _{VIL}		1	02			0.8	V	
			2,3				0.4		
CE IN Threshold Logic High	CE _{VIH}	V _{CC} =5V	1	02			3.0	V	
			2,3				3.5		
CE IN Pull-Up Current	CE IN _{PI}		1,2,3	02			1.0	25	μA
CE OUT Output Voltage High	CE _{VOH}	I _{SOURCE} =800μA	1,2,3	02			V _{OUT} -0.5		V
		I _{SOURCE} =1μA					V _{OUT} -0.05		
CE Output Voltage Low	CE _{VOL}	I _{SINK} =1.6mA	1,2,3	02				0.4	V
CE Propagation Delay	t _{PDCE}	V _{CC} =5V	9	02				150	ns
			10,11					250	
OSCILLATOR									
OSC IN Input Current	OSCI _{IN}		1,2,3	All				25	μA
OSC SEL Input Pull-Up Current	OSC SEL _{IN}	V _{CC} =5V	1,2,3	All		1		25	μA
OSC IN Frequency Range	OSC IN _{frq}	OSC SEL=0V, V _{CC} =5V	9,10,11	All		0		250	kHz
OSC IN Frequency	OSC _{IN}	OSC SEL=0V, C _{OSC} =47pF NOTE 4	9	All		4			kHz

NOTE 2: V_{CC}=full operating range, V_{BATT}=+2.8V.

NOTE 3: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125kΩ

NOTE 4: Typical for design purposes only but not tested.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	16 pin CERDIP	MAX696MJE/883B	5962-9312502MEA
01	20 pin LCC	MAX696MLP/883B	5962-9312502M2C
02	16 pin CERDIP	MAX697MJE/883B	5962-9312501MEA
02	20 pin LCC	MAX697MLP/883B	5962-9312501M2C

TERMINAL CONNECTIONS:

	MAX696	MAX696	MAX697	MAX697
	J16	L20	J16	L20
1	V _{BATT}	NC	TEST	NC
2	V _{OUT}	V _{BATT}	NC	TEST
3	V _{CC}	V _{OUT}	V _{CC}	NC
4	GND	V _{CC}	LLIN	V _{CC}
5	BATT ON	GND	GND	LLIN
6	$\overline{\text{LOWLINE}}$	NC	$\overline{\text{LOWLINE}}$	NC
7	OSC IN	BATT ON	OSC IN	GND
8	OSC SEL	$\overline{\text{LOWLINE}}$	OSC SEL	$\overline{\text{LOWLINE}}$
9	PFI	OSC IN	PFI	OSC IN
10	$\overline{\text{PFO}}$	OSC SEL	$\overline{\text{PFO}}$	OSC SEL
11	WDI	NC	WDI	NC
12	NC	PFI	$\overline{\text{CE OUT}}$	PFI
13	LLIN	$\overline{\text{PFO}}$	$\overline{\text{CE IN}}$	$\overline{\text{PFO}}$
14	$\overline{\text{WDO}}$	WDI	$\overline{\text{WDO}}$	WDI
15	$\overline{\text{RESET}}$	NC	$\overline{\text{RESET}}$	$\overline{\text{CE OUT}}$
16	RESET	NC	RESET	NC
17		LLIN		$\overline{\text{CE IN}}$
18		$\overline{\text{WDO}}$		$\overline{\text{WDO}}$
19		$\overline{\text{RESET}}$		$\overline{\text{RESET}}$
20		RESET		RESET

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.