BT151S-650S

SCR

23 July 2018 **Product data sheet**

1. General description

Passivated sensitive gate Silicon Controlled Rectifier (SCR) in a SOT428 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct interfacing with low power drivers and microcontrollers
- High bidirectional blocking voltage capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Sensitive gate for logic level control

3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances
- Protection circuits for Switched-Mode Power Supplies (SMPS)
- Protection circuits in lighting ballasts

4. Quick reference data

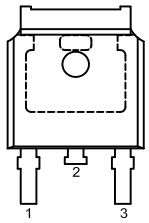
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	650	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 100$ °C; Fig. 1		-	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 100$ °C; Fig. 2; Fig. 3		-	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	90	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	100	A
T_j	junction temperature			-	-	125	°C
Static characteristics							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		20	50	200	µA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 436 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		50	100	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **DPAK (SOT428)**	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151S-650S	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Marking

Table 4. Marking codes

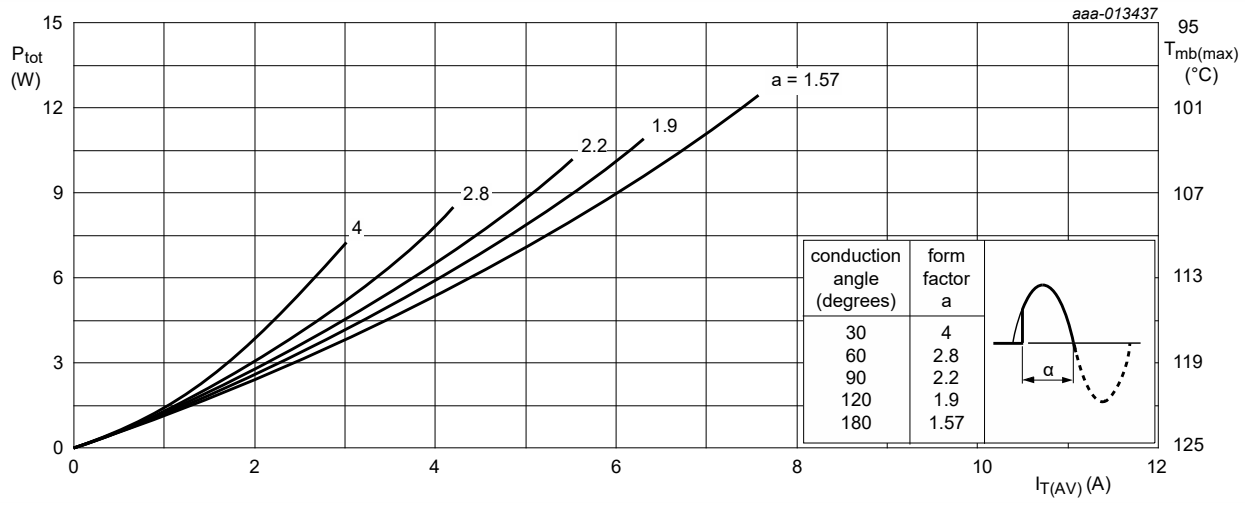
Type number	Marking code
BT151S-650S	BT151S-650S

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	650	V
V_{RRM}	repetitive peak reverse voltage			-	650	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 100$ °C; Fig. 1		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 100$ °C; Fig. 2; Fig. 3		-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	90	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	100	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	41	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 50$ mA		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C



α = conduction angle

a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

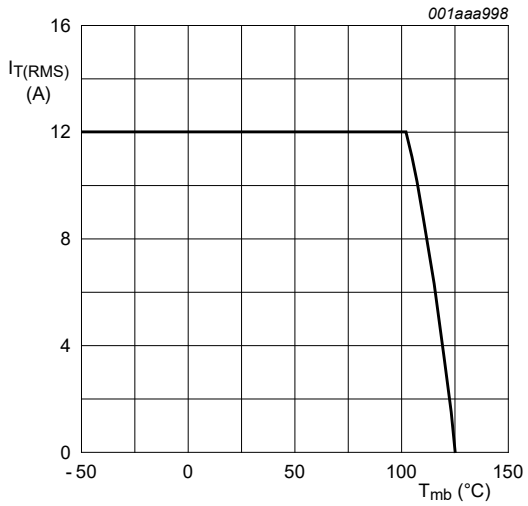
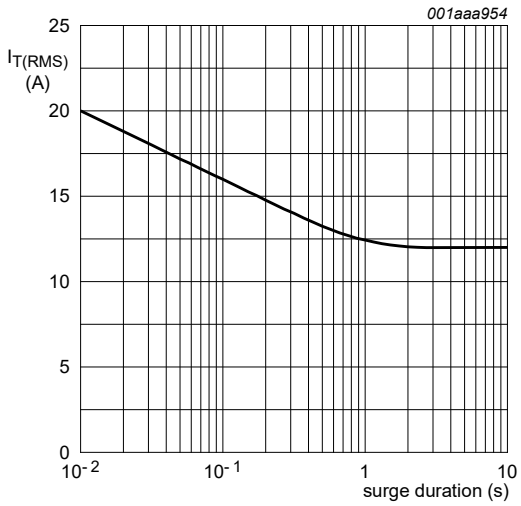
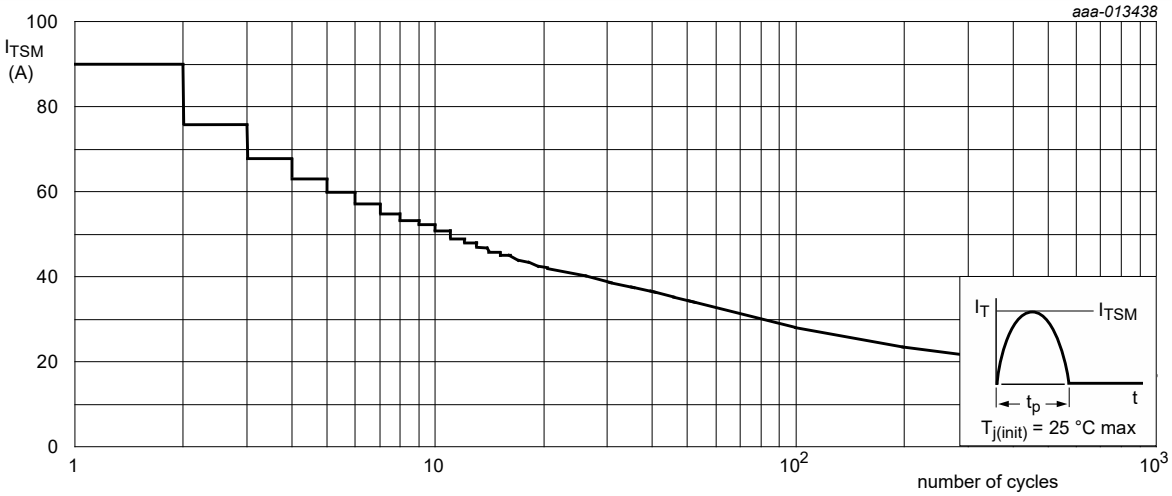


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



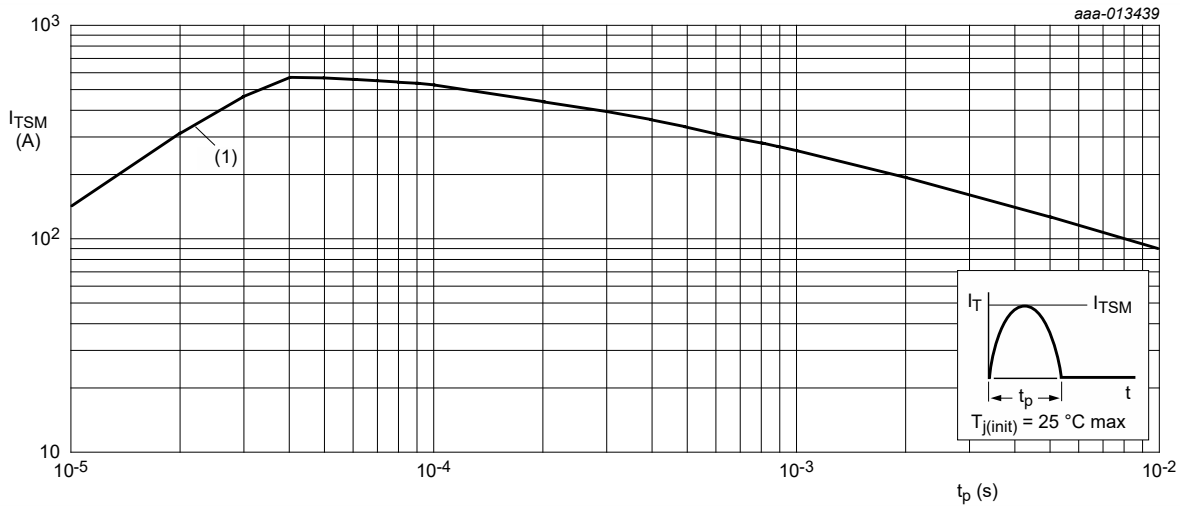
f = 50 Hz; T_{mb} = 103 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms
(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	mounted on an FR4 printed-circuit board; Fig. 7		-	7	-	K/W

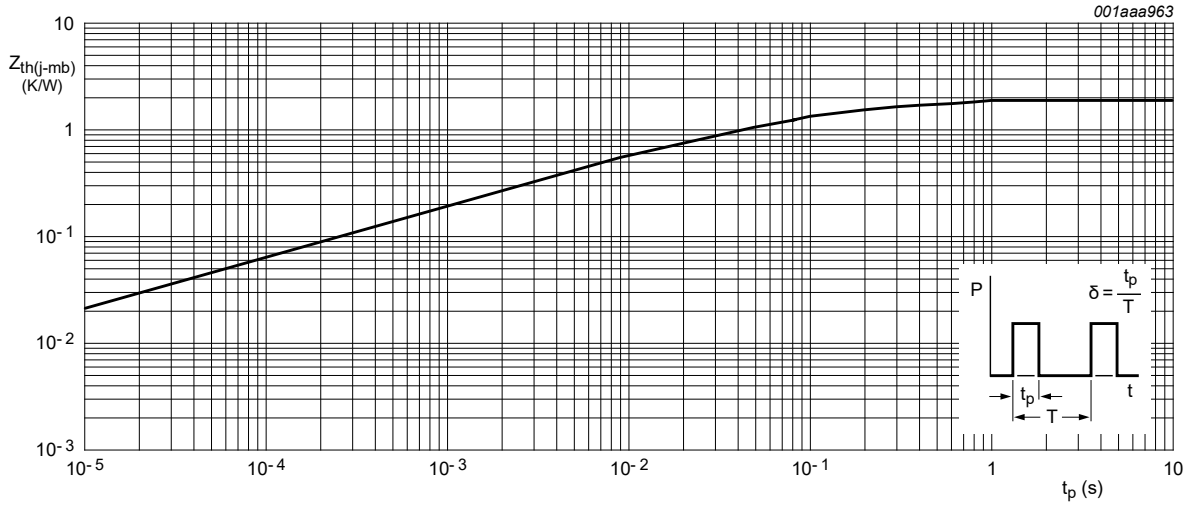
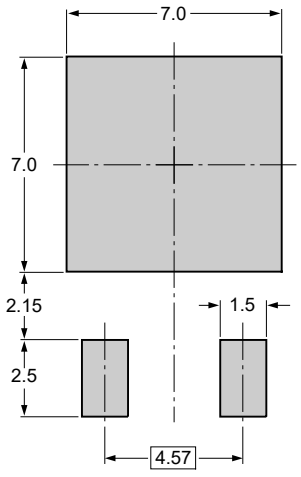


Fig. 6. Transient thermal impedance from junction to mounting base as as function of pulse width



001aab021 all dimensions are in mm

Fig. 7. Minimum footprint SOT428

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		20	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 9		-	0.4	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	0.3	6	mA
V_T	on-state voltage	I_T = 20 A; T_j = 25 °C; Fig. 11		-	1.3	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 12		-	0.6	1	V
		V_D = 650 V; I_T = 0.1 A; T_j = 110 °C; Fig. 12		0.1	0.2	-	V
I_D	off-state current	V_D = 650 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 650 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 436 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		50	100	-	V/µs

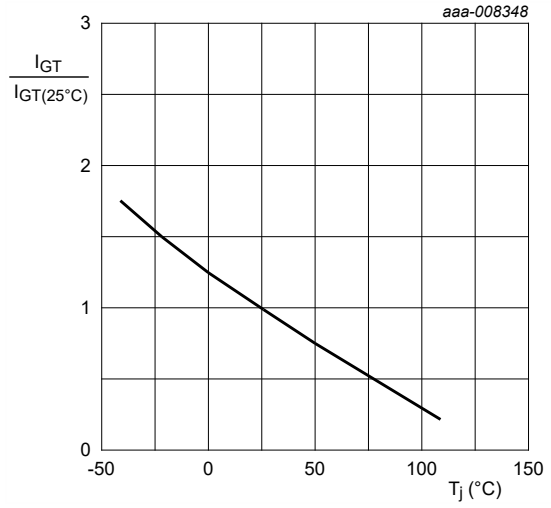


Fig. 8. Normalized gate trigger current as a function of junction temperature

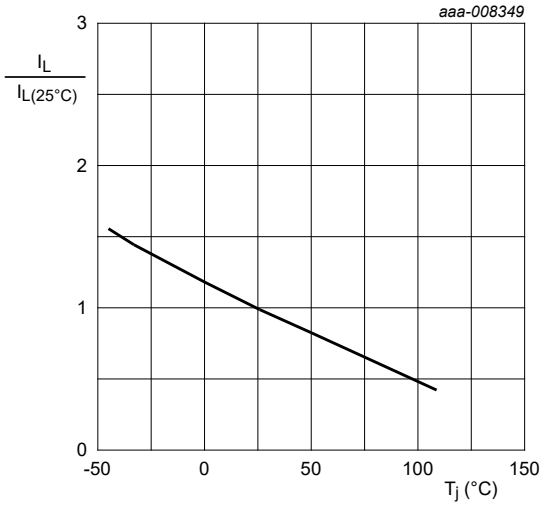


Fig. 9. Normalized latching current as a function of junction temperature

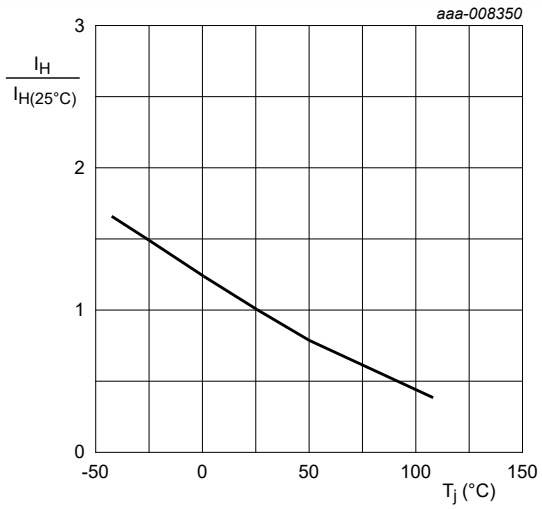
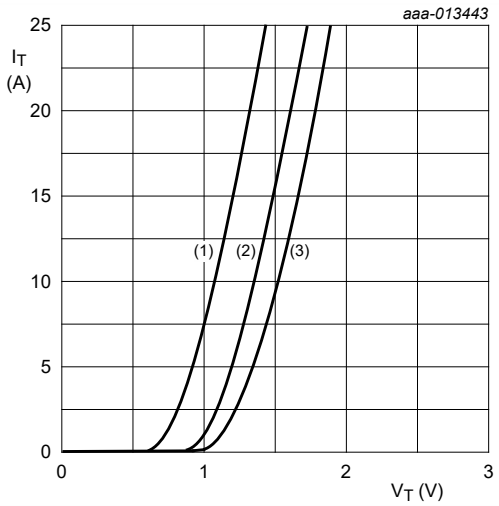


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.075 V; R_s = 0.028 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

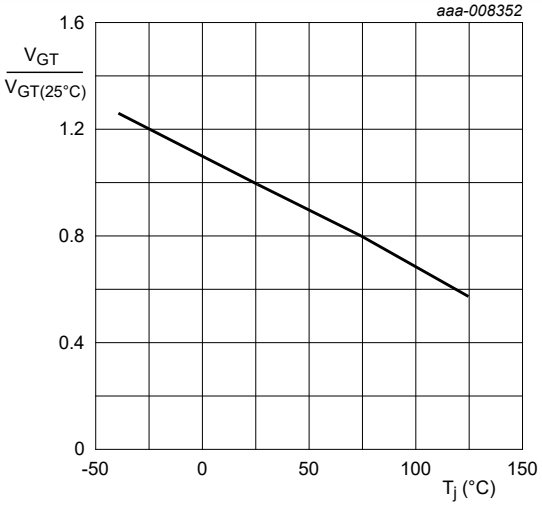
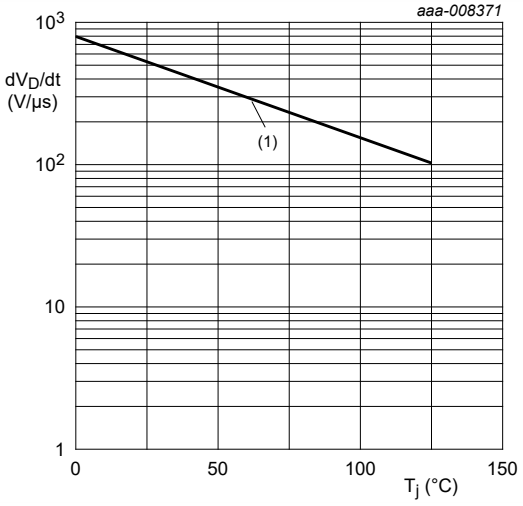


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

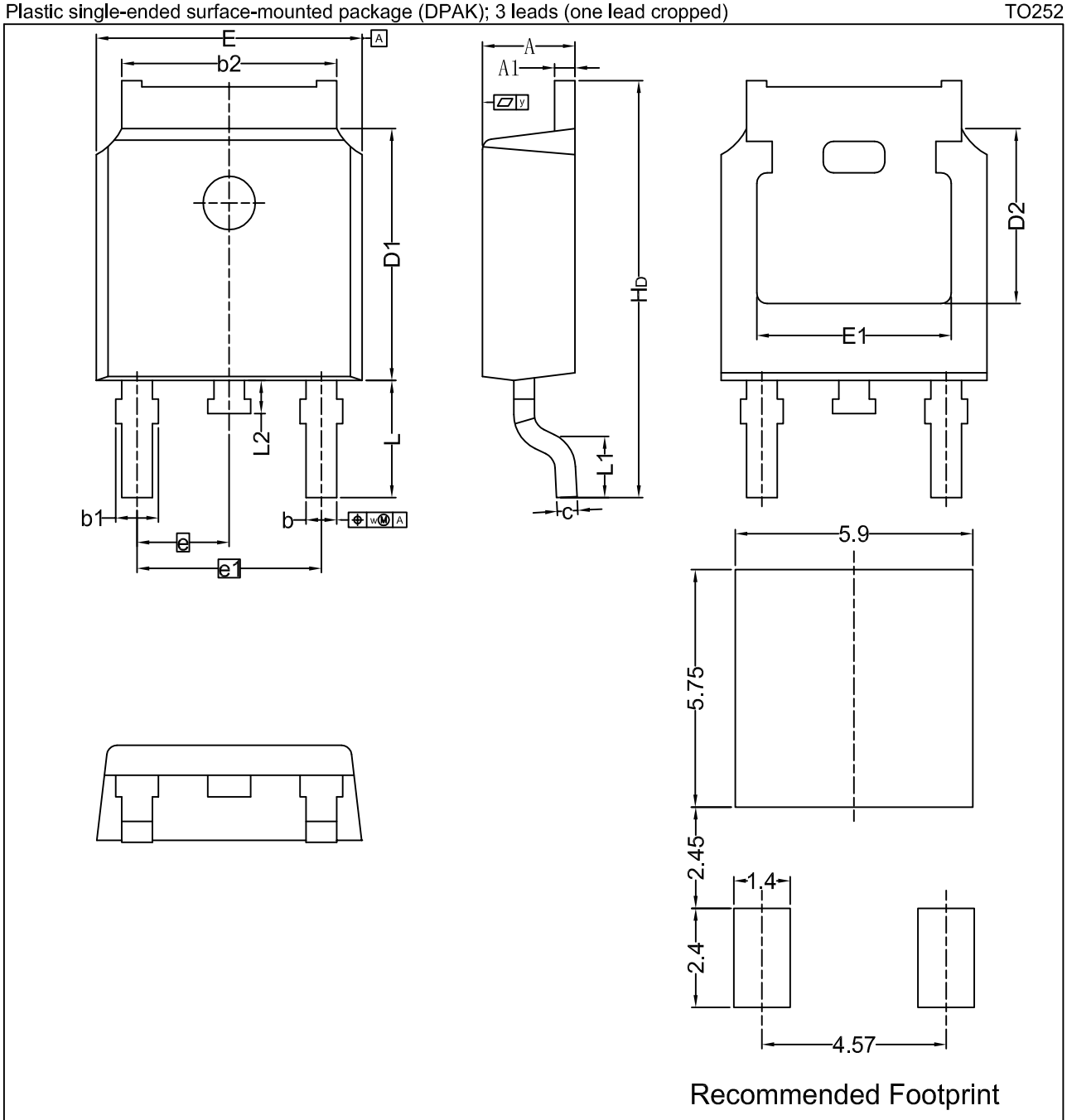


(1) R_{GK} = 100 Ω

Fig. 13. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Unit	A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45	2.285	4.57	9.60	2.90 (Ref.)	0.50	0.50	0.20	
mm nom																		
max	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		0.20

Fig. 14. Package outline DPAK (SOT428)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

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