Product Brief

MPC533PB/D
Rev. 0, 2/2003

MPC533/MPC534
Product Brief

MOTOROLA intelligence everywhere™ | digital dna™

This document provides an overview of the MPC533/MPC534 microcontroller, including a block diagram showing the major modular components, sections that list the major features, and differences between the MPC533 and the MPC555. The MPC533 and MPC534 devices are members of the Motorola MPC500 RISC Microcontroller family. The parts herein will be referred to only as MPC533 unless specific parts need to be referenced.

Table 1. MPC533/MPC534 Features

Device	Flash	Code Compression
MPC533	512 Kbytes	Code compression not supported
MPC534	512 Kbytes	Code compression supported

1 Introduction

The MPC533 device offers the following features:

- 32-bit single issue PowerPC™ core
- Unified system integration unit (USIU) with a flexible memory controller and enhanced interrupt controller (EIC)
- 64-bit floating-point unit (FPU)
- 512-Kbytes of Flash EEPROM memory
  - Typical endurance of 100,000 write/erase cycles @ 25ºC
  - Typical data retention of 100 years @ 25ºC
- 32-Kbytes of static RAM in one CALRAM module, configured as
  - 28-Kbyte normal access only array
  - 4-Kbyte normal access or overlay access array (eight 512-byte regions)
- One 22-timer channel modular I/O system (MIOS14)
- One TouCAN module (TouCAN B)
- Enhanced queued analog system (QADC64E)
- One queued serial multi-channel module (QSMCM), which contains one queued serial peripheral interface (QSPI) and two serial controller interfaces (SCI/UART)
- One peripheral pin multiplexing module (PPM) with a parallel to serial driver

- Debug features:
  - Nexus debug port (Level 3)
  - Background debug mode (BDM)
  - IEEE1194.1 compliant interface (JTAG)
- Plastic ball grid array (PBGA) packaging
  - 388 ball PBGA
  - 27 mm x 27 mm body size
  - 1.0 mm ball pitch
- 40-MHz operation
- -40°C–85°C
- Two power supplies
  - 5-V I/O (5.0 ± 0.25 V)
  - 2.6 ± 0.1-V external bus with a 5-V tolerant I/O system
  - 2.6 ± 0.1-V internal logic
  - IRAMSTBY on-chip voltage regulator

1.1 Block Diagram

Figure 1 is a block diagram of the MPC533.

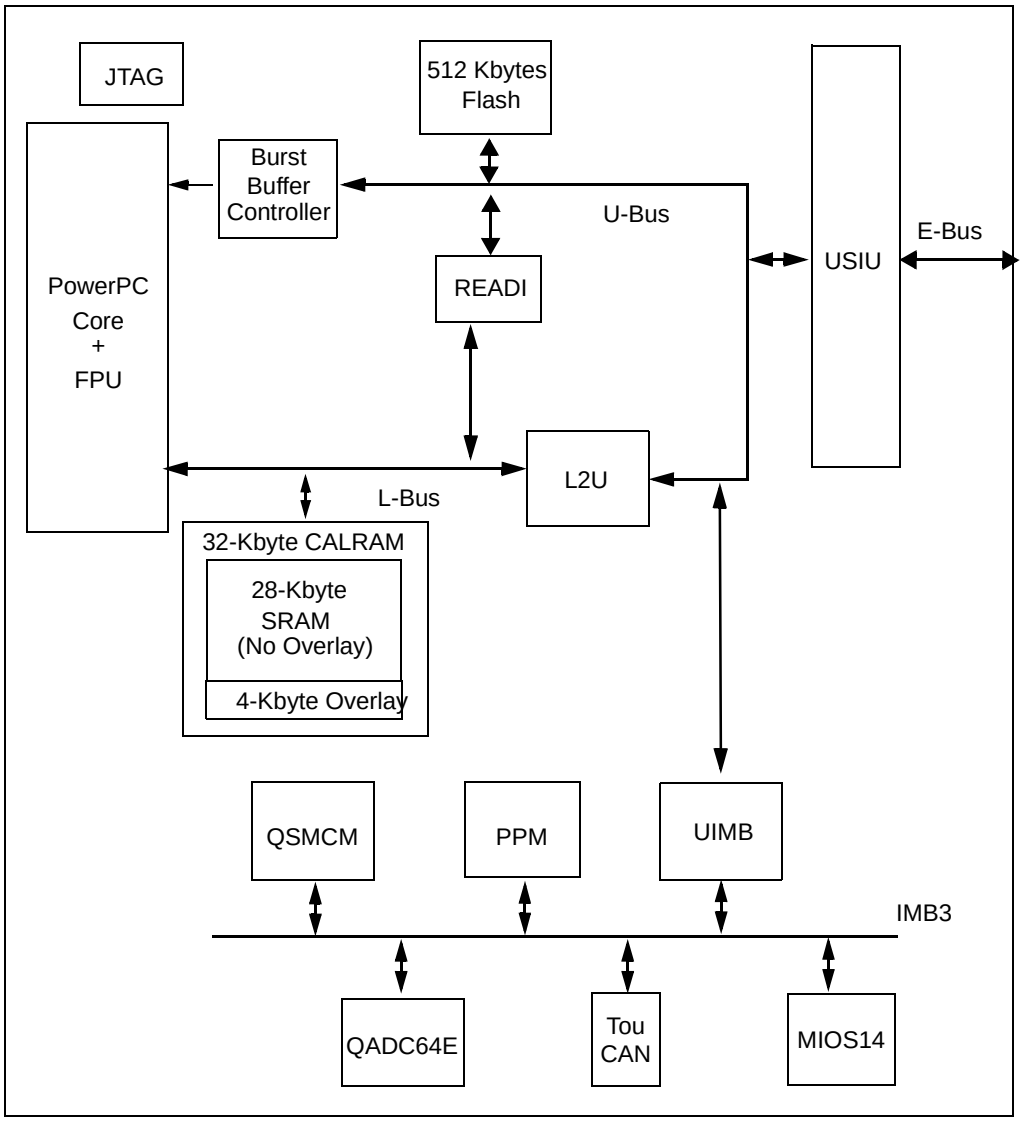

Figure 1. MPC533 Block Diagram

1.2 Key Features

The MPC533 key features are explained in the following sections.

1.2.1 High Performance CPU System

- Fully static design
- Four major power saving modes
  - On, doze, sleep, deep-sleep, and power-down

1.2.1.1 RISC MCU Central Processing Unit (RCPU)

- 32-bit single issue PowerPC core
- Precise exception model
- 64-bit floating point unit (FPU)
- Code compression supported on MPC534
  - Reduces usage of internal/external Flash memory (up to 50% for code)
  - The code compression feature is optimized for automotive (non-cached) applications
- Extensive system development support
  - On-chip watchpoints and breakpoints
  - Program flow tracking

1.2.1.2 MPC500 System Interface (USIU)

- System configuration and protection features:
  - Periodic-interrupt timer
  - Bus monitor
  - Software watchdog timer
  - Real-time clock (RTC)
  - PPC decrementer
  - Time base
- Clock synthesizer
- Power management
- Reset controller
- External bus interface that tolerates 5-V inputs, provides 2.6-V outputs, and supports multiple-master designs
- Enhanced interrupt controller that supports up to eight external and 40 internal interrupts, simplifies the interrupt structure, and decreases interrupt processing time
- USIU supports dual mapping to map part of one internal/external memory to another external memory
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

1.2.1.3 Burst Buffer Controller (BBC) Module

- Support for enhanced interrupt controller (EIC)
- Support for enhanced exception table relocation feature
- Branch target buffer
- Contains 2 Kbytes of decompression RAM (DECRAM) for code compression. This RAM may also be used as general-purpose RAM when code compression feature not used.

1.2.1.4 Flexible Memory Protection Unit

- Flexible memory protection units (MPU) in BBC and L2U
- Default attributes available in one global entry
- Attribute support for speculative accesses
- Up to eight memory regions are supported, four for data and four for instructions

1.2.1.5 Memory Controller

- Four flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4-Kbyte to one 16-Mbyte (data) or 4-Gbyte (instruction) region size support
- Supports enhanced external burst
- Up to eight-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four regions

1.2.1.6 512-Kbytes of CDR3 Flash EEPROM Memory (UC3F)

- One 512-Kbyte module
- Page read mode
- Block (64 Kbytes) erasable
- External 4.75- to 5.25-V VFLASH power supply for program, erase, and read operations
- Typical endurance of 100,000 write/erase cycles @ 25ºC
- Typical data retention of 100 years @ 25ºC

1.2.1.7 32-Kbyte Static RAM (CALRAM)

- Composed of one 32-Kbyte CALRAM module
  - 28-Kbyte static RAM
  - 4-Kbyte calibration (overlay) RAM feature that allows calibration of flash-based constants
- Eight 512-byte overlay regions
- One clock fast accesses
- Two clock cycle access option for power saving
- Keep-alive power (IRAMSTBY) for data retention

1.2.1.8 General Purpose I/O Support (GPIO)

- 24 address pins and 32 data pins can be used for general-purpose I/O in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 2.6-V outputs on external bus pins
- 5-V outputs with slew rate control

1.2.2 Nexus Debug Port (Class 3)

- Compliant with Class 3 of the IEEE-ISTO 5001-1999
- Program trace via branch trace messaging (BTM)
- Data trace via data write messaging (DWM) and data read messaging (DRM)
- Ownership trace via ownership trace messaging (OTM)
- Run-time access to on-chip memory map and special purpose registers (SPRs) via the READI read/write access protocol
- Watchpoint messaging via the auxiliary port
- 9 or 16 full-duplex auxiliary pin interface for medium and high visibility throughput
- All features configurable and controllable via the auxiliary port
- Security features for production environment
- Supports the RCPU debug mode via the auxiliary port
- READI module can be reset independent of system reset

1.2.3 Integrated I/O System

1.2.3.1 22-Channel Modular I/O System (MIOS14)

- Six modulus counter sub-modules (MCSM)
- 10 double-action sub-modules (DASM)
- 12 dedicated PWM sub-modules (PWMSM)
- One MIOS14 16-bit parallel port I/O sub-modules (MPIOSM)

1.2.3.2 Enhanced Queued Analog-to-Digital Converter Module (QADC64E)

- Queued analog-to-digital converter module (QADC64E_A) providing a total of 16 analog channels using internal multiplexing
- Directly supports up to four external multiplexers
- Up to 41 total input channels on the QADC64E module with external multiplexing
- Software configurable to operate in enhanced or legacy (MPC555 compatible) mode
- Unused analog channels can be used as digital input/output pins
- GPIO on all channels in enhanced mode
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of less than 5 µs (>200 K samples/second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - External edge trigger
  - Software command
  - Periodic/interval timer within QADC64E module, that can be assigned to both queue 1 and 2
  - External gated trigger (queue 1 only)
- 64 result registers
  - Output data is right- or left-justified, signed or unsigned.
- Alternate reference input (ALTREF), with control in the conversion command word (CCW)

1.2.3.3 One CAN 2.0B Controller (TouCAN) Module

- One TouCAN module (TouCAN B)
- TouCAN provides the following features:
  - 16 message buffers, programmable I/O modes
  - Maskable interrupts
  - Independent of the transmission medium (external transceiver is assumed)
  - Open network architecture, multi-master concept
  - High immunity to EMI
  - Short latency time for high-priority messages
  - Low-power sleep mode, with programmable wake-up on bus activity

1.2.3.4 Queued Serial Multi-Channel Module (QSMCM)

- One queued serial module with one queued SPI and two SCIs (QSMCM)
- QSMCM matches full MPC555 QSMCM functionality
- Queued SPI
  - Provides full-duplex communication port for peripheral expansion or inter-processor communication
  - Up to 32 preprogrammed transfers, reducing overhead
  - Synchronous serial interface with baud rate of up to system clock / 4
  - Four programmable peripheral-selects pins:
  - Support up to 16 devices with external decoding
  - Support up to eight devices with internal decoding
  - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
  - UART mode provides NRZ format and half- or full-duplex interface
  - 16 register receive buffers and 16 register transmit buffers on one SCI
  - Advanced error detection and optional parity generation and detection
  - Word-length programmable as eight or nine bits
  - Separate transmitter and receiver enable bits, and double buffering of data
  - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

1.2.3.5 Peripheral Pin Multiplexing (PPM)

- Synchronous serial interface between the microprocessor and an external device
- Two internal parallel data sources can be multiplexed through the PPM
  - MIOS14: 12 PWM channels, four MDA channels
  - Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
- Software configurable stream size
- Software configurable clock (TCLK) based on system clock
- Software selectable clock modes (SPI mode and TDM mode)

- Software selectable operation modes
  - — Continuous mode
  - — Start-transmit-receive (STR) mode
- Software configurable internal modules interconnect (shorting)

1.3 MPC533 Optional Features

The following features of the MPC533 are optional features and may not appear in certain configurations:

- Code compression on MPC534

2 Comparison of MPC533 and MPC555

The MPC533 is a derivative of the MPC555. Most functional features of the MPC555 are unchanged on the MPC533. Refer to Table 2 for a comparison of features.

Table 2. Differences Between MPC555 and MPC533

Module	MPC555	MPC533
CPU Core	Identical	
BBC	Basic	Enhanced Code Compression (classes scheme with 2 Kbytes DECRAM) Code Compression is available only on MPC534.
L2U	Identical	
SRAM	26 Kbytes	32 Kbytes calibration SRAM with overlay features
Flash	448-Kbyte CMF (2 modules, 256-Kbyte and 192-Kbyte)	512-Kbyte UC3F (1 module)
USIU	Basic	Enhanced Interrupt Controller
JTAG	Selectable by RCW	Selectable at $\overline{\text{PORESET}}$
READI	None	New Debut Module (Class 3 Nexus IEEE-ISTO 5001-1999)
UIMB	Identical	
QADC64	(2)	(1) Enhanced
QSMCM	(1) Identical (1)	
MIOS	MIOS1	MIOS14 4 Extra PWMSM 4 Extra MCSM no Real-Time Clock
TouCAN	(2) Identical (1)	
PPM	—	New Module

2.1 Additional MPC533 Differences

- The MPC533 is very similar to the MPC555 with the following differences:
  - CDR3 technology
  - Two power supplies: 5.0-V I/O, 2.6-V external bus pins, 2.6-V internal logic
  - New modules: READI, CALRAM, PPM
  - One less TouCAN module, 6 Kbytes extra of SRAM on L-bus (32 Kbytes total) (with CALRAM overlay features)
- QADC64
  - GPO on all channel pins in addition to GPI functions
- TouCAN, QSMCM, UIMB, Core, L2U
  - No changes
- BBC
  - Enhanced interrupt controller support
  - Enhanced exception relocation table
  - Branch target buffer
  - 2 Kbytes of decompression RAM for code compression. This may also be used as general-purpose RAM while not used for code compression.
- CALRAM (with overlay features)
  - New module
  - Overlay features allow calibration of Flash-based constants
- UC3F (U-bus CDR3 Flash module)
  - 512 Kbytes of non-volatile memory (NVM)
  - Designed for use in embedded microcontroller (MCU) applications targeted for high speed read performance and high density byte count requirements
- READI
  - New module
- USIU
  - Enhanced interrupt controller
  - ENGCLK default frequency
  - READI support
  - Reduced data setup time
  - Enhanced external burst support
- MIOS14
  - Four additional PWM channels
  - Four additional MCSM timers
- PPM (peripheral pin multiplexing)
  - New module
  - Two-to-one multiplexing
  - Parallel to serial (SPI and TDM)

3 SRAM Keep-Alive Power Behavior

One keep-alive power pin (IRAMSTBY) provides keep-alive power to RAM.

The IRAMSTBY pin can be powered directly from a battery using an internal shunt regulator or via a small battery for standby use. See Figure 2.

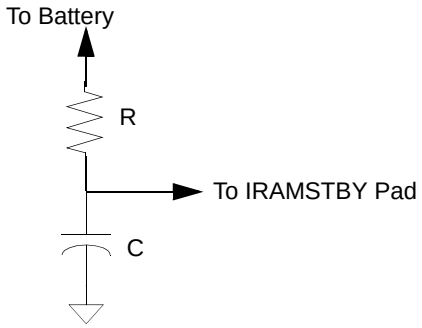

Figure 2. Recommended Connection Diagram for IRAMSTBY

While power is off to the MPC533, the IRAMSTBY supply powers the following:

- 32-Kbyte CALRAM
- 2-Kbyte BBC DECRAM module

4 MPC533 Address Map

The internal memory map is organized as a single 4-Mbyte block. The user can assign this block to one of eight locations by programming a register in the USIU (IMMR[ISB]). The eight possible locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000 (refer to Figure 3). The programmability of the internal memory map location allows the user to implement a multiple-chip system.

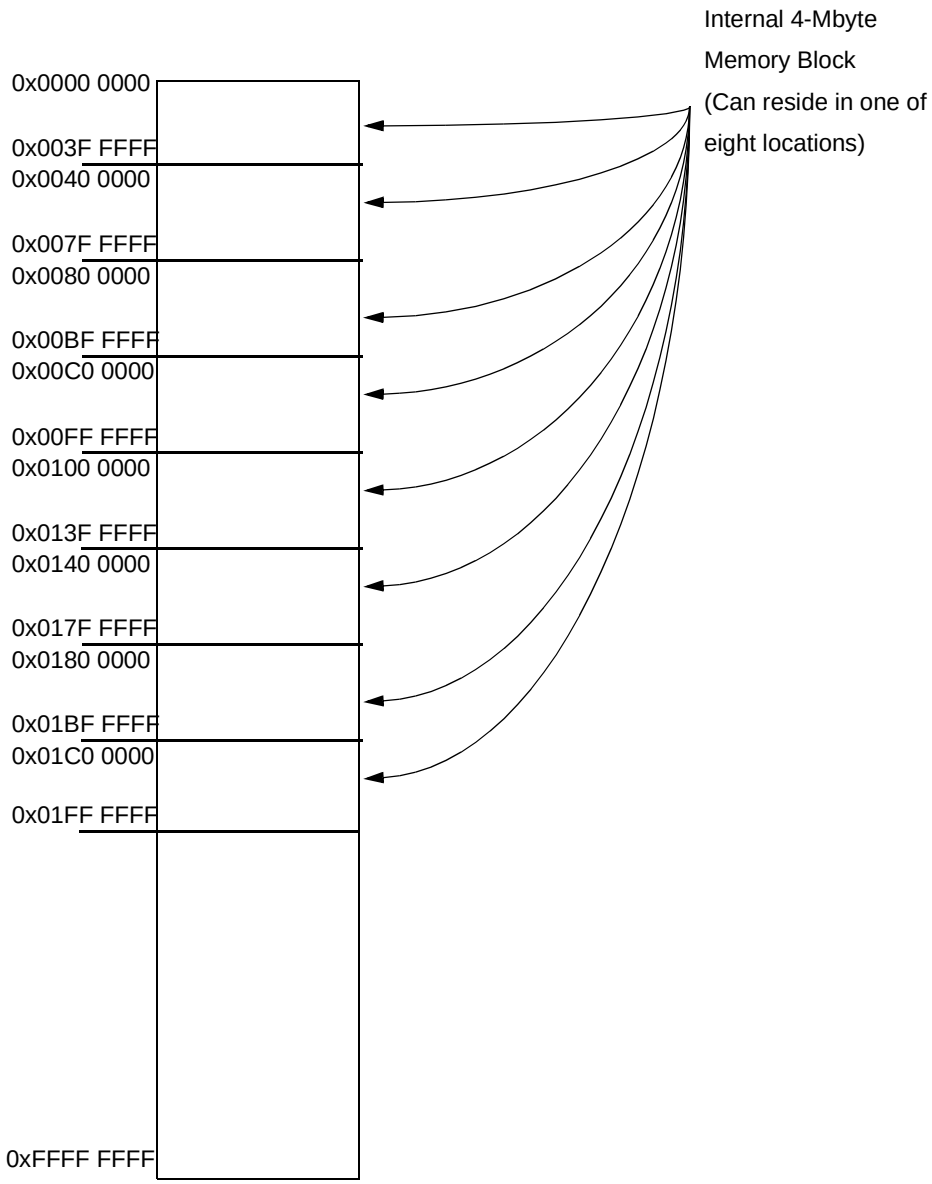

Figure 3. MPC533 Memory Map

The internal memory space is divided into the following sections. Refer to Figure 4.

- Flash memory (512-Kbytes)
- CALRAM static RAM memory (32-Kbytes)
- Control registers and IMB3 modules (64 Kbytes)
  - — BBC control registers (16-Kbytes)
  - — USIU and Flash control registers (16-Kbytes)
  - — UIMB interface and IMB3 modules (32-Kbytes)
  - — CALRAM/READI control registers (256-bytes)

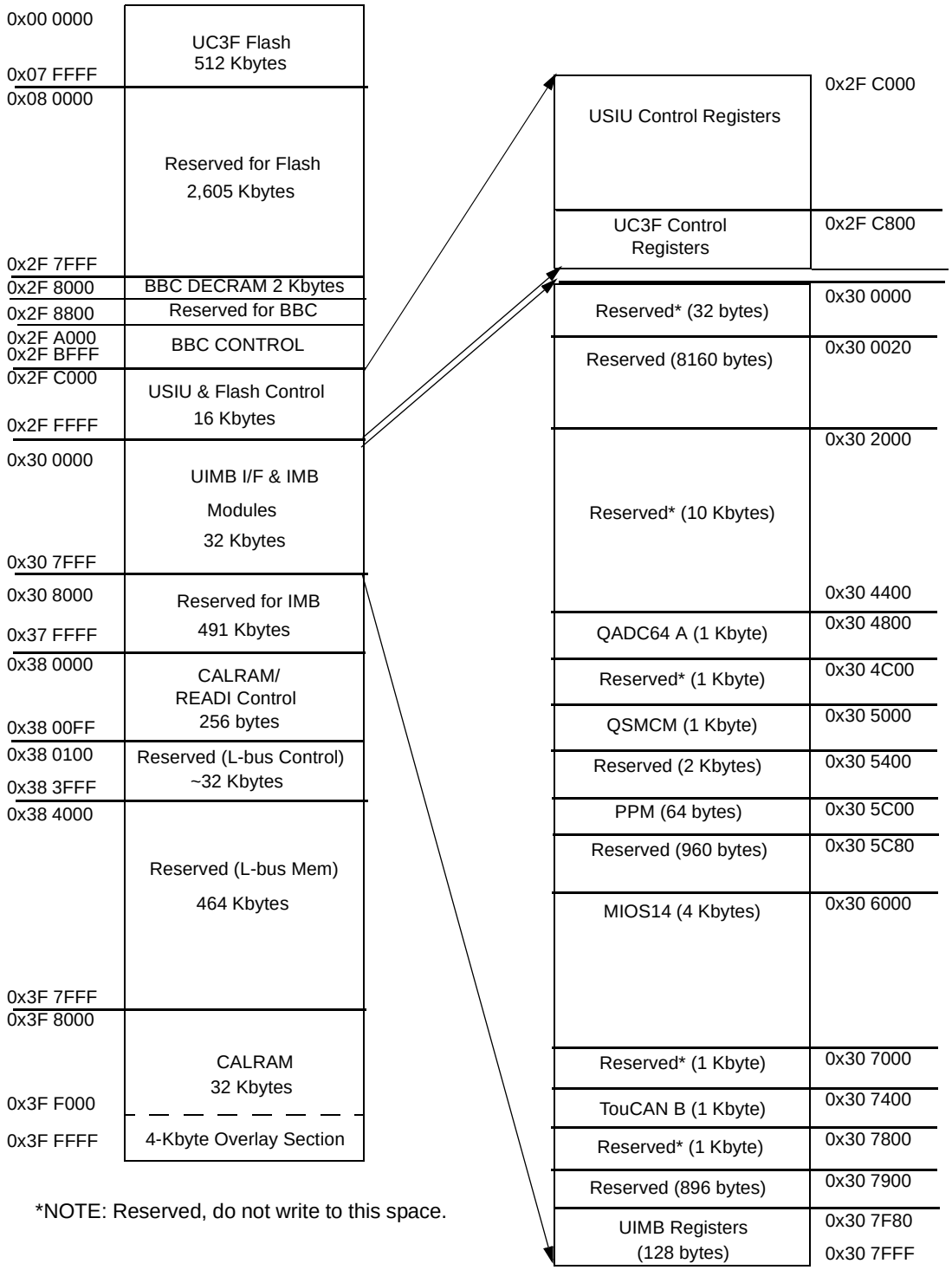

Figure 4. MPC533 Internal Memory Map

5 MPC533 Pinout Diagram

Figure 5 shows the pinout for the MPC533.

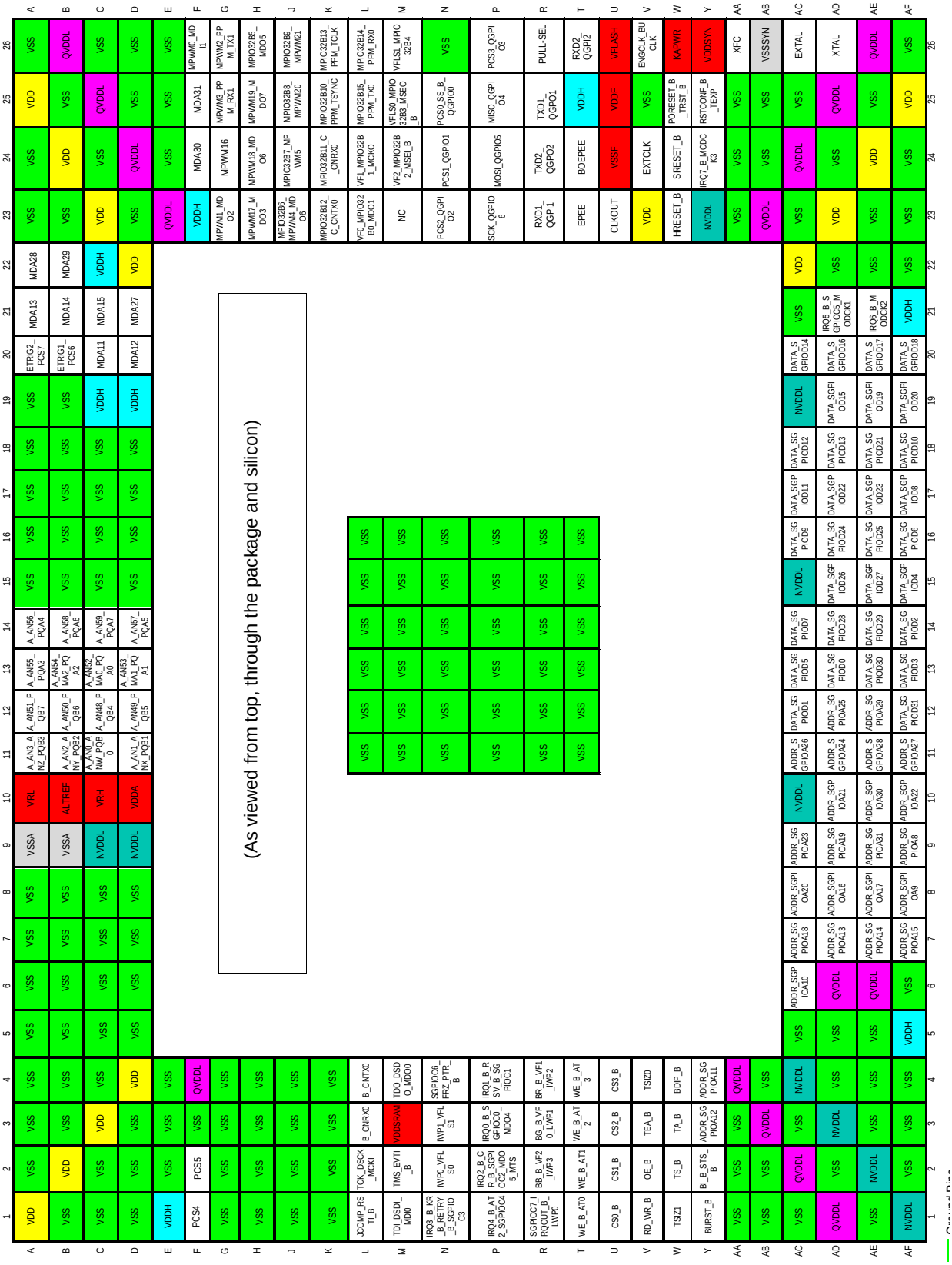

Figure 5. MPC533 Pinout Diagram

6 Supporting Documentation List

This list contains references to currently available and planned documentation.

- *MPC555 User's Manual* (MPC555UM/AD)
- *MPC533 Reference Manual* (MPC533RM/D)
- *RCPU Reference Manual* (RCPURM/AD)
- Nexus Standard Specification (non-Motorola document)
- Nexus Web Site: http://www.nexus5001.org/
- IEEE 1149.1 Specification (non-Motorola document)

THIS PAGE INTENTIONALLY LEFT BLANK

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

MOTOROLA

MPC533PB/D