A8672

Fixed Frequency High Current Synchronous Buck Regulator With Fault Warnings and Power OK

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 1, 2016

Recommended Substitutions: no direct replacement

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Fixed Frequency High Current Synchronous Buck Regulator With Fault Warnings and Power OK

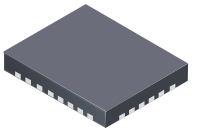
Features and Benefits

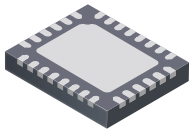
- High efficiency integrated FETs optimized for lower duty cycle voltage conversion: 27 mΩ high side, 12 mΩ low side
- Power input voltage range: 3 to 16 V
- Control input voltage range: 4.5 to 16V
- Adjustable output voltage, down to 0.6 V
- 5 V LDO Regulator
- Extremely short minimum controllable on-time; example: allows 12 V conversion to 0.6 V at >1 MHz
- Reference accuracy of ±1% throughout temperature range
- $\overline{\text{FAULT}}$ and Power OK pins for operating and protection modes
- Low power mode (LPM) or fixed continuous conduction mode (FCCM) operation
- Programmable soft-start / hiccup shutdown period
- Ultra-fast transient response

Applications

- Servers
- Point of load supplies
- Network and telecom
- Storage

Package: 28-contact QFN with exposed thermal pad (suffix EG)





Approximate size

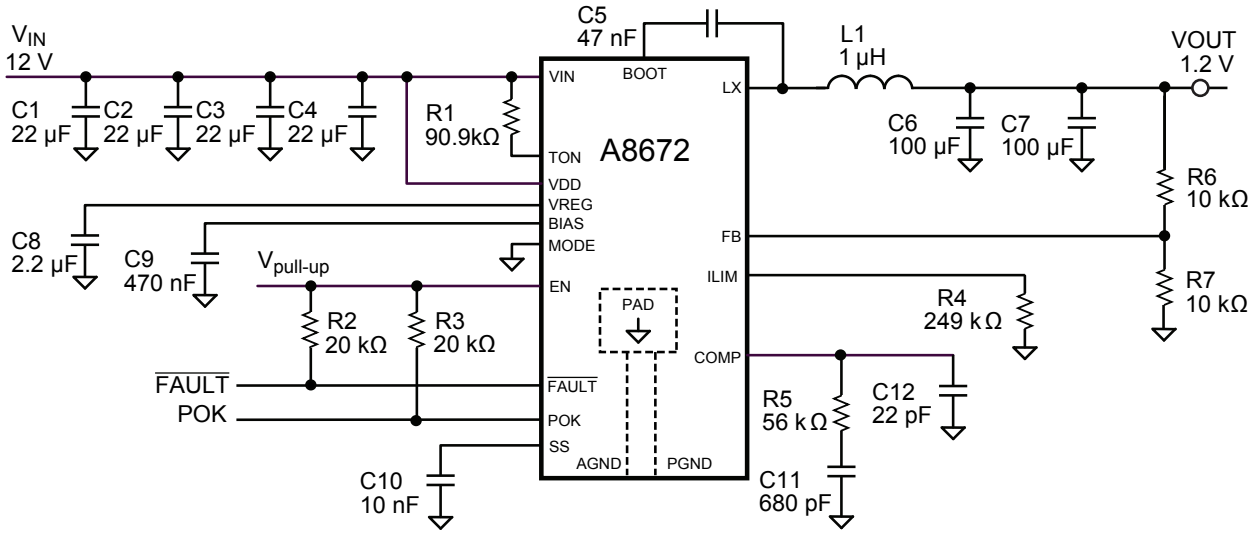
Description

The A8672 is a synchronous buck converter capable of delivering up to 8 A. The A8672 utilizes valley current mode control, allowing very short on-times to be achieved. This makes it ideal for applications that require very low output voltages relative to the input voltage, combined with high switching frequencies. Valley current mode control inherently provides improved transient response over traditional switcher schemes, through the use of a voltage feedforward loop and frequency modulation during large signal load changes.

The A8672 includes a comprehensive set of diagnostic flags, allowing the host platform to react to a myriad of different conditions. A fault output indicates when either the temperature is becoming unusually high, or a single point failure has occurred; for example, the switching node (LX) shorted to ground, or the timing resistor going open-circuit. A Power OK (POK) output is also provided after a fixed delay, to indicate when the output voltage is within regulation. The selectable pulse-by-pulse current limit avoids the requirement to oversize the inductor to cope with large fault currents.

The device package (EG) is a 28-contact, 4 mm × 5 mm, 0.75 mm nominal overall height QFN with exposed thermal pad. The package is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram



V_{IN} = 12 V, V_{OUT} = 1.2 V, and f_{SW} = 500 kHz

Selection Guide

Part Number	Packing*
A8672EEGTR-T	7000 pieces per 13-inch reel

*Contact Allegro™ for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
VIN, VDD, TON, VREG, BIAS and EN Pin Voltage	V_I	With respect to GND	–0.3 to 18	V
LX Pin Voltage	V_{LX}	With respect to GND	–0.6 to V_{IN} + 0.3	V
		t < 50 ns, with respect to GND	–2.0	V
BOOT Pin Voltage	V_{BOOT}	With respect to GND	V_{LX} – 0.3 to V_{LX} + 8.0	V
All Other Pins	–		–0.3 to 7.0	V
Operating Ambient Temperature	T_A	E temperature range	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

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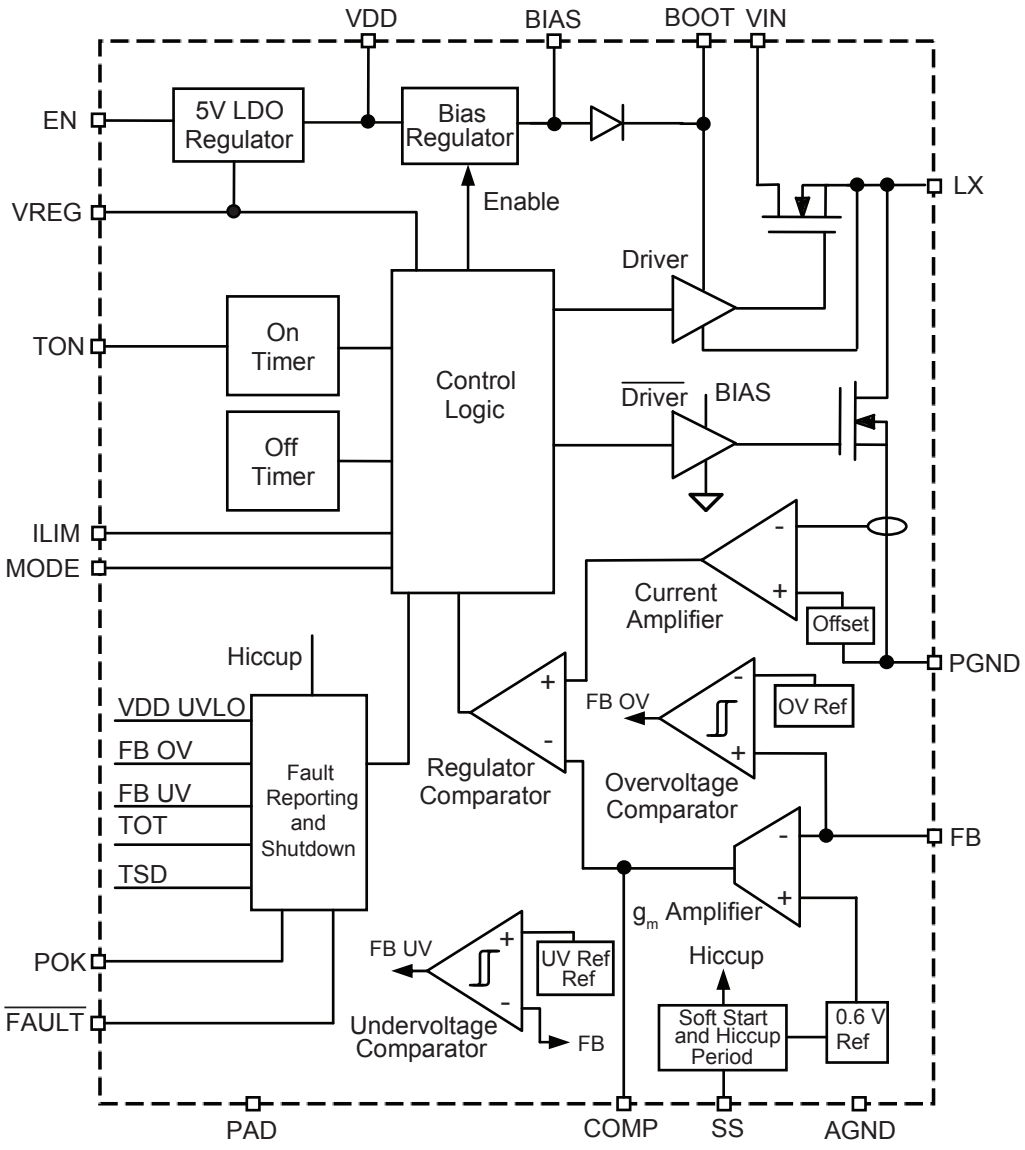
Functional Block Diagram

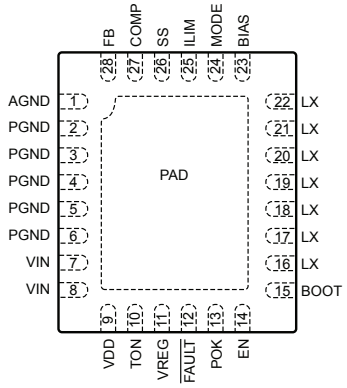


Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Estimated, on 4-layer PCB based on JEDEC standard	33	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro website

Pin-out Diagram



Terminal List Table

Number	Name	Function
1	AGND	Analog ground. Connect to PGND at PAD of device. This pin should be used as the FB resistor divider ground reference for optimal accuracy (see Typical Applications section circuit diagrams).
2,3,4,5,6	PGND	Power ground. Connect to PAD of device.
7,8	VIN	Power input to the drain of the internal high-side MOSFET. This pin must be locally bypassed (see Typical Applications section circuit diagrams).
9	VDD	Power input for the control circuit and drive signals for the internal switching MOSFETs. This pin can be either connected directly to VIN, or in applications where a low VIN voltage is used, it can be driven by a separate power source to ensure adequate overdrive of the switching MOSFETs and control supply.
10	TON	On-Time pin. The resistor connected between this pin and VIN defines the on-time of the regulator. This in turn defines the switching frequency for a given output voltage.
11	VREG	5 V LDO regulator output and supply for internal control circuitry.
12	$\overline{\text{FAULT}}$	Open drain $\overline{\text{FAULT}}$ output. This pin is logic low if the on-time exceeds a certain value, if the LX node is shorted to ground, or if the thermal shutdown threshold (T_J > 140°C) has been reached (see Fault Handling and Reporting table).
13	POK	Open drain Power Okay (power good) output. This pin is logic low if any fault (as defined in the Fault Handling and Reporting table) occurs, other than an overtemperature condition (T_J > 140°C).
14	EN	Enable pin. This pin is a logic input that turns the converter on or off. When EN > V_{ENHI}, the part turns on.
15	BOOT	High-side gate drive supply input. This pin supplies the drive for the high-side switching MOSFET switch.
16,17,18,19, 20,21,22	LX	The source of the internal high-side switching MOSFET. The output inductor and BOOT capacitor should be connected to this pin (see Typical Applications section circuit diagrams).
23	BIAS	Internal regulated bias supply for the control circuit and drives for switching MOSFETs (see Typical Applications section circuit diagrams for recommended capacitors).
24	MODE	When pulled to the VREG supply via a 10 kΩ resistor, fixed continuous conduction mode (FCCM) is maintained across the full load range. When pulled directly to GND, the switcher enters lower power mode (LPM) at light loads.
25	ILIM	Valley current limit setting. Connect a resistor to ground to set a voltage between 2.75 and 1.5 V that corresponds to a valley overload current of between 9 and 3 A (typ).
26	SS	Soft-start ramp pin. The capacitor connected to this pin defines the rate of rise of the output voltage and the effective inrush current. Soft-start also defines the hiccup shutdown period with either an overload or overvoltage condition.
27	COMP	Output of the error amplifier and compensation node. Connect a series R-C network from this pin to GND for control loop regulation.
28	FB	Feedback input pin of the error amplifier. Connect a resistor divider from the converter output voltage node, VOUT, to this pin to set the converter output voltage. This pin is also monitored for both output overvoltage and undervoltage conditions (see Fault Handling and Reporting table for more details).
–	PAD	Exposed pad of the package provides both electrical contact to the ground and good thermal contact to the PCB. This pad must be soldered to the PCB for proper operation and should be connected to the ground plane by through-hole vias (see Layout section for further details).

ELECTRICAL CHARACTERISTICS[1] Valid at T_J = –20°C to 125°C and V_{IN} = 12 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General						
Input Voltage Range (Power)	V_{IN}		3	–	16	V
Input Voltage Range (Control)	V_{DD}		4.5	–	16	V
Input V_{IN} Leakage Current	I_{leak}	V_{IN} = 12 V, LX = GND	–	–	5	µA
Input V_{DD} Quiescent Current	I_{DD}	V_{EN} = 5 V, V_{FB} = 1.2 V, no switching	–	–	3	mA
		V_{DD} = 16 V, V_{EN} = 0 V	–	1	10	µA
Feedback Voltage	V_{FB}	7.0 V ≤ V_{IN} ≤ 16 V, V_{FB} = V_{COMP}	0.594	0.600	0.606	V
Maximum Switching Frequency	$f_{sw(max)}$		–	1000	–	kHz
Minimum Switching Frequency	$f_{sw(min)}$		–	200	–	kHz
On-Time Tolerance	Δt_{on}	R_{TON} = 60 kΩ	–10	–	10	%
Maximum On-Time Period	$t_{on(max)}$		2.5	3.5	4.5	µs
Minimum On-Time Period	$t_{on(min)}$		–	50	90	ns
Minimum Off-Time Period	$t_{off(min)}$		–	–	350	ns
High-Side MOSFET On-Resistance	$R_{DS(on)HS}$	I_{DS} = 0.2 A	–	27	–	mΩ
Low-Side MOSFET On-Resistance	$R_{DS(on)LS}$	I_{DS} = 0.2 A	–	12	–	mΩ
Soft Start Source Current[2]	$I_{SS(src)}$	V_{SS} > V_{SSPWM}	–	–30	–	µA
Soft Start Sink Current[2]	$I_{SS(snk)}$		–	5	–	µA
Soft Start Threshold	V_{SSPWM}	V_{SS} rising	–	600	–	mV
Soft Start Ramp Time[1]	t_{SS}	C_{SS} = 10 nF	–	200	–	µs
5 V LDO Regulator						
Output Voltage	V_{REG}	I_{REG} = 0 to 30 mA, V_{IN} > 6 V	4.75	5.00	5.25	V
Amplifier and Power Stage Gain						
Feedback Input Bias Current[2]	I_{FB}	V_{FB} = 0.6 V	–	±50	±250	nA
Error Amplifier Open Loop Voltage Gain[1]	A_{VEA}		–	60	–	dB
Error Amplifier Transconductance[1]	g_{mCOMP}		600	800	1000	µA/V
Error Amplifier Maximum Source/Sink Current[2]	$I_{COMP(max)}$	V_{FB} = V_{FB0} ±0.4 V	–	±52	–	µA
COMP Voltage to Current Gain[1]	g_{mPOWER}		–	4	–	A/V
Enable						
Enable High Threshold	V_{ENHI}		1.8	–	–	V
Enable Low Threshold	V_{ENLO}		–	–	0.8	V
Enable Hysteresis	V_{ENHYS}		150	250	–	mV
Enable Current[2]	I_{EN}	V_{EN} = 3.3 V	–	50	–	µA

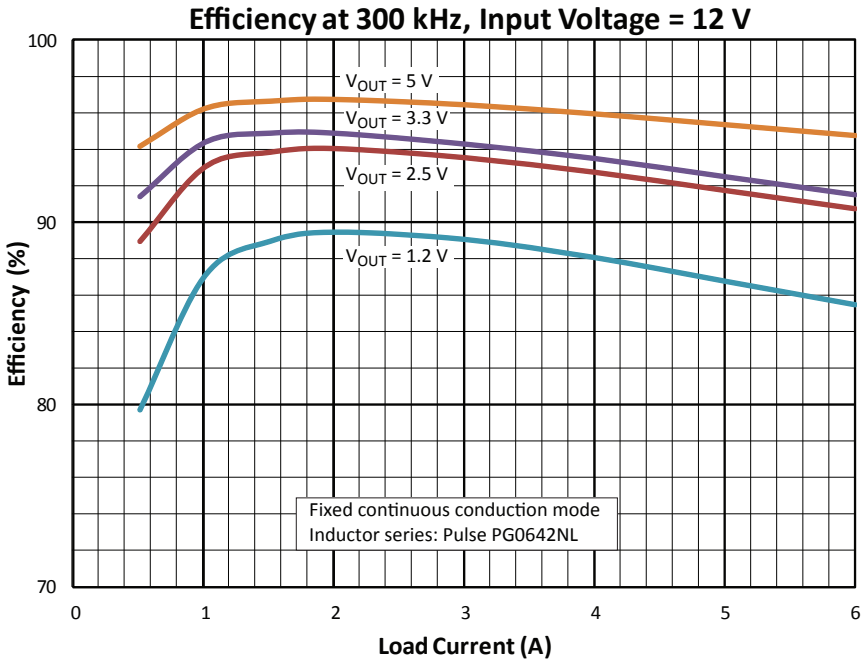
Continued on the next page…

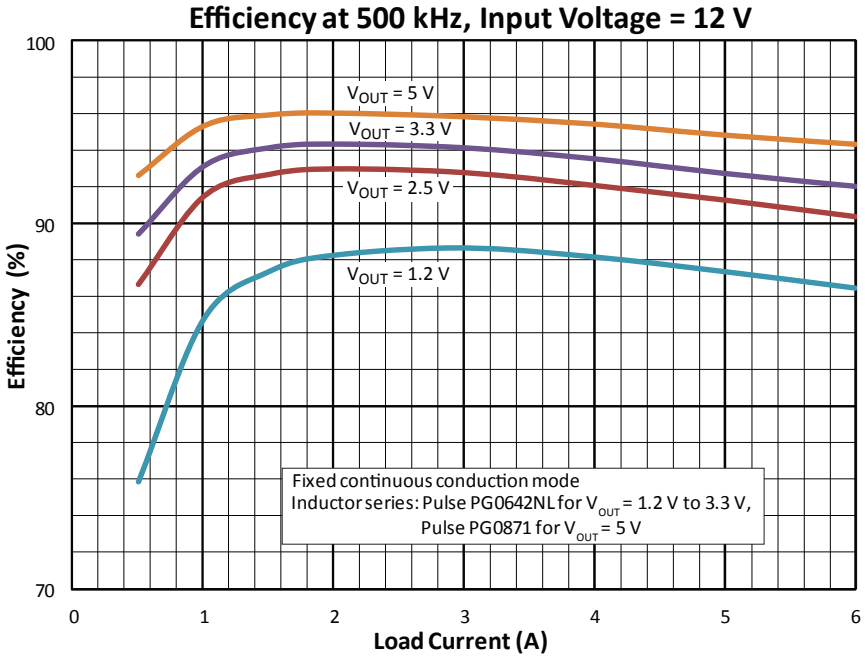
ELECTRICAL CHARACTERISTICS[1] (continued) Valid at T_J = –20°C to 125°C and V_{IN} = 12 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power OK						
Power Good Threshold (Rising)	$V_{POK(HI)}$	Feedback voltage relative to reference voltage, POK = high	92	95	98	%
Power Good Threshold (Falling)	$V_{POK(LO)}$	Feedback voltage relative to reference voltage, POK = high	107	110	113	%
Power Good Hysteresis	V_{POKHYS}	POK= low	–	5	–	%
POK Rising Delay	t_{dPOK}		–	90	–	µs
POK Output Voltage	V_{POK}	I_{POK} = 10 mA, POK asserted	–	–	500	mV
POK Leakage Current	I_{POK}	V_{POK} = 5.5 V, POK not asserted	–	–	1	µA
Fault Reporting						
$\overline{\text{FAULT}}$ Overtemperature	T_{OT}	Temperature rising	–	140	–	°C
$\overline{\text{FAULT}}$ Overtemperature Hysteresis	T_{OTHYS}	Fault release = T_{OT} – T_{OTHYS}	–	20	–	°C
$\overline{\text{FAULT}}$ Output Voltage	V_{FAULT}	I_{FAULT} = 10 mA, fault asserted	–	–	500	mV
$\overline{\text{FAULT}}$ Leakage	I_{FAULT}	V_{FAULT} = 5.5 V, fault not asserted	–	–	1	µA
Protection						
Undervoltage Threshold (Falling)	V_{UVFB}	Feedback voltage relative to reference voltage	–	75	–	%
Undervoltage Hysteresis	V_{UVHYS}		–	5	–	%
Overvoltage Threshold (Rising)	V_{OVFB}	Feedback voltage relative to reference voltage	115	120	125	%
Overvoltage Hysteresis	V_{OVHYS}		–	5	–	%
Valley Current Limit Voltage Range	I_{LIMVR}		1.0	–	2.75	V
Valley Current Limit	I_{LIM}	ILIM resistor = 169 kΩ	3.0	4.0	5.0	A
		ILIM resistor = 249 kΩ	6.0	8.0	10.0	A
Hiccup On Period[1]	t_{HICOC}	Either valley current limit or overvoltage condition reached	–	50	–	µs
Hiccup Shutdown Period[1]	t_{HICSD}	C_{SS} = 10 nF, first shutdown event	–	10	–	ms
		C_{SS} = 10 nF, second and subsequent shutdown events	-	1.2	-	ms
Pulse-by-Pulse Negative Valley Current Limit	I_{NLIM}	FCCM selected	–2.4	–1.9	–1.4	A
FB Overvoltage Duration	t_{UVFB}	High-side MOSFET off, low-side MOSFET on	–	50	–	µs
High-Side MOSFET Protection Current	I_{HIPRO}	LX node short-circuited to GND	–	25	–	A
High-Side MOSFET Protection Voltage	V_{HIPRO}	LX node short-circuited to GND	450	650	850	mV
VDD Undervoltage Lockout (Rising)	V_{UVLO}		–	4.2	4.45	V
VDD Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$		–	300	–	mV
Thermal Shutdown Threshold	T_{SD}	Temperature rising	–	165	–	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	Recovery = T_{SD} – T_{SDHYS}	–	15	–	°C

[1]Specifications throughout the junction temperature, T_J, range of –20ºC to 125ºC are assured by design and characterization unless otherwise noted.
[2]Positive current is into the node or pin, negative current is out of the node or pin.

Characteristic Performance





Functional Description

Basic Operation

At the beginning of a switching cycle, the high-side switch is turned on for a duration determined by the current flowing into TON. The magnitude of current is determined by the value of the input voltage and the value of the on-time resistor (RTON, R1 in the Typical Applications section circuit diagrams).

During the on-time period, the current builds up through the inductor at a rate determined by the voltage developed across it and the inductance value. When the on-time period elapses, the output of an RS latch resets, turning off the high-side switch. After a small dead-time delay, the low-side switch is turned on.

The current through the inductor decays at a rate determined by the output voltage and the inductance value. The current is sensed through the low-side switch and is compared to the *current demand signal*. The current demand signal is generated by comparing the output voltage (stepped down to the FB pin) with an accurate reference voltage.

When the current through the low-side switch drops to the current demand level, the low-side switch is turned off. After a further dead-time delay, the high-side switch is turned on again, and the process is repeated.

Output Voltage Selection

The output voltage (V_{OUT}) of the converter is set by selecting the appropriate feedback resistors using the following formula:

$$V_{OUT} = V_{FB} \times \left(\frac{R_6}{R_7} + 1 \right) + I_{FB} \times \frac{R_6 \times R_7}{R_6 + R_7} \qquad (1)$$

where:

V_{FB} is the reference voltage,

R6 and R7 are as shown in the Typical Applications section circuit diagrams, and

I_{FB} is the reference bias current.

It is important to consider the tolerance of the feedback resistors, because they directly affect the overall setpoint accuracy of the output voltage.

It is also important to consider the actual resistor values selected and consider the trade-offs. High value resistors will minimize the shunt current flowing through the feedback network, enhancing efficiency. However, the offset error produced by the reference bias current will increase, affecting the regulation. In addition, high value resistors are more prone to noise pick-up effects which may affect performance. As some kind of compromise, it is recommended that R7 be in the region of 10 kΩ.

Switch On-Time and Switching Frequency

The switching frequency of the converter is selected by choosing the appropriate on-time. The on-time can be estimated to a first order by using the following formula:

$$t_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \qquad (2)$$

where:

V_{OUT} is the output voltage,

f_{SW} is the switching frequency, and

V_{IN} is the nominal input voltage.

To factor-in the effects of resistive voltage drops in the converter circuit, the following formula can be used to produce a more accurate estimate of what the on-time has to be for a required switching frequency:

$$t_{on} = \frac{V_{OUT} + (R_{DS(on)LS} + DCR_L) \times I_{OUT}}{V_{IN} + (R_{DS(on)LS} - R_{DS(on)HS}) \times I_{OUT}} \times \frac{1}{f_{SW}} \qquad (3)$$

where:

$R_{DS(on)LS}$ is the low-side MOSFET on-resistance,

$R_{DS(on)HS}$ is the high-side MOSFET resistance, and

DCR_L is the inductive resistance.

The switching frequency will vary slightly as the resistive voltage drops in the circuit change, either due to temperature effects or to input voltage variations.

Note that when selecting the switching frequency, care should be taken to ensure the converter does not operate near either the minimum on-time (50 ns) or the minimum off-time (250 ns). Minimum on-times will typically occur in combinations of maximum input voltage, minimum output voltage with minimum load, and maximum switching frequency. Minimum off-times will typically occur in combinations of minimum input voltage, maximum output voltage with maximum load, and maximum switching frequency.

The t_{on} from either of the above formulae can be used to determine the TON resistor value, R_{TON} (R1 in Typical Applications section circuit drawings):

$$R_{TON} = (V_{IN} - 0.67) \times \frac{t_{on} - 8 \times 10^{-9}}{25 \times 10^{-12}} - 500 \quad (4)$$

Table 1 provides preferred resistor values for a given output voltage at target switching frequencies of 500 kHz, 700 kHz, and 1 MHz:

Valley Current Limit

The Valley Current Limit (I_{LIM}) threshold can be programmed to any level between 9 and 3 A by selecting an appropriate resistor (R_{LIM}) connected between the ILIM pin and ground. The resistor can be selected either by using the following formula, or by using the graph in figure 1 for the typical Valley Current Limit:

$$R_{LIM} = (21.8 \times I_{LIM}) + 79 \quad (5)$$

where R_{LIM} is in kΩ.

Inductor Selection

The main factor in selecting the inductance value is the ripple current. The ripple current affects the output voltage ripple and current limit. A reasonable figure of merit for the ripple current (I_{ripp}) is 25% of the maximum load. So for a maximum load of 6 A, the peak-to-peak ripple current should be 1.5 A.

Table 1: Recommended RTON Resistor Values

Switching Frequency, f_{SW}					
500 kHz		700 kHz		1 MHz	
V_{OUT} (V)	R_{TON} (kΩ)	V_{OUT} (V)	R_{TON} (kΩ)	V_{OUT} (V)	R_{TON} (kΩ)
5.0	374	5.0	267	5.0	182
3.3	243	3.3	174	3.3	121
2.5	187	2.5	133	2.5	90.9
1.8	137	1.8	95.9	1.8	64.9
1.5	113	1.5	80.6	1.5	54.9
1.2	90.9	1.2	63.4	1.2	43.2
1.0	76.8	1.0	52.3	1.0	35.7
0.8	60.4	0.8	42.2	0.8	28.7
0.6	44.2	0.6	30.9	0.6	23.2

The maximum peak-to-peak ripple current occurs at the maximum input voltage. To a reasonable approximation, the minimum duty cycle can be found:

$$D(\text{min}) = \frac{V_{OUT}}{V_{IN}(\text{max})} \quad (6)$$

The required (minimum) inductance can be found:

$$L(\text{min}) = \frac{V_{IN} - V_{OUT}}{I_{ripp}} \times D(\text{min}) \times \frac{1}{f_{SW}} \quad (7)$$

Note that the inductor manufacturer tolerances on the inductance value should be taken into account. This can be as high as ±30%.

It is recommended that gapped ferrite solutions be used as opposed to powdered iron solutions. This is because powdered iron cores exhibit relatively high core losses, especially at higher switching frequencies. Higher core losses do have a detrimental impact on the long term reliability of the component.

Inductors are typically specified at two current levels:

- ***Saturation Current (I_{sat})*** The worst case maximum peak current should not exceed the saturation current and indeed some margin should be allowed. The maximum peak current in an inductor occurs during an overload condition where the circuit operates in current limit. The typical valley current limit (I_{LIM}) is 8 A, with R4 = 249 kΩ. The peak current through the inductor is effectively the valley current limit plus the ripple current:

$$I_{sat} > I_{LIM} + I_{ripp} \quad (8)$$

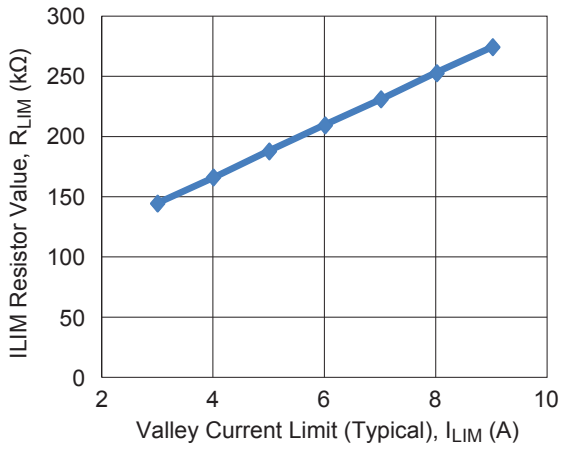


Figure 1: Valley Current Limit determination: value of external resistor on ILIM pin versus valley current limit

- ***Rms Current (I_{rms})*** It is important to understand how the rms current level is specified in terms of ambient temperature. Some manufacturers quote an ambient whilst others quote a temperature that includes a self-temperature rise. For example, if an inductor is rated for 85°C and includes a self-temperature rise of 25°C at maximum load, then the inductor cannot be safely operated beyond an ambient temperature of 60°C at full load.

  The rms current through the inductor should not exceed the rating for the inductor, taking into account the maximum ambient temperature. The maximum rms current is effectively the valley current limit (I_{LIM}) plus half of the ripple current:

$$I_{rms}(max) > I_{LIM} + I_{ripp} / 2 \quad (9)$$

A final consideration in the selection of the inductor is the series resistance (DCR). A lower DCR will reduce the power loss and enhance power efficiency. The trade-off in using an inductor with a relatively low DCR is the physical size is typically larger.

Recommended inductor: PIMC065T-*XX*MN-11 (XX is value) series manufactured by Cyntec or the PG0871 series manufactured by Pulse Electronics. Table 2 provides preferred inductor values for a given output voltage, 2 A output at target switching frequencies of 500 kHz, 700 kHz, and 1 MHz.

Output Capacitor Selection

The output capacitor has two main functions: influence the control loop response (see the Control Loop section), and determine the magnitude of the output voltage ripple.

Table 2: Recommended Inductor Values

Switching Frequency, f_{SW}					
500 kHz		700 kHz		1 MHz	
V_{OUT} (V)	L (µH)	V_{OUT} (V)	L (µH)	V_{OUT} (V)	L (µH)
5.0	3.7	5.0	2.6	5.0	2.2
3.3	3.7	3.3	2.2	3.3	1.7
2.5	2.6	2.5	1.7	2.5	1.2
1.8	2.2	1.8	1.7	1.8	1
1.5	1.7	1.5	1.2	1.5	1
1.2	1.2	1.2	1	1.2	0.8
1.0	1.2	1.0	1	1.0	0.54
0.8	1	0.8	0.8	0.8	0.47
0.6	0.8	0.6	0.47	0.6	0.47

The output voltage ripple can be approximated to:

$$V_{ripp} = \frac{I_{ripp}}{8 \times f_{SW} \times C_{OUT}} \quad (10)$$

where:

I_{ripp} is the peak-to-peak current in the inductor (see the Inductor Selection section), and

C_{OUT} is the output capacitance.

It is recommended that ceramic capacitors be used, taking into account: size, cost, reliability, and performance. It is imperative that ceramic type X5R or X7R are used. On no account should Y5V, Y5U, Z5U, or similar be used, because the capacitance tolerance and the temperature stability is very poor.

There is generally no need to consider the effects of heating caused by the ripple current flowing into the output capacitor. This is because the equivalent series resistance (ESR) of ceramic capacitors is extremely low.

When using ceramic capacitors, it is important to consider the effects of capacitance reduction due to the E-field. To avoid this voltage bias effect, it is recommended that the capacitor rated voltage be at least twice that of the actual output voltage. So for example, with a 5 V output, the capacitor should be rated to 10 V.

For the majority of applications, a capacitance of 200 µF is recommended to ensure good transient response.

Input Capacitor Selection

The function of the input capacitor is to provide a low impedance shunt path for the current drawn by the A8672 when the high-side switch is on. This minimizes the amount of ripple current reflected back into the source supply. This reduces the potential for higher conducted electromagnetic interference (EMI).

In a correctly designed system, with a quality capacitor positioned adjacent to the VIN pin and the PGND pin, this capacitor should supply the high-side switch current minus the average input current. During the high-side switch off-cycle, the capacitor is charged by the average input current.

The effective rms current that flows in the input filter capacitor is:

$$I_{rms} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \times \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2} \quad (11)$$

The amount of ripple voltage (V_{ripp}) that appears across the input terminals (VIN with respect to GND) is determined by the amount of charge removed from the input capacitor during the high-side switch conduction time. If a capacitor technology such as an electrolytic is used, then the effects of the ESR should also be taken into account.

The amount of input capacitance (C_{IN}) required for a given ripple voltage can be found:

$$C_{IN} = \frac{I_{rms} \times t_{on}}{V_{ripp}} \quad (12)$$

where:

t_{on} is the on-time of the high-side switch (see the Switch On-Time and Switching Frequency section; note that maximum ton occurs at minimum input voltage), and

CIN is the input filter capacitance.

As mentioned in the Output Capacitor Selection section, the effects of voltage biasing should be taken into account when choosing the capacitor voltage rating. If ceramic capacitors are being used, then there is generally no need to consider the effects of ESR heating.

Soft-Start, Output Overloads and Overvoltages

The soft-start routine controls the rate of rise of the reference voltage, which in turn controls the FB pin, and thereby the output voltage (V_{OUT})(see figure 2). This function minimizes the amount of inrush current drawn from the input voltage (V_{IN}) and potential voltage overshoot on the output rail (V_{OUT}).

A soft-start routine is initiated when the enable pin (EN) is high, no overvoltage exists on the output, the thermal protection circuitry is not activated, and V_{IN} is above the undervoltage threshold. Immediately after EN goes high, the soft-start capacitor is charged via an internal 10 µA source and PWM switching action occurs.

The Soft-Start Ramp Time, t_{ss}, can be found from the following formula:

$$t_{SS} = \frac{C_{SS} \times 0.6}{30 \times 10^{-6}} \quad (13)$$

where C_{SS} is C11 in the Typical Application circuit diagrams.

During the *Soft-Start Ramp Time* (see A in figure 2), the reference is ramped from 0 up to 0.6 V, and the output voltage (V_{OUT}) tracks the reference voltage. The POK flag is held low until the output voltage reaches 95% (typical) of the target voltage and a delay of 90 µs (typical) occurs.

When an output overcurrent event occurs, the regulator immediately limits the valley current at a constant level on a pulse-by pulse basis. The output voltage will tend to fold back, depending on how low the output impedance is. When the output voltage drops below 90% (typical) of the target voltage, the POK flag goes low. If the overload occurs for shorter than the *Hiccup On Period* (<50 µs; B in figure 2), the output will automatically recover to the target level. If the overload occurs for longer than the Hiccup On Period (>50 µs; C in figure 2), the regulator will shut down, the soft-start capacitor will be discharged, and (assuming no other fault conditions exist and the enable pin is still high) the regulator will be delayed by the *Hiccup Shutdown Period* (D in figure 2).

The Hiccup Shutdown Period ensures that prolonged overload conditions do not cause excessive junction temperatures to occur. After the Hiccup Shutdown Period has elapsed, the output voltage is again brought up, controlled by the soft-start function. However, if the overload condition still exists and still remains after the Soft-Start Ramp Time has elapsed, the regulator will shut down and the process will repeat until the fault is removed.

The Hiccup Shutdown Period is determined by the discharge of the soft-start capacitor to zero voltage. During normal operation, the soft-start capacitor C_{SS} is charged to 5 V. In the event of an overload where the Hiccup On Period exceeds 50 µs, the length of the first Hiccup Shutdown Period event can be found:

$$t_{SS(first)} = (C_{SS} \times 5) / 5 \times 10^{-6} \quad (14)$$

So for example, with a C_{SS} of 10 nF, the first Hiccup Shutdown Period event is 10 ms.

Assuming the overload is still applied, the length of the second and subsequent Hiccup Shutdown Periods depends on the load resistance applied and how far the soft-start capacitor is charged before switching action occurs. The Hiccup Shutdown Period is approximately ten times the length of the switching period.

The overvoltage protection operates in a similar way to the overcurrent protection using the same Hiccup Circuitry.

Although the A8672 is optimized for ceramic output capacitors, large value electrolytic capacitors can be used where either special hold-up, or power sequencing is required. Note the guidelines for selecting large value capacitors in the Control Loop section.

When selecting larger-value output capacitors, it is important that the soft-start period is appropriately scaled to take into account the charging of these capacitors. For example, if the soft-start is optimized for a 200 µF ceramic output capacitor and a 2000 µF capacitor is added to the output, there is every possibility that the converter will remain in an overload condition after the soft-start and the Hiccup On Period have elapsed. This mode of operation could prevent the output ever reaching the target output voltage.

To demonstrate the above, consider the following example: a regulator programmed for a 5 V output, 200 µF output capacitor, and a soft-start time-off of 1 ms.

Assume there is no load current draw until 5 V is reached. At start-up, the regulator has to charge the output capacitor. From $C \times V = I \times t$, the charging current into the capacitor is:

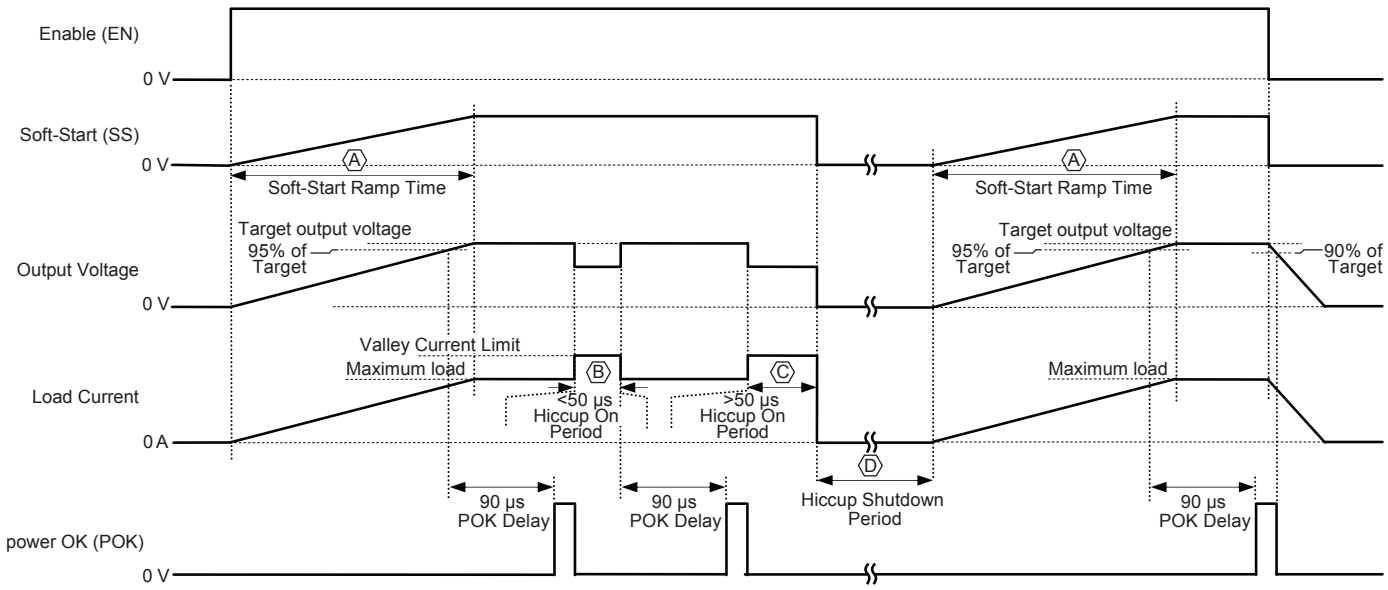


Figure 2: Operation of the Soft-Start Function

$$I = 200\ \mu F \times 5 / 1\ ms = 1\ A$$

Now if a 2000 µF capacitor is added to the output, the capacitor would require a charge current of:

$$I = 2000\ \mu F \times 5 / 1\ ms = 10\ A$$

In this condition, the A8672 would run into the pulse-by-pulse current limit, limiting the average charge current to 8.75 A (typ). An average current of 8.75 A, assumes a valley current limit of 8 A and a half ripple current of 0.75 A. This means that after the soft-start delay of 1 ms, the output voltage would only be charged to:

$$V = 8.75\ A \times 1\ ms / 2000\ \mu F = 4.375\ V$$

After the soft-start period is completed, the output capacitor would be charged for a short duration, defined by the Hiccup On Period. Then the converter would shut down and, after the Hiccup Shutdown Period had elapsed, would enter the start-up process again. This mode is highly undesirable and a more appropriate soft-start capacitor should be selected.

The effects of adding an output capacitor with too-large value would be a condition similar to starting-up into a short-circuit across the output; where the regulator enters a hiccup mode of operation.

If the output of the A8672 is pre-biased at start-up, the switcher will remain in a high impedance state until the soft-start has reached the feedback voltage (V_{FB}) amplitude. This avoids the output voltage being discharged. After the soft-start threshold exceeds the FB pin voltage, PWM switching action occurs and the output voltage is brought up under the control of the soft-start circuit (see Figure 3).

Note that when the regulator is turned off, it enters a high impedance mode (all switches off) and if the output voltage is discharged it is done so by the load (at A in figure 3). If the load does not discharge the output, the output voltage remains in a pre-biased condition.

Fault Handling and Reporting

Table 3 describes the action taken for particular faults including the status of the $\overline{\text{FAULT}}$ and POK flags.

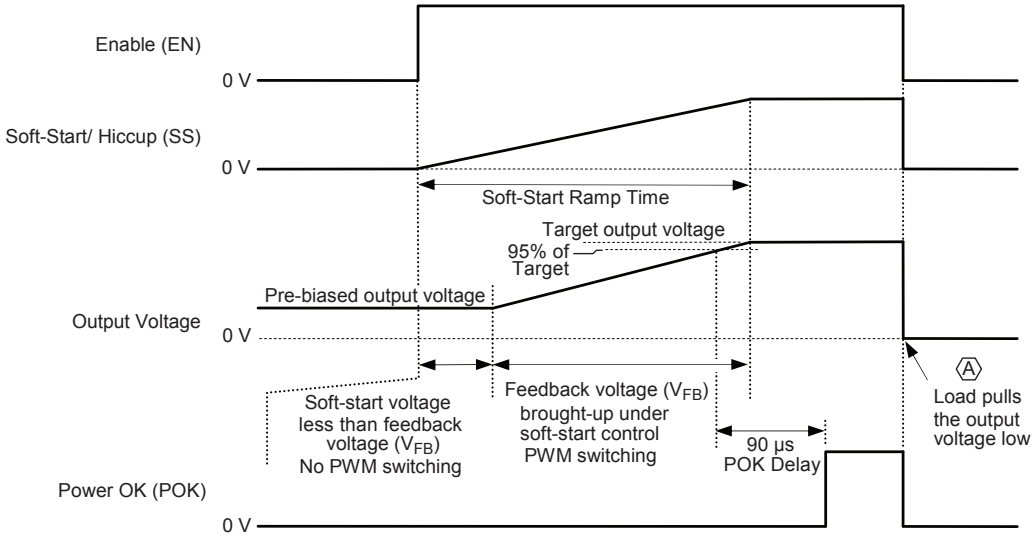


Figure 3: Operation of the Soft-Start Function with Pre-Biasing

Table 3: Fault Handling and Reporting

A8672 Condition	Comments	POK Flag	$\overline{\text{FAULT}}$ Flag	Action After Fault
95% (typ) < V_{FB} < 110% (typ)	Normal operation.	High	High	–
V_{FB} < 95% (typ)	During start-up, the feedback voltage (V_{FB}) is increased under control of the soft-start circuit.	Low	High	–
V_{FB} < 90% (typ)	After start-up, if an overload occurs for less than the Hiccup On Period (50 µs), the regulator maintains switching operation.	Low	High	Auto-recovery
	After start-up, if an overload occurs for greater than the Hiccup On Period (50 µs), the regulator turns off for Hiccup Shutdown Period and then initiates a soft-start cycle.	Low	High	Auto-restart under control of soft-start
V_{FB} > 120% (typ)	High-side MOSFET turns off and low-side MOSFET switching is maintained. If the feedback voltage (V_{FB}) drops to <75% of target V_{FB} (undervoltage condition) within 50 µs (Hiccup On Period), a soft-start is performed.	Low	High	Soft-start is performed
	If the feedback voltage (V_{FB}) does not drop to <75% of target V_{FB} within 50 µs (Hiccup On Period), the low-side MOSFET is turned off and the high-side MOSFET remains off for the duration of the Hiccup Shutdown Period.	Low	High	After the Hiccup Shutdown Period, a soft start is performed; then if the fault is not present, normal operation occurs, otherwise the cycle is repeated
V_{DD} < 4.0 V (typ)	Regulator immediately turns off.	Low	High	Auto-restart under the control of the soft-start circuit, when V_{IN} > 4.2 V (typ)
T_J > 140°C (typ)	Regulator keeps operating until TSD threshold is reached (T_J > 165°C (typ)), and then $\overline{\text{FAULT}}$ goes high.	High	Low	–
T_J > 165°C (typ)	Regulator immediately turns off.	Low	Low	Auto-restart under the control of the soft-start circuit, when T_J < 145°C
LX pin shorted to GND	The voltage across the series switch is monitored. If the voltage exceeds 500 mV (typ), the regulator latches off.	Low	Low	Restart by cycling either the Enable pin, EN, or the input voltage pin, VIN, low then high; restarts under the control of the soft-start circuit
t_{on} > 3.5 µs (typ)	Regulator immediately turns off.	Low	Low	Restart by cycling either the Enable pin, EN, or the input voltage pin, VIN, low then high; restarts under the control of the soft-start circuit
Any of the internal bias (BIAS), VREG regulator, or bootstrap supply voltages are below the respective undervoltage threshold	Regulator immediately turns off.	Low	High	Auto-restart under the control of the soft-start circuit when the low voltage rises above the respective UVLO threshold: BIAS, VREG, or BOOT

Control Loop

To a first order, the small-signal loop can be modeled as shown in Figure 4. The control loop can be broken into two sections: power stage and error amplifier.

Power Stage

The power stage includes the output filter capacitor (C_{OUT}), the equivalent load (R_{LOAD}), and: the inner current loop, PWM modulator, and power inductor, which together are modeled as a transconductance amplifier with a gain of 4 A/V. The signal V_c, supplied to the power stage, is effectively the load current demand signal. This signal effectively controls the valley current through the inductor; the higher the load the larger the V_c signal. To simplify matters, we will assume this signal controls the average current through the inductor as opposed to the valley current.

The effective DC gain of the power stage, without the output capacitor and load resistor, is 4 A/V, where the signal V_c is limited to the range 0.36 to 2.75 V. The DC current is converted into V_{OUT} as the current flows into the load resistor. The overall DC gain of the power stage is given as V_{OUT}/V_c (see figure 5). At full load, the V_c signal would be 6/4 = 1.5 V.

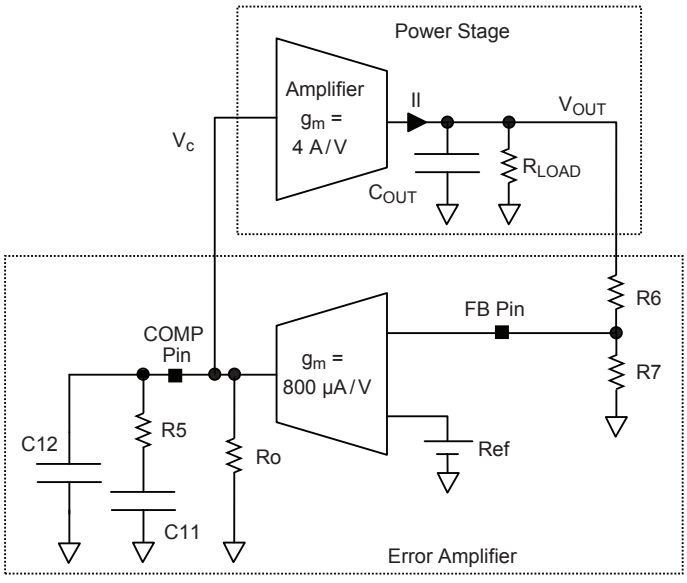


Figure 4: 1st Order Model of the Small-Signal Control Loop (see Typical Applications section circuit diagrams for component references)

From a small-signal point of view, the power inductor behaves like a current source; the inductor can be ignored as far as the bandwidth of the loop is concerned. The output capacitor integrates the ripple current through the inductor, effectively forming a single pole with the output load.

The power stage pole can be found:

$$f_{p(PS)} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} \quad (15)$$

It can be seen that as the load changes, the position of the power pole changes in the frequency domain. This may seem like an issue in terms of where to optimize the loop, however, the change in load also changes the gain in the power stage, thus compensating for this effect. Figure 5 illustrates how the loop response of the power stage changes with a varying load. The position of f_{p1} and G1 is one solution, f_{p2} and G2 is another solution, and so forth.

As the value of R_{LOAD} increases (reducing load), the power pole moves down in frequency and the DC gain increases. Generally speaking this is not a problem, because even if the pole approaches the low frequency pole produced by the error amplifier, there is still plenty of gain in the system. In this case, while the phase margin may be greatly reduced, even to a value approaching 0°, because there is sufficient DC gain in the loop it can be shown from Nyquist theory that the system is conditionally stable. The phase margin must be considered only at the 0 dB crossover frequency.

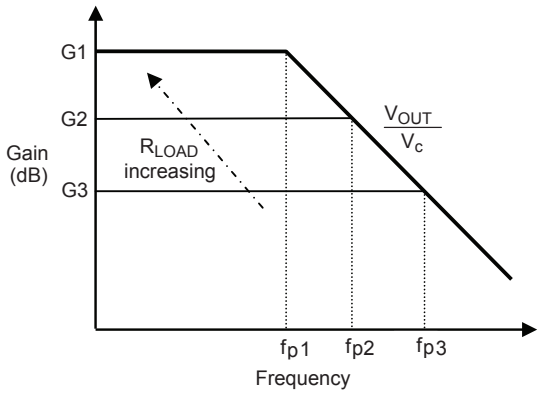


Figure 5: Power Stage DC Gain Characteristic

It is recommended that X5R/ X7R ceramic capacitors be used, however, large-value capacitors such as electrolytic types can be used. Care should be taken when selecting the value of an electrolytic capacitor. As this capacitance is increased, the power pole is pushed to such a low frequency that the gain can fall off sufficiently to cause a loop instability.

If using an electrolytic capacitor, consideration should also be given to the equivalent series resistance (ESR) value, because this introduces a zero with the capacitance itself. It is important to use a low-ESR type capacitor. It should be noted that capacitor manufacturers usually quote an ESR which is a maximum at a particular frequency (such as 100 kHz) and temperature (20°C). The ESR does vary with frequency and temperature, plus there are tolerance effects as well. If the zero produced by the ESR of the output capacitor features in the control loop, it is strongly recommended that a large tolerance be allowed. If necessary, the high frequency pole in the error amplifier can be used to negate the effects of this pole (see the Error Amplifier section).

Error Amplifier

The error amplifier is a transconductance amplifier. The DC gain of the amplifier is 60 dB (1000) and, with a g_m value of 800 µA/V, the effective output impedance of the amplifier can be modeled as:

$$R_O = \frac{1000}{800 \times 10^{-6}} = 1.25\ \text{M}\Omega \quad (16)$$

The transconductance amplifier has a high DC gain to ensure good regulation. The gain is rolled off with a single pole positioned at a low frequency. A zero is positioned at higher frequencies to cancel the effects of the main power stage pole. A second pole can be introduced which should have minimal effect on the loop response, but is useful for reducing the effects of switching noise.

The low frequency pole occurs at:

$$f_{p1(EA)} = \frac{1}{2 \times \pi \times R_O \times C_{11}} \quad (17)$$

The zero occurs at:

$$f_{z(EA)} = \frac{1}{2 \times \pi \times R_5 \times C_{11}} \quad (18)$$

The high frequency pole occurs at:

$$f_{p2(EA)} = \frac{1}{2 \times \pi \times R_5 \times C_{12}} \quad (19)$$

The potential divider formed by R6 and R7 in figure 4 effectively introduces a DC offset to the loop. This can be found from: V_{FB} / V_{OUT}.

Control Loop Design Approach

There are many different approaches to designing the feedback loop. The optimum solution is to select a target phase margin and bandwidth for optimum transient response. This typically requires either simulation software or detailed Bode plot analysis to generate a solution.

The particular approach described here derives a solution through a series of basic calculations. This approach aims for a simple –20 dB/decade roll off, from the low frequency error amplifier pole ($f_{p1(EA)}$) to the 0 dB crossover point (f_{cross}). The 0 dB crossover point is aimed at a thirteenth of the switching frequency (f_{SW}). This factor is chosen as a compromise between good bandwidth and minimizing the phase lag introduced by the second power pole, which occurs between $^1/_3$ and $^1/_6$ of the switching frequency. In theory, this should introduce a phase margin of 90°, however, in practice it will be slightly less, due to the effects of the second power pole. The introduction of this second pole reduces the phase margin below 90°.

It is recommended that the error amplifier high frequency pole should be positioned one octave below the switching frequency. This provides some attenuation of the switching ripple whilst having minimum impact on the closed loop response.

To achieve a –20 dB/decade roll off, the error amplifier zero is positioned to coincide with the power pole at maximum load.

Figure 6 illustrates the power stage gain, the error amplifier gain, and then the combined overall loop response (power stage and error amplifier).

Design Example

Assuming: output voltage (V_{OUT}) = 1.2 V, maximum load (I_{OUT}) = 6 A, switching frequency (f_{SW}) = 500 kHz, and output capacitance (C_{OUT}) = 200 µF. Analyze the response at full load.

1. Crossover frequency:

$$f_{cross} = \frac{500 \times 10^3}{13} = 38.5 \text{ kHz} \quad (20)$$

2. Overall DC gain (refer to figure 6):

$$\text{DC gain (PS)} = 20 \text{ Log}_{10}\left(\frac{V_{OUT}}{V_c}\right) \quad (21)$$

$$\text{DC gain (EA)} = 60 \text{ dB} + 20 \text{ Log}_{10}\left(\frac{V_{FB}}{V_{OUT}}\right) \quad (22)$$

$$\begin{aligned}\text{DC gain (All)} &= \text{DC gain (PS)} + \text{DC gain (EA)} \quad (23)\\ &= 20 \text{ Log}_{10}\left(\frac{V_{OUT}}{V_c}\right) + 60 \text{ dB} + 20 \text{ Log}_{10}\left(\frac{V_{FB}}{V_{OUT}}\right)\\ &= 20 \text{ Log}_{10}\left(\frac{1.2}{1.5}\right) + 60 \text{ dB} + 20 \text{ Log}_{10}\left(\frac{0.6}{1.2}\right)\\ &= 52 \text{ dB}\end{aligned}$$

Note: With a power stage gain of 4 A/V and a load of 6 A, the corresponding $V_c = 6/4 = 1.5$ V.

3. With a 38.5 kHz crossover and a 20 dB/decade increase in gain, at what frequency does the gain reach 52 dB? The –20 dB/decade roll off can be described as a single pole with this transfer function for magnitude (G):

$$G = \frac{1}{2 \times \pi \times f \times RC} \quad (24)$$

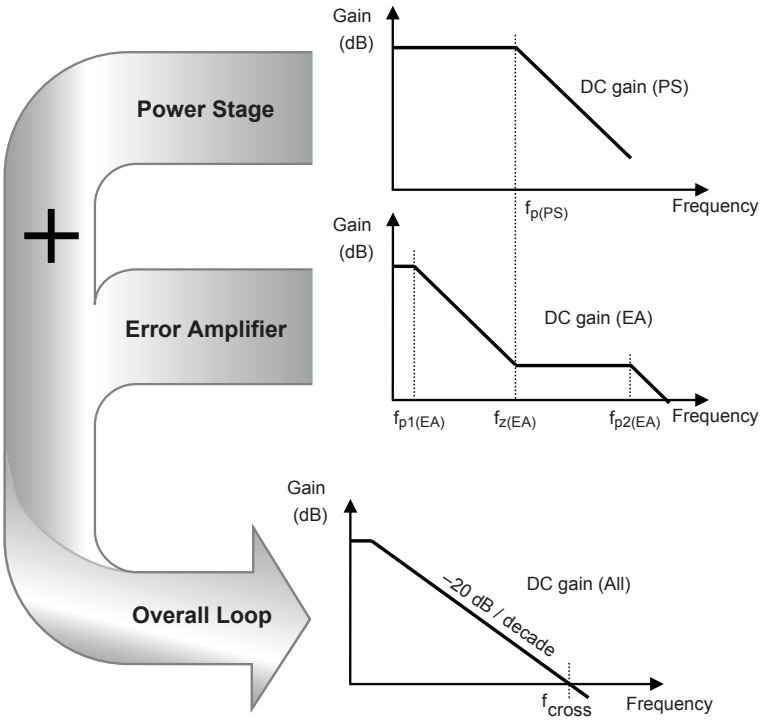


Figure 6: Power Stage, Error Amplifier, and Combined Overall Control Loop Response

3a. We know that at 38.5 kHz the gain is 0 dB (1). Therefore the constant RC can be worked out:

$$RC = \frac{1}{2 \times \pi \times 38.5 \times 10^3 \times 1} = 4.13 \times 10^{-6} \quad (25)$$

3b. A magnitude of 52 dB requires a gain of 398. The error amplifier pole ($f_{p1(EA)}$), the frequency at which 398 is reached, is:

$$f_{p1(EA)} = \frac{1}{2 \times \pi \times 4.13 \times 10^{-6} \times 398} = 96.8 \text{ Hz} \quad (26)$$

So the overall loop response objective is shown in figure 7.

4. Select the RC components.

4a. The error amplifier pole ($f_{p1(EA)}$) occurs at 96.8 Hz. Therefore, C11 can be found:

$$C_{11} = \frac{1}{2 \times \pi \times R_O \times f_{p1(EA)}} = \frac{1}{2 \times \pi \times 1.25 \times 10^6 \times 96.8} = 1.3 \text{ nF} \quad (27)$$

The nearest preferred value is 1.5 nF.

4b. The power pole ($f_{p(PS)}$) can be found, because the output capacitor (C_{OUT}) and maximum load (R_{LOAD}) are known:

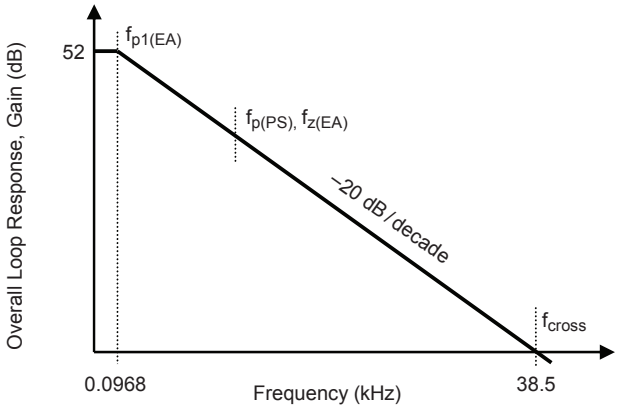


Figure 7: Design Example Objective: overall control loop response (power stage and error amplifier)

$$f_{p(PS)} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} = \frac{1}{2 \times \pi \times 0.2 \times 200 \times 10^{-6}} = 3979 \text{ Hz} \quad (28)$$

4c. The error amplifier zero ($f_{z(EA)}$) also occurs at 3.979 kHz to cancel the effects of the power pole. Therefore, as C11 is known, R5 can be found:

$$R_5 = \frac{1}{2 \times \pi \times C_{11} \times f_{p(PS)}} = \frac{1}{2 \times \pi \times 1.5 \times 10^{-9} \times 3979} = 26.67 \text{ k}\Omega \quad (29)$$

Nearest preferred value = 27 kΩ.

4d. The error amplifier high frequency pole ($f_{p2(EA)}$) is set an octave below the switching frequency. Therefore, C12 can be found:

$$C_{12} = \frac{1}{2 \times \pi \times R_5 \times (f_{SW}/2)} = \frac{1}{2 \times \pi \times 27 \times 10^3 \times (500 \times 10^3 / 2)} = 24 \text{ pF} \quad (30)$$

Nearest preferred value = 22 pF.

4e. Using the above compensation component selection technique, table 4 provides preferred component values for a given output voltage, 6 A output, at target switching frequencies of 500 kHz, 700 kHz, and 1 MHz.

Table 4: Recommended R5 and C11 Values

Switching Frequency, f_{SW}								
500 kHz			700 kHz			1 MHz		
V_{OUT} (V)	R4 (kΩ)	C7 (nF)	V_{OUT} (V)	R4 (kΩ)	C7 (nF)	V_{OUT} (V)	R4 (kΩ)	C7 (nF)
5.0	110	1.5	5.0	162	1.0	5.0	240	0.68
3.3	75	1.5	3.3	110	1.0	3.3	160	0.68
2.5	56	1.5	2.5	82	1.0	2.5	120	0.68
1.8	39	1.5	1.8	62	1.0	1.8	91	0.68
1.5	33	1.5	1.5	51	1.0	1.5	75	0.68
1.2	27	1.5	1.2	39	1.0	1.2	59	0.68
1.0	22	1.5	1.0	33	1.0	1.0	51	0.68
0.8	18	1.5	0.8	27	1.0	0.8	39	0.68
0.6	13	1.5	0.6	20	1.0	0.6	20	0.68

Thermal Considerations

For a given set of conditions, the junction temperature of the A8672 can be estimated by carrying out a few calculations. This is important to ensure an adequate safety margin with respect to the maximum junction temperature (150°C) to enhance reliability. This exercise also helps to understand the overall efficiency of the regulator.

The general approach is to work out what thermal impedance ($R_{\theta J\text{-}A}$) is required to maintain the junction temperature at a given level, for a particular power dissipation. It should be noted that this process is usually iterative to achieve the optimum solution.

The following steps can be used as a guideline for determining a suitable thermal solution. First, estimate the maximum ambient temperature (T_A) of the application. Second, define the maximum junction temperature (T_J). Note that the absolute maximum is 150°C. Third, determine the worst case power dissipation. This will typically occur at maximum load and minimum V_{IN}.

Design Example

Assuming: input voltage (V_{IN}) = 12 V, output voltage (V_{OUT}) = 1.2 V, maximum load (I_{OUT}) = 6 A, switching frequency (f_{SW}) = 500 kHz, target junction temperature (T_J) ≤ 125ºC, maximum ambient temperature (T_A) = 85°C, and inductive resistance (DCR_L) = 6.7 mΩ.

1. The main power loss contributors are calculated separately:

• *Switch static losses*

a. Estimate the $R_{DS(on)}$ of the high-side switch at the maximum target junction temperature:

$$R_{DS(on)HS(TJ)} = R_{DS(on)HS(25C)}\left(1+\frac{T_J-25}{200}\right) \quad (31)$$
$$= 20\times10^{-3}\left(1+\frac{125-25}{200}\right)$$
$$= 0.03\ \Omega$$

where $R_{DS(on)HS(25C)}$ is the $R_{DS(on)HS}$ value that can be found from the Electrical Characteristics table in this datasheet.

b. Estimate the $R_{DS(on)}$ of the low side switch at the given junction temperature:

$$R_{DS(on)LS(TJ)} = R_{DS(on)LS(25C)}\left(1+\frac{T_J-25}{200}\right) \quad (32)$$
$$= 8\times10^{-3}\left(1+\frac{125-25}{200}\right)$$
$$= 0.012\ \Omega$$

where $R_{DS(on)LS(25C)}$ is the $R_{DS(on)LS}$ value that can be found from the Electrical Characteristics table in this datasheet.

c. Estimate the duty cycle (D) by applying equation 3 (t_{on}):

$$D = t_{on}\times f_{SW} \quad (33)$$
$$= \left(\frac{V_{OUT}+(R_{DS(on)LS}+DCR_L)\times I_{OUT}}{V_{IN}+(R_{DS(on)LS}-R_{DS(on)HS})\times I_{OUT}}\times\frac{1}{f_{SW}}\right)\times f_{SW}$$
$$= \left(\frac{1.2+(0.012+0.0067)\times 6}{12+(0.012-0.03)\times 6}\times\frac{1}{500\times10^3}\right)\times 500\times10^3$$
$$= 0.11$$

d. The high side static loss can be determined:

$$P_{staticHI} = I_{OUT}^2\times D\times R_{DS(on)HS(TJ)} \quad (34)$$
$$= 6^2\times 0.11\times 0.03$$
$$= 0.119\ \text{W}$$

e. The low side static loss can be determined:

$$P_{staticLO} = I_{OUT}^2\times 1-D\times R_{DS(on)LS(TJ)} \quad (35)$$
$$= 6^2\times(1-0.11)\times 0.012$$
$$= 0.385\ \text{W}$$

• *Switching losses* The combined turn on and turn off losses for both switches are calculated as:

$$P_{switch} = \frac{V_{IN}}{2}\times I_{OUT}\times 6\times10^{-9}\times f_{SW}\times 2$$
$$= \frac{12}{2}\times 6\times 6\times10^{-9}\times 500\times10^3\times 2 \quad (36)$$
$$= 0.216\ \text{W}$$

• ***Recirculation diode losses*** The recirculation diode losses (low-side switch) are calculated as:

$$P_{recirc} = 0.8 \times I_{OUT} \times 6 \times 10^{-9} \times f_{SW} = 0.8 \times 6 \times 6 \times 10^{-9} \times 500 \times 10^{3} = 0.014 \text{ W} \quad (37)$$

• ***Diode transit losses*** The recirculation diode losses (low-side switch) are calculated as:

$$P_{transit} = V_{IN} \times I_{OUT} \times 3 \times 10^{-9} \times f_{SW} = 12 \times 6 \times 3 \times 10^{-9} \times 500 \times 10^{3} = 0.108 \text{ W} \quad (38)$$

• ***BIAS losses*** The supply bias losses are calculated as:

$$P_{bias} = V_{IN} \times 20 \times 10^{-3} = 0.24 \text{ W} \quad (39)$$

2. The total losses in the A8672 can be estimated:

$$P_{total} = P_{staticHI} + P_{staticLO} + P_{switch} + P_{recirc} + P_{transit} + P_{bias} = 0.119 + 0.385 + 0.216 + 0.014 + 0.108 + 0.24 = 1.082 \text{ W} \quad (40)$$

3. The thermal impedance required for the solution can be found:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{total}} = \frac{125 - 85}{1.082} = 37 \text{ °C/W} \quad (41)$$

For this particular solution, a high thermal efficiency board is required to ensure the junction temperature is kept below 125°C. It is recommended to use a PCB with at least four layers. The A8672 should be mounted onto a thermal pad. A number of vias should connect the thermal pad to at least one of the internal layers and the bottom side of the PCB. Both of these layers should be a ground plane. See the Layout section for more information.

Regulator Efficiency

The overall regulator efficiency can be determined by including the inductor loss. In the above thermal characteristics example, the inductor resistance, $DCR_L = 6.7\ m\Omega$. Therefore the inductor power loss can be found::

$$P_L = DCR_L \times I_{OUT}^2 = 0.0067 \times 6^2 = 0.241 \text{ W} \quad (42)$$

The overall regulator efficiency can be found:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + P_{total} + P_L} = \frac{1.2 \times 6}{(1.2 \times 6) + 1.082 + 0.241} = 84.5\ \% \quad (43)$$

Layout

Although the power dissipation in the A8672 is very low, it is recommended that the thermal pad of the device should be soldered to an appropriate pad on the printed circuit board (PCB) to help minimize the junction temperature and enhance the efficiency. The PCB pad should in turn be connected to multiple ground planes by several thermal vias. As a suggestion, the following could be used: twenty vias, arranged in 5 rows of 4, with diameter 0.25 mm and spaced (pitch) 0.6 mm apart. The PCB pad not only acts as a thermal connection, but also forms the star connection for the grounding system.

Figure 8 illustrates the key objectives in the grounding system. The filtering capacitors (C1 through C4, and C6 through C9) should be connected as close as possible to the respective pins. The ground connections for each of the capacitors should be returned directly to the star connection (PCB pad). Again, these connections should be as short as possible. Both the PGND and AGND connections should connect directly to the PCB pad to form the star connection.

The ground return connection for the feedback resistor should be Kelvin-connected directly back to the star ground. Note: To avoid voltage offset errors in the output voltage, the feedback resistor should not be connected to the filter capacitor or load grounds returns.

The support components (C10, C11, and C12), which are ground referenced, should be connected together locally and then returned directly to the star connection. Again, this ground should not pick-up any of the filter capacitors or load ground returns.

Due to the high impedance nature of the COMP node, it is important to ensure the compensation components are connected as close as possible. The feedback trace from R6 and R7 to the FB pin is also a high impedance input and should be as short as possible and be placed well away from noisy connections such as LX. It is recommended to keep any ground planes well away from the LX node to avoid any potential noise coupling effects.

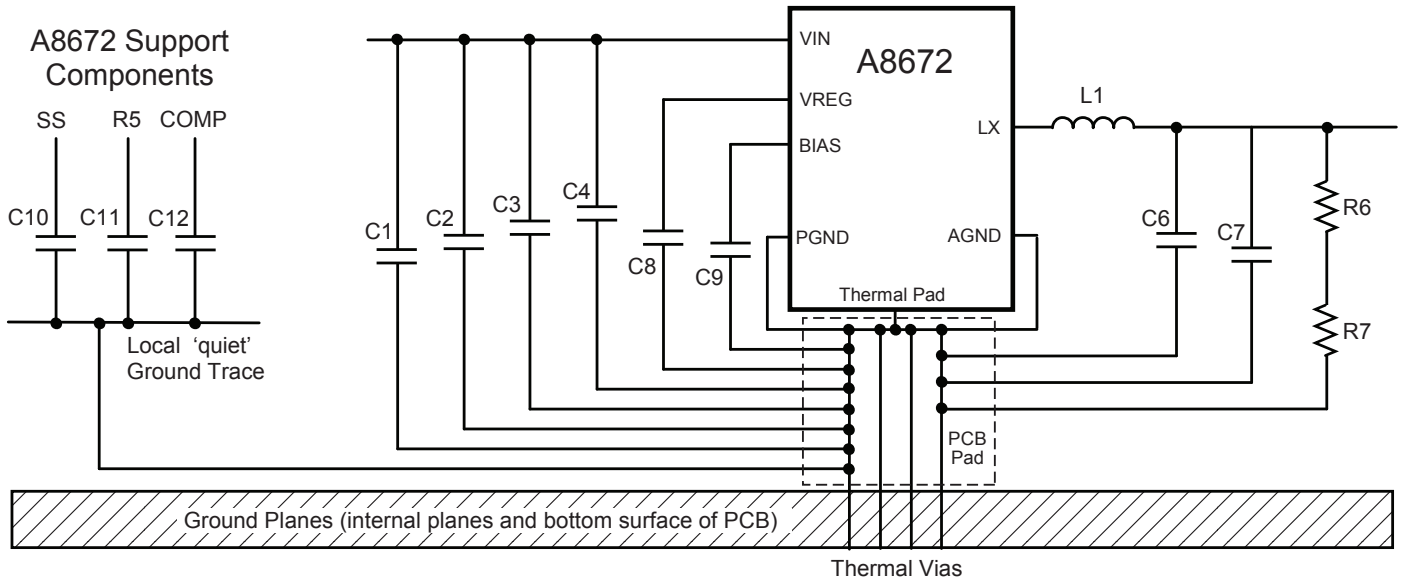
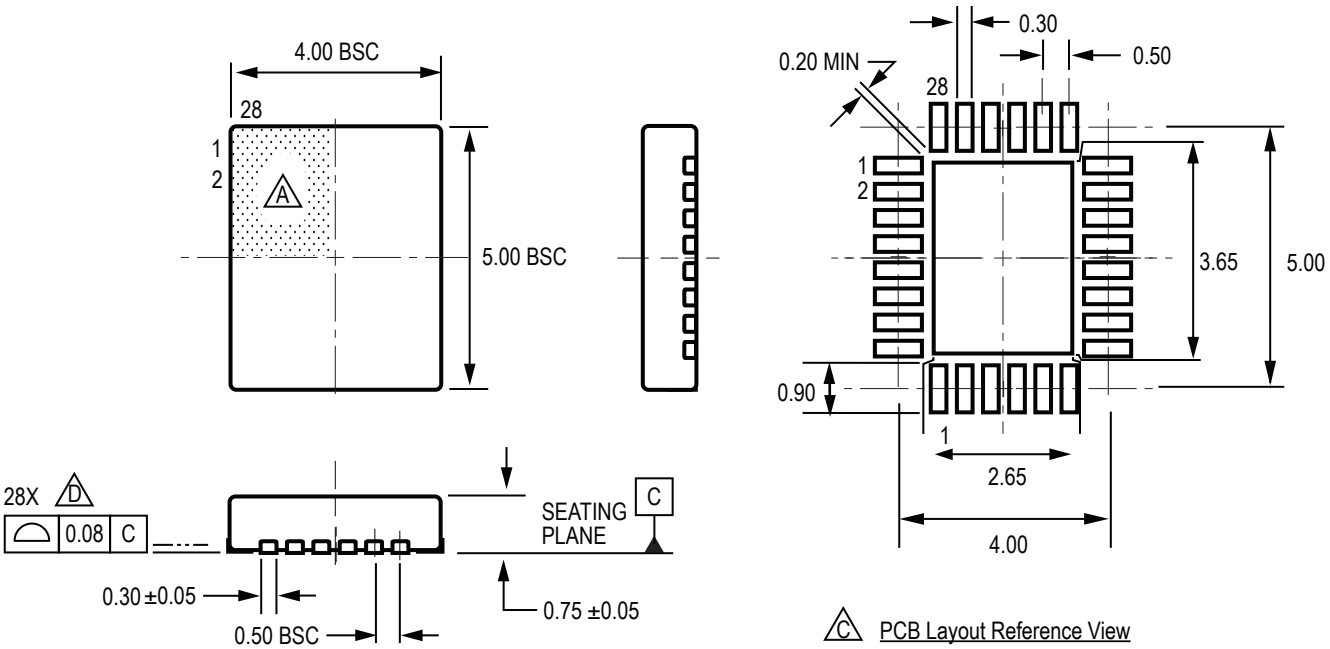
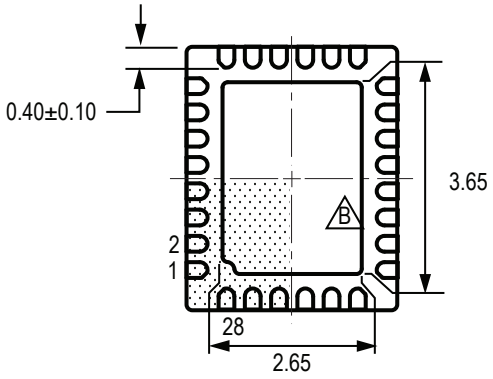


Figure 8: Layout Considerations for Mounting the A8672

Package EG, 28-Contact QFN





Concept Drawing For Reference Only; not for tooling use
(reference JEDEC MO-220WGHD-3 except for contact length)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X500X080-29M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision	Date	Change
1	April 16, 2014	Revised Selection Guide
2	December 5, 2016	Updated product status to Discontinued

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