



A New Direction in Mixed-Signal

February 2014

XRP6274/XRP6275

2A and 3A Ultra Low Dropout Voltage Regulators

Rev. 1.0.1

GENERAL DESCRIPTION

The XRP6274 and XRP6275 are ultra-low dropout voltage regulators capable of delivering 2Amp and 3Amp output currents respectively. They are unique in the industry in being able to operate from a single supply rail of 1.045V to 2.625V without the need for a noise generating charge pump.

With their ultra-low dropout voltage of 140mV at full load guaranteed over temperature, the XRP6274 and XRP6275 achieve conversions previously unavailable.

The output voltage can be set as low as 0.6V with $\pm 0.5\%$ accuracy making the XRP6274 and XRP6275 perfectly suited for powering low voltage devices such as FPGAs, DSPs, ASICs, and other SOCs.

An enable function, soft start and Power Good flag complete the feature set. Built-in current limit, reverse bias and thermal protection ensures safe operation under abnormal operating conditions.

The XRP6274 and XRP6275 are offered in RoHS compliant, "green"/halogen free 10-pin DFN package.

EVALUATION BOARD MANUAL



FEATURES

- **3A Output Current XRP6275**
- **2A Output Current XRP6274**
- **1.045V to 2.625V Single Input Voltage**
 - Adjustable Output Voltage $\geq 0.6V$
 - $\pm 0.5\%$ Output Voltage Accuracy (Room)
 - $\pm 1.0\%$ Output Voltage Accuracy (Temp)
- **Ultra Low Dropout Voltage XRP6275**
 - 138mV Max over temp @ 3A
 - 74mV Max over temp @ 2A
- **Ultra Low Dropout Voltage XRP6274**
 - 140mV Max over temp @ 2A
- **Enable & Soft Start**
- **Current Limit, Thermal and reverse bias Protection**
- **Power Good Flag**

EVALUATION BOARD SCHEMATICS

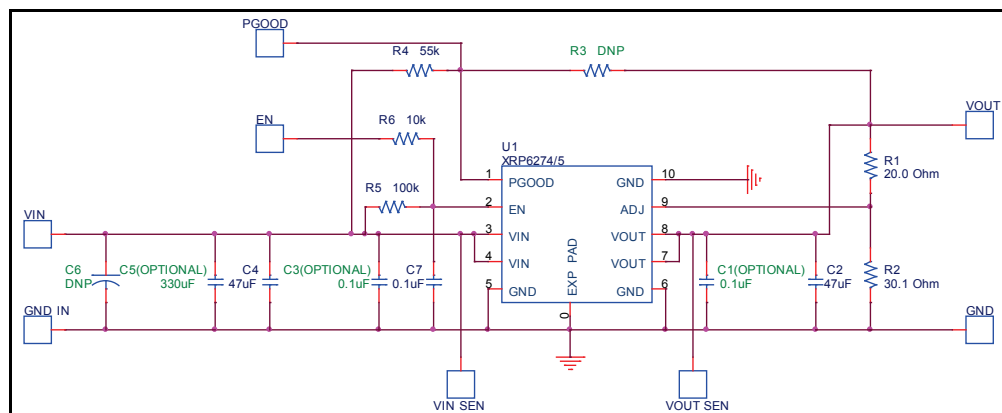


Fig. 1: XRP6274/5 Evaluation Board Schematics

PIN ASSIGNMENT

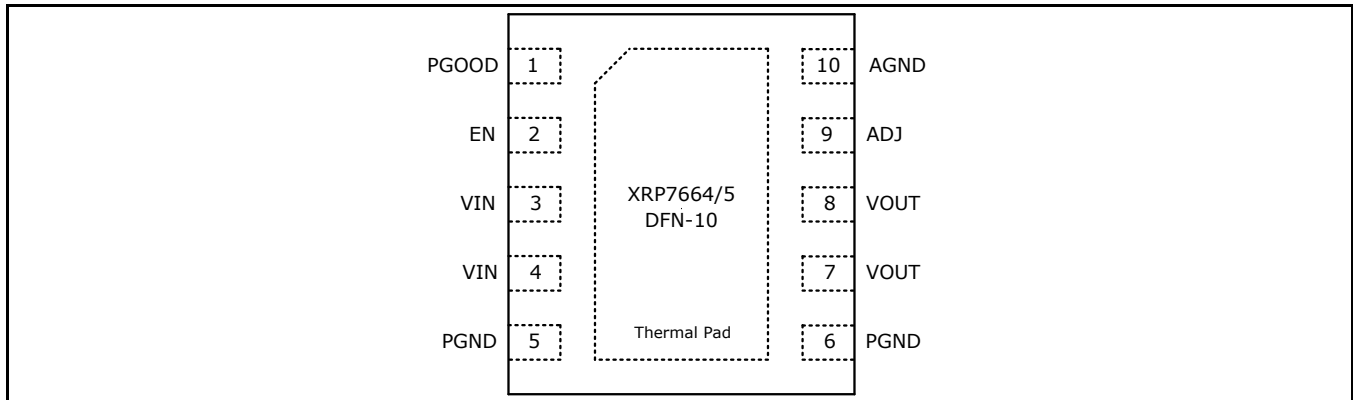


Fig. 2: XRP6274/5 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
EN	2	Enable Input Pin. This is a high impedance MOS input. CMOS compatible; Logic high enables the device; logic low disables the device. Do not pull this pin higher than $V_{IN}+0.5V$.
VIN	3, 4	Power Input Pin. Must be closely decoupled to PGND pin with a $4.7\mu F$ or greater ceramic capacitor.
PGOOD	1	Power Good open Drain Output. When used it should be pulled up to V_{IN} with a resistor.
VOUT	7, 8	Regulator Output pin.
ADJ	9	Adjustable Pin. Connect to a resistive voltage divider to set the output voltage of the device.
PGND	5, 6	Power Ground
Ther. Pad	---	Connect to PGND.
AGND	10	Signal ground. Connect with a separate trace to the ground of the output being regulated.
EN	2	Enable Input Pin. This is a high impedance MOS input. CMOS compatible; Logic high enables the device; logic low disables the device. Do not pull this pin higher than $V_{IN}+0.5V$.
VIN	3, 4	Power Input Pin. Must be closely decoupled to PGND pin with a $4.7\mu F$ or greater ceramic capacitor.

ORDERING INFORMATION

Refer to XRP6274/5's datasheet and/or www.exar.com for exact and up to date ordering information.



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USING THE EVALUATION BOARD

POWERING UP

Use short/thick leads and connect the input power supply to 'VIN/GND IN' connectors. Use short/thick leads and connect the load to 'VOUT/GND' connectors. Apply VIN (1.2V-2.625V). The XRP6274/5 will power up and regulate the output to 1V.

ENABLE (EN)

If Enable is used, then R5 and C7 are not necessary and must be removed. If $V_{IN} \leq EN \leq (V_{IN} + 0.5V)$ then R6 is not necessary. When using the EN pin with a control signal greater than $(V_{IN} + 0.5V)$, R6 is necessary to limit the EN pin current to less than 100uA. EVB has $R6 = 10k$. This will allow a control signal up to 1V above VIN. Populating R6 with a 20k will allow a control signal up to 2V above VIN.

PGOOD

Power Good Flag can be monitored using the PGOOD test point.

MEASURING DROPOUT

Measuring dropout voltage on the XRP6274 and XRP6275 can be a challenge. Typical dropout voltages are less than 80mV at 3Amps and 40mV at 2Amps. As a result, measuring dropout at the input and output terminals of the board will result in a much higher dropout than the part is actually providing. VIN SEN and VOUT SEN test points have been provided to accurately measure dropout performance.

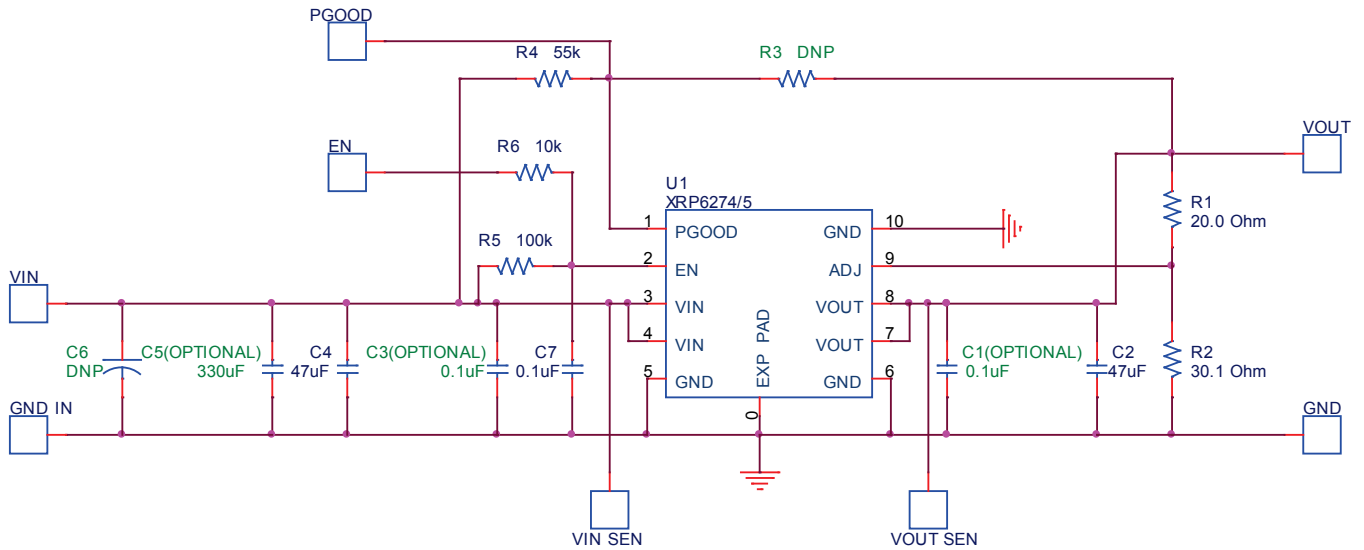


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EVALUATION BOARD SCHEMATICS



Note: C1, C3 and C5 are optional. The purpose of C5 is to help maintain a "stiff" voltage at the input of the Evaluation Board EVB.



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BILL OF MATERIAL

Reference Designator	Qty.	Manufacturer	Manufacturer Part Number	Size	Component
PCB	1	Exar	XRP6274EVB, XRP6275EVB		XRP6274-XRP6275 Evaluation kit
U1	1	Exar	XRP6274, XRP6275	DFN-10	Low Dropout Regulator
C1, C3, C7	3	Murata	GRM188R71H104KA93D	0603	CERAMIC CAP., 0.1uF, 50V, X7R, 10%
C2, C4	2	Murata	GRM32ER71A476KE15L	1210	CERAMIC CAP., 47uF, 10V, X7R, 10%
C5	1	Murata	ECASD90G337M008K00	7.3x4.3mm	Polymer ALUM 330UF 4V 20% SMD
C6	0	---	---	---	---
R1	1	Panasonic	ERJ-3EKF20R0V	0603	Resistor 20 Ω , 1/10w, 1%, SMD
R2	1	Panasonic	ERJ-3EKF30R1V	0603	Resistor 30.1 Ω , 1/10w, 1%, SMD
R3	0	---	---	---	---
R4	1	Panasonic	ERJ-3EKF5492V	0603	Resistor 54.9k Ω , 1/10W, 1%, SMD
R5	1	Panasonic	ERJ-3EKF1003V	0603	Resistor 100k Ω , 1/10W, 1%, SMD
R6	1	Panasonic	ERJ-3EKF1002V	0603	Resistor 10k Ω , 1/10W, 1%, SMD
VIN, VOUT	2	Johnson/Emerson	108-0902-001		CONN. JACK BANANA RED
GND IN, GND	2	Johnson/Emerson	108-0903-001		CONN. JACK BANANA BLK
EN, PGOOD, VIN SEN, VOUT SEN	4	Vector	K24C/M	0.042"	Test Point Post

EVALUATION BOARD LAYOUT

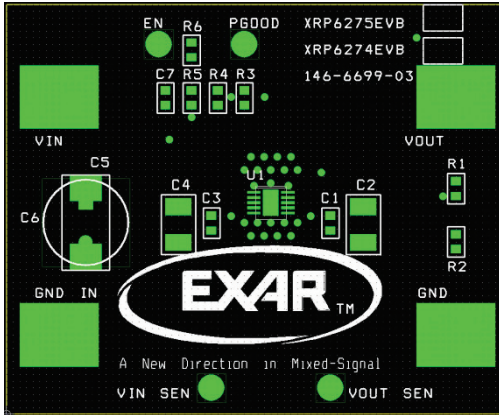


Fig. 3: Component Placement – Top Side

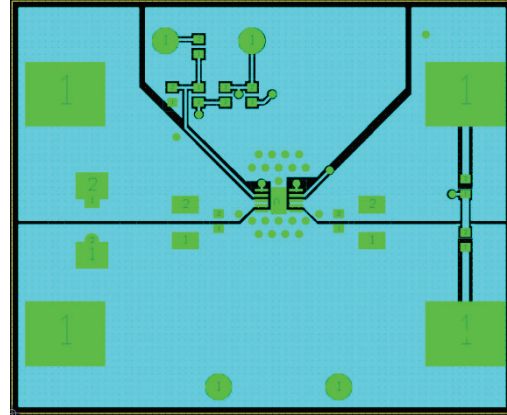


Fig. 4: Layout – Top Side

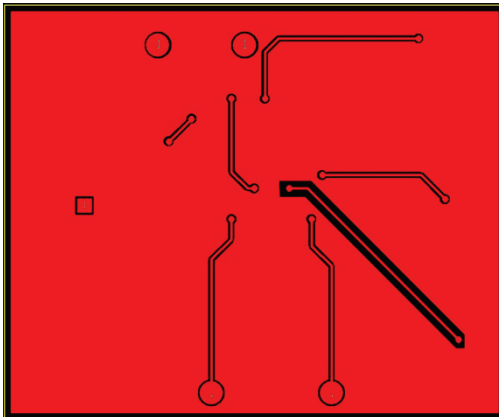


Fig. 5: Layout – Bottom Side

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	01/13/14	Initial release of document
1.0.1	02/05/14	Corrected R1, R2 value in BOM

BOARD REVISION HISTORY

Board Revision	Date	Description
146-6699-03	12/17/13	Initial release of evaluation board

FOR FURTHER ASSISTANCE

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Exar Technical Documentation:

<http://www.exar.com/TechDoc/default.aspx?>



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