ALPHA & OMEGA SEMICONDUCTOR

AON2809

12V Dual P-Channel MOSFET

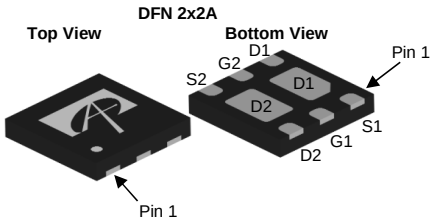
General Description

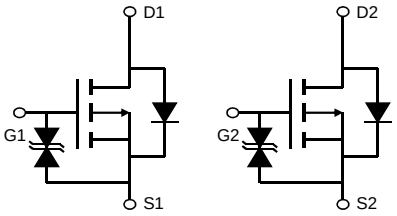
The AON2809 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Product Summary

V_{DS}	-12V
I_D (at V_{GS}=-4.5V)	-2A
$R_{DS(ON)}$ (at V_{GS}=-4.5V)	< 68mΩ
$R_{DS(ON)}$ (at V_{GS}=-2.5V)	< 90mΩ
$R_{DS(ON)}$ (at V_{GS}=-1.8V)	< 118mΩ
Typical ESD protection	**HBM Class 2**

Green Product





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [G]	T_A=25°C	I_D	-2	A
	T_A=70°C		-1.6	
Pulsed Drain Current [C]		I_{DM}	-8	
Power Dissipation [B]	T_A=25°C	P_D	2.1	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	60	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		80	100	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-12			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±6V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250µA	-0.3	-0.6	-0.9	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-8			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-2A		55	68	mΩ
		T_J=125°C		72	89	
		V_{GS}=-2.5V, I_D=-1A		70	90	mΩ
		V_{GS}=-1.8V, I_D=-1A		90	118	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-2A		8		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-1.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-6V, f=1MHz		415		pF
C_{oss}	Output Capacitance			115		pF
C_{rss}	Reverse Transfer Capacitance			78		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		26		Ω
SWITCHING PARAMETERS						
Q_g(4.5)	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-6V, I_D=-2A		4.4		nC
Q_{gs}	Gate Source Charge			0.8		nC
Q_{gd}	Gate Drain Charge			0.9		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-6V, R_L=3Ω, R_{GEN}=3Ω		11.8		ns
t_r	Turn-On Rise Time			24.5		ns
$t_{D(off)}$	Turn-Off DelayTime			54.5		ns
t_f	Turn-Off Fall Time			37.3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-2A, dI/dt=100A/µs		21		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-2A, dI/dt=100A/µs		5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $R_{\theta JA}$ t ≤ 10s and the maxminum maximum allowed junction temperature of 150° C.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

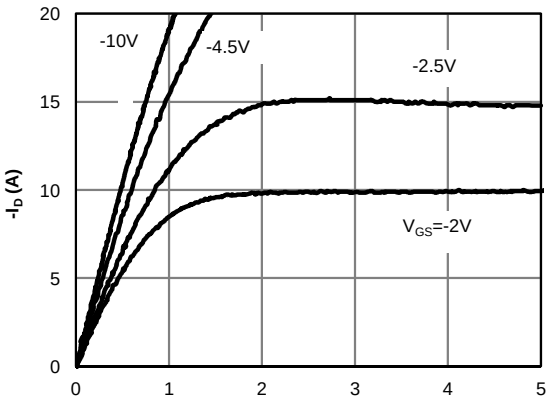


Fig 1: On-Region Characteristics

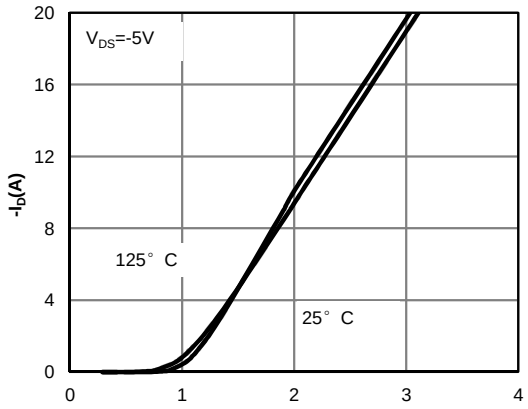


Figure 2: Transfer Characteristics

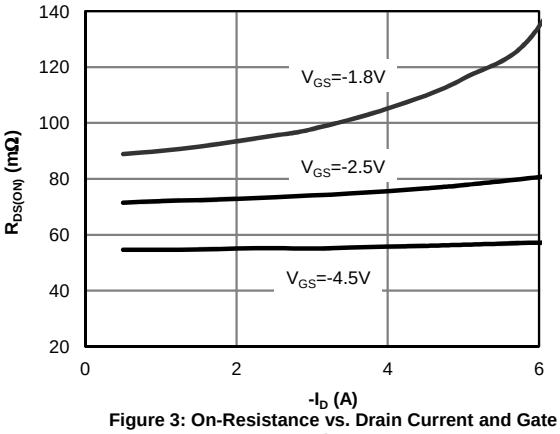


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

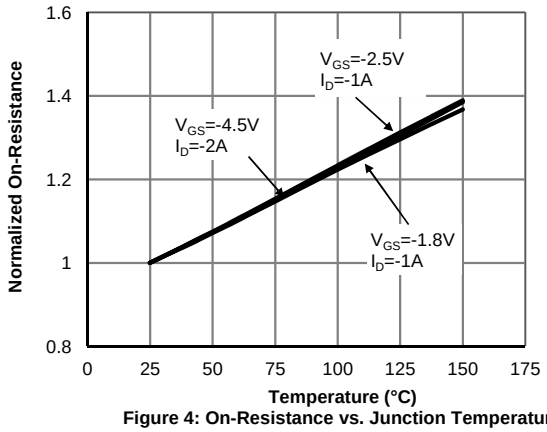


Figure 4: On-Resistance vs. Junction Temperature

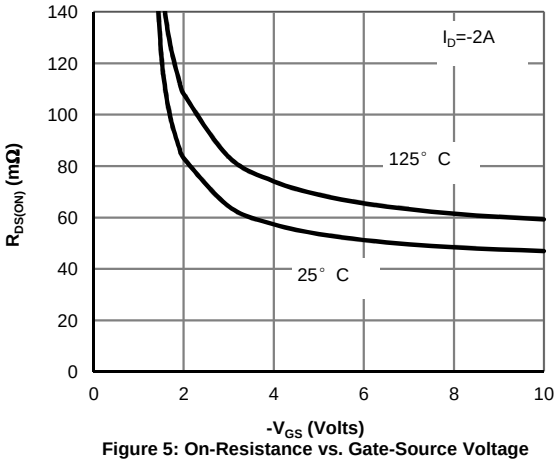


Figure 5: On-Resistance vs. Gate-Source Voltage

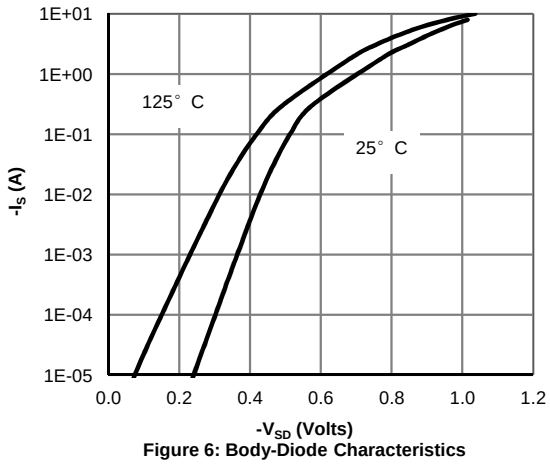


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

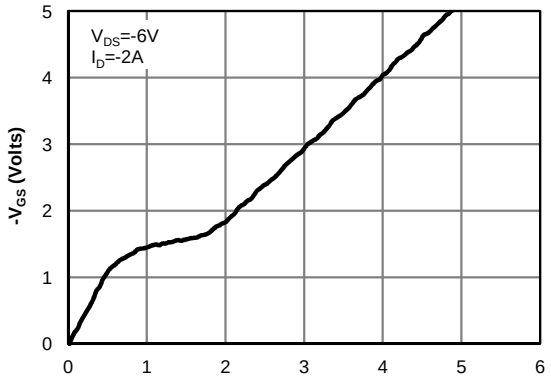


Figure 7: Gate-Charge Characteristics

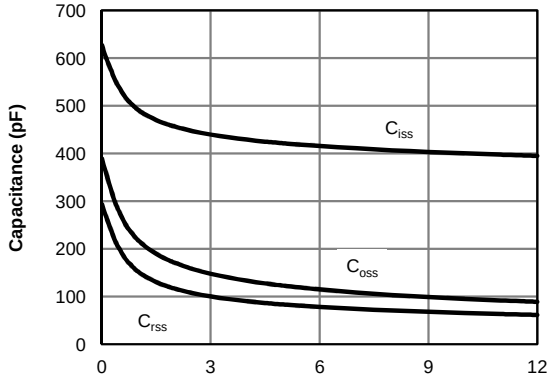


Figure 8: Capacitance Characteristics

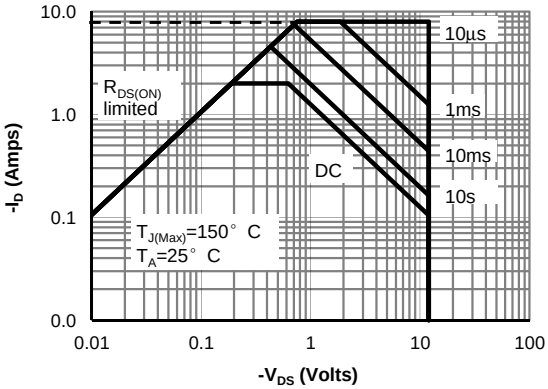


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

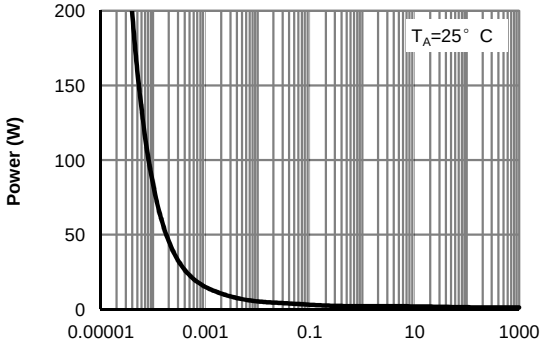


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

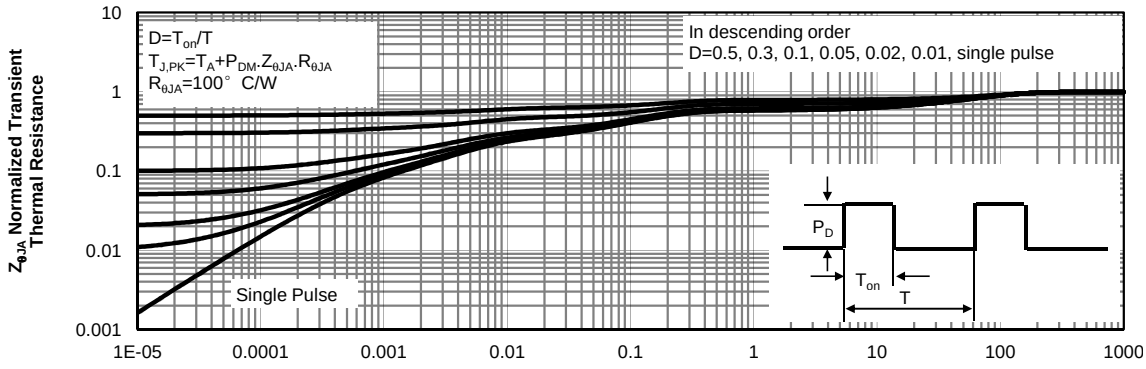
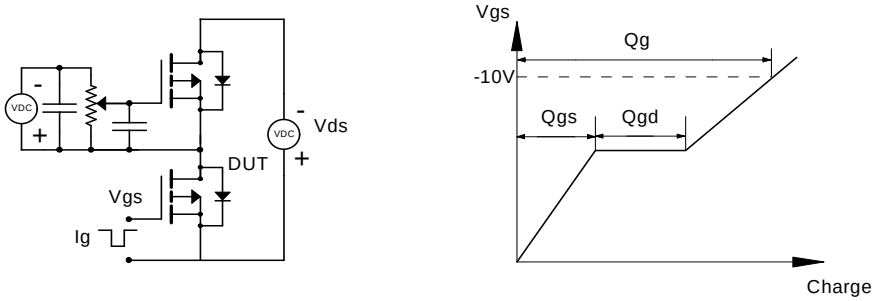
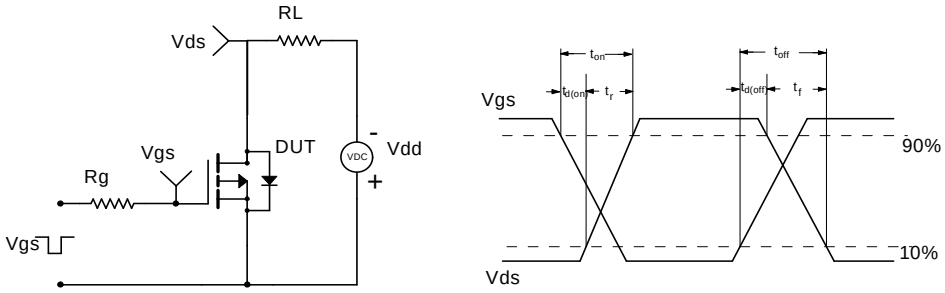


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms