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# Product Specifications

## AN17822A

**APPROVED**  
 Ref No. PS-C3 A  
**EXTERNAL ISSUE**  
 Total Page 17  
 DEPARTMENT CONTROL  
 Page No. 1

Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pin Plastic Package (Power Type with Fin)
Application	Low Frequency Amplifier
Function	BTL 5.0W x 2ch Power Amplifier with Standby Function and Volume Function

A Absolute Maximum Ratings					
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	°C	1
2	Operating Ambient Temperature	Topr	-25 ~ +70	°C	1
3	Operating Ambient Pressure	Popr	1.013x10 <sup>5</sup> ± 0.61x10 <sup>5</sup>	Pa	
4	Operating Constant Acceleration	Gopr	9810	m/s <sup>2</sup>	
5	Operating Shock	Sopr	4900	m/s <sup>2</sup>	
6	Supply Voltage	Vcc	14.4	V	2
7	Supply Current	Icc	2.0	A	
8	Power Dissipation	Pd	1.92	W	Ta=70°C

Operating Supply Voltage Range	Vcc	3.5V ~ 13.5V
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Note 1: The temperature of all items shall be Ta = 25°C except storage temperature and operating ambient temperature.  
 Note 2: At no signal input

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**Product Specifications**

**AN17822A**

**APPROVED**  
 Ref No. B-1  
**EXTERNAL ISSUE**  
 Total Page 17  
 DOCUMENT No. 2

No	Item	Symbol	Test Cct.	Conditions	Limits			Unit	Note
					Min	Typ	Max		
					(Unless otherwise specified, the ambient temperature is 25°C ± 2°C, Vcc = 8.0V, frequency = 1kHz and RL = 8 Ω)				
1	Quiescent Circuit Current	I <sub>CQ</sub>	1	V <sub>in</sub> = 0V, V <sub>ol</sub> = 0V	-	45	100	mA	
2	Standby Current	I <sub>STB</sub>	1	V <sub>in</sub> = 0V, V <sub>ol</sub> = 0V	-	1	10	μA	
3	Output Noise Voltage	V <sub>NO</sub>	1	R <sub>g</sub> = 10kΩ, V <sub>ol</sub> = 0V	-	0.25	0.4	mVrms	1
4	Voltage Gain	G <sub>V</sub>	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 1.25V	39	41	43	dB	
5	Total Harmonic Distortion	THD	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 1.25V	-	0.20	0.5	%	
6	Maximum Power Output 1	P <sub>o1</sub>	1	THD = 10%, V <sub>ol</sub> = 1.25V	2.4	3.0	-	W	
7	Maximum Power Output 2	P <sub>o2</sub>	1	V <sub>cc</sub> = 11V THD = 10%, V <sub>ol</sub> = 1.25V	4.0	5.0	-	W	
8	Ripple Rejection Ratio	RR	1	R <sub>g</sub> = 10kΩ, V <sub>ol</sub> = 0V V <sub>r</sub> = 0.5Vrms, f <sub>r</sub> = 120Hz	30	50	-	dB	1
9	Output Offset Voltage	V <sub>off</sub>	1	R <sub>g</sub> = 10kΩ, V <sub>ol</sub> = 0V	-200	0	200	mV	
10	Volume Attenuation Ratio	Att	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 0V	70	80	-	dB	1
11	Channel Balance 1	CB1	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 1.25V	-1	0	1	dB	
12	Channel Balance 2	CB2	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 0.6V	-2	0	2	dB	
13	Middle Voltage Gain	G <sub>Vm</sub>	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 0.6V	27.5	30.5	33.5	dB	
14	Channel Crosstalk	CT	1	P <sub>o</sub> = 0.5W, V <sub>ol</sub> = 1.25V	40	55	-	dB	

Note 1) For this measurement, use the BPF = 15Hz ~ 30kHz (12dB/OCT)

Eff. Date	Eff. Date	Eff. Date	Eff. Date
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**Product Specifications**  
 (Reference Data for Design)  
**AN17822A**

**APPROVED**  
**INTERNAL ISSUE**

Ref No. B-2  
 Total Page 17  
 Page No. 3

MSD  
 05.04.04  
 DOCUMENT CONTROL

No	Item	Symbol	Test Cct.	Conditions	Limits			Unit	Note
					Min	Typ	Max		
1	Standby pin current	I <sub>STB2</sub>	1	V <sub>in</sub> = 0V, V <sub>STB</sub> = 3.0V	-	-	25	μA	
2	Volume pin current	I <sub>Vol</sub>	1	V <sub>in</sub> = 0V, V <sub>ol</sub> = 0V	-12	-	-	μA	
3	Input Impedance	Z <sub>i</sub>	1	V <sub>in</sub> = ±0.3V <sub>DC</sub>	24	30	36	kΩ	

Note) The above characteristics are reference values determined for IC design, but not guaranteed values for shipping inspection. If problems were to occur, counter measures will be sincerely discussed.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

Prepared	<i>[Signature]</i>	<b>Product Specifications</b>	Ref No.	C
Checked	<i>[Signature]</i>		Total Page	17
Approved	<i>[Signature]</i>		Page No.	4

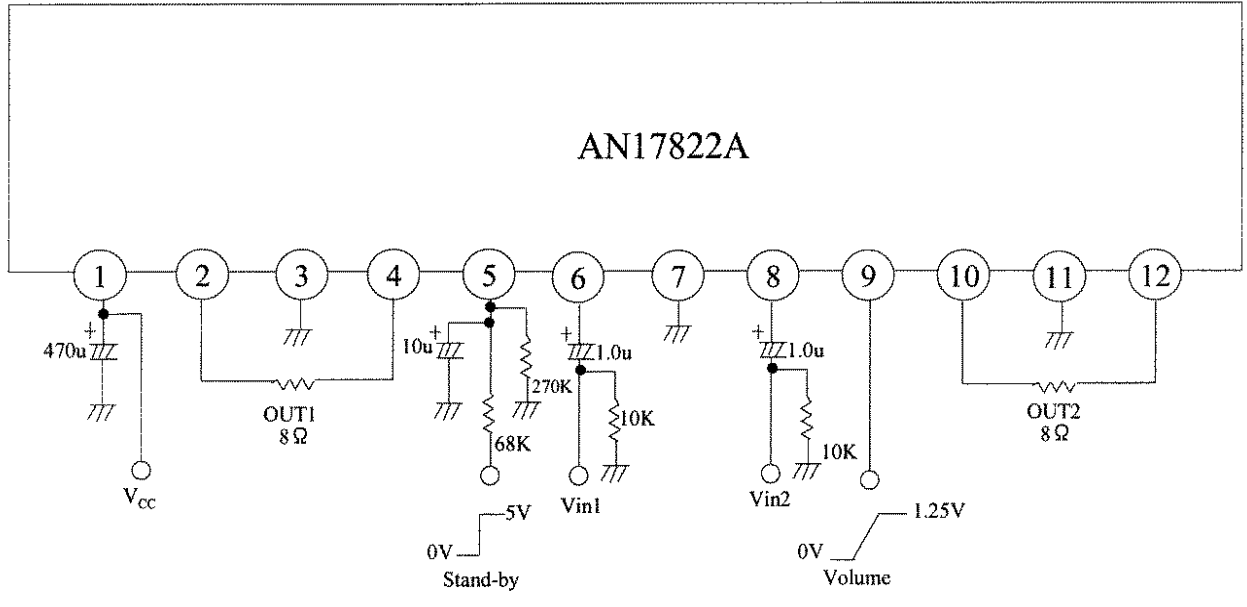
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## AN17822A



(Description of test circuit and test method)

Test Circuit 1



Note) If the standby pin is open or 0V, the IC is on standby state.  
 The IC is in the state of volume minimum if the Volume pin is ground.  
 The IC is in the state of volume maximum if the Volume pin is open.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
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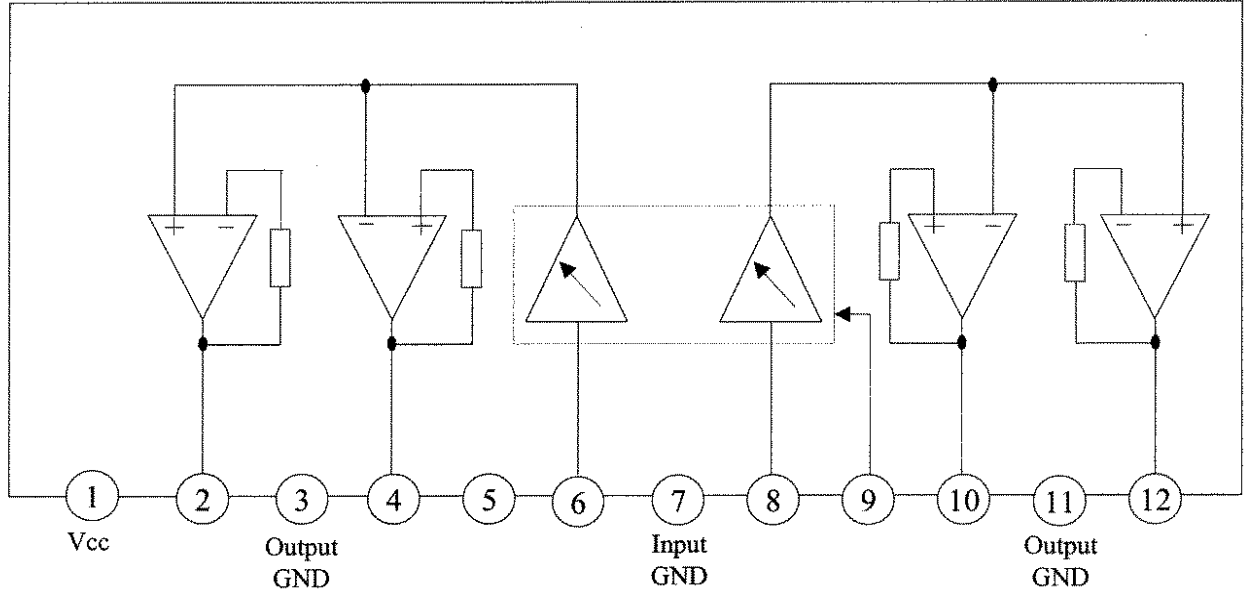
## AN17822A

**APPROVED**  
 Ref No. D  
 Total Page 17  
 Page No. 5

**EXTERNAL ISSUE**

DOCUMENT CONTROL

### Circuit Function Block Diagram



### Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Vcc	7	GND (Input)
2	Ch.1 Output (+)	8	Ch.2 Input
3	GND (Ch. 1 Output)	9	Volume
4	Ch.1 Output (-)	10	Ch.2 Output (-)
5	Standby	11	GND (Ch.2 Output)
6	Ch.1 Input	12	Ch.2 Output (+)

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

Prepared	Lim Fuey Sheen
Checked	Kenneth Law
Approved	Yasuo Higuchi

**Product Specifications**  
**AN17822A**

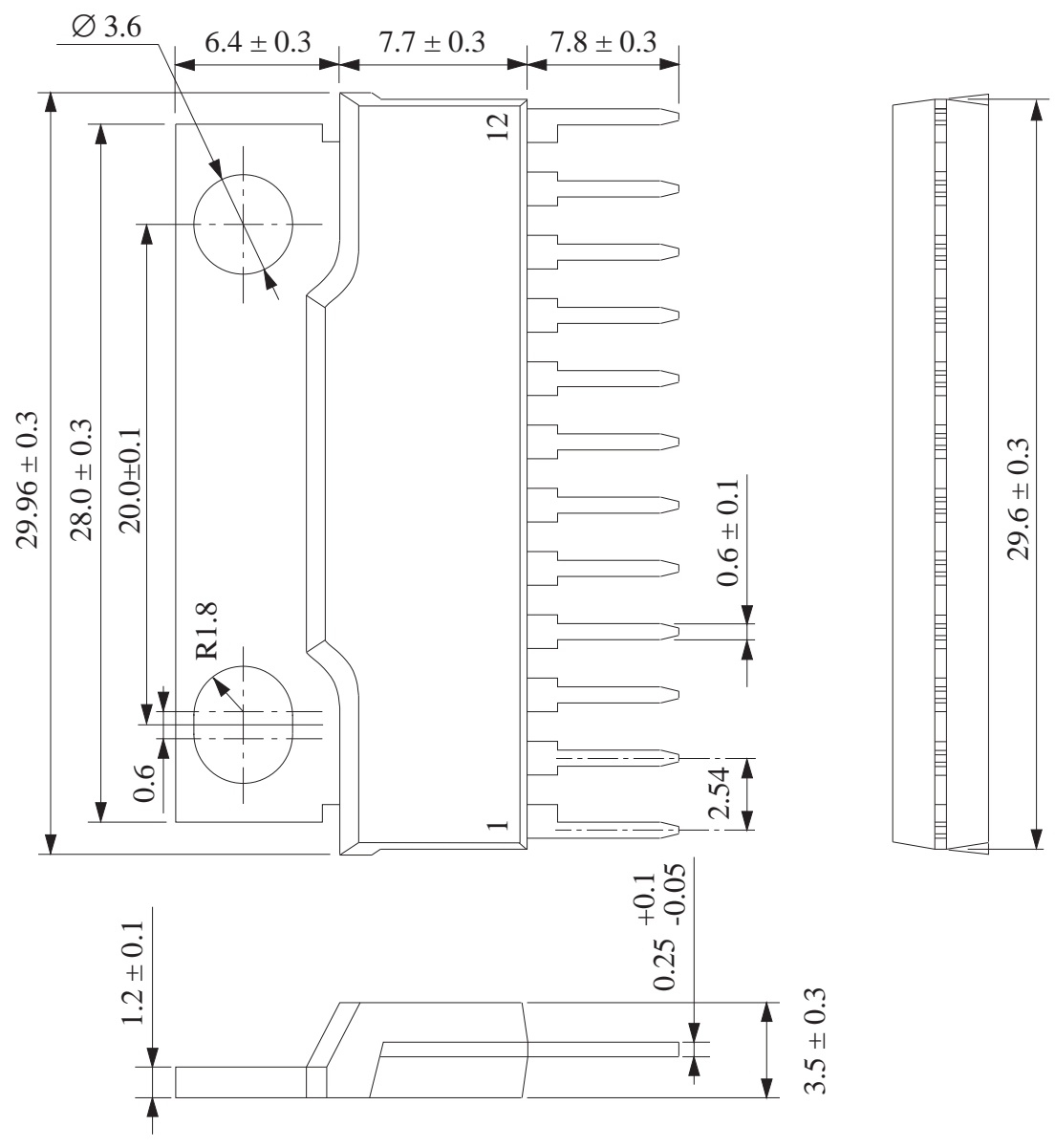
Ref No.	E
Total Page	17
Page No.	6

**APPROVED**  
**EXTERNAL ISSUE**

**12-SIL(FP)**

Package Name	FP-12S
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Unit : mm



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Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003	-	28-MAR-05	



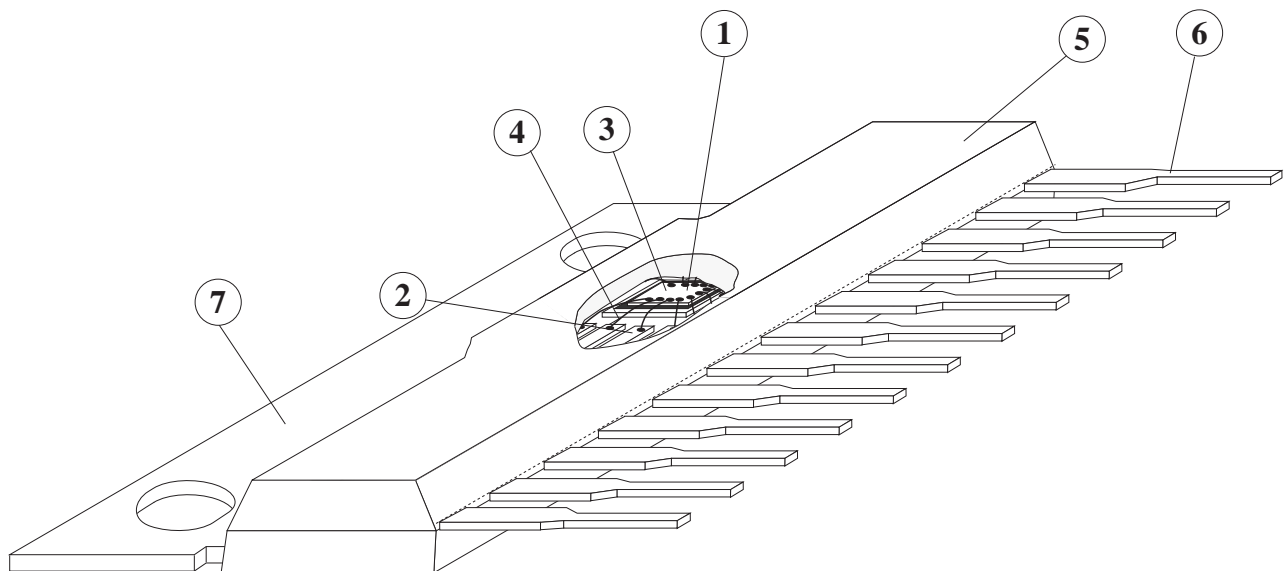
**(Structure Description)**

Chip surface passivation	SiN, PSG, Others ( )	①
Lead frame material	Fe group, Cu group, Others ( )	②, ⑥
Inner lead surface process	Ag plating, Au plating, Others ( )	②
Outer lead surface process	Solder plating (98Sn-2Bi), Solder dip, Others ( )	⑥
Chip mounting method	Ag paste, Au-Si alloy, Solder (95.5Pb-2.5Ag-2Sn)**	③
Wire bonding method	Thermalsonic bonding, Others ( )	④
Wire material	Au, Others ( )	④
Mold material	Epoxy, Others ( )	⑤
Molding method	Transfer mold, Multiplunger mold, Others ( )	⑤
Fin material	Cu group, Others ( )	⑦

\*1  
\*1

**Package FP-12S**

\*\*Under RoHS exemption clause, Lead (Pb) in high melting temperature type solder (i.e. tin-lead solder alloys containing more than 85% of lead), is exempted until 2010.



\*1

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**Product Specification**  
(Technical Data)  
**AN17822A**

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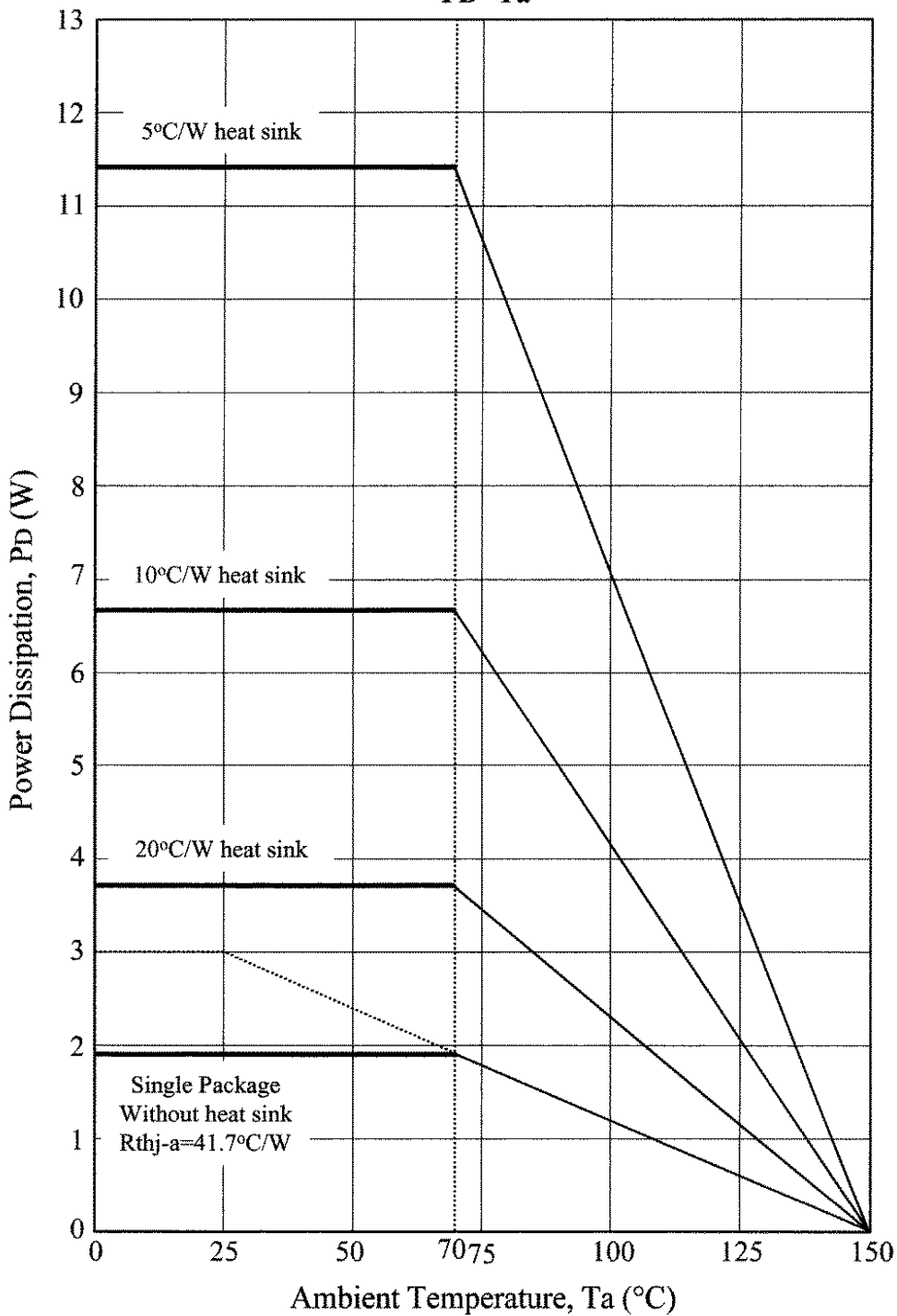
Ref No. G-1  
Total Page 17  
Page No. 8

**EXTERNAL ISSUE**

MS05  
05.01.04  
DOCUMENT CONTROL

$$\begin{pmatrix} R_{th(j-c)} = 2^{\circ}\text{C/W} \\ R_{th(j-a)} = 41.7^{\circ}\text{C/W} \end{pmatrix}$$

**FP-12S Package Power Dissipation**  
**PD- Ta**



Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

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**Product Specifications**  
 (Technical Data)

**AN17822A**

**APPROVED**

Ref No. G-2  
 Total Page 17  
 Date 05/01/04  
 DOCUMENT No. 9

**EXTERNAL ISSUE**

	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
1	VCC		This is the power supply pin.	Typ 8V
2	Channel 1 Output(+)		This is the positive output terminal of channel 1.	Vcc/2
3	GND		Channel 1 Ground	0V
4	Channel 1 Output(-)		This is the negative output terminal of channel 1.	Vcc/2
5	Standby		Standby Control Pin  Standby "ON" = 0V Standby "OFF" = 5V	Typ 5V

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

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**Product Specification**  
 (Technical Data)

**AN17822A**

**APPROVED**  
 Ref No. G-2  
 Total Page 17  
 Page No. 10  
 05.01.04  
 DOCUMENT CONTROL

Pin No.	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
6	Channel 1 Input		This is the channel 1 input terminal.	1.45V
7	GND		Input Ground	0V
8	Channel 2 Input		This is the channel 2 input terminal.	1.45V
9	Volume		Volume Control Pin  Volume "OFF" = 0V Max Volume = 1.25V	

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

**APPROVED**  
**EXTERNAL ISSUE**

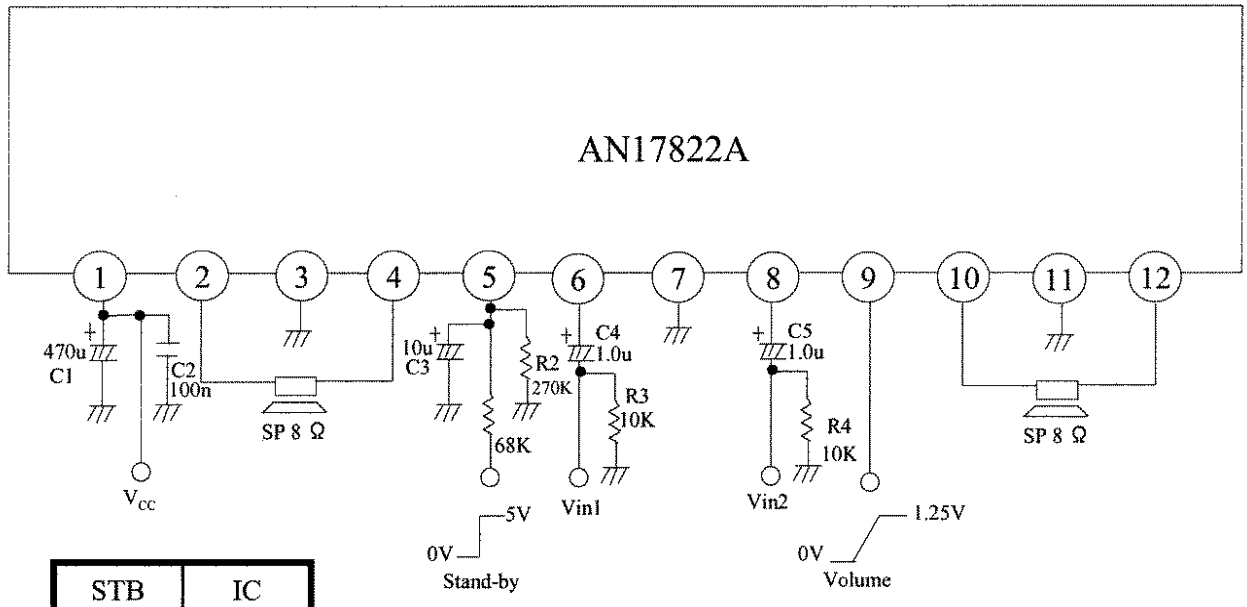
MS05  
 05.01.04  
 DOCUMENT CONTROL

Prepared	<i>[Signature]</i>	<b>Product Specification</b> (Technical Data)	Ref No. <b>6-2</b>
Checked	<i>[Signature]</i>	<b>AN17822A</b>	Total Page <b>17</b>
Approved	<i>[Signature]</i>		Page No. <b>11</b>

Pin No.	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
10	Channel 2 Output(-)		This is the negative output terminal of channel 2.	Vcc/2
11	GND		Channel 2 Ground.	0V
12	Channel 2 Output(+)		This is the positive output terminal of channel 2.	Vcc/2

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

Application Circuit



STB	IC
0V	OFF
5V	ON

Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

Prepared	<i>[Signature]</i>	<b>Product Specifications</b> (Technical Data) <b>AN17822A</b>	<b>APPROVED</b> <b>EXTERNAL ISSUE</b>	Ref No. G-4
Checked	<i>[Signature]</i>		MS03 05.01.04 DOCUMENT CONTROL	Total Page 17
Approved	<i>[Signature]</i>		Page No. 13	

## Application Information

### Supply Decoupling

To ensure a stable supply and achieve better ripple rejection, decoupling capacitors need to be connected to VCC. (Pin1)

Decoupling capacitors should have small Equivalent Series Resistance (ESR). This is to prevent resistive losses and introduction of undesirable phase shift to internal circuits.

A ceramic capacitor of 100nF in parallel with a non-ceramic (Tantalum or Aluminum Electrolytic) capacitor of 470uF are suggested. This combination has a small ESR over a wide frequency range.

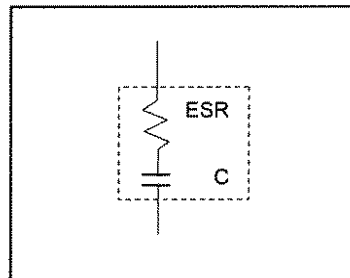


FIG 1. A Practical Capacitor

Although small in size and ESR, large valued ceramic capacitor is not advisable to use. Current surges during power ON/OFF might store energy in the inductances of the power leads; and a large voltage spike could be created when the stored energy is transferred from the inductances to the ceramic capacitor. The amplitude of the spike could exceed twice the supply voltage.

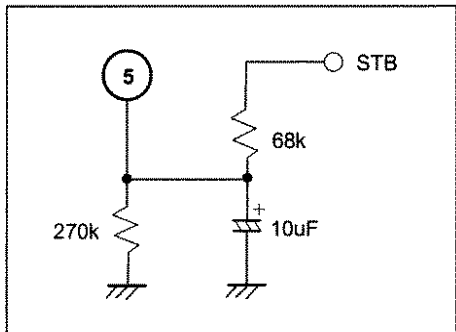


FIG 2. Standby Circuits

### Standby Operation

Standby pin should be connected with carefully selected components in order to avoid "Pop Noise" during Standby ON/OFF transient.

The 68k resistor and 10uF capacitor pair can delay the rising of voltage at Pin5 to reach the Standby threshold. When Standby is switching on together with supply, this delay would be very useful to ensure no "Pop Noise".

If the Standby voltage is provided by a microcontroller, the suppression of "Pop" could even be better.

The microcontroller can set a delay of 100-200ms between the supply and Standby ON/OFF.

The 68k and 270k resistor also form a voltage divider, which determines the Standby threshold.

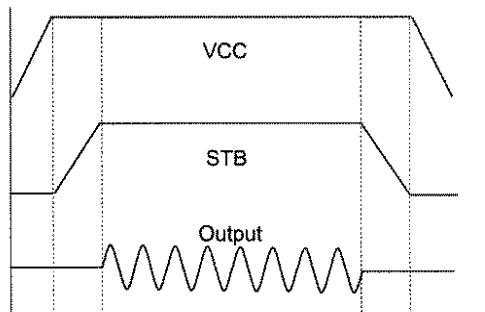


FIG 3. Standby ON/OFF Logic

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				



Prepared	<i>[Signature]</i>	<b>Product Specifications</b> (Technical Data) <b>AN17822A</b>	<b>APPROVED</b>	Ref No.	G-4
Checked	<i>[Signature]</i>		<b>EXTERNAL ISSUE</b>	Total Page	17
Approved	<i>[Signature]</i>		05.01/04 DOCUMENT CONTROL	Page No.	14

### Power Dissipation and Heat Sink

Before start of the discussion, a few terms have to be defined.

- PD: Power Dissipation
- TJ: Junction Temperature
- Tc: Case Temperature
- TA: Ambient Temperature
- $\theta_{JC}$ : Thermal Resistance (Junction to Case)
- $\theta_{CA}$ : Thermal Resistance (Case to Ambient, normally of heat sink)

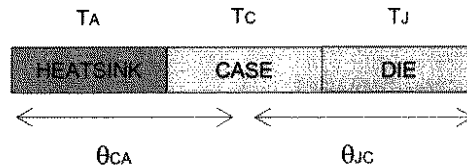


FIG 4. Simplified Illustration of IC and Heat Sink Attached

The following two equations represent the relations of these terms.

$$(T_J - T_c) / \theta_{JC} = P_D \quad (1)$$

$$(T_c - T_A) / \theta_{CA} = P_D \quad (2)$$

For reliable, long-term, continuous operation, junction temperature should not exceed 125°C and  $\theta_{JC}$  for FP-12S package is 2°C/W. Put these values in Equation 1. After specify the PD, Tc can be determined.

Assume no heat loss at the casing, i.e. all power is dissipated to the ambient through heat sink, which is quite true. So  $P_D = P_D'$ . Since Tc is also known, one can determine the following using Equation 2:

- a) The rating of heat sink for specific maximum operating ambient temperature, or
- b) The maximum operating ambient temperature for specific heat sink rating.

A more general equation can be used for rough calculation.

$$(T_J - T_A) / \theta_{JA} = P_D \quad (3)$$

$$\theta_{JA} = \theta_{CA} + \theta_{JC} \quad (4)$$

In this case,  $\theta_{JA}$  is total thermal resistance of the heat sink and IC package. Therefore, for specified power dissipation, either heat sink rating or maximum operating ambient temperature can be decided if the other is known.

Take note that it's essential to know PD value before hand in order to work out other quantities. PD calculation is as shown.

$$P_D = V_{CC} \times I_{CC} - P_{O\_TOTAL} \quad (5)$$

- Vcc: DC supply voltage
- Icc: RMS value of IC current
- PO\_TOTAL: Total output power

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				



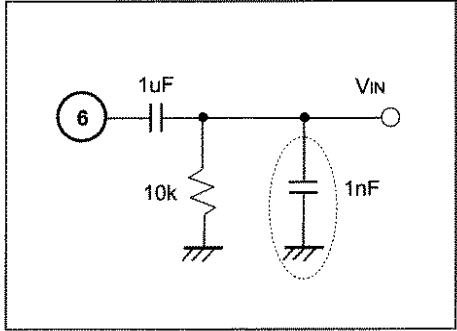
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Approved	<i>[Signature]</i>

**Product Specification**  
(Technical Data)  
**AN17822A**

**APPROVED**  
**EXTERNAL ISSUE**

Ref No. G-4  
Total Page 17  
Page No. 15

MSCS  
05.01.04  
DOCUMENT CONTROL



**FIG 5. Input DC Decoupling**

*Input DC Decoupling*

Before the input signal reaches differential amplifier stage, its DC component should be removed.

The capacitor of 1uF pass only AC signal and the 10k resistor forms a DC path to ground.

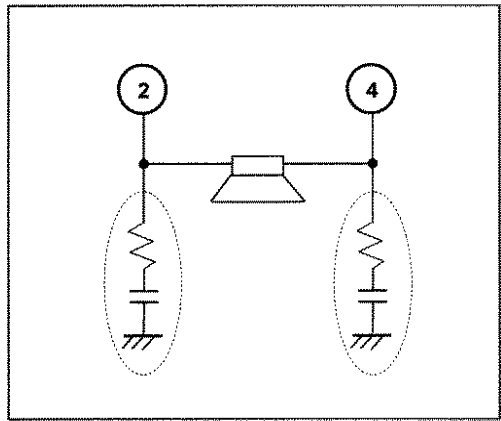
The 1nF capacitor in parallel to the 10k resistor is optional and it serves to filter out high frequency noise at the input.

*Output Zobel Network*

It should be noted that this device is designed such that the Zobel network (RC pair) at the output pins is not necessary for stable operation.

In practical application, the Zobel network may be applied optionally for two reasons:

- a) Ensuring stability for different PCB layout and speaker types.
- b) Ability to withstand to high ESD levels.



**FIG 6. Output Zobel Network**

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				

Prepared	<i>[Signature]</i>
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Approved	<i>[Signature]</i>

**Product Specifications**  
(Technical Data)  
**AN17822A**

<b>APPROVED</b>		Ref No.	G-4
<b>EXTERNAL ISSUE</b>		Total Page	17
05-01-04 DOCUMENT CONTROL		Page No.	16

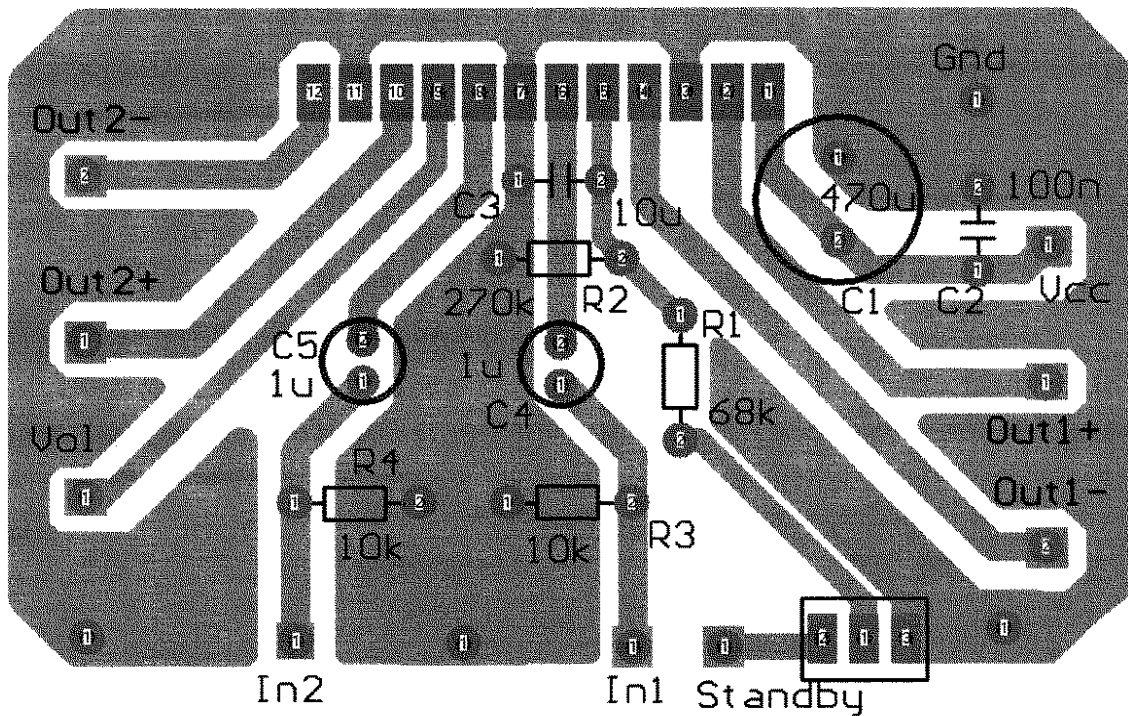
**PCB Layout**

Good PCB layout can improve chip's performances.


To reduce stray capacitances at the inputs and outputs, external components are to be placed as close to the pins as possible.

PCB traces conducting huge current, such as those connected to supply or outputs, should be kept short and wide. This will keep inductances low and resistive loss to a minimum.

The Layout of test board is as shown below.



Eff. Date	Eff. Date	Eff. Date	Eff. Date
24-DEC-2003			

Prepared	<i>[Signature]</i>	<b>Product Specification</b> <b>AN17822A</b>	<b>APPROVED</b> <b>EXTERNAL ISSUE</b>	Ref No.	II
Checked	<i>[Signature]</i>			Total Page	17
Approved	<i>[Signature]</i>			Page No.	17

**(Precautions for use)**

1. Make sure that the IC is free of any pin short-circuiting, ground short-circuiting, pin shift and reverse insertion.
2. Ground the radiation fin so that there will be no difference in electric potential between the radiation fin and ground.
3. The thermal protection circuit operates at a Tj of approximately 150°C. The thermal protection circuit is reset automatically when the temperature drops.
4. Make sure that the heat radiation design is effective enough if the Vcc is comparatively high or the IC operates high output power.
5. Connect only ground pin for signal sources to the signal GND pin of the amplifier on the previous stage.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				