NXP Semiconductors
Technical Data

Document Number: A2T08VD020N
Rev. 1, 05/2017

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 2 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 728 to 960 MHz.

900 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = I_{DQB} = 40 mA, P_{out} = 2 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)
920 MHz	19.3	21.3	–43.4
940 MHz	19.3	21.5	–43.8
960 MHz	19.1	21.1	–43.9

700 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = I_{DQB} = 40 mA, P_{out} = 2 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)
728 MHz	19.2	18.9	–42.3
748 MHz	19.2	19.2	–42.6
768 MHz	18.9	18.7	–42.6

Features

- Greater negative gate-source voltage range for improved Class C operation
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (1)
- Integrated ESD protection

A2T08VD020NT1

728–960 MHz, 2 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR

PQFN 8 × 8 PLASTIC

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

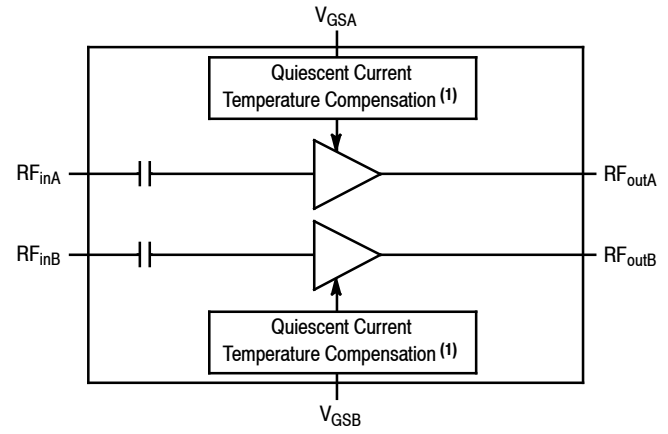
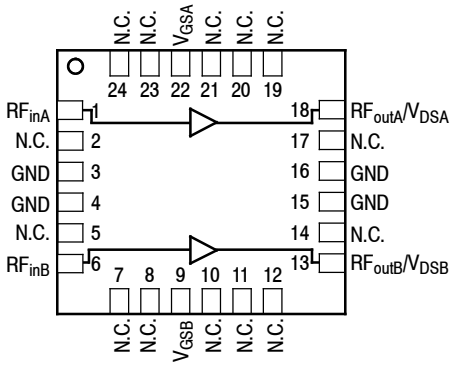


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (2,3)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 2 W CW, 48 Vdc, I_{DQA} = I_{DQB} = 40 mA, 940 MHz	$R_{\theta JC}$	3.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.nxp.com/RF/calculators.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 26 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, I_{DQ} = 80 mAdc)	$V_{GS(Q)}$	—	2.5	—	Vdc
Fixture Gate Quiescent Voltage (2) (V_{DD} = 48 Vdc, I_{DQ} = 80 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.0	5.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 64 mAdc)	$V_{DS(on)}$	0.1	0.21	0.8	Vdc
Functional Tests (3) (In NXP Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = I_{DQB} = 40 mA, P_{out} = 2 W Avg., f = 960 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.0	19.1	21.0	dB
Drain Efficiency	η_D	20.0	21.1	—	%
Adjacent Channel Power Ratio	ACPR	—	–43.9	–41	dBc
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQA} = I_{DQB} = 40 mA, f = 940 MHz, 10 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 55 Vdc, 35 W Pulsed CW Output Power (3 dB Input Overdrive from 26.9 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = I_{DQB} = 40 mA, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	18.6	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	21.9	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	–10.5	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	120	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 2 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.017	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T08VD020NT1	T1 Suffix = 1,000 Units, 16 mm Tape Width, 13-inch Reel	PQFN 8 × 8

1. Each side of device measured separately.
2. Side A and Side B are tied together for this measurement.
3. Part internally input matched.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

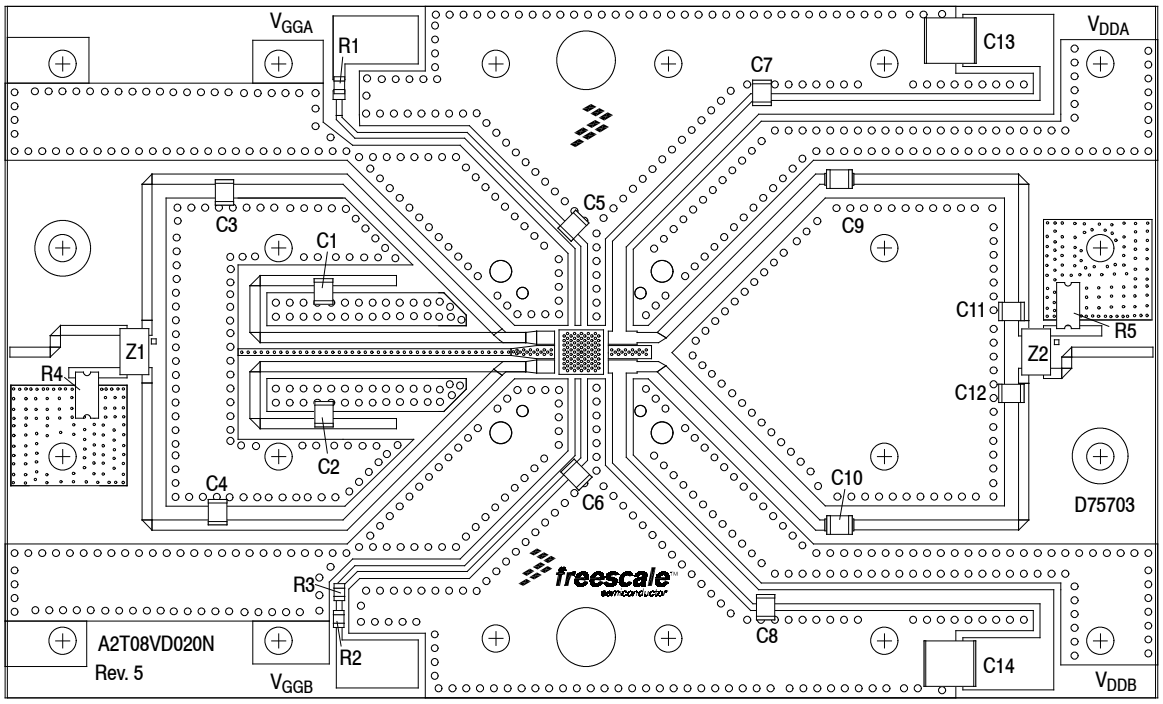


Figure 3. A2T08VD020NT1 Test Circuit Component Layout

Table 7. A2T08VD020NT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C5, C6, C7, C8, C9, C10	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C3, C4	1.1 pF Capacitors	ATC100B1R1BT500XT	ATC
C11, C12	2 pF Chip Capacitors	ATC100B2R0BT500XT	ATC
C13, C14	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
R1, R2	2 kΩ, 1/8 W Chip Resistors	SG73P2ATTD2001F	KOA Speer
R3	0 Ω, 1.5 A Chip Resistor	CWCR08050000Z0EA	Vishay
R4, R5	50 Ω, 10 W Chip Resistors	C8A50Z4A	Anaren
Z1, Z2	600–900 MHz Band, 90°, 3 dB Hybrid Couplers	X3C09F1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D75703	MTL

TYPICAL CHARACTERISTICS

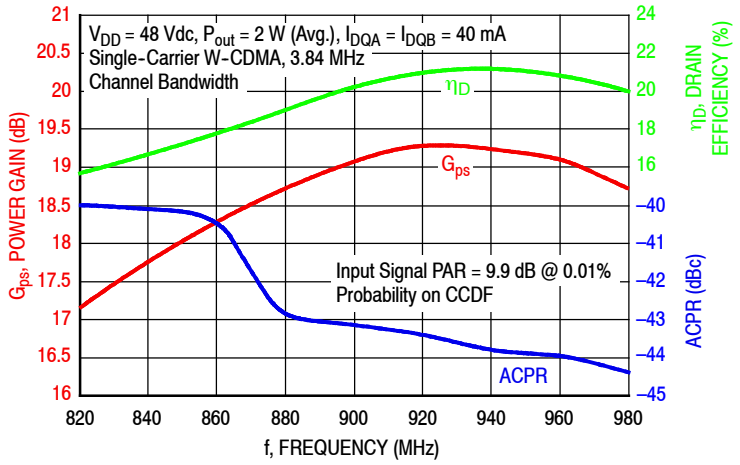


Figure 4. Broadband Performance @ P_{out} = 2 Watts Avg.

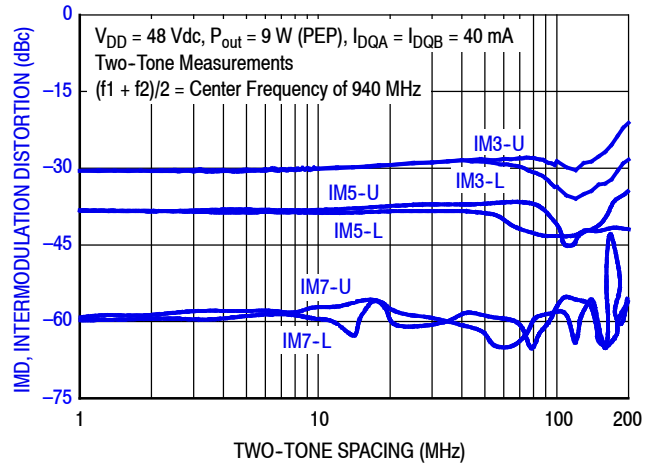


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

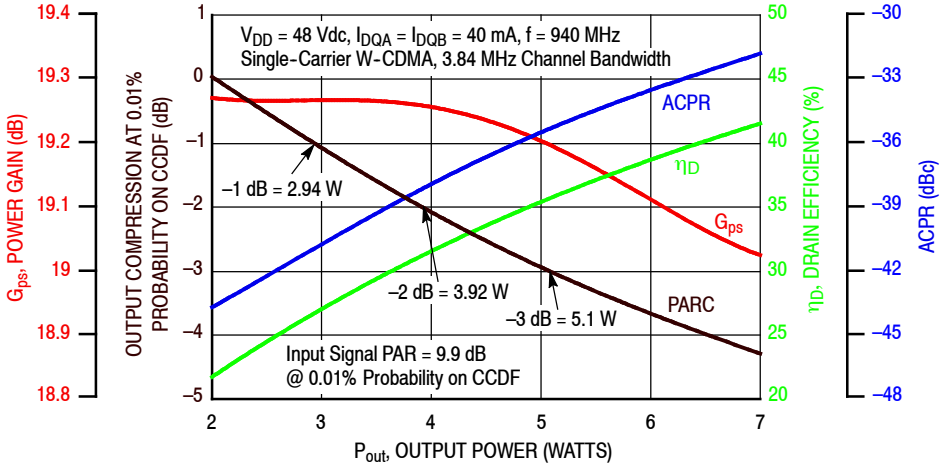


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

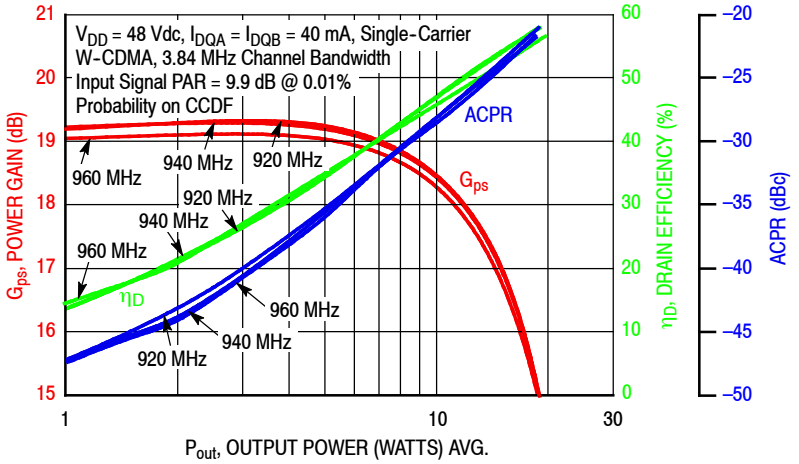


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

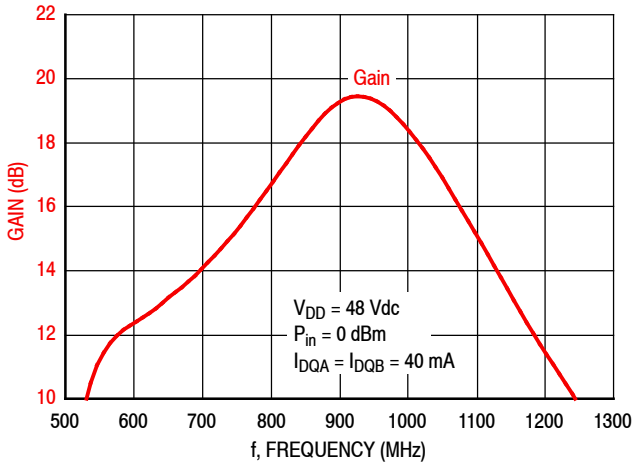


Figure 8. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 40 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	41.8 + j35.9	34.1 – j36.2	19.4 + j28.6	18.7	40.8	12	56.7	–7
940	33.0 + j36.5	31.9 – j33.8	24.2 + j26.5	18.7	41.2	13	61.8	–8
960	32.2 + j41.2	27.6 – j31.3	27.8 + j24.6	18.5	41.3	14	61.7	–9

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	41.8 + j35.9	34.8 – j35.7	25.0 + j28.7	16.7	41.8	15	63.3	–9
940	33.0 + j36.5	32.2 – j34.6	27.5 + j24.4	16.5	42.0	16	62.3	–10
960	32.2 + j41.2	27.4 – j32.2	30.3 + j23.1	16.3	42.0	16	62.4	–11

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 40 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	41.8 + j35.9	29.0 – j28.6	17.2 + j47.6	20.0	38.9	8	69.1	–9
940	33.0 + j36.5	27.8 – j29.3	18.5 + j42.2	19.9	39.6	9	70.9	–11
960	32.2 + j41.2	24.3 – j27.6	19.3 + j41.0	19.7	39.8	9	71.0	–12

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	41.8 + j35.9	31.3 – j31.3	21.2 + j45.2	17.8	40.5	11	72.3	–13
940	33.0 + j36.5	28.3 – j31.2	18.9 + j41.2	17.8	40.4	11	71.0	–15
960	32.2 + j41.2	24.5 – j29.3	19.8 + j39.3	17.6	40.6	11	70.7	–16

(1) Load impedance for optimum P1dB efficiency.

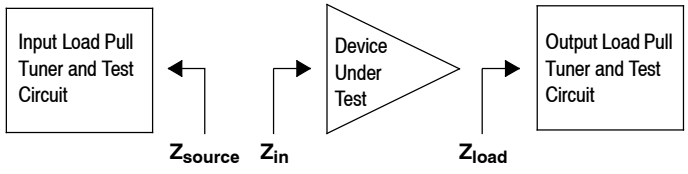
(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

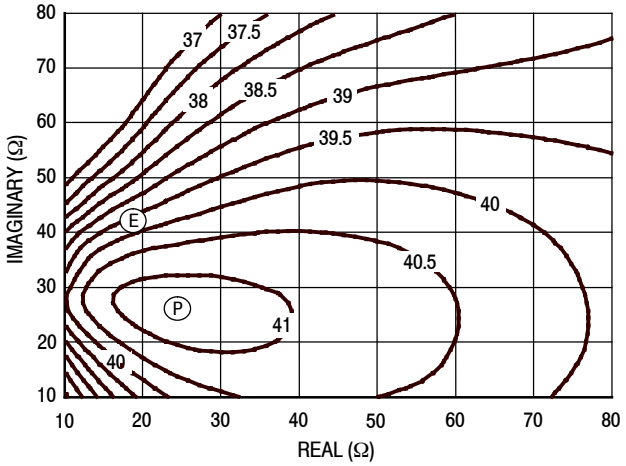


Figure 9. P1dB Load Pull Output Power Contours (dBm)

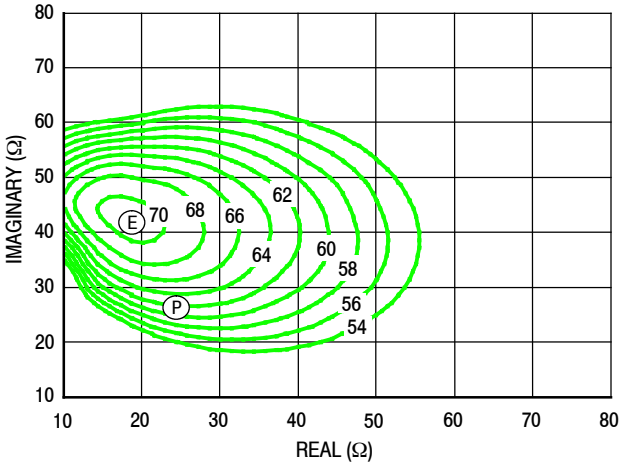


Figure 10. P1dB Load Pull Efficiency Contours (%)

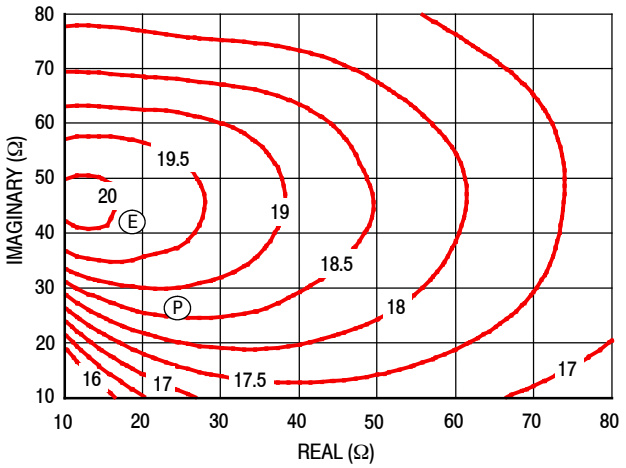


Figure 11. P1dB Load Pull Gain Contours (dB)

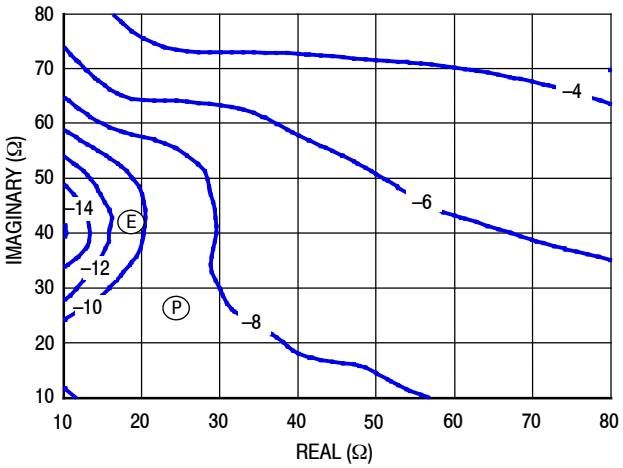


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

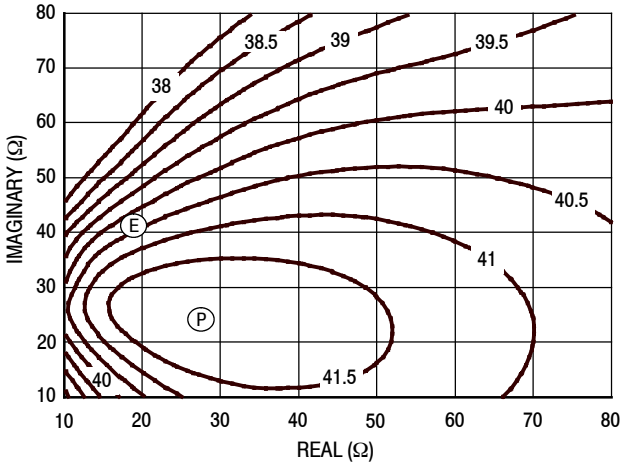


Figure 13. P3dB Load Pull Output Power Contours (dBm)

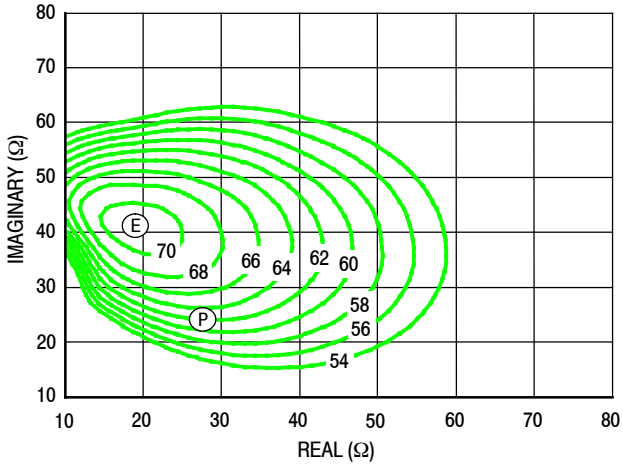


Figure 14. P3dB Load Pull Efficiency Contours (%)

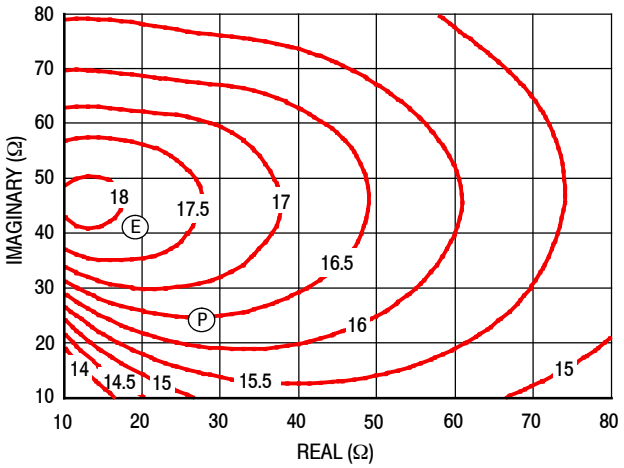


Figure 15. P3dB Load Pull Gain Contours (dB)

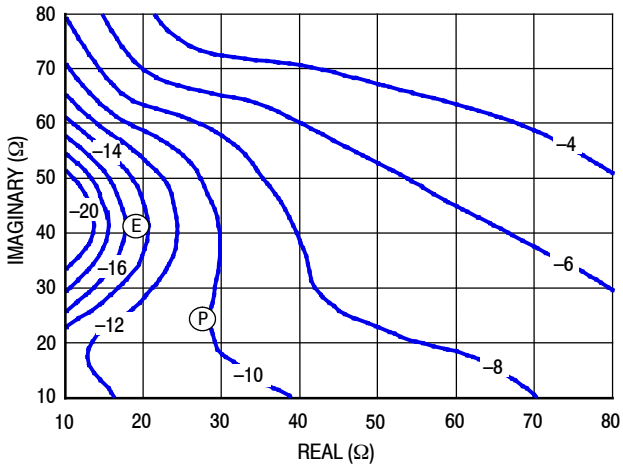


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

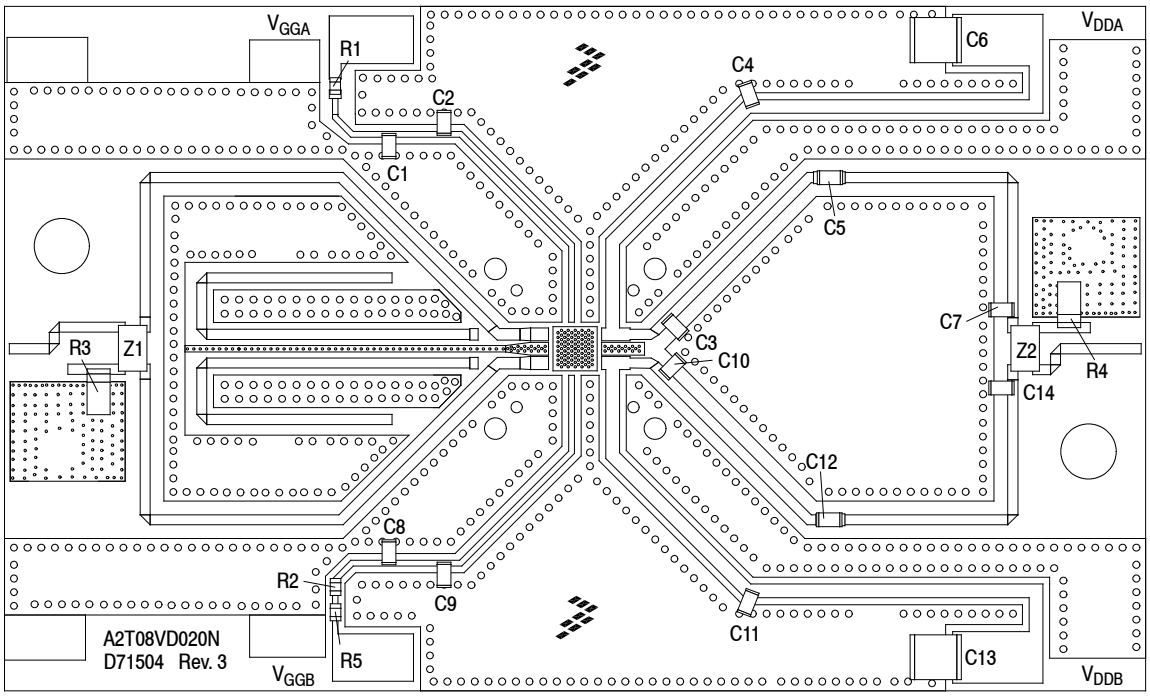


Figure 17. A2T08VD020NT1 Test Circuit Component Layout — 728–768 MHz

Table 10. A2T08VD020NT1 Test Circuit Component Designations and Values — 728–768 MHz

Part	Description	Part Number	Manufacturer
C1, C8	2.2 μF Chip Capacitors	C3225X7R0H225M	TDK
C2, C4, C5, C9, C11, C12	68 pF Chip Capacitors	ATC100B680JT500XT	ATC
C3, C7, C10, C14	3.9 pF Chip Capacitors	ATC100B3R9BT500XT	ATC
C6, C13	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
R1, R5	2 kΩ, 1/8 W Chip Resistors	SG73P2ATTD2001F	KOA Speer
R2	0 Ω, 1.5 A Chip Resistor	CWCR08050000Z0EA	Vishay
R3, R4	50 Ω, 10 W Chip Resistors	C8A50Z4A	Anaren
Z1, Z2	600–900 MHz Band, 90°, 3 dB Hybrid Couplers	X3C07F1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D71504	MTL

TYPICAL CHARACTERISTICS — 728–768 MHz

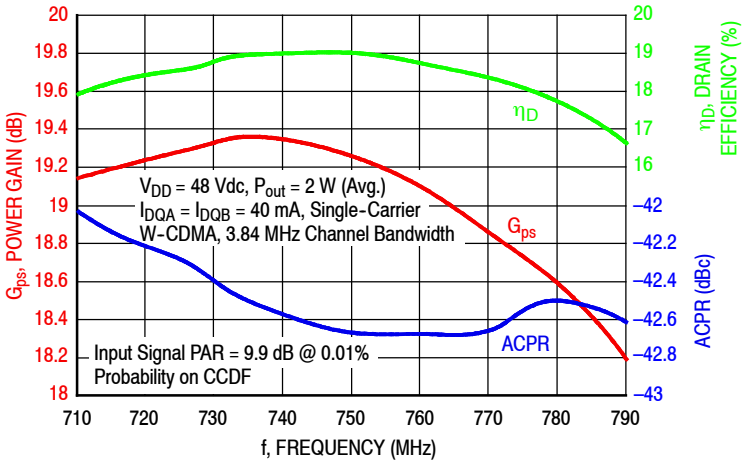


Figure 18. Broadband Performance @ P_{out} = 2 Watts Avg.

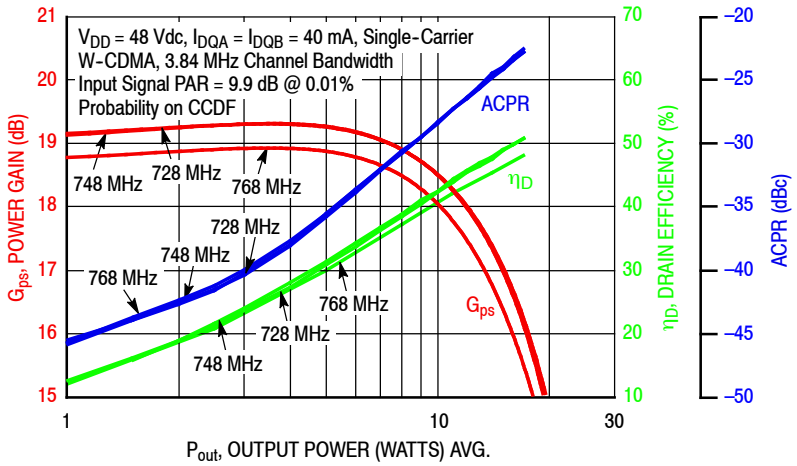


Figure 19. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

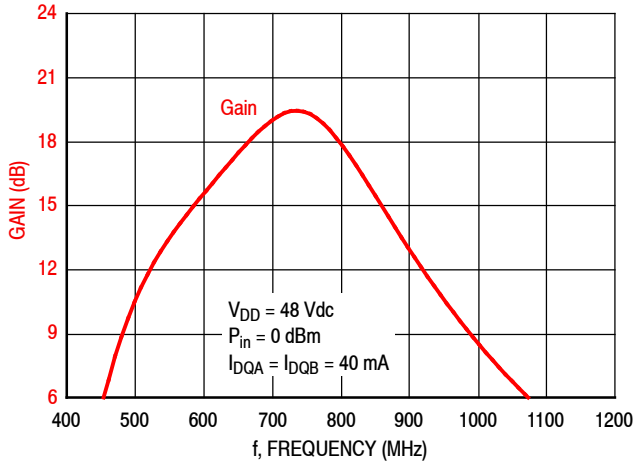


Figure 20. Broadband Frequency Response

Table 11. Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 40 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	46.6 – j11.0	61.7 + j5.77	40.4 + j26.1	19.0	41.2	13	60.7	–8
748	51.5 – j10.2	66.0 + j0.74	39.9 + j26.8	19.0	41.3	14	61.8	–8
768	51.6 – j5.44	67.2 – j4.42	39.7 + j24.8	18.8	41.4	14	61.5	–8

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	46.6 – j11.0	63.6 + j7.43	39.6 + j24.6	16.8	41.9	16	61.2	–9
748	51.5 – j10.2	68.6 + j2.36	39.5 + j24.5	16.8	42.0	16	62.0	–9
768	51.6 – j5.44	69.9 – j3.72	40.7 + j22.8	16.7	42.1	16	62.2	–9

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 12. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 40 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	46.6 – j11.0	61.8 – j9.22	31.6 + j57.1	20.5	39.4	9	71.4	–11
748	51.5 – j10.2	61.7 – j11.9	33.0 + j54.0	20.3	39.6	9	69.8	–10
768	51.6 – j5.44	59.9 – j14.8	33.7 + j51.8	20.2	39.8	9	69.4	–10

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	46.6 – j11.0	64.0 – j5.03	32.4 + j55.2	18.4	40.3	11	71.3	–13
748	51.5 – j10.2	65.2 – j9.06	33.6 + j52.7	18.3	40.4	11	69.8	–12
768	51.6 – j5.44	65.1 – j11.0	37.5 + j46.3	17.9	41.0	12	69.5	–11

(1) Load impedance for optimum P1dB efficiency.

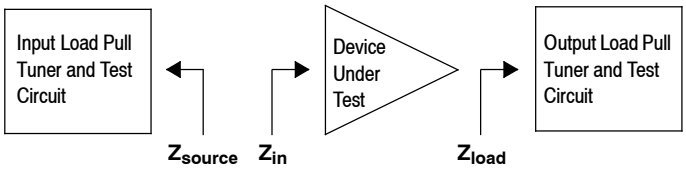
(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 748 MHz

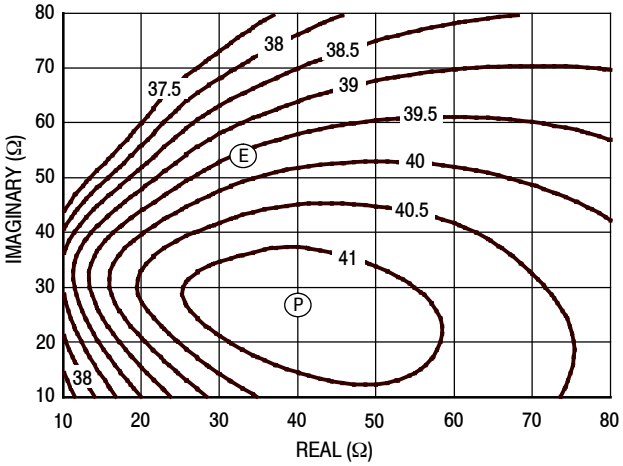


Figure 21. P1dB Load Pull Output Power Contours (dBm)

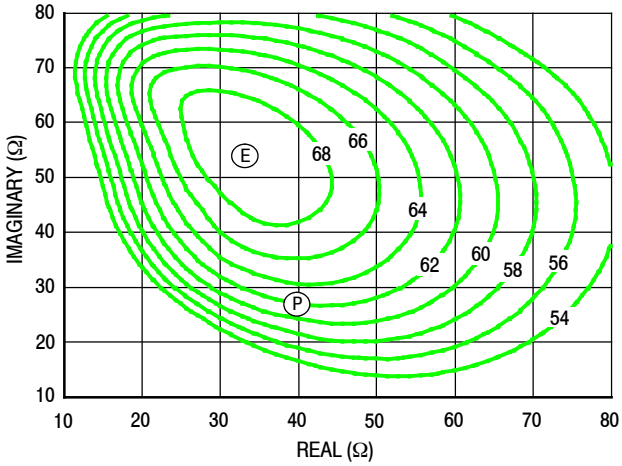


Figure 22. P1dB Load Pull Efficiency Contours (%)

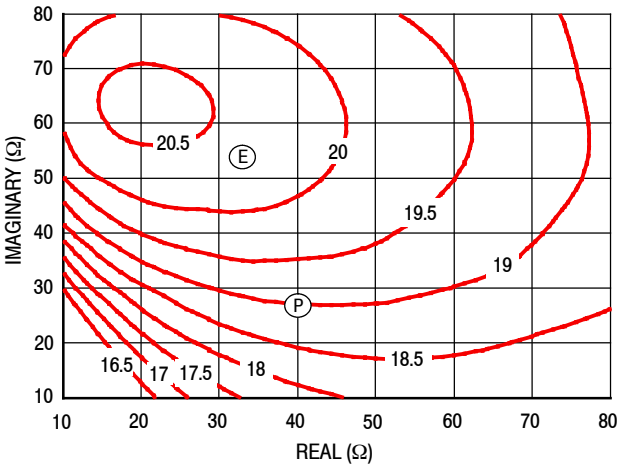


Figure 23. P1dB Load Pull Gain Contours (dB)

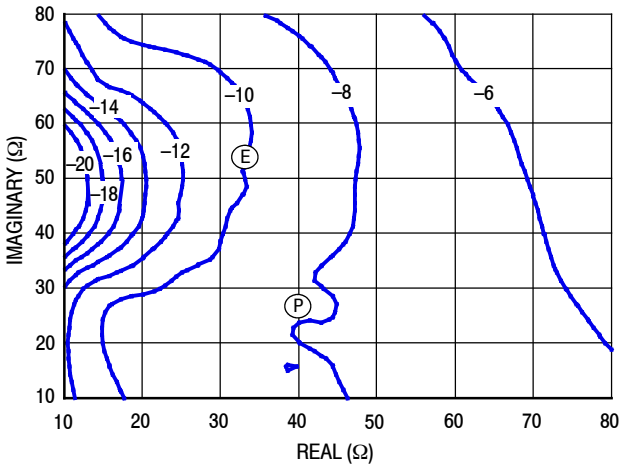


Figure 24. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 748 MHz

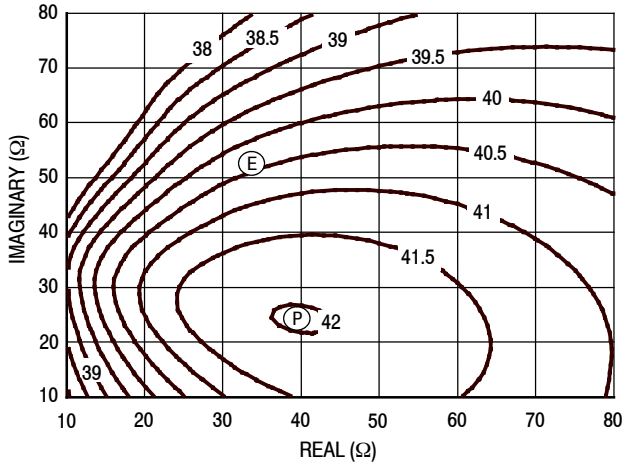


Figure 25. P3dB Load Pull Output Power Contours (dBm)

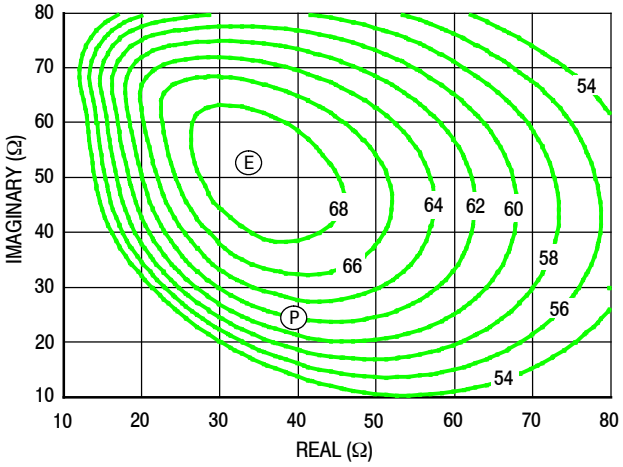


Figure 26. P3dB Load Pull Efficiency Contours (%)

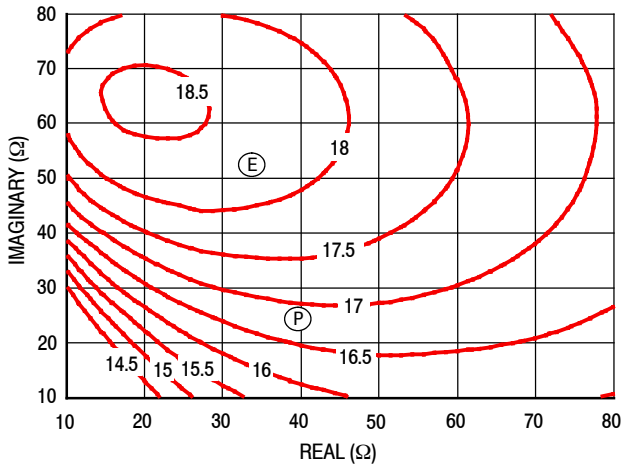


Figure 27. P3dB Load Pull Gain Contours (dB)

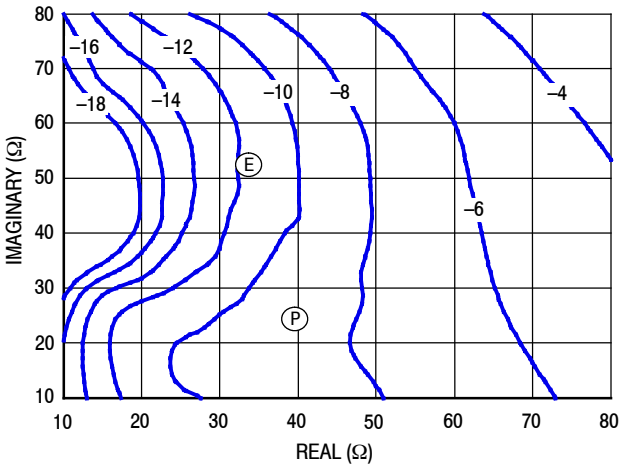


Figure 28. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

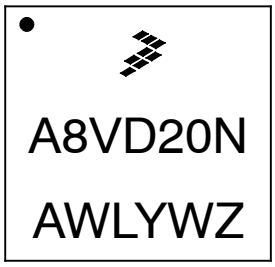
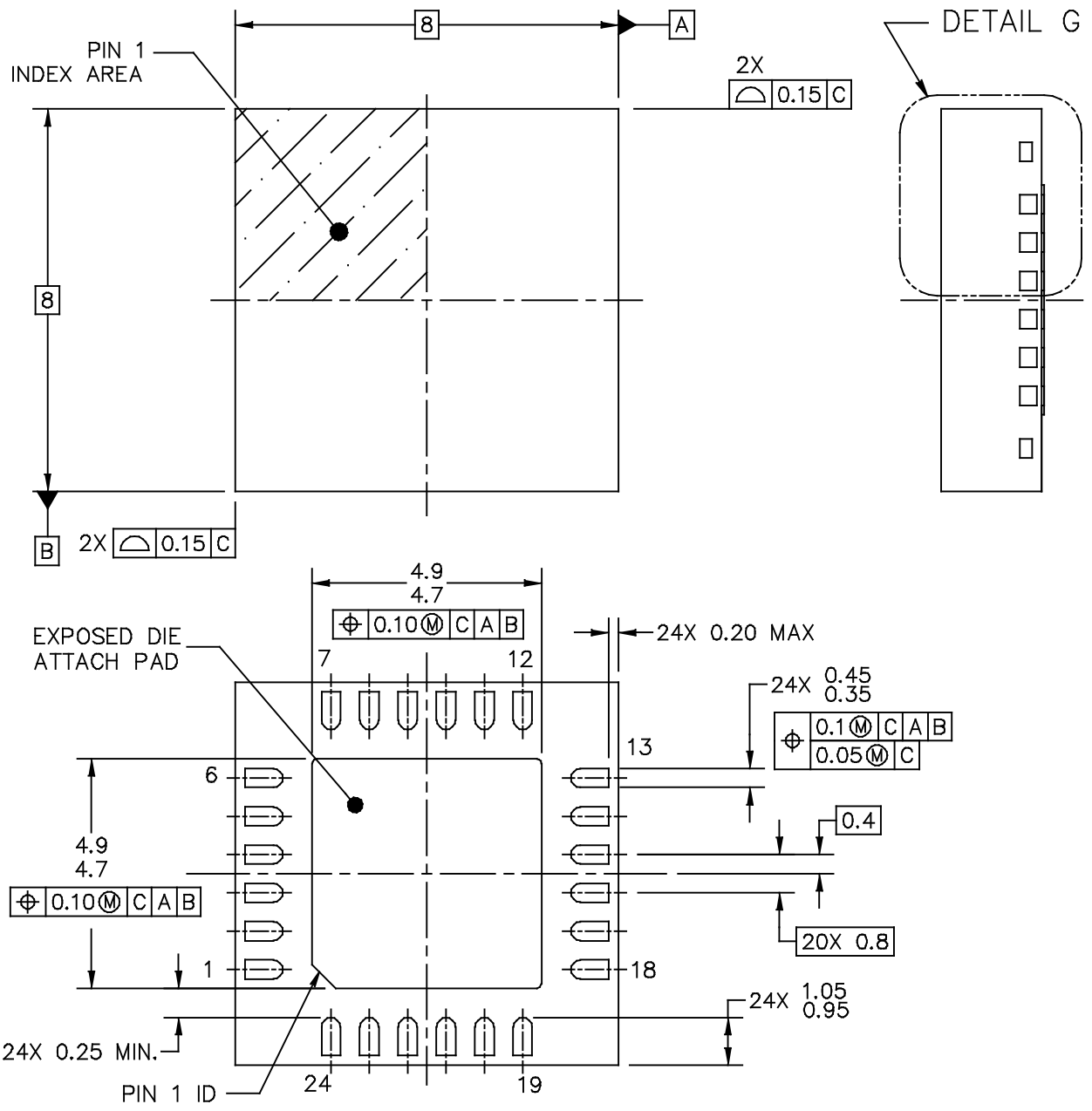


Figure 29. Product Marking

PACKAGE DIMENSIONS



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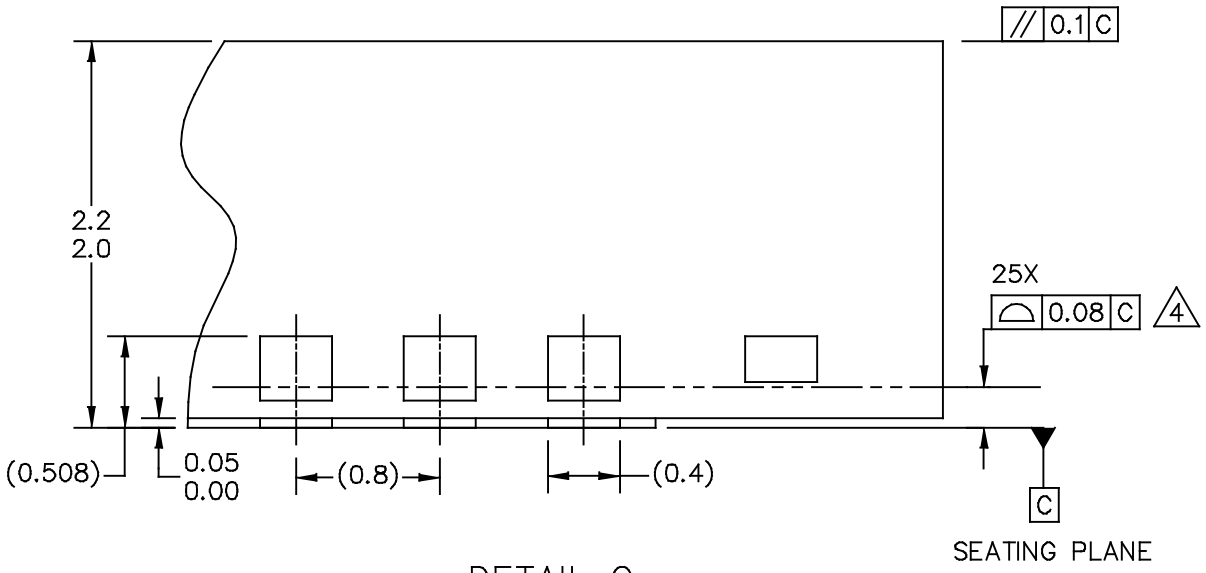
	SOT1664-1	11 MAR 2016



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	SOT1664-1	11 MAR 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2016	• Initial release of data sheet
1	May 2017	• Fig. 29, Product Marking: added product marking information to the data sheet, p. 15

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