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Data Sheet, Confidential

AS3517

Stereo Audio Codec with enhanced System Power Management

1 General Description

The AS3517 is a low power stereo audio codec and is designed for Portable Digital Audio Applications. It allows playback and recording in CD quality. It has a variety of audio inputs and outputs to directly connect electret microphones, 16Ω/32Ω headsets and auxiliary signal sources via a 10-channel mixer. It only consumes 20mW in playback mode.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player with flash or harddisk memory are supplied by the AS3517. The different regulated supply voltages are programmable via the serial control interface. The power management block generates 11 different supply voltages out of a single battery supply. CPU, NAND flash, SRAM, memory cards, harddisk, LCD, LCD backlight, USB-HOST and USB-OTG can be powered. AS3517 also contains a charger. The single supply voltage may vary from 3.0V to 5.5V.

The AS3517 has an on-chip, phase locked loop (PLL) controlled, clock generator. It generates 44.1kHz, 48kHz and other sample rates defined in MP3, AAC, WMA, OGG VORBIS etc. No additional external crystal or PLL is needed in slave mode. Further the AS3517 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU.

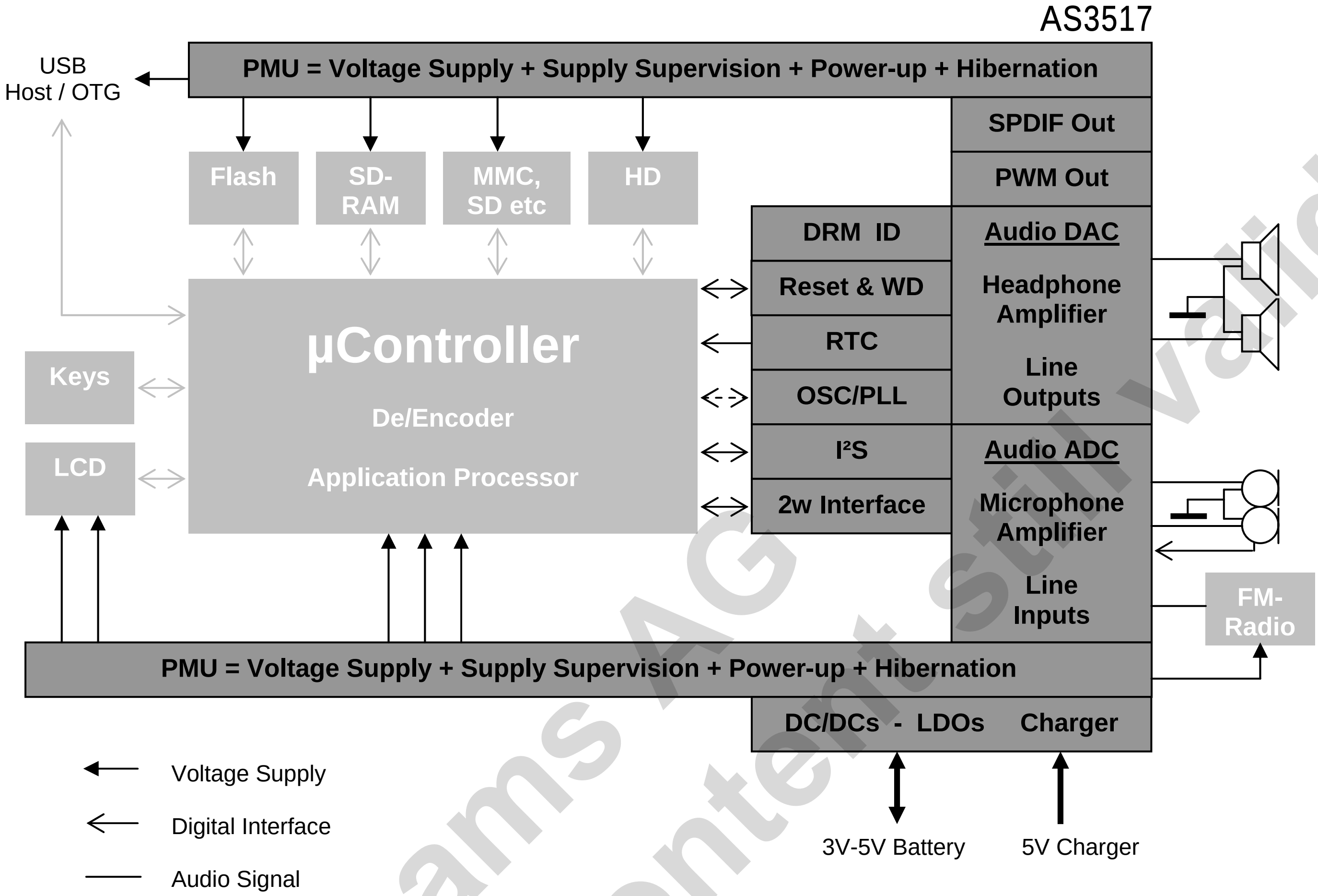
2 Key Features

- Multi-bit Sigma Delta Converters
  – DAC: 94dB SNR ('A' weighted) @ 2.9V
  – ADC: 90dB SNR ('A' weighted) @ 2.9V
  – Sampling Frequency: 8-48kHz
- 2 Microphone Inputs
  – 3 gain pre-setting (28dB/34dB/40dB) and AGC
  – 32 gain steps @1.5dB and MUTE
  – supply for electret microphone
  – microphone detection
  – remote control by switch
- 2 Line Inputs
  – volume control via serial interface
  – 32 steps @1.5dB and MUTE
  – stereo or 2x mono or mono differential
- Audio Mixer
  – 10 channel input/output mixer with AGC
  – mixes line inputs and microphones with DAC
  – left and right channels independent
- 2 Line Outputs
  – volume control via serial interface
  – 32 steps @1.5dB and MUTE
  – 1Vp @10kΩ
  – Stereo 2*5mW to 16ohm
  – Differential 10mW to 32ohm (earpiece)
- High Efficiency Headphone Amplifier
  – volume control via serial interface
  – 32 steps @1.5dB and MUTE
  – 2x60mW @16Ω driver capability
  – headphone and over-current detection
  – phantom ground eliminates large capacitors
- Power Management
  – step down for CPU core (0.65V-3.4V, 250mA)
  – step down for peripheral (0.65V-3.4V, 250mA)
  – step down for harddisk (0.65V-3.4V, 500mA)
  – step up for backlight (15V (25V), 38mA),
  – LDO for digital supply (2.9V, 200mA)
  – LDO for analog supply (2.9V, 200mA)
  – LDO for peripherals (1.2V-3.5V, 200mA)
  – LDO for peripherals (1.2V-3.5V, 200mA)
  – LDO for RTC (1.0V-2.5V, 2mA)
  – power supply supervision
  – hibernation modes
  – 5sec and 10sec emergency shut-down
- Battery Charger
  – automatic trickle charge (50mA)
  – prog. constant current charging (50-460mA)
  – prog. constant voltage charging (3.9V-4.25V)
- Real Time Clock
  – ultra low power 32kHz oscillator
  – 32bit RTC sec counter, 96 days auto wake-up
  – selectable alarm (seconds or minutes)
  – 128bit free SRAM for random settings
  – 32kHz clock output to peripheral
- Auxiliary Oscillator (only for master clock mode)
  – low power 12-24MHz oscillator
  – master clock input/output (e.g. from/to CPU)
- General Purpose ADC
  – 10bit resolution
  – 21 inputs analog multiplexer
- Interfaces
  – I²S digital audio interface and SPDIF
  – 2 wire serial control interface
  – reset pin, watchdog, power good pin
  – PWM output
  – 128bit unique ID (OTP)
  – 30 different interrupts
- Package CTBGA81 [9.0x9.0x1.15mm] 0.8mm pitch

3 Application

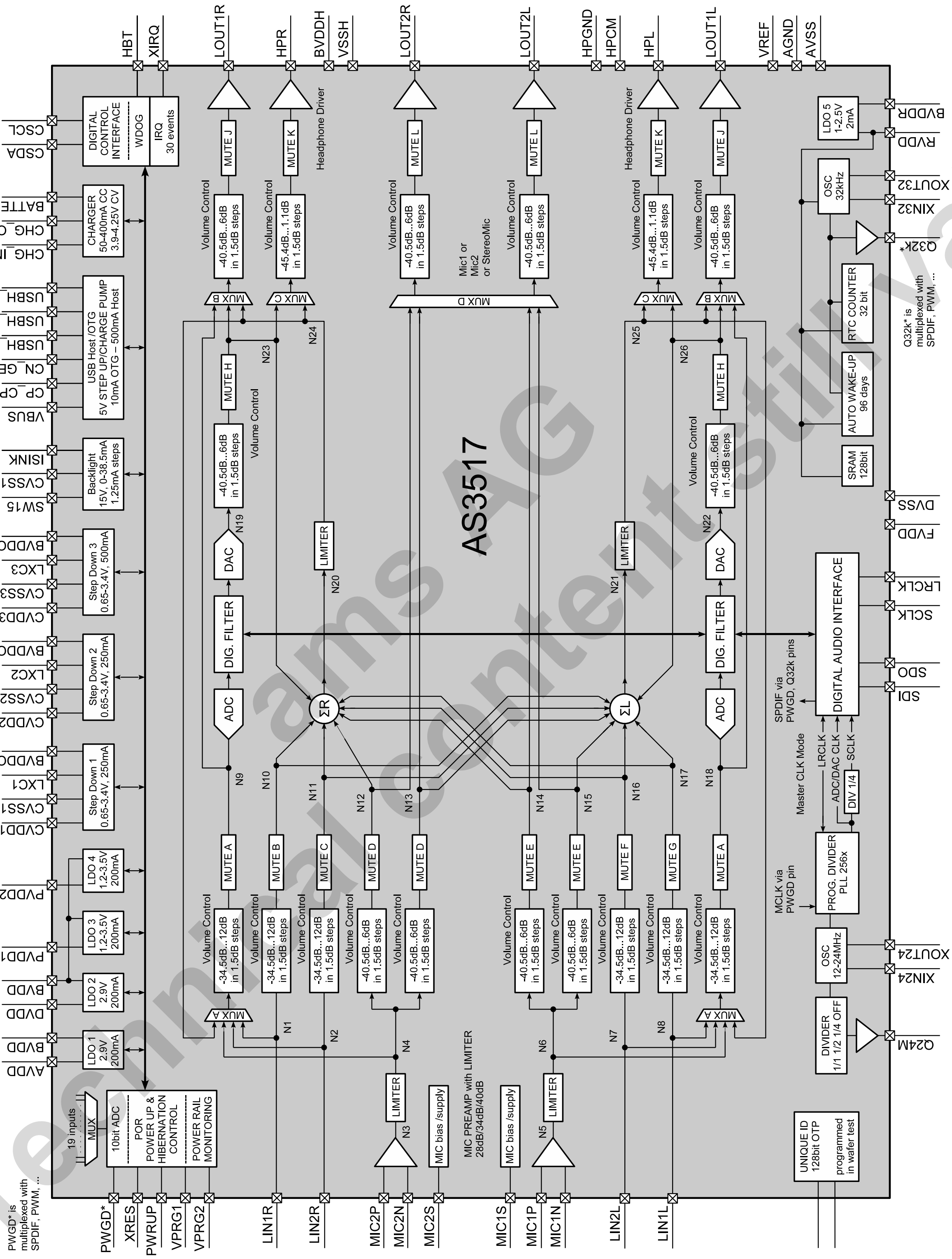
Portable Digital Audio Player and Recorder
PDA, Smartphone

4 Functional Overview



5 Block Diagram

Figure 1 AS3517 Block Diagram



Contents

Revision History

Revision	Date	Owner	Description
0.99	6.10.2006	pkm	Corrected version
1.0	12.10.2006	pkm	Changed block diagram of DCDC15
			Inserted register overview
			Corrected some typos
1.1	26.1.2007	pkm	Corrected block diagram (DAC mute)
			Corrected start-up sequence (VPROG1 and VPROG2 exchange)
1.2	6.4.2007	pkm	Added Typical Application Information
			Changed chip version for V17
			RTCT register reset corrected to RVDD-POR
			USB & CHGIN 0ms de-bounce time changed to 8ms
1.3	24.9.2008	pkm	Updated marking and ordering information

6 Pinout and Packaging

6.1 Pin Description

Table 1 Pinlist CTBGA81

Ball	PinName	Type	Function
G7	AGND	Analog I/O	Analog Reference Voltage (AVDD/2) buffer cap terminal
H7	AVDD	Supply	Analog Circuit VDD, connected to LDO1 on BGA substrate
J9	AVSS	Supply	Analog Circuit VSS
E2	BATTEMP	Analog I/O	Charger Battery Temperature Sensor input (100kΩ NTC)
D3	BVDD	Supply	Positive (Battery) Supply Terminal, 5.5V max.
E3	BVDD	Supply	Positive (Battery) Supply Terminal, 5.5V max.
B8	BVDDH	Supply	Positive (Battery) Supply Terminal of Headphone Amplifier, 5.5V max.
A8	BVDDC1	Supply	Positive (Battery) Supply Terminal of DCDC1, 5.5V max.
A4	BVDDC2	Supply	Positive (Battery) Supply Terminal of DCDC2, 5.5V max.
B4	BVDDC3	Supply	Positive (Battery) Supply Terminal of DCDC3, 5.5V max.
F2	BVDDR	Supply	RTC Positive (Battery) Supply terminal, 5.5V max
F1	CHG_IN	Analog Input	Charger Positive Supply Terminal, 5.5V max
E1	CHG_OUT	Analog Output	Charger Output prog. for Ichg 50-400mA or Vchg 3.9-4.25V
C1	CN_GEXT	Digital output	USB charge pump CN of flying cap / Output to control USB-Host DCDC N-Switch
C2	CP_CP	Digital output	USB charge pump CP of flying cap
G3	CSCL	Digital input with pull up	Clock Input of two wire interface
H3	CSDA	Digital I/O with pull up	Data I/O of two wire interface
B7	CVDD1	Analog Input	CVDD1 and Feedback pin
B5	CVDD2	Analog Input	CVDD2 and Feedback Pin
B3	CVDD3	Analog Input	CVDD3 and Feedback Pin
A6	CVSS1	Supply	CVDD1 StepDown Neg. Supply terminal
B6	CVSS2	Supply	CVDD2 StepDown Neg. Supply terminal
A2	CVSS3	Supply	CVDD3 Stepdown Neg. Supply terminal
B2	CVSS15	Supply	DCDC15V Neg. Supply terminal
G1	DVDD	Supply	Digital Circuit VDD, connected to LDO2 on BGA substrate
J2	DVSS	Supply	Digital Circuit VSS
H2	FVDD	Supply	ADC&DAC Digital Circuit VDD (1.8-3.6V)
F3	HBT	Digital input with pull down	Heartbeat Input for CPU supervision
C8	HPCM	Analog Output	Headphone Common GND Output for DC-coupled speakers
D9	HPGND	Analog I/O	Headphone Amplifier reference buffer cap terminal
A9	HPL	Analog Output	Headphone Amplifier Output Left Channel
C9	HPR	Analog Output	Headphone Amplifier Output Right Channel
B1	ISINK	Analog Output	DCDC15V Load Current Sink terminal (e.g. white LED)
D7	LIN1L	Analog Input	Line Input 1 Left Channel
D6	LIN1R	Analog Input	Line Input 1 Right Channel
F8	LIN2L	Analog Input	Line Input 2 Left Channel
F7	LIN2R	Analog Input	Line Input 2 Right Channel
C7	LOUT1L	Analog Output	Line Output Left Channel
C6	LOUT1R	Analog Output	Line Output Right Channel
D8	LOUT2L	Analog Output	Line Output Left Channel
E7	LOUT2R	Analog Output	Line Output Right Channel
G4	LRCLK	Digital I/O with pull down	I2S Left/Right Clock
A7	LXC1	Digital output	CVDD1 StepUp switch output to coil
A5	LXC2	Digital output	CVDD2 StepUp switch output to coil
A3	LXC3	Digital output	CVDD3 StepUp switch output to coil

Ball	PinName	Type	Function
H9	MIC1N	Analog Input	Microphone Input 1N
G9	MIC1P	Analog Input	Microphone Input 1P
G8	MIC1S	Analog I/O	Microphone Supply 1 (2.95V) / Remote Input 1
E9	MIC2N	Analog Input	Microphone Input 2N
F9	MIC2P	Analog Input	Microphone Input 2P
E8	MIC2S	Analog I/O	Microphone Supply 2 (2.95V) / Remote Input 2
D2	PVDD1	Analog Output	LDO3 Regulator Output
D1	PVDD2	Analog Output	LDO4 Regulator Output
F6	PWGD	Digital I/O multiplexed	Power Good, SPDIF, PLL clock, PWM digital output. Configurable as open drain or push pull. Master CLK digital input (e.g. from CPU)
J6	PWRUP	Digital input with pull down	Power Up input
J4	Q24M	Digital output multiplexed	12-24MHz Clock output, PLL clock. Configurable as open drain or push pull.
J3	Q32K	Digital output multiplexed	32kHz Clock output, SPDIF, PLL clock, PWM. Configurable as open drain or push pull.
G2	RVDD	Analog Output	RTC Supply Regulator Output prog. to 1.0-2.5V
F4	SCLK	Digital I/O with pull down	I2S Shift Clock
H4	SDI	Digital input with pull down	I2S Data Input to DAC
G5	SDO	Digital output	I2S Data output from ADC
A1	SW15	Analog Output	DCDC15V switch terminal
D4	USBH_CSN	Analog Input	USB-Host Step Up neg. Current sense terminal to 100mΩ resistor
C4	USBH_CSP	Analog Input	USB-Host Step Up pos. Current sense term. to 100mΩ resistor (BVDD)
C5	USBH_PG	Digital output	Output to control USB-Host DCDC high Side P-Switch
G6	VPRG1	Analog Input	5 State Prog Input to define power up sequence
H6	VPRG2	Analog Input	5 State Prog Input to define default regulator voltages
H8	VREF	Analog I/O	Analog Reference (filtered AVDD) decoupling cap terminal
C3	VBUS	Analog I/O	USB supply terminal for supervision and charge pump or StepUp feedback
B9	VSSH	Supply	Headphone Amplifier Neg. Supply terminal
J7	XIN24	Analog I/O	24MHz Oscillator Crystal terminal
H1	XIN32	Analog I/O	32kHz RTC Oscillator Crystal terminal
H5	XIRQ	Digital output	Interrupt Request Output. Configurable as open drain or push pull, active high or active low
J8	XOUT24	Analog I/O	24MHz Oscillator Crystal terminal
J1	XOUT32	Analog I/O	32kHz RTC Oscillator Crystal terminal
J5	XRES	Digital output open drain	Reset Output

6.2 Ball Assignment

6.2.1 CTBGA81

Figure 2 Ball Assignment CTBGA81

	1	2	3	4	5	6	7	8	9	
A	SW15	CVSS3	LXC3	BVDDC2	LXC2	CVSS1	LXC1	BVDDC1	HPL	A
B	ISINK	CVSS15	CVDD3	BVDDC3	CVDD2	CVSS2	CVDD1	BVDDH	VSSH	B
C	CN_GEXT	CP_CP	VBUS	USBH_CSP	USBH_PG	LOUT1R	LOUT1L	HPCM	HPR	C
D	PVDD2	PVDD1	BVDD	USBH_CSN	nc	LIN1R	LIN1L	LOUT2L	HPGND	D
E	CHG_OUT	BATTEMP	BVDD	nc	nc	nc	LOUT2R	MIC2S	MIC2N	E
F	CHG_IN	BVDDR	HBT	SCLK	nc	PWGD	LIN2R	LIN2L	MIC2P	F
G	DVDD	RVDD	CSCL	LRCLK	SDO	VPRG1	AGND	MIC1S	MIC1P	G
H	XIN32	FVDD	CSDA	SDI	XIRQ	VPRG2	AVDD	VREF	MIC1N	H
J	XOUT32	DVSS	Q32K	Q24M	XRES	PWRUP	XIN24	XOUT24	AVSS	J
	1	2	3	4	5	6	7	8	9	

6.3 Package Drawings

6.3.1 CTBGA81

Marking

Figure 3 CTBGA81 Marking

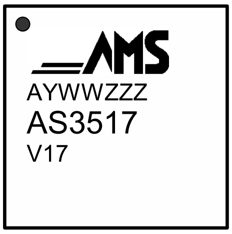
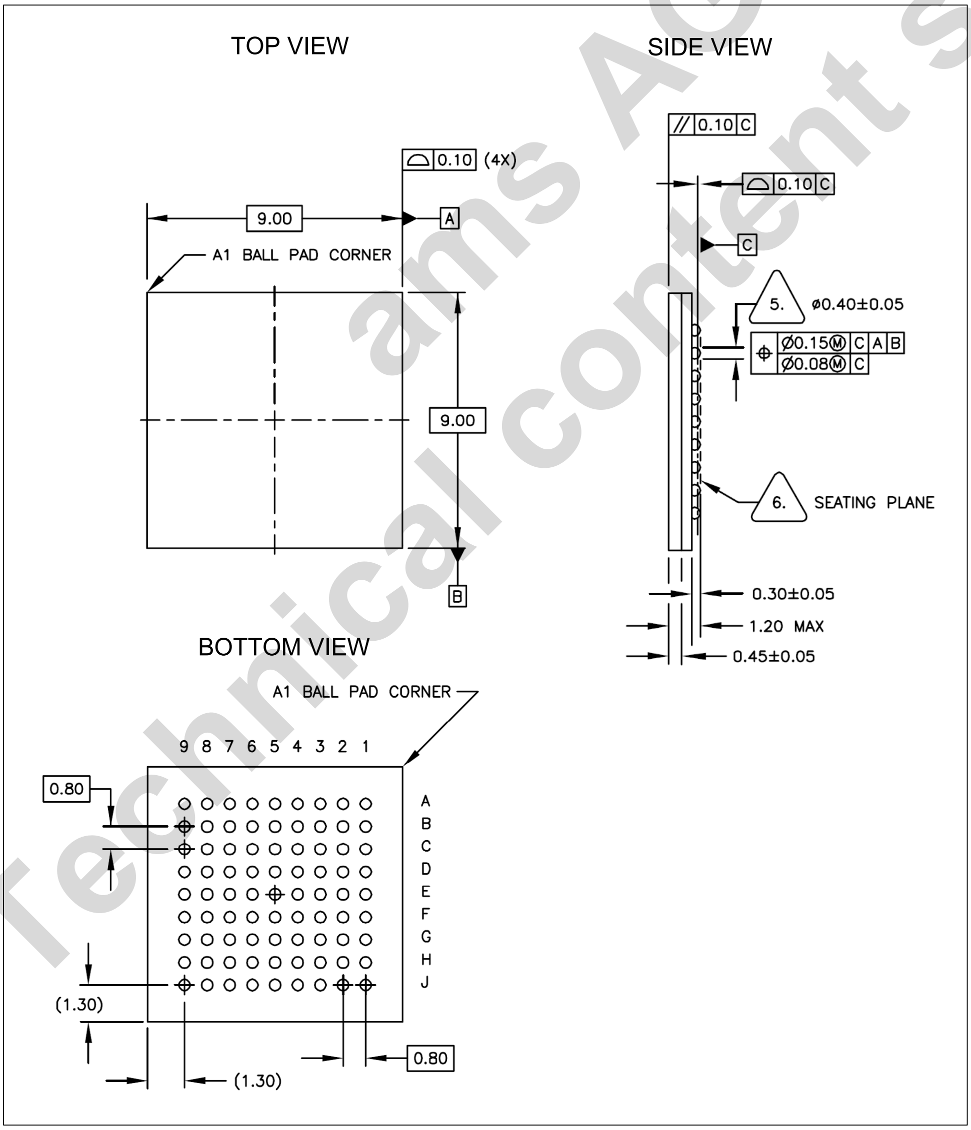


Table 2 Package Code AYWWZZZ

A	Y	WWW	ZZZ
A ... for PB free	Year	Working week assembly/packaging	Free choice

Dimensions

Figure 4 CTBGA81 9x9mm 0.8mm pitch



7 Ordering Information

Device ID	Version	Temperature Range	Package Type	Delivery Form
AS3517H-ECTP	V17	-20 to +85 °C	CTBGA81; 9x9mm package size, 0.8mm ball pitch	Tape & Reel DryPack
AS3517H-ECTS	V17	-20 to +85 °C	CTBGA81; 9x9mm package size, 0.8mm ball pitch	Tray DryPack

8 Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_5V}	5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDH, BVDDC1, BVDDC2, BVDDC3, BVDDR, CHG_IN, VBUS
V_{IN_SW15}	15V pin	-0.5	17	V	Applicable for pin SW15
V_{IN_VSS}	Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins CVSS3, CVSS15, CVSS1, CVSS2, VSSH, AVSS, DVSS
V_{IN_DVDD}	3.3V pins with diode to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins LRCK, SCLK, SDI, VPRG1, VPRG2, BATTEMP, ISINK, XIN32, XOUT32, XIN24, XOUT24, XIRQ, XRES, PWGD, Q32K, Q24M, HBT
V_{IN_xDVDD}	pins with no diode to DVDD	-0.5	7.0V	V	Applicable for pins CSCL, CSDA, PWRUP
V_{IN_AVDD}	3.3V pins with diode to AVDD	-0.5	5.0 AVDD+0.5	V	Applicable for pins HPCM, HPGND, LOUT1L/R, LOUT2L/R, VREF, AGND, LIN1L/R, LIN2L/R, MIC1P/N, MIC2P/N, MIC1S, MIC2S
V_{IN_REG}	voltage regulator pins with diodes to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD, DVDD, PVDD1/2, CVDD1/2/3, UVDD
V_{IN_RVDD}	voltage regulator pin with diode to BVDD	-0.5	3.6 BVDD+0.5	V	Applicable for pins RVDD
V_{IN_BVDD}	pins with diode to BVDD	-0.5	7.0 BVDD+0.5	V	Applicable for pins HPR/L, CHG_OUT
I_{scr}	Input Current (latchup immunity)	-100	100	mA	Norm: JEDEC 17
ESD	Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
P_t	Total Power Dissipation (all supplies and outputs)		1000	mW	BGA81, T_{amb}=70°C
H	Humidity non-condensing	5	85	%	

Table 4 Soldering Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_{body}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
T_{peak}	Solder Profile*	235	245	°C	
D_{well}		30	45	s	above 217 °C

* austriamicrosystems AG strongly recommends to use underfill.

8.1 Operating Conditions

8.1.1 Supply Voltages

Table 5 Operating conditions for supply voltages

Symbol	Parameter	Min	Max	Unit	Note
BVDDx	Battery Supply Voltage BVDD, BVDDH, BVDDC1, BVDDC2, BVDDC3, BVDDR	3.0	5.5	V	
VBUS	USB VBUS Voltage	4.0	5.5	V	
CHG_IN	Charger Supply Voltage	4.5	5.5	V	
DVDD	Digital Supply Voltage	2.8	3.6	V	Digital Audio Supply Voltage (LDO2)
AVDD	Analogue Supply Voltage	2.8	3.6	V	Analog Audio Supply Voltage (LDO1)
AGND	Analogue Ground Voltage		AVDD/2		
V_{DELTA-}	Difference of Negative Supplies CVSS1, CVSS2, CVSS3, CVSS15, VSSH, AVSS, DVSS	-0.1	0.1	V	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.
V_{DELTA+}	Difference of Positive Supplies	-0.25	0.25	V	AVDD-DVDD

Table 6 Electrical Specification of other function blocks

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{POR_ON}	Power-on Reset Activation Level		2.15		V	Power-on Reset activation level when DVDD decreases
V_{POR_OFF}	Power-on Reset Release Level		2.0		V	Power-on Reset release when DVDD increases
V_{POR_HY}	Power-on Hysterisis		100		mV	
f_{LRCLK_WD}	LRCLK Frequency Watchdog	2	4.1	8	kHz	
t_{ON_DELAY}	Delay Time of pin PWRUP		10		ms	Minimum key press time
V_{DO_L}	Digital Output Driver Capability (drive LOW)			0.3	V	Pins XRES, XIRQ, PWGD @ 8mA, SDO
V_{DO_H}	Digital Output Driver Capability (drive HIGH)	2.6			V	Pins XRES, XIRQ @ 8mA, push/pull mode only, SDO
I_{PU}	Internal Pull-up Current Source		10		µA	Pins XRES, XIRQ, PWGD
V_{PWRUP_L}	Digital Input Level LOW, BVDD>3V			0.5	V	Pin PWRUP
V_{PWRUP_H}	Digital Input Level HIGH, BVDD>3V	BVVD/3			V	Pin PWRUP
V_{PWRUP_H}	Digital Input Level HIGH, BVDD<=3V	1			V	Pin PWRUP
R_{PWRUP}	Internal Pull-down resistor		360		kΩ	Pin PWRUP
V_{DI_L}	Digital Input Level LOW		DVDD/2 *0.3	0.42	V	Pin HBT, SDI, SCLK, MCLK, LRCK
V_{DI_H}	Digital Input Level HIGH	1.02	DVDD/2 *0.7		V	Pin HBT, SDI, SCLK, MCLK, LRCK
I_{PD}	Internal Pull-down current source		10		µA	Pin HBT
f_{CLK}	Audio Clock Frequency	8		48	kHz	LRCK according to streamed audio data

8.1.2 Operating Currents

Table 7 Supply currents

Symbol	Parameter	Typ	Max	Unit	Note
I_{HPH}	Headphone current from BVDDH	1		mA	quiescent current, no load
$I_{DAC->HP}$	DAC playback current	6.4		mA	no load, including PMU
$I_{Line->HP}$	Line Input playback current	1.9		mA	no load, including PMU

8.1.3 Temperature Range

Table 8 Temperature Range

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{amb}	Operating temperature range	-20	25	85	°C	
T_j	Junction temperature range	0		110	°C	
R_{th}	Thermal Resistance		39		°C/W	For CTBGA81 package

8.1.4 Audio Specification

Table 9 Audio Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
DAC Input to Line Output						
FS	Full Scale Output		0.97		V_{RMS}	1kHz FS input
SNR	Signal to Noise Ratio		91		dB	A-weighted, no load, silence input
DR	Dynamic Range		88		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-90		dB	1kHz FS input
SINAD	Signal to Noise and Distortion		85		dB	A-weighted, 1kHz FS input
Line Input to Line Output						
FS	Full Scale Output		0.96		V_{RMS}	1kHz 1V_{RMS} (FS) input
SNR	Signal to Noise Ratio		92		dB	A-weighted, no load, silence input
THD	Total Harmonic Distortion		-90		dB	1kHz 1V_{RMS} (FS) input
SINAD	Signal to Noise and Distortion		86		dB	A-weighted, 1kHz FS input
CS	Channel Separation		89		dB	
DAC Input to HP Output						
FS	Full Scale Output		0.895		V_{RMS}	R_L= 32Ω
			0.89		V_{RMS}	R_L= 16Ω
SNR	Signal to Noise Ratio		94		dB	A-weighted, no load, silence input
DR	Dynamic Range		90		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-95		dB	no load, 1kHz FS input
			-75		dB	Pout=20mW, R_L= 32Ω, f=1kHz FS input
			-69	-60	dB	Pout=40mW, R_L= 16Ω, f=1kHz FS input
SINAD	Signal to Noise and Distortion		91		dB	A-weighted, no load, 1kHz FS input
			73		dB	A-weighted,Pout=20mW, R_L= 32Ω, f=1kHz FS input
			68		dB	A-weighted,Pout=40mW, R_L= 16Ω, f=1kHz FS input
CS	Channel Separation		74		dB	R_L = 32Ω
			68		dB	R_L = 16Ω
Line Input to HP Output						
FS	Full Scale Output		0.875		V_{RMS}	R_L= 32Ω, 1kHz 1V_{RMS}(FS) input
			0.87		V_{RMS}	R_L= 16Ω, 1kHz 1V_{RMS} (FS) input
SNR	Signal to Noise Ratio		95		dB	A-weighted, no load, silence input
DR	Dynamic Range		95		dB	A-weighted, no load, -60dB FS 1kHz (FS) input
THD	Total Harmonic Distortion		-91		dB	no load, 1kHz 1V_{RMS} input
			-75		dB	Pout=20mW, R=32Ω, 1kHz 1V_{RMS} (FS) input
			-70	-60	dB	Pout=40mW, R=16Ω, 1kHz 1V_{RMS} (FS) input
SINAD	Signal to Noise and Distortion		87		dB	A-weighted, no load, 1kHz 1V_{RMS} input

Symbol	Parameter	Min	Typ	Max	Unit	Note
			74		dB	A-weighted, Pout=20mW, R=32Ω, 1kHz $1V_{RMS}$ (FS) input
			68		dB	A-weighted, Pout=40mW, R=16Ω, 1kHz $1V_{RMS}$ (FS) input
CS	Channel Separation		75		dB	R_L = 32Ω
			70		dB	R_L = 16Ω
MIC Input to Line Output						
FS	Full Scale Output		0.97		V_{RMS}	1kHz FS input
SNR	Signal to Noise Ratio		81		dB	A-weighted, no load, silence input
DR	Dynamic Range		83		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-78		dB	1kHz $27mV_{RMS}$ (-3dB FS) input
SINAD	Signal to Noise and Distortion		75		dB	A-weighted, 1kHz $27mV_{RMS}$ (-3dB FS) input
Line Input to ADC Output						
SNR	Signal to Noise Ratio		90		dB	A-weighted, no load, silence input
DR	Dynamic Range		90		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-78		dB	1kHz $1V_{RMS}$ (-3dB FS) input
SINAD	Signal to Noise and Distortion		78		dB	A-weighted, 1kHz $1V_{RMS}$ (-3dB FS) input

9 Detailed Functional Description

9.1 Audio Functions

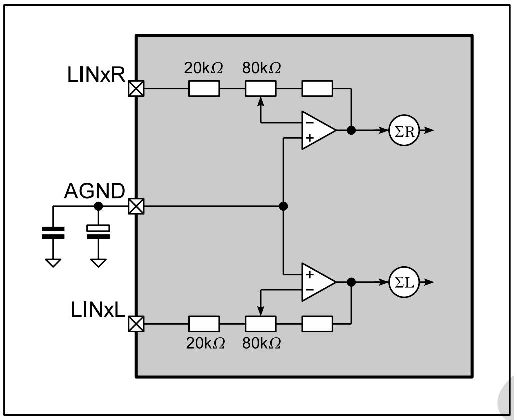
9.1.1 Audio Line Inputs (2x)

General

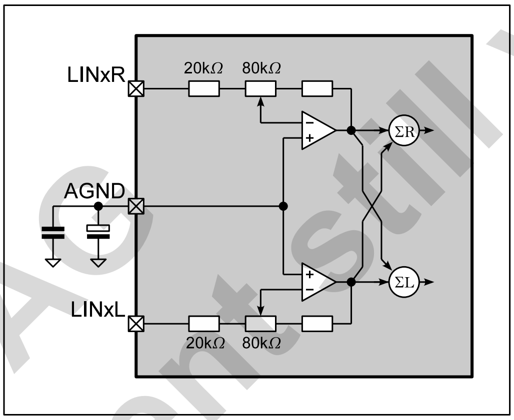
The chip features includes two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

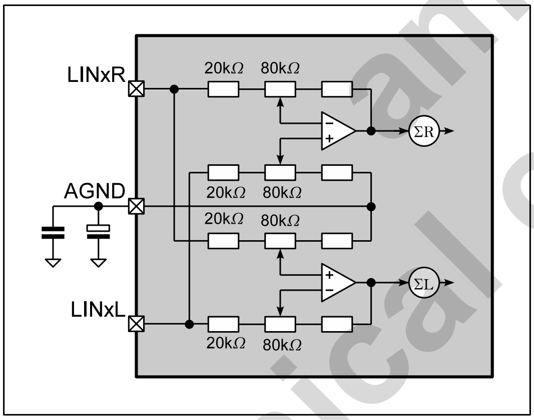
Figure 5 Line Inputs



Stereo Mode



Mono Single Ended Mode



Mono Differential Mode

Parameter

Table 10 Line Input Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{LIN}	Input Signal Level		1.0		V_{PEAK}	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD
R_{LIN}	Input Impedance		20-100		kΩ	depending on gain setting
ΔR_{LIN}	Input Impedance Tolerance		±15		%	
C_{LIN}	Input Capacitance		5		pF	
A_{LIN}	Programmable Gain	-34.5		+12	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
$A_{LINMUTE}$	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25°C, fs=48kHz unless otherwise mentioned

Register Description

Table 11 Line Input Related Register

Name	Base	Offset	Description
LINE_IN1_R	2-wire serial	0Ah	Right Line Input 1 settings
LINE_IN1_L	2-wire serial	0Bh	Left Line Input 1 settings
LINE_IN2_R	2-wire serial	0Ch	Right Line Input 2 settings
LINE_IN2_L	2-wire serial	0Dh	Left Line Input 2 settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

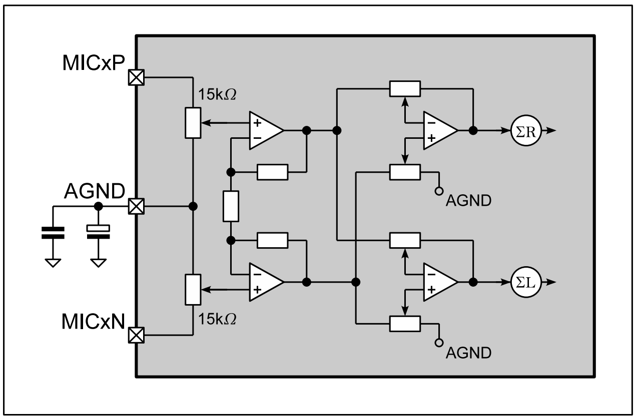
Line Inputs have to be enabled in register 14h first before other settings in register 0Ah to 0Dh can be programmed.

9.1.2 Microphone Inputs (2x)

General

The AFE offers two microphone inputs and 2 low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Figure 6 Microphone Input



Microphone Preamplifier and Gain Stage

Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electrete microphones signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPHCM. The supply is designed for ≤2mA and has a 10mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 30kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP–stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICxS terminals as ADC-10 input to monitor external voltages the 30kOhm pull-up can be disabled.

Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

Parameter

Table 12 Microphone Inputs Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{MICIN}0$	Input Signal Level		40		mV_{PEAK}	A_{MICPRE} = 28dB; A_{MIC} = 0dB
$V_{MICIN}1$			20		mV_{PEAK}	A_{MICPRE} = 34dB; A_{MIC} = 0dB
$V_{MICIN}2$			10		mV_{PEAK}	A_{MICPRE} = 40dB; A_{MIC} = 0dB
R_{MICIN}	Input Impedance		15		kΩ	MICP, MICN to AGND
Δ_{MICIN}	Input Impedance Tolerance		±15		%	
C_{MICIN}	Input Capacitance		5		pF	
A_{MICPRE}	Microphone Preamplifier Gain		28 34 40		dB dB dB	Preamplifier has 3 selectable (fixed) gain settings
A_{MIC}	Programmable Gain	-40.5		+6	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Precision		±0.25		dB	
$V_{MICLIMIT}$	Limiter Activation Level		1		V_{PEAK}	
$A_{MICLIMIT}$	Limiter Gain Overdrive		15*2		dB	
t_{ATTACK}	Limiter Attack Time		50		µs/6dB	
t_{DECAY}	Limiter Decay Time		120		ms/6dB	
$A_{MICMUTE}$	Mute Attenuation		100		dB	
V_{MICSUP}	Microphone Supply Voltage		2.9		V	
I_{MICMAX}	Max. Microphone Supply Current		10		mA	microphones nominally need a bias current of 0.5mA-1mA
V_{NOISE}	Microphone Supply Voltage Noise		5		µV	
I_{MICDET}	Microphone Detection Current		50		µA	
I_{REMDET}	Max. Remote Detection Current		500		µA	

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

Register Description

Table 13 Microphone Related Register

Name	Base	Offset	Description
MIC1_R	2-wire serial	06h	Right Microphone Input 1 volume settings, AGC control
MIC1_L	2-wire serial	07h	Left Microphone Input 1 volume settings, MIC 1 supply control
MIC2_R	2-wire serial	08h	Right Microphone Input 2 volume settings, AGC control
MIC2_L	2-wire serial	09h	Left Microphone Input 2 volume settings, MIC 2 supply control
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input
IRQ_ENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

Microphone inputs have to be enabled in register 14h first before other settings in register 06h to 09h can be programmed.

9.1.3 Audio Line Outputs (2x)

General

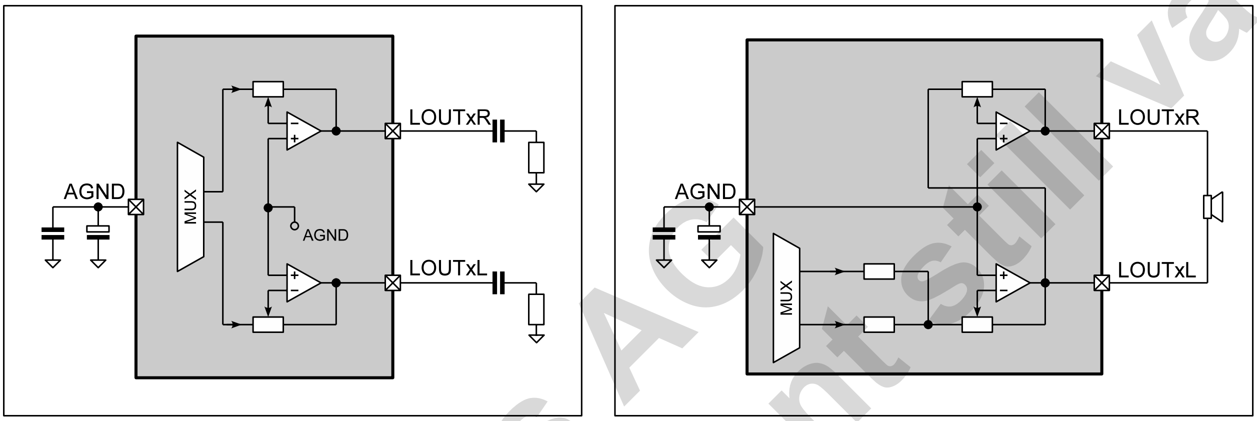
The line outputs are designed to provide the audio signal with typical $1V_{PEAK}$ at a load of minimum 10kΩ, which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is $1.45V_{PEAK}$. The load however can decrease to 64Ohm. In addition these line output can be configured as mono differential to drive $1V_{PEAK}$ @ 32Ω load (e.g. an earpiece of a mobile phone).

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. A zero cross detection allows to control the actual execution of new gain settings.

If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

If using the output in mono differential mode, the volume setting for the right channel should be set to 0dB.

Figure 7 Line Output



Stereo Mode

Mono Differential Mode (please observe that gain of right channel amplifier has to best to 0dB)

Parameter

Table 14 Line Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
R_{L_LO}	Load Impedance (Stereo Mode)	64			Ω	line inputs nominally have 10kΩ
C_{L_LO}	Load Capacitance (Stereo Mode)			100	pF	
A_{LO}	Programmable Gain	-40.5		+6	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
A_{LOMUTE}	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Register Description

Table 15 Line Output Related Register

Name	Base	Offset	Description
LINE_OUT1_R	2-wire serial	00h	Right Line Output 1 volume settings, MUX control
LINE_OUT1_L	2-wire serial	01h	Left Line Output 1 volume settings
LINE_OUT2_R	2-wire serial	04h	Right Line Output 2 volume settings, MUX control
LINE_OUT2_L	2-wire serial	05h	Left Line Output 2 volume settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

Line output have to be enabled in register 14h first before other settings in register 00h and 01h can be programmed.

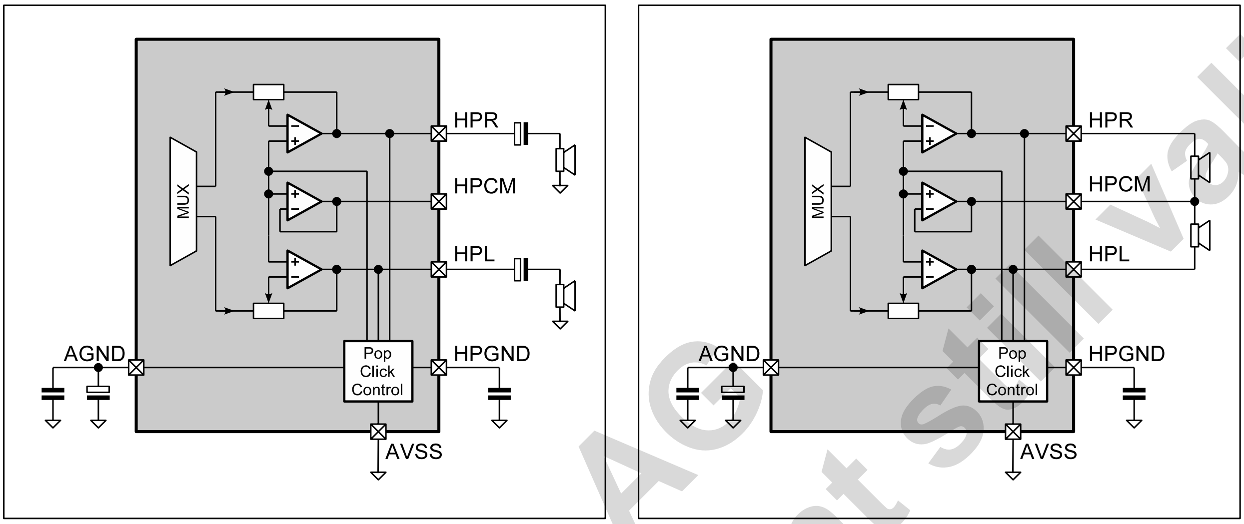
9.1.4 Headphone Output

General

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones. If the limiters (N20/N21) are disabled a maximum output of 2x60mW@16Ω or 2x30mW@32Ω can be achieved.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –43.43dB to +1.07dB. A zero cross detection allows to control the actual execution of new gain settings.

Figure 8 Headphone Output



Headphones connected via decoupling capacitors

Headphones connected to Phantom Ground (Common Mode)

Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc decoupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x100µF capacitors.

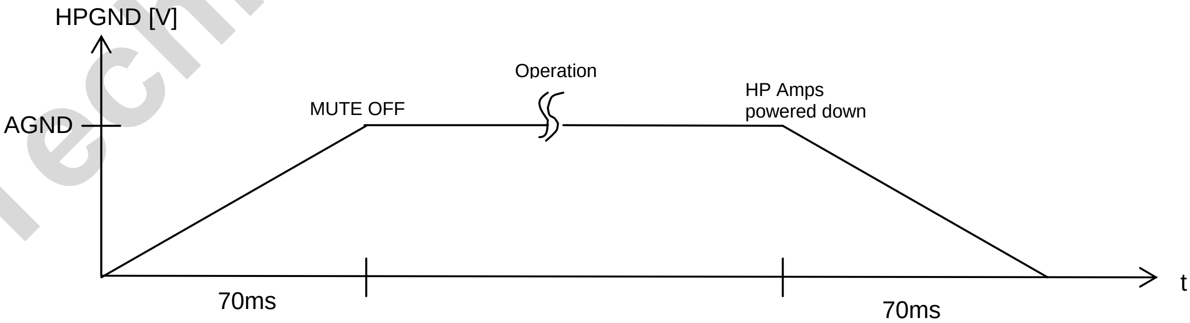
No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-1.45V-0V) at pins HPR/HPL is incorporated into the AFE. The 100nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 100nF buffer capacitor. To avoid Pop-Click noise one has to wait for 150ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

The output is automatically set to mute when the output stage is disabled.

Figure 9 HP POP-Click Suppression



Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power the headphone amplifier down for a programmable timeout period (512ms, 256ms, 128ms). The current threshold is at 150mA for HPR/HPL and 300mA for HPCM. There is a corresponding interrupt available to be enabled.

Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected. Together with switching off the phantom ground this gives 4 possible operating modes.

Table 16 Headphone Power-Save Options

HPCM_OFF	IBR_HPH	IDD_HPH (typ.)	Load
0	0	2.2mA	16 Ohm
1	0	1.5mA	16 Ohm
0	1	1.5mA	32 Ohm
1	1	1.0mA	32 Ohm

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Parameter

Table 17 Power Amplifier Block Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
R_{L_HP}	Load Impedance	16			Ω	stereo mode
C_{L_LO}	Load Capacitance			100	pF	stereo mode
P_{HP}	Nominal Output Power		40mW 20mW			RL=16Ω, limiter enabled RL=32Ω, limiter enabled
P_{HP_MAX}	Max. Output Power		60mW 30mW			RL=16Ω RL=32Ω
A_{LO}	Programmable Gain	-45.5		+1	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
	Over current limit		150 300		mA mA	HPR/HPL pins HPCM pin
P_{SRRHP}	Power Supply Rejection Ratio		90		dB	200Hz-20kHz, 720mVpp, RL=16Ω
A_{LOMUTE}	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Register Description

Table 18 Headphone Related Register

Name	Base	Offset	Description
HPH_OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
HPH_OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet_3	2-wire serial	16h	Power save options, common mode buffer
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

9.1.5 DAC, ADC and I2S Digital Audio Interface

Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCLK the alignment clock is input to the DAC digital filters. LRCLK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCLK are synchronous with SCLK. SDI is an inputs; LRCLK and SCLK are either inputs or outputs depending on the master/slave operation mode. SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the 20 bit ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCLK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCLK are synchronous with SCLK. SDO is an output; LRCLK and SCLK are either inputs or outputs depending on the master/slave operation mode. SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

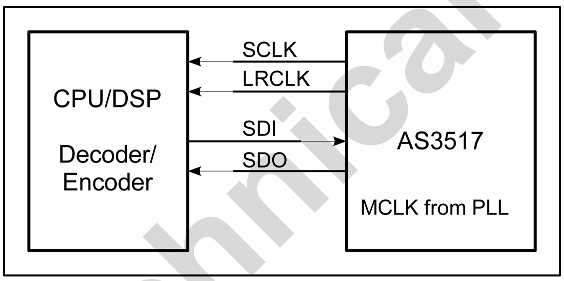
I2S Modes

The AFE can be operated either in Master Mode, Slave Mode or additionally in Slave Mode with the master clock directly signalled via pin PWGD (pin PWGD is multiplexed for I2S Direct Mode). The difference between Master and Slave Mode is whether the AFE or the externally attached decoder/encoder device is generating the interface clocks. The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g. 256*fs, fs=audio sampling frequency).

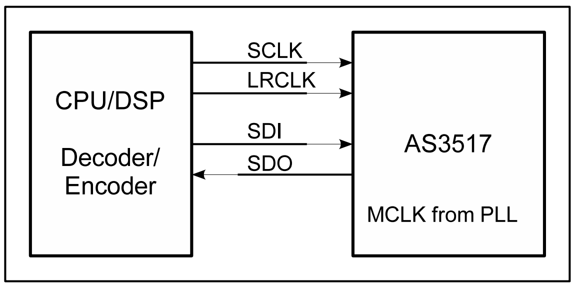
Due to the internal structure left and right audio samples are exchanged in I2S Direct Mode.

In Slave Mode the PLL generates the master clock based on LRCLK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-12kS (8kHz-12kHz) and 16kS-48kS (16kHz-48kHz). Please refer to register 0x1Dh.

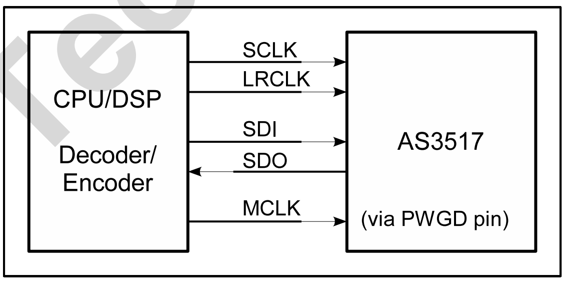
Table 19 I2S Modes



Master Mode



Slave Mode, internal PLL of the AFE generates MCLK



Slave Mode with I2S direct, the master clock is signalled via pin PWGD

Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption.

Clock Supervision

The digital audio interface automatically checks the LRCLK. An interrupt can be generated when the state of the LRCLK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCLK.

Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 20 bit. If more SCLK pulses are provided, only the first 20 will be significant. All following bits will be “0”.

SCLK has not to be necessarily synchronous to LRCLK but the high going edge has to be separate from LRCLK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCLK.

Please observe that in slave mode LRCLK has to be activated before enabling the ADC.

In Master Mode operation SCLK has 32 clock cycles for each sample word.

$$SCLK = \frac{MCLK}{4} = \frac{LRCLK * 256}{4} = LRCK * 64$$

Sample Rates

In Master Mode AS3517 allows programming various sample rates. The master clock is generated by the 12-24MHz oscillator. Sampling frequencies from 8kHz to 48kHz can be selected. For certain division ratios between master clock and sample ratio a certain deviation is system inherent.

$$LRCLK = f_{OSC} * \frac{1}{(PLLMode+1)*2} * \frac{1}{RD+2}$$

f_{osc} .... *Quarzoscillator frequency*

$PLLMode$ ...... *PLL factor* (1,2)

RD .... *RateDivider* (0 – 511)

Table 20Table 21 I2S Master clock PLL settings

f_{OSC}	fsample (LRCK)	PLL-Mode	RD (Rate Divider)	Deviation
24MHz	48.00kS	1	123	0.00%
24MHz	44.10kS	1	134	0.04%
24MHz	32.00kS	1	186	-0.27%
24MHz	24.00kS	1	248	0.00%
24MHz	22.05kS	1	270	0.04%
24MHz	16.00kS	1	373	0.00%
24MHz	12.00kS	2	248	0.00%
24MHz	11.025kS	2	270	0.04%
24MHz	8.00kS	2	373	0.00%
f_{OSC}	**fsample (LRCK)**	**PLL-Mode**	**RD (Rate Divider)**	**Deviation**
16MHz	48.00kS	1	81	0.40%
16MHz	44.10kS	1	179	-0.33%
16MHz	32.00kS	1	123	0.00%
16MHz	24.00kS	1	165	-0.20%
16MHz	22.05kS	1	179	0.22%
16MHz	16.00kS	1	248	0.00%
16MHz	12.00kS	2	165	-0.20%
16MHz	11.025kS	2	179	0.22%
16MHz	8.00kS	2	248	0.00%
f_{OSC}	**fsample (LRCK)**	**PLL-Mode**	**RD (Rate Divider)**	**Deviation**
12MHz	48.00kS	1	61	-0.79%
12MHz	44.10kS	1	66	0.04%
12MHz	32.00kS	1	92	0.27%
12MHz	24.00kS	1	123	0.00%
12MHz	22.05kS	1	134	0.04%
12MHz	16.00kS	1	185	0.27%
12MHz	12.00kS	2	123	0.00%
12MHz	11.025kS	2	134	0.04%
12MHz	8.00kS	2	185	0.27%

Parameter

Figure 10 I2S Left Justified Mode

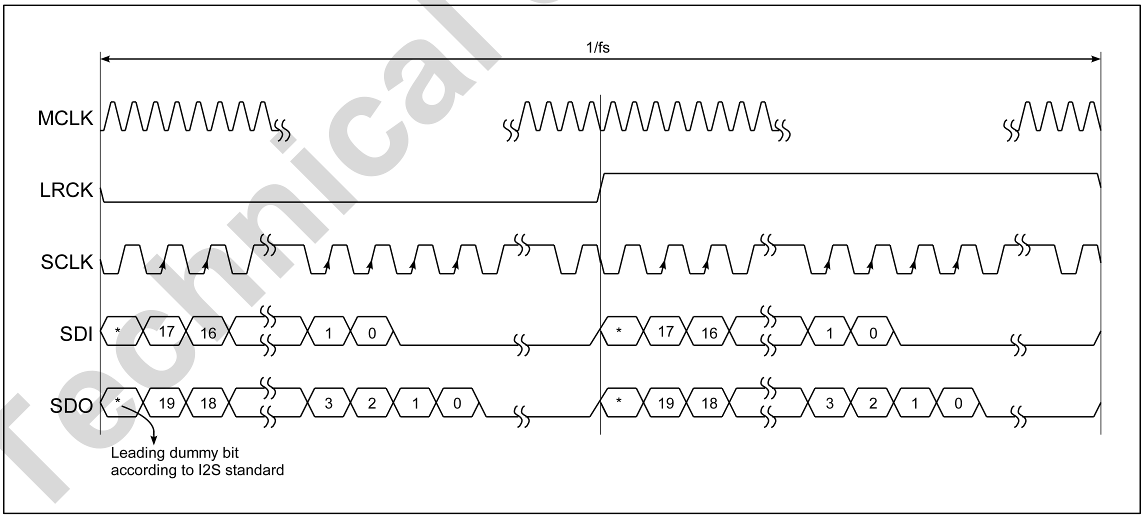


Figure 11 I2S Timing

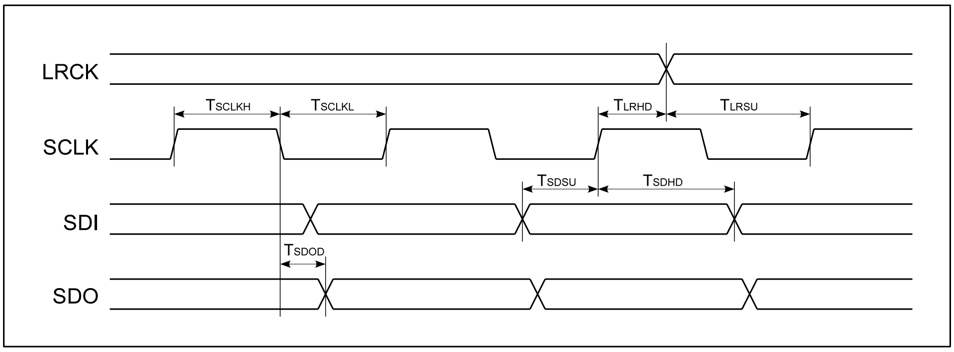


Table 22 Audio Converter Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{SCLK}	SCLK Cycle Time	160			ns	
t_{SCLKH}	SCLK Pulse Width High	80			ns	
t_{SCLKL}	SCLK Pulse Width Low	80			ns	
T_{LRSU}	LRCLK Setup Time before SCLK rising edge	80			ns	
T_{LRHD}	LRCLK Hold Time after SCLK rising edge	80			ns	
t_{SDSU}	SDI setup time before SCLK rising edge	25			ns	
t_{SDHD}	SDI hold time after SCLK rising edge	25			ns	
t_{SDOD}	SDO Delay from SCLK falling edge			25	ns	
t_{JITTER}	Jitter of LRCLK	-20		20	ns	internal PLL generates MCLK from LRCLK
I2S Direct mode						
T_{SCD}	SCLK delay after MCLK rising edge	0.5		1.5	ns	
T_{LRD}	LRLCK delay after SCLK rising edge	0.5		1.5	ns	
t_{SDSU}	SDI setup time before SCLK rising edge	5			ns	
t_{SDHD}	SDI hold time after SCLK rising edge	5			ns	
t_{SDOD}	SDO Delay from SCLK falling edge			15	ns	
V_{I2SH}	SCLK, LRCLK, SDI, MCLK High Input Level	1.02			V	DVDD/2*0.7
V_{I2SL}	SCLK, LRCLK, SDI, MCLK Low Input Level			0.42	V	DVDD/2*0.3
V_{SDOH}	SDO High Output Level	2.6			V	at 2mA
V_{SDOL}	SDO Low Output Level			0.3	V	at 2mA
V_{I2SOH}	SCLK, LRCLK, High Output Level	2.6			V	at 8mA master mode only
V_{I2SOL}	SCLK, LRCLK, Low Output Level			0.3	V	at 8mA master mode only

BVDD=3.3V, T_A=25°C, Slave Mode, fs=48kHz, MCLK = 256*fs, unless otherwise specified

Register Description

Table 23 Audio Converter Related Register

Name	Base	Offset	Description
DAC_R	2-wire serial	0Eh	DAC input volume settings
DAC_L	2-wire serial	0Fh	DAC input volume settings
ADC_R	2-wire serial	10h	ADC output volume settings, source multiplexer settings
ADC_L	2-wire serial	11h	ADC output volume settings
I2S	2-wire serial	1Eh	I2S master mode settings
I2S_PLL_OSC	2-wire serial	1Dh	I2S master mode and PLL settings
AudioSet_1	2-wire serial	14h	Enable/disable ADC
AudioSet_2	2-wire serial	15h	Enable/disable DAC and power save options
AudioSet_3	2-wire serial	16h	Enable/disable mixer input
IRQ_ENRD_1	2-wire serial	25h	Interrupt settings for LRCK changes

DAC and ADC have to be enabled in register 14h first before other settings in register 0Eh to 11h can be programmed.

9.1.6 Audio Output Mixer

General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1 & 2 (stereo microphone)
- Line Input 1
- Line Input 2
- Digital Audio Input (DAC)

The mixing ratios have to be with the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

Register Description

Audio Mixer Related Register

Name	Base	Offset	Description
AudioSet_2	2-wire serial	15h	Enable/disable mixer stage and AGC
AudioSet_3	2-wire serial	16h	Enable/disable DAC, MIC or Line Inputs to mixer stage

9.1.7 2-Wire-Serial Control Interface

General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Ch_write
- 8Dh_read

Protocol

Table 24 I2C Symbol Definitions

Symbol	Definition	R/W (AS3517 Slave)	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b 8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge
	AS3517 (=slave) receives data		
	AS3517 (=slave) transmits data		

Figure 12 Byte Write

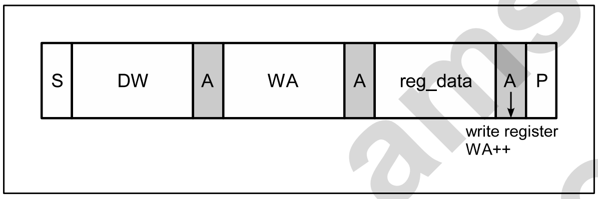
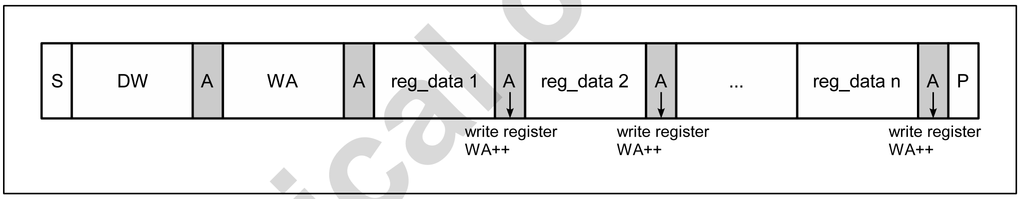


Figure 13 Page Write

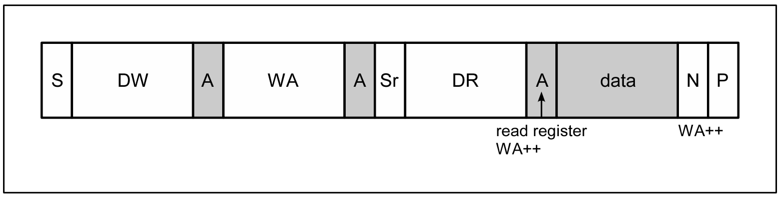


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 14 Random Read

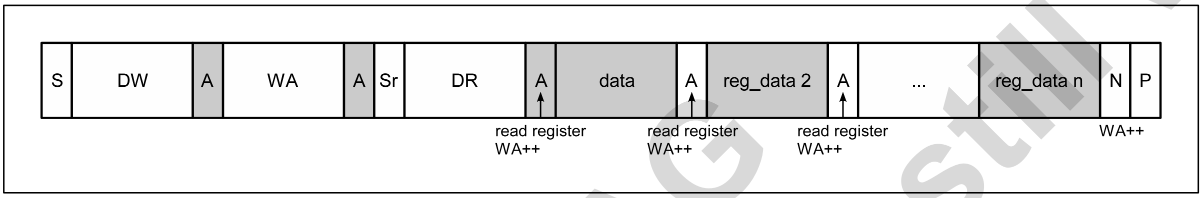


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

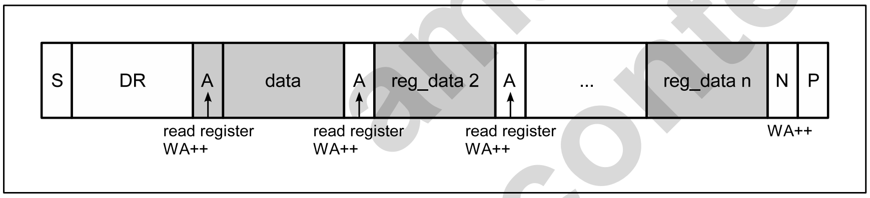
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 15 Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behaviour of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 16 Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

Parameter

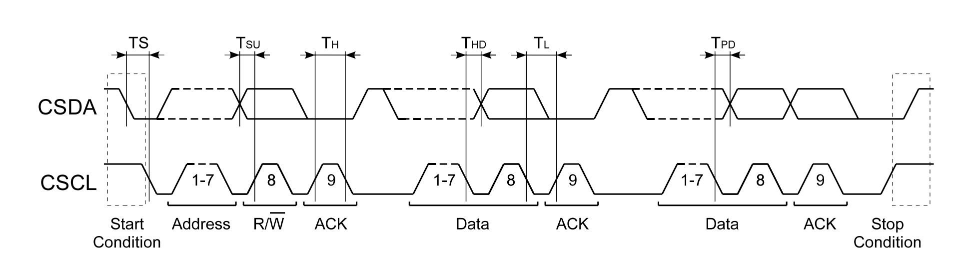


Figure 17 I2C timing

Table 25 I2C Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CSL}	CSCL, CSDA Low Input Level	0	-	0.87	V	(max 30%DVDD)
V_{CSH}	CSCL, CSDA High Input Level	2.03	-	5.5	V	CSCL, CSDA (min 70%DVDD)
HYST	CSCL, CSDA Input Hysteresis	200	450	800	mV	
V_{OL}	CSDA Low Output Level	-	-	0.4	V	at 3mA
Tsp	Spike insensitivity	50	100	-	ns	
T_H	Clock high time	500			ns	max. 400kHz clock speed
T_L	Clock low time	500			ns	max. 400kHz clock speed
T_{SU}		250	-	-	ns	CSDA has to change Tsetup before rising edge of CSCL
T_{HD}		0	-	-	ns	No hold time needed for CSDA relative to rising edge of CSCL
TS		200	-	-	ns	CSDA H hold time relative to CSDA edge for start/stop/rep_start
T_{PD}			50		ns	CSDA prop delay relative to lowgoing edge of CSCL

DVDD =2.9V, T_{amb}=25ºC; unless otherwise specified

9.2 Power Management Functions

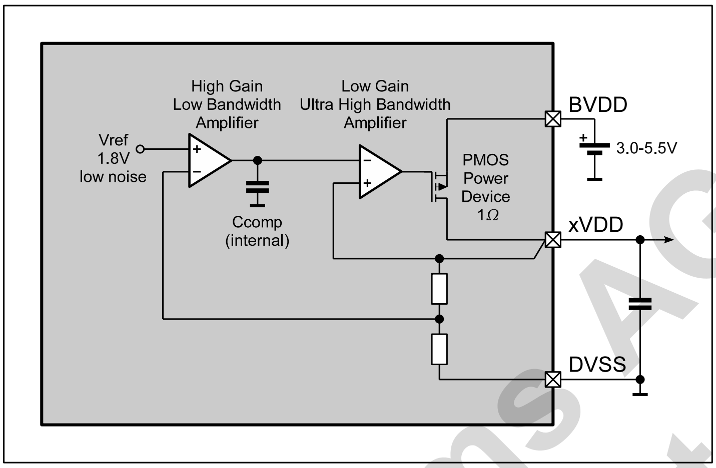
9.2.1 Low Drop Out Regulators

General

These LDO's are designed to supply sensitive analogue circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices.The design is optimised to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF +/-20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 18 LDO Block Diagram



LDO1

This LDO generates the analog supply voltage used for the AFE itself.

- Input voltage is BVDD
- Output voltage is AVDD (typ. 2.9V)
- Driver strength: 200mA

It is set to a fixed output voltage of 2.9V, 200mA$_{max}$. It supplies the analog part of the AFE. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the sensitive AVDD supply pin.

LDO2

This LDO generates the digital supply voltage used for the AFE itself.

- Input Voltage is BVDD
- Output Voltage is DVDD (typ. 2.9V)
- Driver strength: 200mA

It is set to a fixed output voltage of 2.9V, 200mA$_{max}$. It supplies the digital part of the AFE. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the DVDD supply pin but is not as critical as AVDD.

LDO3 & LDO4

These LDO can used to generate the periphery voltage for the digital processor or other external components (e.g. ext. DAC, USB-PHY, SD-Cards, NAND-Flashes, FM-Tuner ...)

- Input Voltage BVDD
- Output Voltage is PVDD1 & PVDD2 (1.2 to 3.5V)
- Default value at start-up is defined by VPROG1 and VPROG2 pins
- Driver strength: 200mA

Parameter

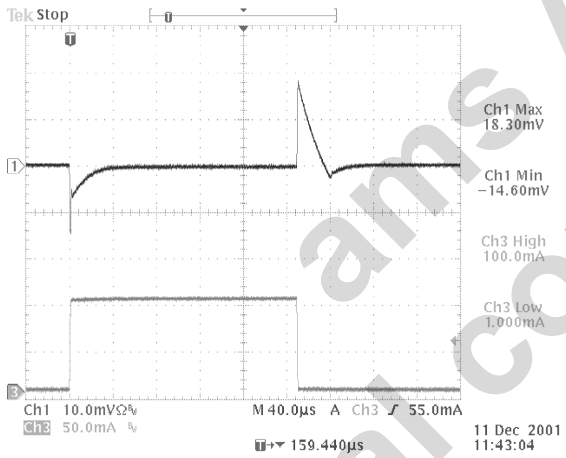
Table 26 LDOs Block Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
R_{ON}	On resistance			1	Ω	
PSRR	Power supply rejection ratio		70		dB	f=1kHz
			40		dB	f=100kHz
I_{OFF}	Shut down current		100		nA	
I_{VDD}	Supply current		50		µA	without load
Noise	Output noise		50		μV_{rms}	10Hz < f < 100kHz
t_{start}	Startup time		200		µs	
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation		<1		mV	LDO1, Static
			<10		mV	LDO1, Transient;Slope: t_r=10µs
$V_{LoadReg}$	Load regulation		<1		mV	LDO1, Static
			<10		mV	LDO1, Transient;Slope: t_r=10µs
I_{LIMIT}	Current limitation		400		mA	LDO1, LDO2, LDO3, LDO4

BVDD=4V; I_{LOAD}=150mA; T_{amb}=25ºC; C_{LOAD} =2.2µF (Ceramic); unless otherwise specified

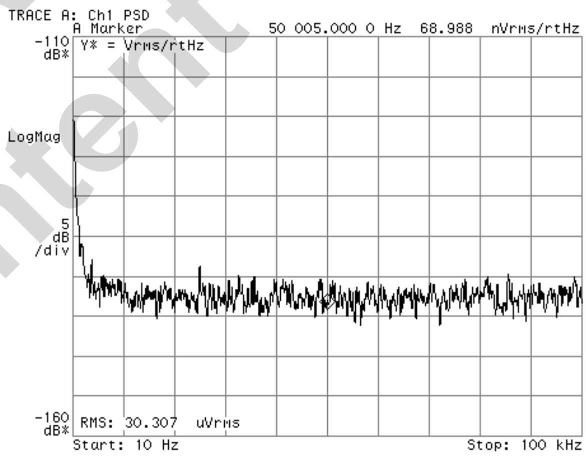
Figure 19 Typical Performance Characteristics

Load regulation



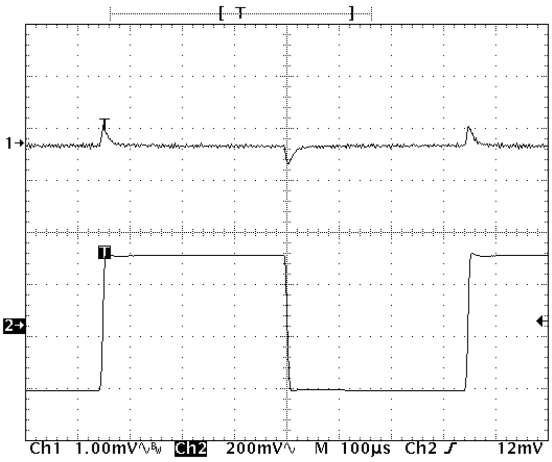
transient load: 1mA – 100mA
slope: 1µs

Output noise



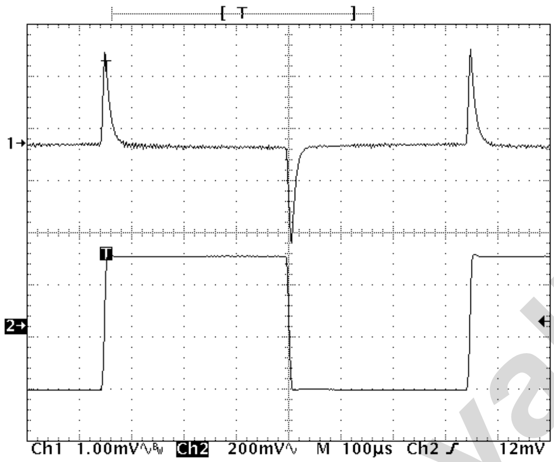
Output load: 150mA

Load Regulation



output load: 10mA
transient input voltage ripple: 500mV

Load Regulation



output load: 150mA
transient input voltage ripple: 500mV

Register Description

Table 27 LDO Related Register

Name	Base	Offset	Description
PMU PVDD1	2-wire serial	17h-1	PVDD1 (LDO3) control and voltage settings
PMU PVDD2	2-wire serial	17h-2	PVDD2 (LDO4) control and voltage settings
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 17h-1, 17h-2

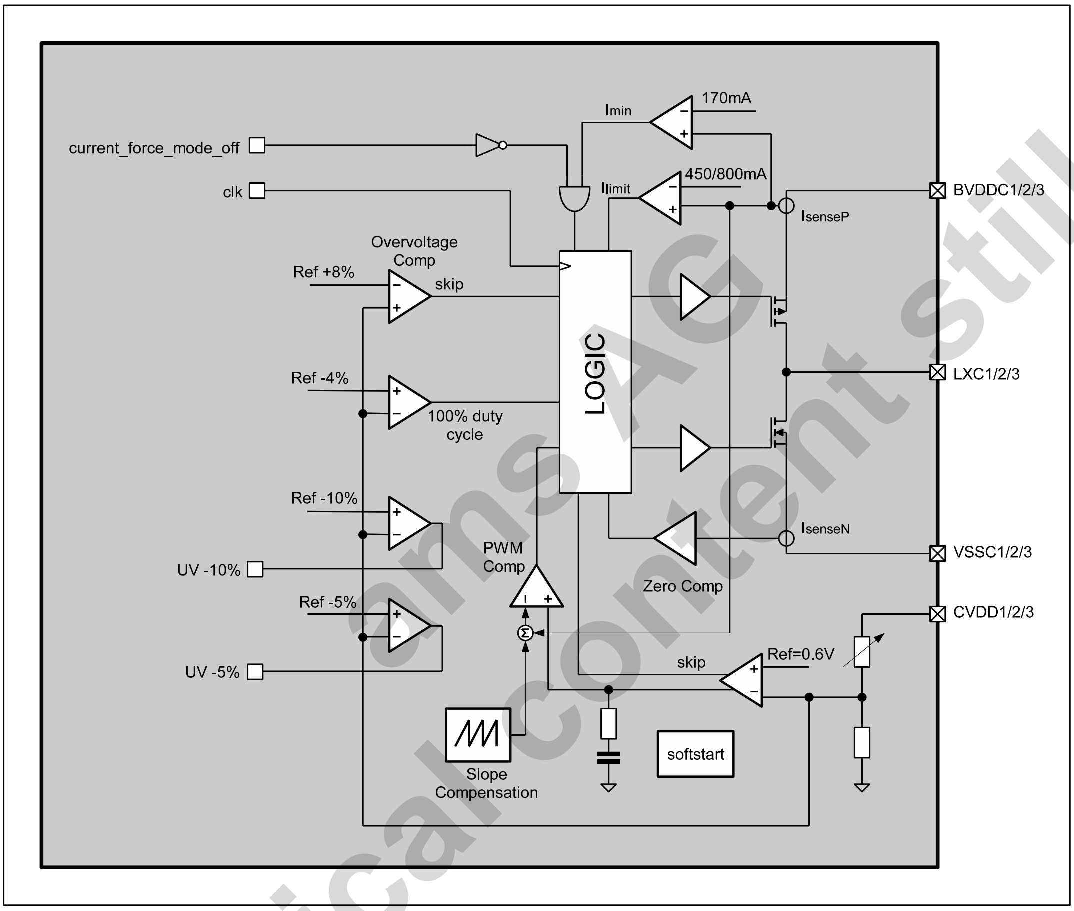
9.2.2 DCDC Step-Down Converter (3x)

General

These converters are meant to convert the battery voltage down to voltages which fit to the core and peripheral supply voltage requirements for microprocessors.

- Input Voltage BVDDC1, BVDDC2 & BVDDC3 (usually connected to the battery)
- Output Voltage CVDD1, CVDD2 & CVDD3
- output voltage levels can be programmed independently form 0.65V to 3.4V
- the default value at start-up is defined by VPROG1 and VPROG2 pins
- driver strength 250mA (500mA for DCDC 3)

Figure 20 DCDC Step-Down Block Diagram



Functional Description

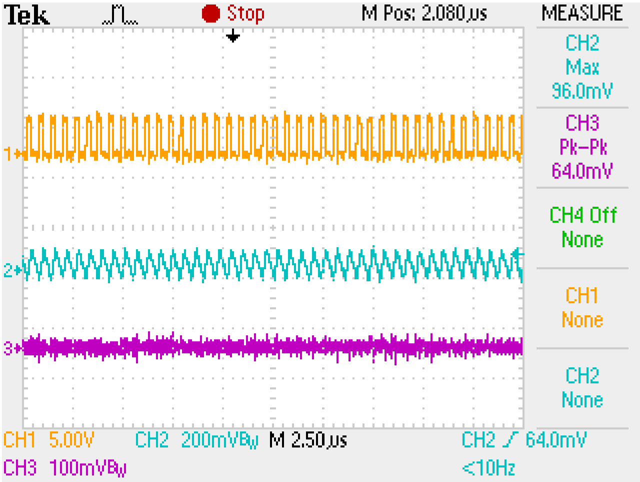
The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 250mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

To achieve optimised performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

Low ripple, low noise operation:

In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. Especially in the case of an inverted coil current the regulator will not operate in pulse skip mode.

Figure 21 –DCDC buck with disabled current force / pulse skip mode

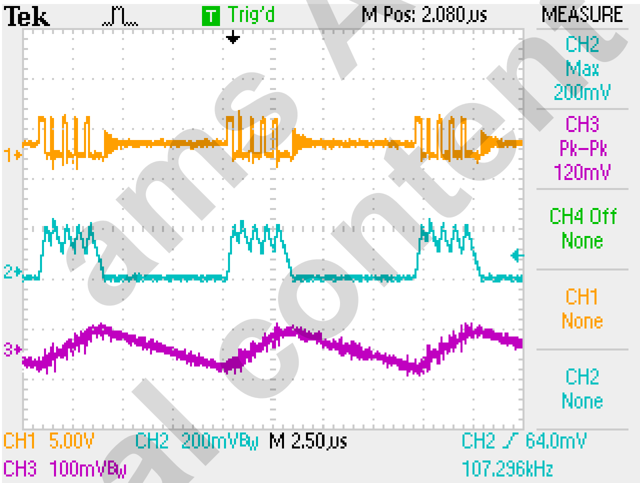


1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

High efficiency operation:

In this mode there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure 22 –DCDC buck with enabled current force / pulse skip mode



1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

It's also possible to switch between these two modes dynamically during operation:

100% PMOS ON mode for low dropout regulation:

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode. This feature is enabled if the output voltage drops by more than 4%.

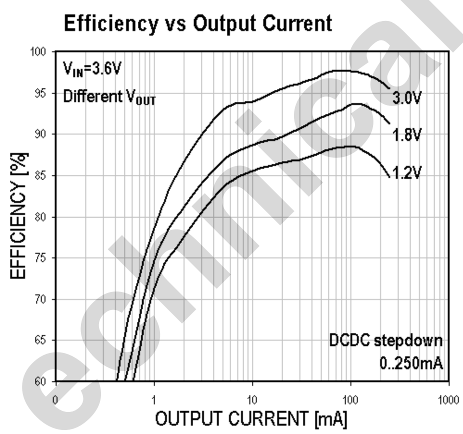
Parameter

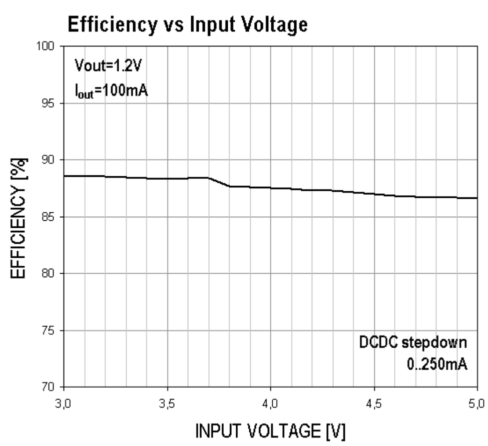
Table 28 DCDC Buck Typical Performance Parameter

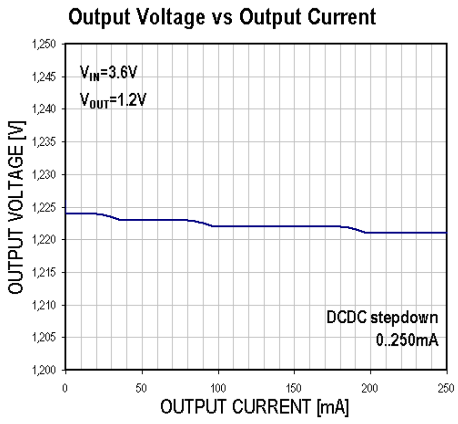
Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IN}	Input voltage	3.0		5.5	V	BVDD
V_{OUT}	Regulated output voltage	0.65		3.4	V	
V_{OUT_tol}	Output voltage tolerance	-50		50	mV	
I_{LOAD}	Maximum Load current		250		mA	DCDC 1&2
			500		mA	DCDC 3
I_{LIMIT}	Current limit		450		mA	DCDC 1&2
			800		mA	DCDC 3
R_{PSW}	P-Switch ON resistance		0.5	0.7	Ω	BVDD=3.0V; DCDC 1&2
			0.34	0.7	Ω	BVDD=3.0V; DCDC 3
R_{NSW}	N-Switch ON resistance		0.5	0.7	Ω	BVDD=3.0V; DCDC 1&2
			0.37	0.7	Ω	BVDD=3.0V; DCDC 3
f_{SW}	Switching frequency		1.2		MHz	
f_{SWsc}	Switching frequency		0.6		MHz	in shortcut case
C_{out}	Output capacitor		10		µF	Ceramic, +/- 10% tolerance
Lx	Inductor	3.3		4.7	µH	+/- 10% tolerance
η_{eff}	Efficiency		97		%	Iout=100mA, Vout=3.0V
I_{VDD}	Current consumption		220 100 0.1		µA	Operating current without load Low power mode current Shutdown current
t_{MIN_ON}	Minimum on time		80		ns	
t_{MIN_OFF}	Minimum off time		40		ns	
$V_{LineReg}$	Line regulation		2		mV	Static
			10		mV	Transient; Slope: t_r=10µs, 100mV step, 200mA load
$V_{LoadReg}$	Load regulation		5		mV	Static
			50		mV	Transient; Slope: t_r=10µs, 100mA step

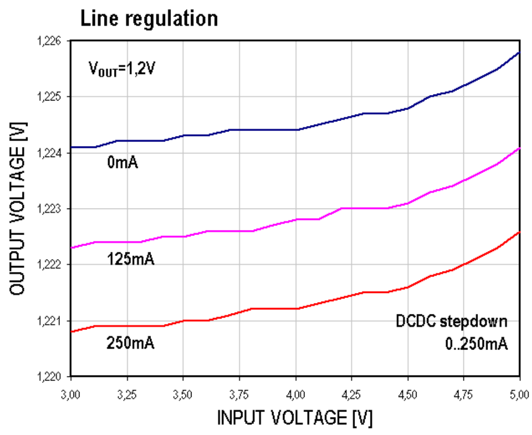
BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

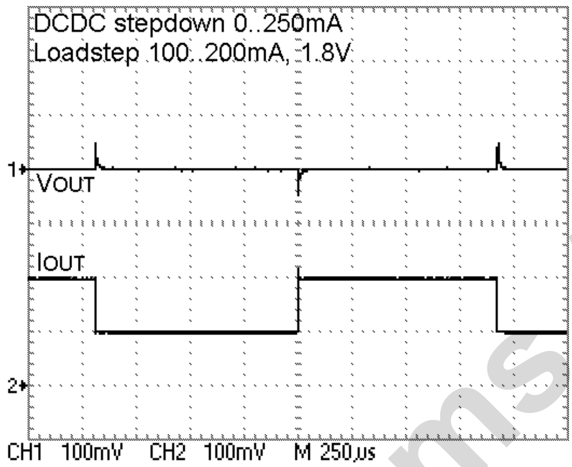
Figure 23 DCDC Step-down Performance Characteristics

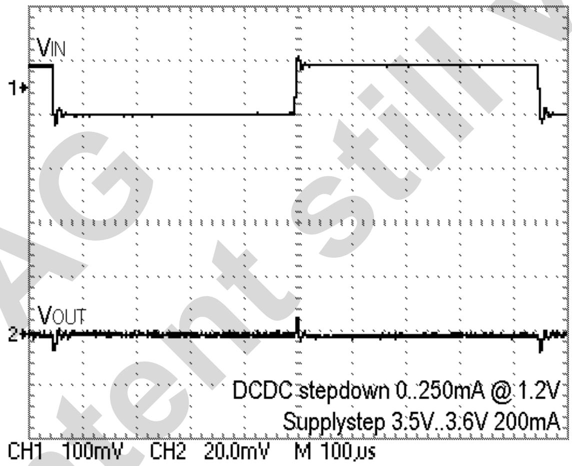


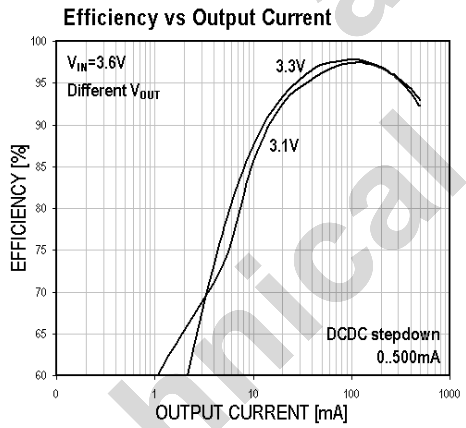












Register Description

Table 29 DCDC Buck Related Register

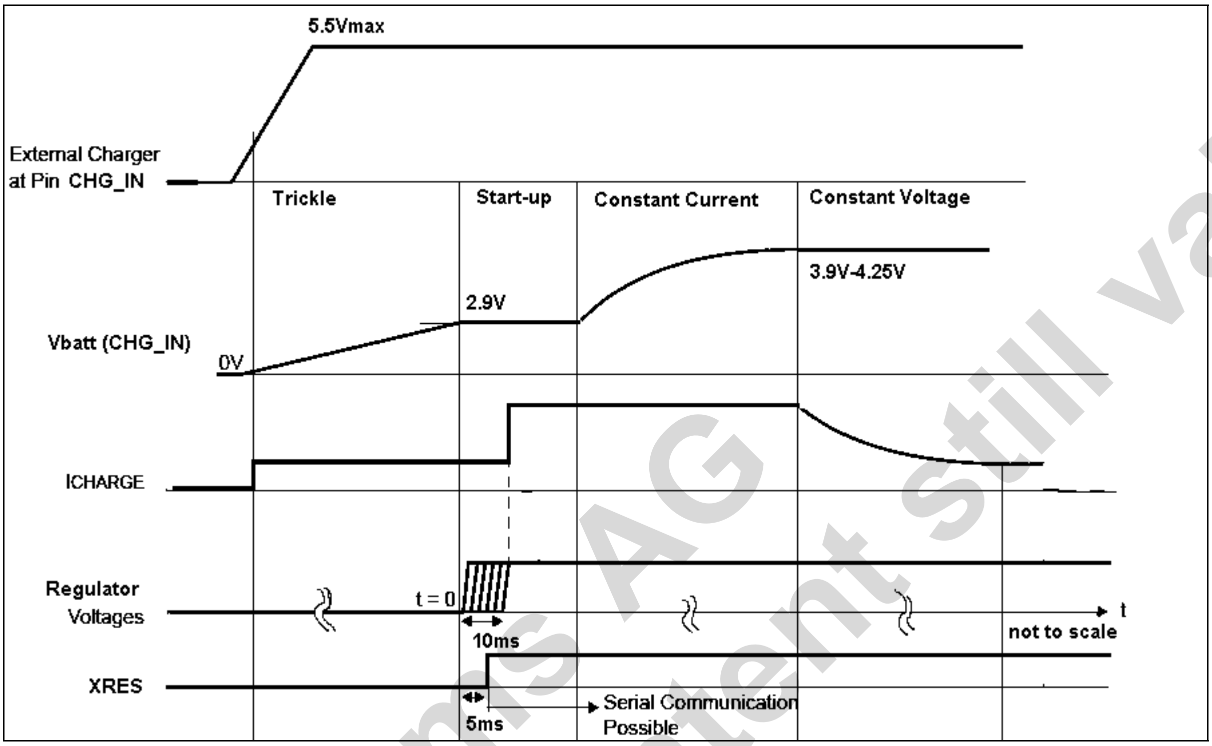
Name	Base	Offset	Description
PMU CVDD1	2-wire serial	17h-3	CVDD1 (DCDC1) control and voltage settings
PMU CVDD2	2-wire serial	17h-4	CVDD2 (DCDC2) control and voltage settings
PMU CVDD3	2-wire serial	17h-5	CVDD2 (DCDC2) control and voltage settings
PMU ENABLE	2-wire serial	18h	Enables writings to extended registers 17h-3, 17h-4

9.2.3 Charger

General

This block can be used to charge a 4V Li-Io accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (50 to 400mA) and maximum charging voltage (3.9 to 4.25V).

Figure 24 Charger States



Trickle Charge

If BVDD is below 3V in systems where the battery is not separated from BVDD, the charger goes automatically in trickle charge mode with 50mA charging current and 3.9V endpoint voltage. In this mode charging current and voltage are not precise, but provide a charger function also for deep discharged batteries. The temperature supervision is not enabled in trickle charge mode.

As soon as BVDD reaches 3V the AFE switches on and starts-up the regulators with the power-up sequence selected by pins VPRG1 and VPRG2. Afterwards the CPU can set the modes and the charging currents via the 2-wire serial interface.

If the battery (CHGOUT) voltage is below 2.9V the charging current cannot be set higher than 50mA, also when using a battery separation circuit to supply the AFE (BVDD) from USB or another voltage source.

Temperature Supervision

This charger block also features a 15uA supply for an external 100k NTC resistor to measure the battery temperature while charging. If the temperature is too high (>45°C), an interrupt can be generated. If the battery temperature drops below 42°C the charger will start charging again. The temperature supervision is not enabled in trickle charge mode.

If the NTC resistor does not have 100kΩ its value can be corrected with a resistor in series or in parallel.

Parameter

Table 30 Charger Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{CHG_trick}	Charging Current (trickle charge)	37	68	111	mA	BVDD<=3V, CHGIN = 5.5V
		17	32	55	mA	BVDD<=3V, CHGIN = 4.0V
V_{CHG_trick}	Charger Endpoint Voltage (trickle charge)	0.70* CHGIN	0.72* CHGIN	0.74* CHGIN	V	BVDD<=3V, CHGIN = 4.4V
I_{CHG} (0-7)	Charging Current	I_{NOM} -20%	I_{NOM}	I_{NOM} +20%	mA	BVDD > 3V
V_{CHG} (0-7)	Charging Voltage	V_{NOM} -50mV	V_{NOM}	V_{NOM} +30mV	V	BVDD > 3V, end of charge is true
V_{ON_ABS}	Charger On Voltage IRQ		3.1	4.0	V	BVDD = 3V
V_{ON_REL}	Charger On Voltage IRQ		170	240	mV	CHGIN-CHGOUT
V_{OFF_REL}	Charger Off Voltage IRQ	40	77		mV	CHGIN-CHGOUT
V_{BATEMP_ON}	Battery Temp. high level (45°C)		610		mV	BVDD >3V
V_{BATEMP_OFF}	Battery Temp. low level (42°C)		700		mV	BVDD >3V
I_{CHG_OFF}	End Of Charge current level	5% I_{NOM}	10% I_{NOM}	15% I_{NOM}	mA	BVDD >3V
I_{REV_OFF}	Reverse current shut down		<1		uA	BVDD = 5V, CHGIN open

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Register Description

Table 31 Charger Related Register

Name	Base	Offset	Description
CHARGER	2-wire serial	22h	Charger voltage, current and temp. supervision control
IRQ_ENRD_2	2-wire serial	25h	Enable/disable EOC and battery over-temperature interrupt Read out charger status

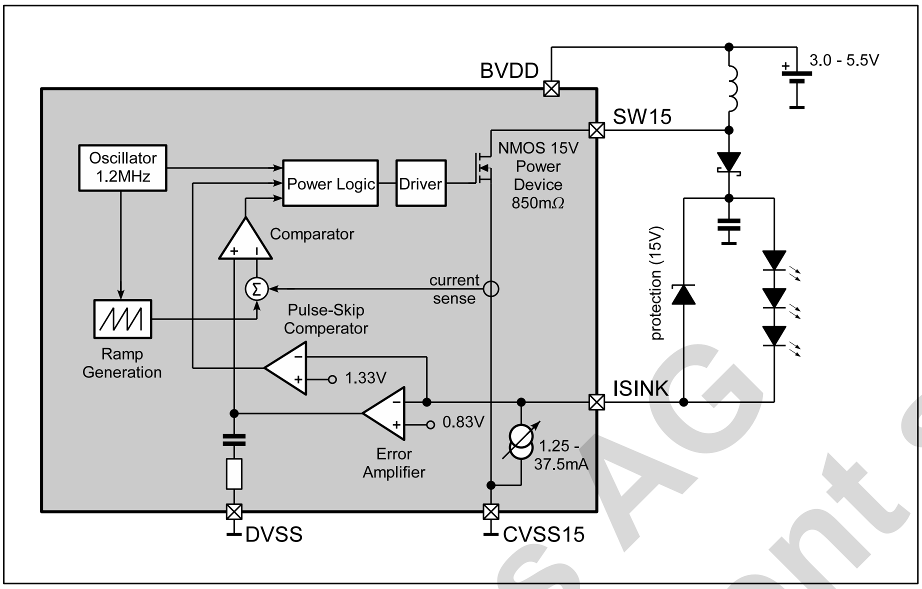
9.2.4 15V Step-Up Converter

General

The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 15V. A constant switching-frequency results in a low noise on supply and output voltages. When using an additional transistor the output voltage can be up to 25V to drive 6 white LED in series.

It has an adjustable sink current (1.25 to 37.5mA) to provide e.g. dimming function when driving white LEDs as back-light.

Figure 25 DCDC15 Block Diagram



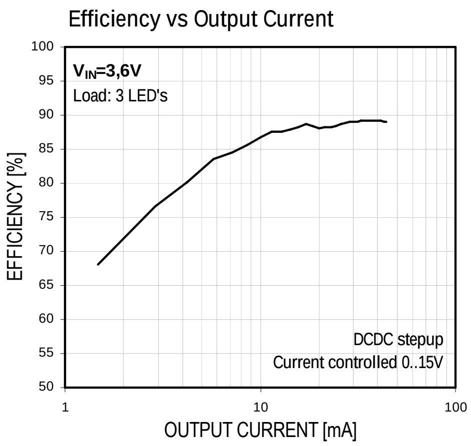
Parameter

Table 32 15V Step-Up Converter Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{SW}	High Voltage Pin	0		15	V	Pin SW15
I_{VDD}	Quiescent Current		140		µA	Pulse Skipping mode
V_{FB}	Feedback Voltage, Transient	0		5.5	V	Pin ISINK
V_{FB}	Feedback Voltage, during Regulation	0.65	0.83	1.0	V	Pin ISINK
I_{SW_MAX}	Current Limit	350	510	750	mA	V15_ON = 1
R_{SW}	Switch Resistance		0.85	1.54	Ω	V15_ON = 0
I_{LOAD}	Load Current	0		45	mA	@ 15V output voltage
$V_{PULSESKIP}$	Pulse-skip Threshold	1.2	1.33	1.5	V	Voltage at pin ISINK, pulse skips are introduces when load current becomes too low.
F_{IN}	Fixed Switching Frequency	0.5	0.55	0.6	MHz	
C_{OUT}	Output Capacitor		1		µF	Ceramic
L (Inductor)	I_{LOAD} > 20mA	17	22	27	µH	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficency
	I_{LOAD} < 20mA	8	10	27		
t_{MIN_ON}	Minimum On-Time	90		180	ns	Guaranteed per design
MDC	Maximum Duty Cycle	85	91	98	%	Guaranteed per design

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Figure 26 15V Step-Up Performance Characteristics



Register Description

Table 33 15V Step-Up Related Register

Name	Base	Offset	Description
DCDC15	2-wire serial	1Bh	DCDC15 current and dimming control

9.2.5 USB VBUS Supply

The VBUS voltage converter consists out of a charge pump and a DCDC converter. These 2 blocks share common pins. The charge pump (CP) and is used as USB-OTG (on the go) supply (5V/8mA) and the DCDC step-up converter provides the USB-HOST supply (5V /500mA). Depending on the external configuration either CP mode or DCDC mode is selected. Be aware that only one block can be used in one application. The following description shows how each block operates and how the circuit should be configured.

Additional the USB VBUS generation block features a VBUS comparator to detect different VBUS levels thus complies to SRP (session request protocol) and HNP (host negotiation protocol).

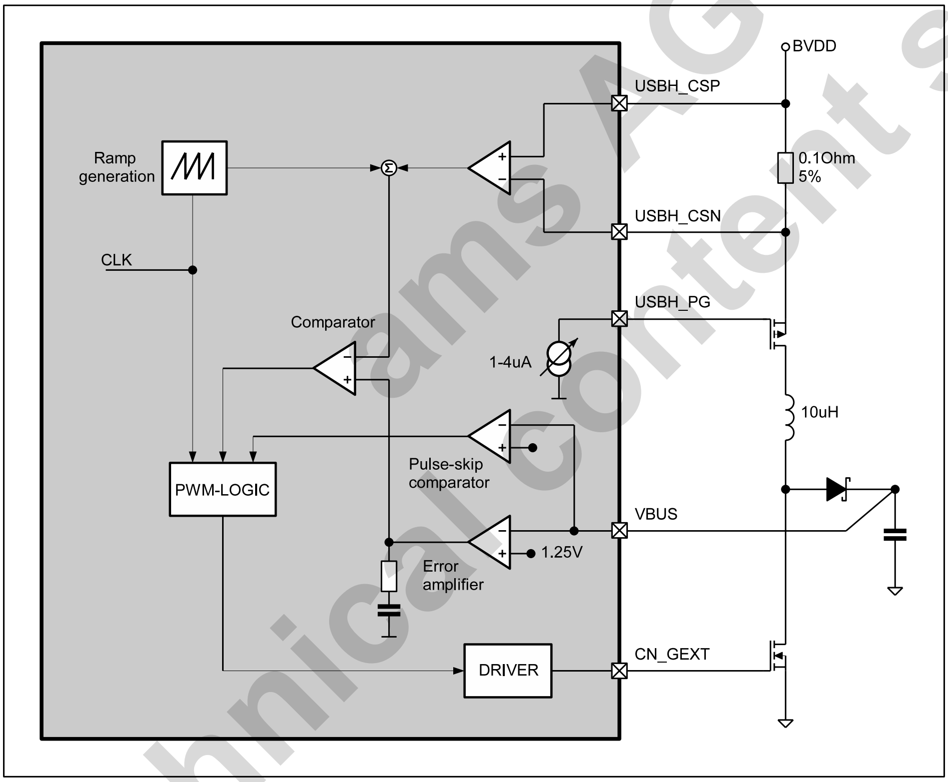
VBUS DCDC (USB Host Supply)

With the pin USBH_CSP connected to the battery voltage the mode USB-HOST mode is selected. This means the DCDC converter supplies 5V and up to 500mA.

For device safety an external PMOS switch is necessary in the case of a short-circuit condition on the VBUS pin. With this PMOS the device can shut off the path between battery and output. During start-up the PMOS switch will be opened very slowly by discharging his gate with a small current sink. Depending on the value of the Gate-Source Capacitance and the start-up time, different current values for the current sink can be programmed.

During start-up and operation the DCDC also monitors the current over the sense resistor. If the current limit will be reached during start-up the DCDC will generate an interrupt signal after 5.3usec de-bounce time. If this over-current condition is still present after 85µs the DCDC converter will be shut off by resetting its register. During start-up, however, an interrupt will be masked until pin USBH_PG is lower than 1V.

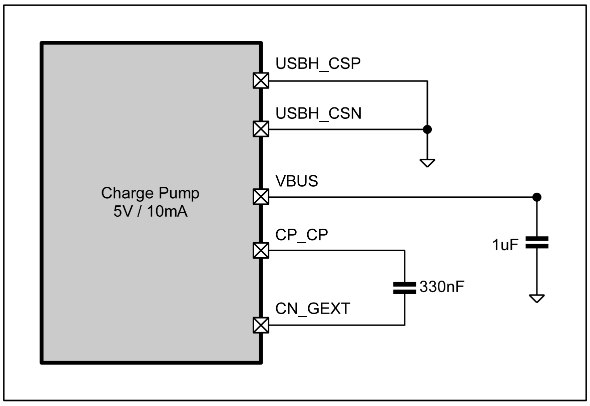
Figure 27 VBUS DCDC Block Diagram



VBUS Charge Pump (USB OTG Supply)

With the pin USBH_CSN and USBH_CSP connected to ground the USB-OTG mode is selected. In this mode the charge pump supplies 5V and 8mA. The charge pump uses the QLDO2 voltage as input and doubles its voltage with the help of the flying capacitor between CP_CP and CN_GEXT to its output VBUS. If the pulse skip bit is set in the related register, the charge pump switches to pulse skip mode for improved efficiency. Enabled pulse skip mode, however, compromises with a higher output voltage ripple.

Figure 28 VBUS CP Block Diagram



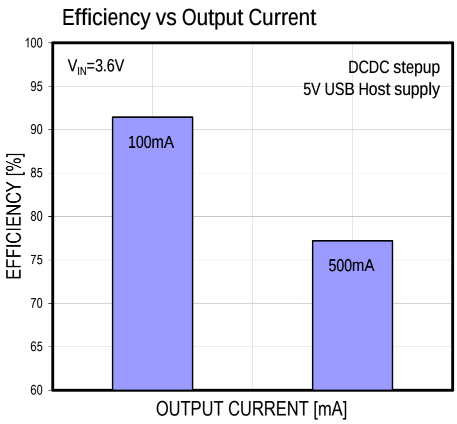
Parameter

Table 34 VBUS Generation Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
CP Mode						
I_{CPOUT}	Output Current			8	mA	@ 4.7V output voltage
I_{VDD}	Quiescent Current		600		µA	
V_{CPOUT}	Output Voltage	4.7	5.0	5.3	V	C_{FLY}=100nF,I_{CPOUT}=0..8mA
F_{IN}	Switching frequency		375		kHz	
C_{FLY}	External flying capacitor		100		nF	ceramic, low ESR capacitor between CP_CP and CN_GEXT
C_{STORE}	External storage capacitor	1	2.2		uF	ceramic, low ESR capacitor between VBUS and VSS
DCDC Mode						
I_{VDD}	Quiescent Current		140		µA	Pulse Skipping mode
V_{Rsense_max}	Current Limit at R_{sense}		100		mV	e.g.: 1A for 0.1 Ohm sense resistor
I_{LOAD}	Load Current	0		500	mA	@ 5V output voltage
f_{IN}	Fixed Switching Frequency		750		KHz	
t_{MIN_ON}	Minimum On-Time		130		ns	
MDC	Maximum Duty Cycle		91		%	
C_{OUT}	Output Capacitor		4.7		µF	Ceramic, +/-20%
L	Inductor		10		µH	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficiency
N_{SW}	NMOS switch					ON-resistance of external switching transistor max. 1Ω
P_{SW}	PMOS switch					ON-resistance of external PMOS transistor as low as possible, because of efficiency
R_{sense}	Current Limit Sense Resistor		100		mΩ	e.g.: 1A for 0.1 Ohm sense resistor

BVDD=3.3V, T_A=25°C, unless otherwise specified

Figure 29 15V Step-Up Performance Characteristics



Register Description

Table 35 USB VBUS Related Registers

Name	Base	Offset	Description
PMU VBUS	2-wire serial	1Ah	DCDC and CP control, VBUS comparator settings

9.3 SYSTEM Functions

9.3.1 SYSTEM

General

The system block handles the power up, power down and regulator voltage settings of the AFE.

Power Up Conditions

The chip powers up when on of the following condition is true:

- High signal on the PWR_UP pin (>80ms, >1V & >1/3 BVDD)
- Rising edge on the VBUS pin (USB plug in: >80ms, BVDD>3V, VBUS>4.5V)
- Rising edge on the CHGIN pin (charger plug in: >80ms, BVDD>3V, CHGIN>4.0V)
- Rising edge on the RTCSUP and consequently on RVDD pin (RTCSUP > 1.35V, BVDD >3V)
- RTC wake-up: The auto wake-up timer is internally connected to the Power-up and Hibernation Control block.

To hold the chip in power up mode the PWR_HOLD bit in the SYSTEM register (0x20h) is set.

Power Down Conditions

The chip automatically shuts off if one of the following conditions arises:

- Clearing the PWR_HOLD bit in SYSTEM register (0x20h)
- I2C watchdog power down(no serial reading for >1s, has to be enabled)
- Heartbeat watchdog via pin HBT(no watchdog reset via HBT pin for > 500ms, has to be enabled)
  Please note, that when using power-up sequence 16 to 25 no power down is performed but a reset puls (86us typ, 60us min) will be performed.
- BVDD drops below the minimum threshold voltage (<2.7V)
- LDO or step down converter output voltage drop below a programmable level (has to be enabled)
- Junction temperature reaches maximum threshold, set in SUPERVISOR register (0x24h)
- High signal on the PWR_UP pin for more than (>5.4s, >1V & >1/3 BVDD).
  With setting SD_TIME bit in register 24h the time can be doubled.

Start-up Sequence

The AFE offers 25 different power-up sequences. The specific start-up sequence can be selected via VPRG1 and VPROG2 pin. Each pin detects 5 logical input states which shall come from an external resistor divider network.

At first, LDO1 (AVDD) and LDO2 (DVDD) is powering up. This cannot be influenced with the selection of specific sequences below. LDO1 and LDO2 are necessary for the internal supply of the AFE.

After power-up sequence selected by pin VPRG1, all voltage settings and power on/off conditions of the described regulators can be programmed via the serial interface.

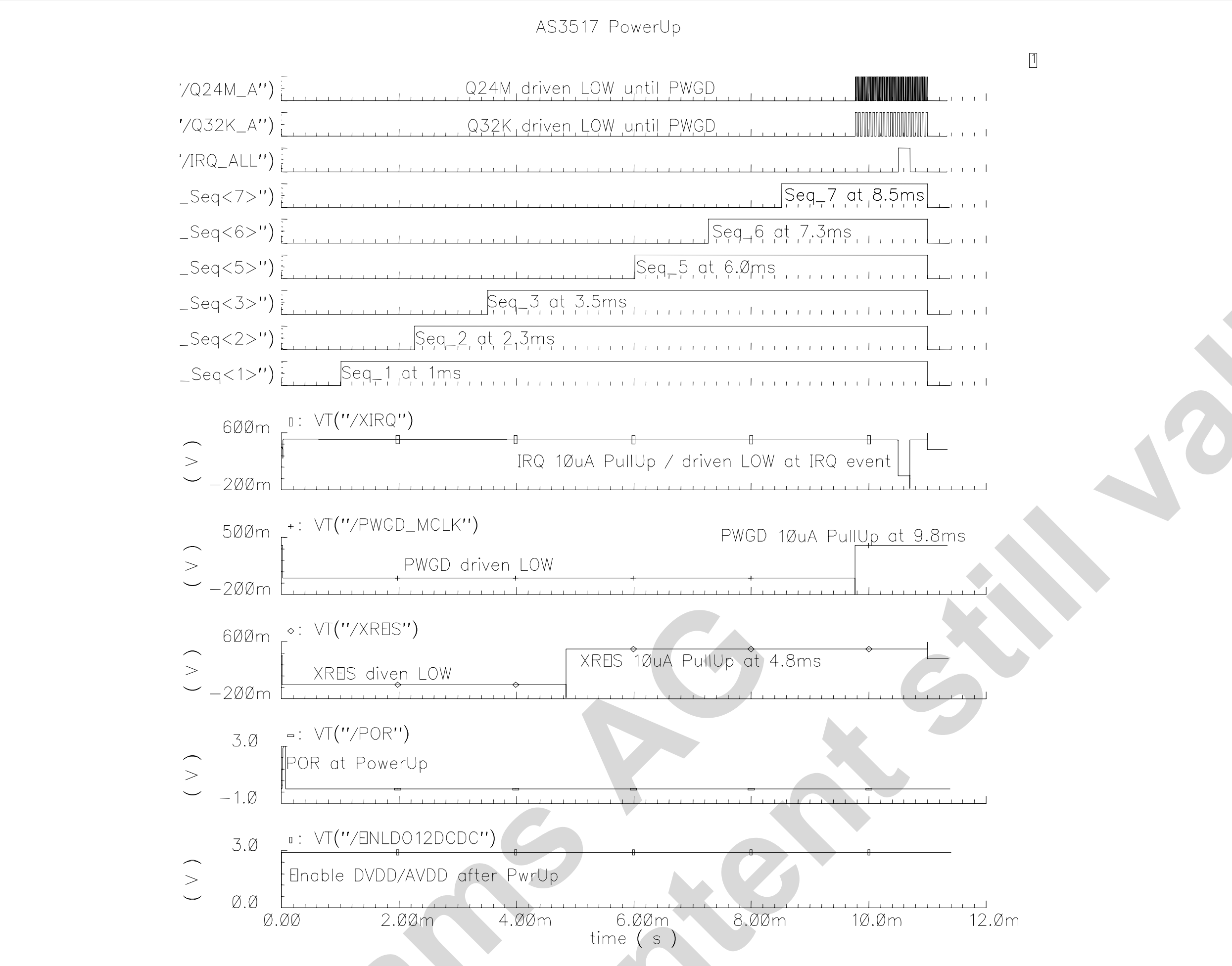
Table 36 Start-up Modes

#	VPRG2	VPRG1	DCDC1		DCDC2		DCDC3		DCDC4		DCDC15		LDO3		LDO4		XRES/	
			CVDD1		CVDD2		CVDD3		VBUS		VLED		PVDD1		PVDD2		PWGD	
1	open	open	1,2V	3rd	3,3V	2nd	3,3V	1st		x		x		x		x	4th	8th
2	open	vdd	1,2V	3rd	2,5V	2nd	3,3V	1st		x		x		x		x	4th	8th
3	open	150k-vdd	1,2V	3rd	2,5V	2nd		x		x		x	3,3V	1st		x	4th	8th
4	open	150k-vss	1,2V	3rd	1,8V	2nd		x		x		x	3,3V	1st		x	4th	8th
5	open	vss	1,2V	3rd		x		x		x		x	3,3V	1st	2,5V	2nd	4th	8th
6	150k-vdd	open	1,5V	3rd	3,3V	2nd	3,3V	1st		x		x		x		x	4th	8th
7	150k-vdd	vdd	1,5V	3rd	2,5V	2nd	3,3V	1st		x		x		x		x	4th	8th
8	150k-vdd	150k-vdd	1,5V	3nd	2,5V	2nd		x		x		x	3,3V	1st		x	4th	8th
9	150k-vdd	150k-vss	1,5V	3rd	1,8V	2nd		x		x		x	3,3V	1st		x	4th	8th
10	150k-vdd	vss	1,5V	3rd		x		x		x		x	3,3V	1st	2,5V	2nd	4th	8th
11	vdd	open	1,8V	3rd	3,3V	2nd	3,3V	1st		x		x		x		x	4th	8th
12	vdd	vdd	1,8V	3rd	2,5V	2nd	3,3V	1st		x		x		x		x	4th	8th
13	vdd	150k-vdd	1,8V	3nd	2,5V	2nd		x		x		x	3,3V	1st		x	4th	8th
14	vdd	150k-vss	1,8V	3rd	1,8V	2nd		x		x		x	3,3V	1st		x	4th	8th
15	vdd	vss	1,8V	3rd		x		x		x		x	3,3V	1st	2,5V	2nd	4th	8th
16	vss	open	1,2V	1st	1,8V	2nd	3,3V	3rd	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
17	vss	vdd	1,2V	1st	1,8V	2nd	3,0V	3rd	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
18	vss	150k-vdd	1,2V	1st	2,5V	2nd	3,3V	3rd	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
19	vss	150k-vss	1,8V	1st	2,5V	2nd	3,3V	3rd	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
20	vss	vss	1,8V	1st	3,3	2nd	3,3V	3rd	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
21	150k-vss	open	1,2V	3rd	1,8V	2nd	3,3V	1st	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
22	150k-vss	vdd	1,2V	3rd	1,8V	2nd	3,0V	1st	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
23	150k-vss	150k-vdd	1,2V	3rd	2,5V	2nd	3,3V	1st	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
24	150k-vss	150k-vss	1,8V	3rd	2,5V	2nd	3,3V	1st	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th
25	150k-vss	vss	1,8V	3rd	3,3	2nd	3,3V	1st	5,0V	5th	5mA	5th	3,0V	6th	3,0V	7th	*	8th

*… in Special Mode the XRES is going High 85us (min 60us) after PwrUp key is released

x … means that this regulator is not started with the start-up sequencer but has to be turned on by the 2-wire serial interface when needed.

Figure 30 Power Up Timing



Register Description

Table 37 System Related Register

Name	Base	Offset	Description
SYSTEM	2-wire serial	20h	Watchdog and Over-temperature control, Power down enable
IRQ_ENRD_1	2-wire serial	24h	Enable/disable wake-up interrupts, set shut-down time
IRQ_ENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt

9.3.2 Hibernation

General

Hibernation allows shutting down a part or the complete system. Hibernation can be terminated by every possible interrupt of the AFE. E.g. one can use the RTC for a time triggered wake-up. The interrupt has to be enabled before going to hibernation

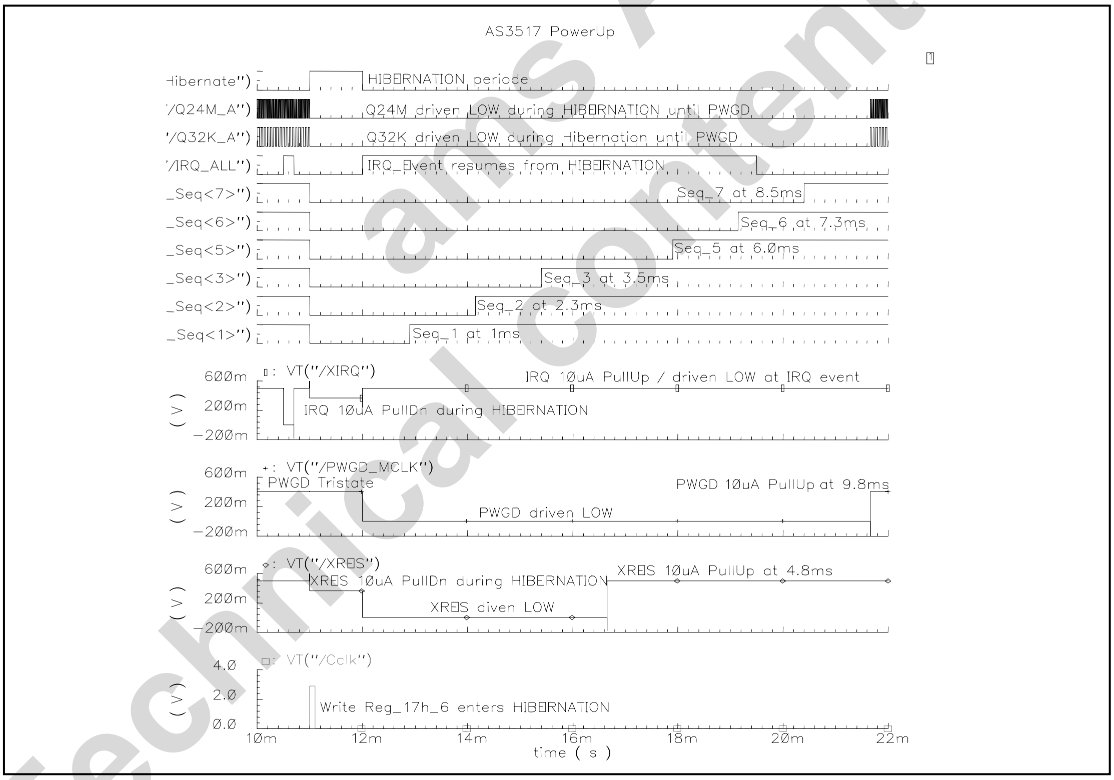
Table 38 Hibernation Modes

Modes	VPRG2	Action	KeepBit	LDOs	DCDCs	VBUS	DCDC15V
1-15	VDD 150k- VDD OPEN	Hib. with Default	OFF	OFF	OFF	OFF	OFF
		Cancel Hibernation	OFF	Default	Default	OFF	OFF
		Hib. with Modif Settings	OFF	OFF	OFF	No Change	No Change
		Cancel Hibernation	OFF	As Before	As Before	No Change	No Change
		Hib. with Modif Settings	ON	No Change	No Change	No Change	No Change
		Cancel Hibernation	ON	No Change	No Change	No Change	No Change
16-25	VSS 150k- VSS	Hib. with Default	OFF	OFF	OFF	Stays ON	OFF
		Cancel Hibernation	OFF	Default	Default	Default	Default
		Hib. with Modif Settings	OFF	OFF	OFF	No Change	OFF
		Cancel Hibernation	OFF	As Before	As Before	ON	As Before
		Hib. with Modif Settings	ON	No Change	No Change	No Change	No Change
		Cancel Hibernation	ON	No Change	No Change	No Change	No Change

"Hibernation with Default" means that, the voltage of the power supply is determined by VPROG1 pin.

"Hibernation with Modified Settings" means, that the voltage of the power supply is controlled by register settings.

Figure 31 Hibernate Timing



Register Description

Table 39 Hibernation Related Register

Name	Base	Offset	Description
PMU Hibernate	2-wire serial	17h-6	Hibernation control
PMU ENABLE	2-wire serial	18h	Enables writings to extended register 17h-6

9.3.3 Supervisor

General

This supervisor function can be used for automatic detection of BVDD brown out or junction over-temperature condition.

BVDD Supervision

The supervision level can be set in 8 steps @ 60mV from 2.74 to 3.16V. If the level is reached an interrupt can be generated. If BVDD reaches 2.7V the AFE shuts down automatically.

Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to –15ºC). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20ºC higher.

Power Rail Monitoring

The 4 main regulators have an extra monitor which measures the output voltage of the regulator. This power rail monitors are independent from the 10bit ADC. To activate these please see related registers.

Register Description

Table 40 Supervisor Related Register

Name	Base	Offset	Description
SUPERVISOR	2-wire serial	21h	Battery and junction temperature supervision threshold levels
IRQ_ENRD_0	2-wire serial	23h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQ_ENRD_1	2-wire serial	24h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQ_ENRD_2	2-wire serial	25h	Enable/disable battery brown out interrupt
IRQ_ENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt

9.3.4 Interrupt Generation

General

All interrupt sources can get enabled or disabled by corresponding bits in the 5 IRQ-bytes. By default no interrupt source is enabled.

The XIRQ output can get configured to be PUSH/PULL or OPEN_DRAIN and ACTIVE_HIGH or ACTIVE LOW with 2 bits in IRQ_ENRD_4 register (27h). Default state is open drain and active_low.

IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

LEVEL

The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled

EDGE

The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

STATUS CHANGE

The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.

De-bouncer

There is a de-bounce function implemented for USB and CHARGER. Since these 2 signals can be unstable for the phase of plug-in or unplug, a de-bounce time of 512ms/256ms/128ms can be selected by 2 bits in the IRQ_ENRD_4 register (27h).

Interrupt Sources

18 IRQ events will activate the XIRQ pin:

- headphone connected
- Microphone 1 connected
- Microphone 2 connected
- Microphone 1 remote control
- Microphone 2 remote control
- Voice activation threshold reached
- RTC sec/min elapsed
- 10bit ADC end of conversion
- I²S changed
- USB changed
- Charger changed
- End of charge (at 10% of programmed current)
- Battery temperature high (at 42°C and 45°C with 100kΩ NTC)
- RVDD low (e.g. after battery was changed)
- Battery low (Brown-out voltage reached)
- wake-up from hibernation
- power-up key (pin PWRUP) pressed
- power rail monitor: PVDD1, PVDD2, CVDD1, CVDD2

9.3.5 Real Time Clock

General

The real time clock block is an independent block, which is still working even when the chip is shut down. The only condition for this operation is that BVDDR has a voltage of above 1.0V. The block uses a standard 32kHz crystal that is connected to a low power oscillator. The total power consumption is typ. 12µA. (Q32k clock buffer not operating)

The RTC seconds counter is 32bit wide and can be programmed via the 2-wire serial interface. The RTC can deliver a seconds or minutes interrupt.

Another 23bit wide counter allows auto wake-up (max. after 96 days). This counter is internally connected to the power-up and hibernation control block.

The RTC voltage regulator (RVDD) further supplies a 128bit SRAM. It can be used to store settings or data before shutdown.

Clock adjustment

The RTC clock is adjustable in steps of 7.6ppm which allows the use of inexpensive 32kHz crystals. The nominal frequency shall be 32.768Hz. This frequency is divided down to 0.25Hz:
f = 32.768 / (4*32*1024)

At the input of this divider one can add corrective counts, which allow to correct an inaccurate crystal in a range from –64 counts (=-488ppm) to +63 counts (=+480ppm):
$f_{corrected} = f_{crystal}$ / [(4*32*1024)-64+RTC_TBC]

Register Description

Table 41 RTC Related Register

Name	Base	Offset	Description
RTCV	2-wire serial	28h	RTC oscillator and counter enable
RTCT	2-wire serial	29h	RTC interrupt and time correction settings
RTC_0 to RTC_3	2-wire serial	2Ah to 2Dh	RTC time-base seconds registers
RTC_WakeUp	2-wire serial	19h	RTC wake-up settings and SDRAM access
IRQ_ENRD_2	2-wire serial	25h	Interrupt settings for RVDD under-voltage detection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for getting a second or minute interrupt

9.3.6 10-Bit ADC

General

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc..

Input Sources

Table 42 ADC10 Input Sources

Nr.	Source	Range	LSB	Description
0	CHGOUT	5.120V	5mV	check battery voltage of 4V Lilo accumulator
1	BVDDR	5.120V	5mV	check RTC backup battery voltage (connected to BVDD inside the package)
2		5.120V	5mV	Source defined by DC_TEST in register 0x18
3	CHGIN	5.120V	5mV	check charger input voltage
4	VBUS	5.120V	5mV	check USB input voltage
5	BatTemp	2.560V	2.5mV	check battery charging temperature
6	MIC1S	2.560V	2.5mV	check voltage on MIC1S for remote control or external voltage measurement
7	MIC2S	2.560V	2.5mV	check voltage on MIC1S for remote control or external voltage measurement
8	VBE_1uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = 0.5*[ADC_bit0:bit9] – 565/2
9	VBE_2uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = 0.5*[ADC_bit0:bit9] – 575/2
10	I_MIC1S	1.024mA typ.	2.0uA	check current of MIC1S for remote control detection
11	I_MIC2S	1.024mA typ.	2.0uA	check current of MIC2S for remote control detection
12	RVDD	2.560V	2.5mV	check RTC supply voltage
13..15	Reserved	1.024V	1mV	for testing purpose only

Reference

AVDD=2.9V is used as reference to the ADC. AVDD is trimmed to +/-20mV with over all precision of +/-29mV. So the absolute accuracy is +/-1%.

Parameter

Table 43 ADC10 Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Notes
R_{DIV}	Input Divider Resistance	138k	180k	234k	Ω	CHGOUT, BVDDR, VBUS, CHGIN
ADC_{FS}	ADC Full Scale Range	2.534	2.56	2.586	V	
Ratio1	Division Factor 1	0.198	0.2	0.202	1	CHGOUT, BVDDR, VBUS, CHGIN
Ratio2	Division Factor 2	0.396	0.4	0.404	1	RVDD, BATTEMP, MIC1S, MIC2S
Gain	ADC Gain Stage	2.475	2.5	2.525	V	
T_{CON}	Conversion Time	-	34	50	µs	
I_MIC_{FS}	I_MICS Full Scale Range	0.7	1.0	1.4	mA	

BVDD=3.6V; T_{amb}=25ºC; unless otherwise specified

Register Description

Table 44 ADC10 Related Register

Name	Base	Offset	Description
ADC_0	2-wire serial	2Eh	ADC source selection, ADC result<9:8>
ADC_1	2 wire serial	2Fh	ADC result <7:0>
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for end of conversion interrupt
PMU_ENABLE	2-wire serial	18h	Extended ADC source selection

9.3.7 Unique ID Code (64 bit OTP ROM)

General

This fuse array is used to store a unique identification number, which can be used for DRM issues. The number is generated and programmed during the production process.

Register Description

Table 45 UID Related Register

Name	Base	Offset	Description
UID_0 to UID_7	2-wire serial	38h to 3Fh	Unique ID register 0 to 7

9.4 Register Description

Table 46 I2C Register Overview

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
00h	LINE_OUT1_R	LO1_MUX_B 0:SUM_Stereo;1:SUM_MDiff 2:ADC_IN; 3:DAC_OUT		-	LO1R_VOL Gain from MUX_B to LOUT1R= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
01h	LINE_OUT1_L	-	MUTE_OFF _J	-	LO1L_VOL Gain from MUX_B to LOUT1L= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
02h	HPH_OUT_R	HP_OVC_TO 0: 256ms; 1: 128ms 2: 512ms; (3: 0ms)		DAC_ DIRECT	HPR_VOL Gain from MUX_C to HPR= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
03h	HPH_OUT_L	MUTE_ON_ K	HP_ON	HPDET_ON	HPL_VOL Gain from MUX_C to HPL= (-45.43dB ... +1.07dB)				
		0	0	0	0	0	0	0	0
04h	LINE_OUT2_R	LO2_MUX_D 0: MIC1; 2: MIC2 1:MIC1_MDiff; 3: Stereo_MIC		-	LO2R_VOL Gain from MUX_D to LOUT2R= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
05h	LINE_OUT2_L	-	MUTE_OFF _L	-	LO2L_VOL Gain from MUX_D to LOUT2L= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
06h	MIC1_R	MIC1_AGC _OFF	PRE1_GAIN 0: 28dB; 1: 34dB 2: 40dB		M1R_VOL Gain from MicAmp (N6) to Mixer (N15) = (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
07h	MIC1_L	M1SUP _OFF	MUTE_OFF _E	RDET1_ OFF	M1L_VOL Gain from MicAmp (N6) to Mixer (N14) = (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
08h	MIC2_R	MIC2_AGC _OFF	PRE2_GAIN 0: 28dB; 1: 34dB 2: 40dB		M2R_VOL Gain from MicAmp (N4) to Mixer (N12) = (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
09h	MIC2_L	M2SUP _OFF	MUTE_OFF _D	RDET2_ OFF	M2L_VOL Gain from MicAmp (N4) to Mixer_In (N13)= (-40.5dB ... +6.0dB)				
		0	0	0	0	0	0	0	0
0Ah	Line_IN1_R	-	-	MUTE_OFF _B	LI1R_VOL Gain from LIN1R to Mixer (N10)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Bh	Line_IN1_L	LI1_MODE 00: SE_Sterep; 01: MonoDiff 10: SE_Mono		MUTE_OFF _G	LI1L_VOL Gain from LIN1L to Mixer (N17)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Ch	Line_IN2_R	-	-	MUTE_OFF _C	LI2R_VOL Gain from LIN2R to Mixer (N11)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Dh	Line_IN2_L	LI2_MODE 00: SE_Sterep; 01: MonoDiff 10: SE_Mono		MUTE_OFF _F	LI2L_VOL Gain from LIN2L to Mixer (N16)= (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
0Eh	DAC_R	-	-	-	DAR_VOL Gain from DAC (N19) to Mixer/MUX (N23)= (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
0Fh	DAC_L	-	MUTE_OFF _H	-	DAL_VOL Gain from DAC (N22) to Mixer/MUX (N26) = (-40.5dB ... +6dB)				
		0	0	0	0	0	0	0	0
10h	ADC_R	ADC_MUX_A 0: Stereo_Mic; 1:LineIN_1 2: LineIN_2; 3: AudioSUM		-	ADR_VOL Gain from MUX_A to ADC (N9) = (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
11h	ADC_L	-	MUTE_OFF_A	-	ADL_VOL Gain from MUX_A to ADC (N18) = (-34.5dB ... +12dB)				
		0	0	0	0	0	0	0	0
12h-1	OutContr1	DRIVE_PWGD 0: 12mA OD; 1: 12mA PP 2: 4mA PP; 3: 2mA PP		MUX_PWGD 0: PWGD; 1: PWM 2: SPDIF; 3: PLL clock		DRIVE_Q32K 0: 12mA PP; 1: 12mA OD 2: 4mA PP; 3: 2mA PP		MUX_Q32K 0: Q32K; 1: PWM 2: SPDIF; 3: PLL clock	
		0	0	0	0	0	0	0	0
12h-2	OutContr2_SPDIF	DRIVE_Q24M 0: 12mA PP; 1: 12mA OD 2: 4mA PP; 3: 2mA PP		MUX_Q24M 0: Q24 1: PLL clock	SPDIF_COPY_OK	SPDIF_MCLK_INV	SPDIF_INVALID	SPDIF_CNTR 0: OFF; 1: 32kS 2: 44.1kS; 3: 48kS	
		0	0	0	0	0	0	0	0
12h-3	PWM	PWM_INVERTED	PWM_CYCLE 0: no pulses; DytyCycle = PWM_CYCLE * 0.3937%						
		0	0	0	0	0	0	0	0
14h	AudioSet_1	ADC_R_ON	ADC_L_ON	LOUT2_ON	LOUT1_ON	LIN2_ON	LIN1_ON	MIC2_ON	MIC1_ON
		0	0	0	0	0	0	0	0
15h	AudioSet_2	BIAS_OFF	SUM_OFF	AGC_OFF	IBR_DAC		DAC_ON	-	
		0	0	0	0	0	0	0	0
16h	AudioSet_3	LIN1MIX_OFF	LIN2MIX_OFF	MIC1MIX_OFF	MIC2MIX_OFF	DACMIX_OFF	ZCU_OFF	IBR_HPH	HPCM_ON
		0	0	0	0	0	0	0	0
17h-1	PMU PVDD1	LDO_PVDD1_OFF	-	PROG_PVDD1	VSEL_PVDD1 0h – Fh:1.2V+VSEL*50mV (1.2V – 1.95V) 10h – 1Fh: 2.0V+(VSEL-10h)*100mV (2.0V – 3.5V)				
		0	0	0	0	0	0	0	0
17h-2	PMU PVDD2	LDO_PVDD2_OFF	-	PROG_PVDD2	VSEL_PVDD2 0h – Fh:1.2V+VSEL*50mV (1.2V – 1.95V) 10h – 1Fh: 2.0V+(VSEL-10h)*100mV (2.0V – 3.5V)				
		0	0	0	0	0	0	0	0
17h-3	PMU CVDD1	SKIP_OFF_CVDD1	PROG_CVDD1	VSEL_CVDD1 0h: OFF; 1h - 38h .... 0.6V+VSEL*50mV → 0.65V – 3.40V; (38h – 3Fh .... 3.4V)					
		0	0	0	0	0	0	0	0
17h-4	PMU CVDD2	SKIP_OFF_CVDD2	PROG_CVDD2	VSEL_CVDD2 0h: OFF; 1h - 38h .... 0.6V+VSEL*50mV → 0.65V – 3.40V; (38h – 3Fh .... 3.4V)					
		0	0	0	0	0	0	0	0
17h-5	PMU CVDD3	SKIP_OFF_CVDD3	PROG_CVDD3	VSEL_CVDD3 0h: OFF; 1h - 38h .... 0.6V+VSEL*50mV → 0.65V – 3.40V; (38h – 3Fh .... 3.4V)					
		0	0	0	0	0	0	0	0
17h-6	PMU Hibernate	-	KEEP_PVDD2	KEEP_PVDD1	KEEP_VLED	KEEP_VBUS	KEEP_CVDD3	KEEP_CVDD2	KEEP_CVDD1
		0	0	0	0	0	0	0	0
18h	PMU Enable	-	DC_TEST 0: unused; 1: AVDD; 2: DVDD; 3: PVDD1 4: PVDD2; 5: CVDD1; 6; CVDD2; 7: CVDD3			PMU_GATE	PMU_WR_ENABLE 1: prog 17h-1 / 12h-1 (PVDD1, OutContr1) 2: prog 17h-2 / 12h-2 (PVDD2, OutContr2) 3: prog 17h-3 / 12h-3 (CVDD1, PWM) 4: prog 17h-4 (CVDD2); 5: prog 17h-5 (CVDD3) 6: prog 17h-6 (Hibernate); 0,7: unused		
		0	0	0	0	0	0	0	0
19h	RTC_WakeUp	1st write/read: WAKEUP_BYTE_1							
		128s	64s	32s	16s	8s	4s	2s	1s
		2nd write/read: WAKEUP_BYTE_2							
		32ks	16ks	8ks	4ks	2ks	1ks	512s	256s
		3rd wirte/read: WAKEUP_BYTE_3							
		EnableWakeup	4k*1ks	2k*1ks	1k*1Ks	512ks	256ks	128ks	64ks
		4th to 19th write/read: SRAM_128							
1Ah	USB_UTIL_DCDC	I_PMOS_GATE 0: 1µA; 1: 2µA 2: 3µA; 3: 4µA		DCDC_PS_OFF	DCDC_PMOS_OFF	VBUS_COMP_TH 0: 4.5V; 1: 3.18V 2: 1.5V; 3: 0.6V		VBUS_SKIP_ON	VBUS_ON
		0	0	0	0	0	0	0	0
1Bh	DCDC15	DIM_UP_DOWN	DIM_RATE 0: no dimming; 1: 150ms 2: 300ms; 3: 500ms		I_BACKLIGHT 0 ... OFF 1-31 ... LED current = 1.25mA*I_BACKLIGHT (1.25mA ... 38.75mA)				
		0	0	0	0	0	0	0	0

Addr	Name	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
1Ch	I2S	Please see master clock divider table							
		0	0	0	0	0	0	0	0
1Dh	I2S_PLL_OSC	I2S_MASTER_ON	OSC24_PD	I2S_ DIRECT	Q24M_DIVIDER 0: /1; 1: /2 2: /4; 3:OFF		PLL_MODE 0: reserved; 1: 16-48kS 2: 8-12kS; 3: reserved		I2S_DIVIDER_8
		0	0	0	0	0	0	0	0
20h	SYSTEM	Design_Version<3:0>				HEARTBEAT_ON	JTEMP_ OFF	WATCHDOG_ON	PWR_HOLD
		1	1	1	1	0	0	0	1
21h	SUPERVISOR	BVDD_SUP V_BrownOut = 2..74V+BVDD_SUP*60mV (2.74V .. 3.16V)			JTEMP_SUP Temp_ShutDown = 140C – JTEMP_SUP*5C (+140C..—15C) Temp_IRQ = 120C – JTEMP_SUP*5C (+120C .. –35C)				
		0	0	1	0	0	0	0	0
22h	CHARGER	BAT_TEMP_OFF	CHG_I Ichg=50mA+50mA*CHG_I (50mA ... 400mA)			CHG_V Vchg=3.9V+50mV*CHG_V (3.9V ... 4.25V)			CHG_OFF
		0	0	0	0	0	0	0	0
23h	IRQ_ENRD_0	CVDD2_ EN_SD	CVDD2_ EN_IRQ	CVDD1_ EN_SD	CVDD1_ EN_IRQ	PDD2_ EN_SD	PDD2_ EN_IRQ	PDD1_ EN_SD	PDD1_ EN_IRQ
		CVDD2_ UNDER	CVDD2_ OVER	CVDD1_ UNDER	CVDD1_ OVER	PDD2_ UNDER	PDD2_ OVER	PDD1_ UNDER	PDD1_ OVER
		0	0	0	0	0	0	0	0
24h	IRQ_ENRD_1	SD_TIME 0: 5.4s 1: 10.9s	-	PWRUP_ IRQ	WAKEUP_ IRQ	VOXM2_ IRQ	VOXM1_ IRQ	CVDD3_ EN_SD	CVDD3_ EN_IRQ
								CVDD3_ UNDER	CVDD3_ OVER
		0	0	0	0	0	0	0	0
25h	IRQ_ENRD_2	BATTEMP_ HIGH	CHG_ EOC	CHG_ STATUS	CHG_ CHANGED	USB_ STATUS	USB_CHANGED	RVDD_LOW	BVDD_LOW
		0	0	0	0	0	0	0	0
26h	IRQ_ENRD_3	JTEMP_HIGH	-	HPH_ OVC	I2S_ STATUS	I2S_ CHANGED	MIC2_ CONNECT	MIC1_ CONNECT	HPH_ CONNECT
		0	0	0	0	0	0	0	0
27h	IRQ_ENRD_4	T_DEB 0: 512ms; 1: 256ms 2: 128ms; 3: 0ms		XIRQ_AH	XIRQ_PP	REM2_DET	REM1_DET	RTC_ UPDATE	ADC_EOC
		0	0	0	0	0	0	0	0
28h	RTCV	V_RVDD V(RVDD)=1V+V_RVDD*0.1V Default is 1.2V.				-		RTC_ON	OSC32_ON
		0	0	1	0	0	0	1	1
29h	RTCT	IRQ_MIN	TRTC<6:0>						
		0	1	0	0	0	0	0	0
2Ah	RTC_0	QRTC<7:0>							
		0	0	0	0	0	0	0	0
2Bh	RTC_1	QRTC<15:8>							
		0	0	0	0	0	0	0	0
2Ch	RTC_2	QRTC<23:16>							
		0	0	0	0	0	0	0	0
2Dh	RTC_3	QRTC<31:24>							
		0	0	0	0	0	0	0	0
2Eh	ADC_0	ADC_Source<3:0> 0: CHGOUT; 1: BVDDR; 2: DC_TEST; 3: CHG_IN; 4: VBUS; 5: BatTemp; 6: MSUP1; 7: MSUP2; 8: VBE_1uA; 9: VBE_2uA; 10: I_MSUP1; 11: I_MSUP2; 12; RVDD; 13, 14, 15: reserved				-	-	ADC<9:8>	
		0	0	0	0	0	0	X	X
2Fh	ADC_1	ADC<7:0>							
		X	X	X	X	X	X	X	X
38-3F	UID_0 .. 7	ID<7:0> ... ID<63:56>							

Table 47 LINE_OUT1_R Register

Name				Base	Default
LINE_OUT1_R				**2-wire serial**	**00h**
Offset: 00h		**Right Line Output 1 Register** Configures MUX_B and the audio gain from MUX_B output to LOUT1R output. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	LO1_MUX_B	00	R/W	Multiplexes the analog audio inputs of MUX_B to LOUT1R and at LOUT1L 00: SUM Stereo 01: SUM mono differential (The gain of LOUT1R shall be 0dB to hold signals in symmetry) 10: ADC (N9/N18) 11: DAC (N23/N26)	
5		0	n/a		
4:0	LO1R_VOL	00000	R/W	volume settings for right line output 1, adjustable in 32 steps @ 1.5dB; gain from MUX_B to LOUT1R 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain	

Table 48 LINE_OUT1_L Register

Name				Base	Default
LINE_OUT1_L				**2-wire serial**	**00h**
Offset: 01h		**Left Line Output 1 Register** Configures the audio gain from MUX_B output to LOUT1L output and controls MUTE switch J This register is reset when the stage is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7		0	n/a		
6	MUTE_OFF_J	0b	R/W	Control of MUTE switch J 0:line output set to mute 1: normal operation	
5		0	n/a		
4:0	LO1L_VOL	00000	R/W	volume settings for left line output 1, adjustable in 32 steps @ 1.5dB; gain from MUX_B to LOUT1L 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain	

Table 49 HPH_OUT_R Register

Name			Base	Default
HPH_OUT_R			**2-wire serial**	**00h**
Offset: 02h		**Right Headphone Output Register**		
		Configures MUX_C and the audio gain from MUX_C output to HPR output. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	HP_OVC_TO	00	R/W	Headphone amplifier over current time out. The headphone amplifier is powered down if an over-current is detected. The current thresholds are 150mA at pins HPR / HPL pin or 300mA at pin HPCM (e.g. shorted headphone outputs) 11: 0 ms (no power down) 10: 512ms 01: 128ms 00: 256 ms
5	DAC_DIRECT	0	R/W	0: MUX_C output connected to limiter (N24/N25) 1: MUX_C output connected to DAC (N23/N26)
4:0	HPR_VOL	00000	R/W	volume settings for right headphone output, adjustable in 32 steps @ 1.5dB; gain from MUX_C to HPR output 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93 dB gain 00000: -45.43 dB gain

Table 50 HPH_OUT_L Register

Name			Base	Default
HPH_OUT_L			**2-wire serial**	**00h**
Offset: 03h		**Left Headphone Output Register**		
		Configures the audio gain from MUX_C output to HPL output and controls MUTE switch K This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MUTE_ON_K	0	R/W	Control of MUTE switch K 0: normal operation 1: headphone output set to mute (mute is on during power-up)
6	HP_ON	0	R/W	0: headphone stage not powered 1: power up headphone stage
5	HPDET_ON	0	R/W	Enables the detection when a headset gets connected. HPCM is used as a sense pin and is biased to 150mV 0: no headphone detection 1: enable headphone detection
4:0	HPL_VOL	00000	R/W	volume settings for left headphone output, adjustable in 32 steps @ 1.5dB; gain from MUX_C output to HPL output 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93 dB gain 00000: -45.43 dB gain

Table 51 LINE_OUT2_R Register

Bit	Bit Name	Default	Access	Bit Description
Name		**Base**		**Default**
LINE_OUT2_R		**2-wire serial**		**00h**
Offset: 04h		**Right Line Output 2 Register** Configures MUX_B and the audio gain from MUX_B output to LOUT2R output. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
7:6	LO2_MUX_D	00	R/W	Multiplexes the analog audio inputs of MUX_D to LOUT2R and at LOUT2L 00: MIC1 01: MIC1 mono differential (The gain of LOUT2R shall be 0dB to hold signals in symmetry) 10: MIC2 11: Stereo MIC
5		0	n/a	
4:0	LO2R_VOL	00000	R/W	volume settings for right line output 2, adjustable in 32 steps @ 1.5dB; gain from MUX_D to LOUT2R 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 52 LINE_OUT2_L Register

Bit	Bit Name	Default	Access	Bit Description
Name		**Base**		**Default**
LINE_OUT2_L		**2-wire serial**		**00h**
Offset: 05h		**Left Line Output 2 Register** Configures the audio gain from MUX_B output to LOUT2L output and controls MUTE switch J This register is reset when the stage is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
7		0	n/a	
6	MUTE_OFF_L	0b	R/W	Control of MUTE switch L 0:line output set to mute 1: normal operation
5		0	n/a	
4:0	LO2L_VOL	00000	R/W	volume settings for left line output 2, adjustable in 32 steps @ 1.5dB; gain from MUX_D to LOUT2L 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 53 MIC1_R Register

Name			Base	Default
MIC1_R			**2-wire serial**	**00h**
Offset: 06h		**Right Microphone Input 1 Register**		
		Configures the gain from microphone 1 amplifier output up to mixer input (Σ). This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MIC1_AGC_OFF	0	R/W	Control of limiter AGC (automatic gain control). Limits high dynamic range of electrete/MEMS microphone (e.g. user shouts or blows into microphone) 0: automatic gain control enabled 1: automatic gain control disabled
6:5	PRE1_Gain	00	R/W	Sets the gain of the microphone 1 preamplifier (gain from microphone inputs to N5) 00: gain set to 28 dB 01: gain set to 34 dB 10: gain set to 40 dB 11: reserved, do not use.
4:0	M1R_VOL	00000	R/W	volume settings for right microphone input 1, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N6) to mixer input (N15) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 54 MIC1_L Register

Name			Base	Default
MIC1_L			**2-wire serial**	**00h**
Offset: 07h		**Left Microphone Input 1 Register**		
		Configures the gain from microphone 1 amplifier output up to mixer input (Σ) and controls MUTE switch D. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	M1SUP_OFF	0	R/W	0: microphone 1 supply enabled 1: microphone supply disabled
6	MUTE_OFF_E	0	R/W	Control of MUTE switch E 0: microphone input 1 set to mute 1: normal operation
5	RDET1_OFF	0	R/W	Disables the microphone 1 detect function (30kOhm pull-up from MIC1S to AVDD) to use the terminal as ADC-10 input 0: microphone 1 detection enabled 1: microphone detection disabled
4:0	M1L_VOL	00000	R/W	volume settings for left microphone 1 input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N6) to mixer input (N14) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 55 MIC2_R Register

Name	Base	Default
MIC2_R	**2-wire serial**	**00h**

Offset	Right Microphone Input 2 Register
Offset: 08h	Configures the gain from microphone 2 amplifier output up to mixer input (Σ). This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.

Bit	Bit Name	Default	Access	Bit Description
7	MIC2_AGC_OFF	0	R/W	Control of limiter AGC (automatic gain control). Limits high dynamic range of electrete/MEMS microphone (e.g. user shouts or blows into microphone) 0: automatic gain control enabled 1: automatic gain control disabled
6:5	PRE2_Gain	00	R/W	Sets the gain of the microphone 2 preamplifier (gain from microphone inputs to N5) 00: gain set to 28 dB 01: gain set to 34 dB 10: gain set to 40 dB 11: reserved, do not use.
4:0	M2R_VOL	00000	R/W	volume settings for right microphone input 2, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N12) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 56 MIC2_L Register

Name	Base	Default
MIC2_L	**2-wire serial**	**00h**

Offset	Left Microphone Input 2 Register
Offset: 09h	Configures the gain from microphone 2 amplifier output up to mixer input (Σ) and controls MUTE switch E. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.

Bit	Bit Name	Default	Access	Bit Description
7	M1SUP_OFF	0	R/W	0: microphone 2 supply enabled 1: microphone supply disabled
6	MUTE_OFF_D	0	R/W	Control of MUTE switch D 0: microphone input 2 set to mute 1: normal operation
5	RDET2_OFF	0	R/W	Disables the microphone 2 detect function (30kOhm pull-up from MIC1S to AVDD) to use the terminal as ADC-10 input 0: microphone 1 detection enabled 1: microphone detection disabled
4:0	M2L_VOL	00000	R/W	volume settings for left microphone 2 input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N13) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 57 LINE_IN1_R Register

Name		Base		Default
LINE_IN1_R		**2-wire serial**		**00h**
Offset: 0Ah		**Right Line Input 1 Registers**		
		Configures the gain from analog line input pin LIN1R to mixer input (Σ) and controls MUTE switch B. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6		00	n/a	
5	MUTE_OFF_B	0	R/W	Control of MUTE switch B 0: right line input is set to mute 1: normal operation
4:0	LI1R_VOL	00000	R/W	volume settings for right line input 1, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1R) to mixer input (N10) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 58 LINE_IN1_L Register

Name		Base		Default
LINE_IN1_L		**2-wire serial**		**00h**
Offset: 0Bh		**Left Line Input 1 Registers**		
		Configures the gain from analog line input pin LIN1L to mixer input (Σ) and controls MUTE switch G. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	LI1_MODE	00	R/W	Configures Line Input 1 (right and left channel) in accordance with the connected input sources 00: inputs switched to single ended stereo 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: reserved, do not use.
5	MUTE_OFF_G	0	R/W	Control of MUTE switch G 0: left line input is set to mute 1: normal operation
4:0	LI1L_VOL	00000	R/W	volume settings for right line input 1, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1L) to mixer input (N17) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 59 LINE_IN2_R Register

Name		Base		Default
LINE_IN2_R		**2-wire serial**		**00h**
Offset: 0Ch		**Right Line Input 2 Register** Configures the gain from analog line input pin LIN2R to mixer input (Σ) and controls MUTE switch C. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6		00	n/a	
5	MUTE_OFF_C	0	R/W	Control of MUTE switch C 0: right line input is set to mute 1: normal operation
4:0	LI2R_VOL	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN2R) to mixer input (N11) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 60 LINE_IN2_L Register

Name		Base		Default
LINE_IN2_L		**2-wire serial**		**00h**
Offset: 0Dh		**Left Line Input 2 Registers** Configures the gain from analog line input pin LIN2L to mixer input (Σ) and controls MUTE switch F. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	LI2_MODE	00	R/W	Configures Line Input 2 (right and left channel) in accordance with the connected input sources 00: inputs switched to single ended stereo 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: reserved, do not use.
5	MUTE_OFF_F	0	R/W	Control of MUTE switch F 0: left line input is set to mute 1: normal operation
4:0	LI2L_VOL	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN2L) to mixer input (N16) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 61 DAC_R Register

Name			**Base**	**Default**
DAC_R			**2-wire serial**	**00h**
Offset: 0Eh		**Right DAC Output Registers** Configures the gain from DAC output to mixer input (Σ) / MUX input. This register is reset when the block is disabled in AudioSet2 register (15h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5		000	n/a	
4:0	DAR_VOL	00000	R/W	Volume settings for right DAC output, adjustable in 32 steps @ 1.5dB; gain from DAC output (N19) to mixer/MUX input (N23). 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 62 DAC_L Register

Name			**Base**	**Default**
DAC_L			**2-wire serial**	**00h**
Offset: 0Fh		**Left DAC output Registers** Configures the gain from DAC output to mixer input (Σ) / MUX input and controls MUTE switch H. This register is reset when the block is disabled in AudioSet2 register (15h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	MUTE_OFF_H	0	R/W	Control of MUTE switch H 0: DAC output is set to mute 1: normal operation
5		0	n/a	
4:0	DAL_VOL	00000	R/W	Volume settings for left DAC output, adjustable in 32 steps @ 1.5dB: gain from DAC output (N22) to mixer/MUX input (N26). 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain 00000: -40.5 dB gain

Table 63 ADC_R Register

Name		Base		Default
ADC_R		**2-wire serial**		**00h**
Offset: 10h		**Right ADC input Registers** Configures MUX_A and the gain from MUX_A output to the ADC input This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	ADC_MUX_A	00	R/W	Connect MUX A output to following inputs 00: Microphone (N4/N6) 01: Line_IN1 (N1/N8) 10: Line_IN2 (N2/N7) 11: Audio SUM (N24/N25)
5		0	n/a	
4:0	ADR_VOL	00000	R/W	Volume settings for right ADC input, adjustable in 32 steps @ 1.5dB; gain from MUX_A output to ADC input (N9). 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 64 ADC_L Register

Name		Base		Default
ADC_L		**2-wire serial**		**00h**
Offset: 11h		**Left ADC input Registers** Configures the gain from MUX_A output to the ADC input and controls MUTE switch A. This register is reset when the block is disabled in AudioSet1 register (14h) or at a DVDD-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	MUTE_OFF_A	0	R/W	Control of MUTE switch A 0: ADC input is set to mute 1: normal operation
5		0	n/a	
4:0	ADL_VOL	00000	R/W	Volume settings for left ADC input, adjustable in 32 steps @ 1.5dB, gain from MUX_A output to ADC input (N18). 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain 00000: -34.5 dB gain

Table 65 Output Control Register

Name		**Base**		**Default**
OutContr1		**2-wire serial**		**00h**
Offset: 12h-1		**Q32k and PWGD Output Control Register**		
		Configures PWGD pin (Power Good) and Q32k pin (output of 32kHz oscillator). This is an extended register and needs to be enabled by writing 001b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	DRIVE_PWGD	00	R/W	Enables the PWGD output pin either to open-drain or push-pull and sets various driving strengths 00: 12mA push-pull output 01: 12mA open-drain output 10: 4mA push-pull output 11: 2mA push-pull output
5:4	MUX_PWGD	00	R/W	Multiplexes various digital signals to the PWGD output pin 00: PowerGood control signal 01: PWM signal to dim LEDs etc. 10: SPDIF converted from SDI to DAC 11: PLL output clock
3:2	DRIVE_Q32K	00	R/W	Enables the Q32k output pin either to open-drain or push-pull and sets various driving strengths 00: 12mA push-pull output 01: 12mA open-drain output 10: 4mA push-pull output 11: 2mA push-pull output
1:0	MUX_Q32K	00	R/W	Multiplexes various digital signals to the Q32k output pin 00: 32kHz RTC clock 01: PWM signal to dim LEDs etc. 10: SPDIF converted from SDI to DAC 11: PLL output clock

Table 66 SPDIF Register

Name		Base		Default
OutContr2_SPDIF		**2-wire serial**		**00h**
Offset: 12h-2		**SPDIF and Q24M Output Control Register** Adds status bits to the SPDIF bit-stream, configures the SPDIF output and the Q24M pin (output of 24MHz oscillator) This is an extended register and needs to be enabled by writing 010b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	DRIVE_Q24M	00	R/W	Enables the Q24M output pin either to open-drain or push-pull and sets various driving strengths 00: 12mA push-pull output 01: 12mA open-drain output 10: 4mA push-pull output 11: 2mA push-pull output
5	MUX_Q24M	0	R/W	Multiplexes various digital signals to the Q24M output pin 0: 24MHz oscillator clock 1: PLL output clock
4	SPDIF_COPY_OK	0		SPDIF copy control bit 0: copy not permitted 1: copy permitted
3	SPDIF_MCLK_INV	0		SPDIF master clock control bit 0: master clock 1: master clock inverted
2	SPDIF_INVALID	0		SPDIF sample status bit 0: sample valid 1: sample invalid
1:0	SPDIF_CNTR	00	R/W	SPDIF output ON/OFF control and sample rate status bits 00: SPDIF output OFF 01: SPDIF output ON (32kS) 10: SPDIF output ON (44.1kS) 11: SPDIF output ON (48kS)

Table 67 PWM Register

Name		Base		Default
PWM		**2-wire serial**		**00h**
Offset: 12h-3		**PWM Output Control Register** Sets the PWM output duty cycle and signal polarity. This is an extended register and needs to be enabled by writing 011b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWM_INVERTED	0	R/W	PWM output polarity 0: not inverted 1: inverted
6:0	PWM_CYCLE	0000000	R/W	Sets the PWM duty cycle Duty Cycle = PWM_CYCLE * 0.3937% PWM_CYCLE = 0 means no pulse

Table 68 AudioSet_1 Register

Name		Base		Default
AudioSet_1		**2-wire serial**		**00h**
Offset: 14h		**First Audio Set Register** Powers the various audio inputs and outputs UP or DOWN. Attention: This control register resets and holds microphone, line out, and ADC related registers in reset. After activation the required register settings need to be re-programmed. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ADC_R_ON	0	R/W	0: ADC right channel powered down 1: ADC right channel enabled for recording
6	ADC_L_ON	0	R/W	0: ADC left channel powered down 1: ADC left channel enabled for recording
5	LOUT2_ON	0	R/W	0: Line output 2 powered down 1: Line output enabled
4	LOUT1_ON	0	R/W	0: Line output 1 powered down 1: Line output enabled
3	LIN2_ON	0	R/W	0: Line input 2 powered down 1: Line input 2 enabled
2	LIN1_ON	0	R/W	0: Line input 1 powered down 1: Line input 1 enabled
1	MIC2_ON	0	R/W	0: Microphone input 2 powered down 1: Microphone input 1 enabled
0	MIC1_ON	0	R/W	0: Microphone input 1 powered down 1: Microphone input 1 enabled

Table 69 AudioSet_2 Register

Name			Base	Default
AudioSet_2			**2-wire serial**	**00h**
Offset: 15h		**Second Audio Set Register**		
		Powers various internal audio blocks UP or DOWN and controls bias current. Attention: This control register resets and holds DAC related registers in reset. After activation the required register settings need to be re-programmed. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BIAS_OFF	0	R/W	Power-down of the AGND bias. This bit can be set, if the AFE is used for digital data transfer and PMU functions only and all the analog audio blocks are not used. 0: bias enabled 1: bias disabled, for power saving in non audio mode
6	SUM_OFF	0	R/W	Power-down of ΣR and ΣL 0: Mixer stage enabled (limits output signal to 1Vp) 1: Mixer stage powered down
5	AGC_OFF	0	R/W	Switches the signal limiter OFF (N20/N21) 0: automatic gain control for summing stage enabled 1: automatic gain control for summing stage disabled
4:3	IBR_DAC<1:0>	00	R/W	Bias current settings for DAC: 00: 50% 01: 60% 10: 75% 11: 100%
2	DAC_ON	0	R/W	0: DAC powered down 1: DAC enabled
1:0				

Table 70 AudioSet_3 Register

Name				Base	Default
AudioSet_3				**2-wire serial**	**00h**
Offset: 16h		**Third Audio Set Register** Sets headphone output bias currents and operation modes and enables audio signal inputs to ΣR and ΣL. This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	LIN1MIX_OFF	0	R/W	Input from line input 1 to ΣR and ΣL 0: ON 1: OFF	
6	LIN2MIX_OFF	0	R/W	Input from line input 2 to ΣR and ΣL 0: ON 1: OFF	
5	MIC1MIX_OFF	0	R/W	Input from microphone 1 to ΣR and ΣL 0: ON 1: OFF	
4	MIC2MIX_OFF	0	R/W	Input from microphone 2 to ΣR and ΣL 0: ON 1: OFF	
3	DACMIX_OFF	0	R/W	Input from DAC to ΣR and ΣL 0: ON 1: OFF	
2	ZCU_OFF	0	R/W	Zero cross gain update of audio outputs. Audio gain settings changes will only be executed when the signal level is close to zero 0: zero cross update enabled 1: zero cross update disabled	
1	IBR_HPH	0	R/W	Bias current increase for the headphone amplifier depending on load conditions 0: 100% 1: 150%	
0	HPCM_ON	0	R/W	Power-up of the headphone common mode buffer: 0: headphone CM buffer is switched off 1: headphone CM buffer is switched on	

Table 71 PMU PVDD1 Register

Name		Base		Default
PMU PVDD1		**2-wire serial**		**00h**
Offset: 17h-1		**PVDD1 Low Drop-Out Regulator (LDO3) Control Register** This is an extended register and needs to be enabled by writing 001b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LDO_PVDD1_OFF	0	R/W	Power-down of LDO for PVDD1 0: PVDD1 (LDO3) enable 1: PVDD1 (LDO3) power-down
6		0	n/a	
5	PROG_PVDD1	0	R/W	Enables settings either selected by external pins (VPRGx) or settings stored in the 17h-1 register 0: VPRGx pins controlled 1: Register controlled
4:0	VSEL_PVDD1	00000	R/W	The voltage select bits set the LDO output in 2 different resolution ranges Range: 00h until 0Fh in 50mV steps PVDD1=1.2V+VSEL_PVDD1*50mV (1.2V until 1.95V) Range: 10h until 1Fh in 100mV steps PVDD1=2.0V+VSEL_PVDD1*100mV (2.0V until 3.5V)

Table 72 PMU PVDD2 Register

Name		Base		Default
PMU PVDD2		**2-wire serial**		**00h**
Offset: 17h-2		**PVDD2 Low Drop-Out Regulator (LDO4) Control Register** This is an extended register and needs to be enabled by writing 010b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LDO_PVDD2_OFF	0	R/W	Power-down of LDO for PVDD2 0: PVDD2 (LDO4) enable 1: PVDD2 (LDO4) power-down
6		0	n/a	
5	PROG_PVDD2	0	R/W	Enables settings either selected by external pin (VPRGx) or settings stored in the 17h-2 register 0: VPRGx pins controlled 1: Register controlled
4:0	VSEL_PVDD2	00000	R/W	The voltage select bits set the LDO output in 2 different resolution ranges Range: 00h until 0Fh in 50mV steps PVDD2=1.2V+VSEL_PVDD1*50mV (1.2V until 1.95V) Range: 10h until 1Fh in 100mV steps PVDD2=2.0V+VSEL_PVDD1*100mV (2.0V until 3.5V)

Table 73 PMU CVDD1 Register

Name				Base	Default
PMU CVDD1				**2-wire serial**	**00h**
Offset: 17h-3		**CVDD1 DC/DC Buck Regulator Control Register**			
		This is an extended register and needs to be enabled by writing 011b to Reg. 18h first. This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	SKIP_OFF_CVDD1	0	R/W	Disables pulse skip mode 0: 170mA current force / pulse skip mode enabled 1: current force / pulse skip mode disabled (only ON without load)	
6	PROG_CVDD1	0	R/W	Enables settings either selected by external pin (VPRGx) or settings stored in the 17h-3 register 0: VPRGx pins controlled 1: Register controlled	
5:0	VSEL_CVDD1	00000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00000: DC/DC powered down 01h until 38h in 50mV steps CVDD1=0.6V+VSEL_CVDD1*50mV (0.65V until 3.4V) 38h until 3Fh = 3.4V (no change)	

Table 74 PMU CVDD2 Register

Name				Base	Default
PMU CVDD2				**2-wire serial**	**0x00**
Offset: 17h-4		**CVDD2 DC/DC Buck Regulator Control Register**			
		This is an extended register and needs to be enabled by writing 100bto Reg. 18h first. This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	SKIP_OFF_CVDD2	0	R/W	Disables pulse skip mode 0: 170mA current force / pulse skip mode enabled 1: current force / pulse skip mode disabled (only ON without load)	
6	PROG_CVDD2	0	R/W	Enables settings either selected by external pin (VPRGx) or settings stored in the 17h-4 register 0: VPRGx pins controlled 1: Register controlled	
5:0	VSEL_CVDD2	00000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00000: DC/DC powered down 01h until 38h in 50mV steps CVDD2=0.6V+VSEL_CVDD1*50mV (0.65V until 3.4V) 38h until 3Fh = 3.4V (no change)	

Table 75 PMU CVDD3 Register

Name			Base	Default
PMU CVDD3			**2-wire serial**	**0x00**
Offset: 17h-5		**CVDD3 DC/DC Buck Regulator Control Register** This is an extended register and needs to be enabled by writing 101bto Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SKIP_OFF_CVDD3	0	R/W	Disables pulse skip mode 0: 170mA current force / pulse skip mode enabled 1: current force / pulse skip mode disabled (only ON without load)
6	PROG_CVDD3	0	R/W	Enables settings either selected by external pin (VPRGx) or settings stored in the 17h-5 register 0: VPRGx pins controlled 1: Register controlled
5:0	VSEL_CVDD3	00000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00000: DC/DC powered down 01h until 38h in 50mV steps CVDD2=0.6V+VSEL_CVDD1*50mV (0.65V until 3.4V) 38h until 3Fh = 3.4V (no change)

Table 76 PMU Hibernate Register

Name			Base	Default
PMU Hibernate			**2-wire serial**	**00h**
Offset: 17h-6		**PMU Hibernation Control Register (PVDD1/2, CVDD1/2/3, VLED)** Hibernation is started when writing to this register. This is an extended register and needs to be enabled by writing 110b to Reg. 18h first. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6	KEEP_PVDD2	0	R/W	Keeps the programmed PVDD2 level during hibernation 0: power down PVDD2 1: keep PVDD2
5	KEEP_PVDD1	0	R/W	Keeps the programmed PVDD1 level during hibernation 0: power down PVDD1 1: keep PVDD1
4	KEEP_VLED	0	R/W	Keeps the 15V DC/DC step-up for backlight switched on 0: power down CVDD1 1: keep CVDD1
3	KEEP_VBUS	0	R/W	Keeps the programmed VBUS level during hibernation 0: power down CVDD2 1: keep CVDD2
2	KEEP_CVDD3	0	R/W	Keeps the programmed CVDD3 level during hibernation 0: power down CVDD3 1: keep CVDD3
1	KEEP_CVDD2	0	R/W	Keeps the programmed CVDD2 level during hibernation 0: power down CVDD2 1: keep CVDD2
0	KEEP_CVDD1	0	R/W	Keeps the programmed CVDD1 level during hibernation 0: power down CVDD1 1: keep CVDD1

Table 77 PMU ENABLE Register

Name		Base		Default
PMU ENABLE		**2-wire serial**		**00h**
Offset: 18h		**PMU Extension Enable Register**		
		Enables 12h and 17h to write into extended registers and allows multiplexing supply voltages for monitoring via ADC10. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	n/a	
6:4	DC_TEST	000	R/W	Allows multiplexing internal and external supply voltages to one DC test node which can be further multiplexed to ADC10. The accuracy is 5mV/LSB (see reg. 2Eh) 000: not used 001: AVDD 010: DVDD 011: PVDD1 100: PVDD2 101: CVDD1 110: CVDD2 111: CVDD3
3	PMU_GATE	0	R/W	Enables all settings made in registers 0x17-x at once. If this bit is set, changes are activated as soon as they are written to the related register. 0: no change 1: change at once
0:2	PMU_WR_ENABLE	000	R/W	Enables extended registers 12h-x and 17h-x 000: not used 001: enables 17h-1 for PVDD1 settings enables 12h-1 for OutCntr1 settings 010: enables 17h-2 for PVDD2 settings enables 12h-2 for OutCntr2_SPDIF settings 011: enables 17h-3 for CVDD1 settings enables 12h-3 for PWM settings 100: enables 17h-4 for CVDD2 settings 101: enables 17h-5 for CVDD3 settings 110: enables 17h-6 for hibernation settings 111: not used

Table 78 RTC_WakeUp Register

Name		Base	Default
RTC_WakeUp		**2-wire serial**	**n/a**
Offset: 19h	**RTC Wake-Up and SRAM Register** Sets and enables the RTC wake-up counter and programs the 128bit SRAM. 3 bytes need to be written in a sequence to set the counter. The 3-byte sequence allows to set the counter to every value between 1sec and 8388608sec (=97 days). The MSB of the 3rd byte enables the wake-up counter. Byte 4 ...19 will program the static 128bit SRAM which is supplied by RVDD. This register is reset at a RVDD-POR.		

Adr.	Byte Name	Default	Access	Bit Description
7:0	WAKE_UP_BYTE0 (1st write to 0x19 is byte 0)	00h	R/W	0000 0001: 1sec 0000 0010: 2sec 0000 0100: 4sec 0000 1000: 8sec 0001 0000: 16sec 0010 0000: 32sec 0100 0000: 64sec 1000 0000: 128sec
7:0	WAKE_UP_BYTE1 (2nd write to 0x19 is byte 1)	00h	R/W	0000 0001: 256sec 0000 0010: 512sec 0000 0100: 1 024sec 0000 1000: 2 048sec 0001 0000: 4 096sec 0010 0000: 8 192sec 0100 0000: 16 384sec 1000 0000: 32 768sec
7:0	WAKE_UP_BYTE2 (3rd write to 0x19 is byte 2)	00h	R/W	000 0001: 65 536sec 000 0010: 131 072sec 000 0100: 262 144sec 000 1000: 524 288sec 001 0000: 1 048 576sec 010 0000: 2 097 152sec 100 0000: 4 194 304sec 0xxx xxxxxb = wake-up disabled 1xxx xxxxxb = wake-up enabled
7:0	SRAM_128 (4th … 19th write to 0x19 programs the 128bit static SRAM)	00000000	R/W	xxxx xxxxb = byte 4 : xxxx xxxxb = byte 19

Table 79 USB_UTIL Register

Name				Base	Default
USB_UTIL_DCDC				**2-wire serial**	**00h**
Offset: 1Ah		**USB Utility Register** Controls VBUS output voltage and the external transistor as well as special mode bits for the DCDC step-down converters This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	I_PMOS_GATE	00	R/W	Sets the gate current level into the external PMOS transistor to control the inrush current to VBUS 00: 1µA 01: 2µA 10: 3µA 11: 4µA	
5	DCDC_PS_OFF	0	R/W	Disables 200uA power saving in skip mode 0: Power savings ON 1: Power savings OFF	
4	DCDC_PMOS_OFF	0	R/W	Disables the PMOS of DCDC step down 1, 2 and 3 to be switched fully on, if the regulator cannot achieve the programmed output voltage anymore. 0: PMOS fully ON 1: PMOS switching	
3:2	VBUS_COMP_TH	00	R/W	Sets the threshold for the VBUS comparator. The output can be read in register 25h. 00: 4.5V 01: 3.18V 10: 1.5V 11: 0.6V	
1	VBUS_SKIP_ON	0	R/W	Enables the skip mode for the VBUS 1:2 charge pump which increases efficiency for small loads connected to VBUS supply, but increases VBUS supply ripple	
0	VBUS_ON	0	R/W	Switches the VBUS output voltage ON and OFF 0: VBUS output voltage disabled 1: VBUS output voltage enabled	

Table 80 DCDC15 Register

Name			Base	Default
DCDC15			**2-wire serial**	**00h**
Offset: 1Bh		**15V DCDC Step-up Control Register**		
		Controls the back-light current and back-light dim rate. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DIM_UP_DOWN	0	R/W	Starts dimming UP/DOWN or switches LED back-light ON/OFF when DIM_RATE = 00b 0: dim DOWN 1: dim UP
6:5	DIM_RATE	00	R/W	Sets the dim rate of the LED back-light current from 0mA to I_BACKLIGHT and vice versa 00: no dimming (immediate ON/OFF) 01: 150ms 10: 300ms 11: 500ms
4:0	I_BACKLIGHT	00000	R/W	Sets the current into pin ISINK in 1.25mA steps (internal current source to control LED backlight current). Setting 11111b enables the voltage feedback mode to supply e.g. OLEDs with a constant voltage supply. 00000: DCDC15 switched off 00001: 1.25mA 00010: 2.5mA .. 11110: 37.5mA 11111: 38.75mA

Table 81 I2S Register

Name			Base	Default
I2S			**2-wire serial**	**00h**
Offset: 1Ch		**I2S Mode Control Register (Master Mode only)**		
		Contains lower 8 bits for I2S master mode clock generation divider. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	I2S_DIVIDER	00h	R/W	Please see master clock divider table

Table 82 I2S_PLL_OSC Register

Name			Base		Default
I2S_PLL_OSC			**2-wire serial**		**00h**
Offset: 1Dh		**I2S, PLL and Oscillator Mode Control Registers** This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	I2S_MASTER_ON	0	R/W	Switched the I2S master mode on 0: I2S slave mode operation 1: I2S master mode	
6	OSC24_PD	0	R/W	Powers the 12-24MHz oscillator down. For operation a 12-24MHz crystal needs to be connected to pins XIN24/XOUT24. 0: 12-24MHz oscillator enabled 1: powered down	
5	I2S_DIRECT	0	R/W	Switches the PWGD pin to an input for an external master clock (e.g. coming form the CPU). This bit overwrites prior setting for the PWGD pin. Only valid fro I2S slave mode operation. 0: disabled 1: enabled	
4:3	Q24M_DIVIDER	00	R/W	Sets the divider for Q24M clock output or powers Q24M clock output buffer down 00: divide by 1 01:divide by 2 10:divide by 4 11: OFF	
2:1	PLL_MODE	00	R/W	Preset of PLL bias for the following sampling frequencies 00: reserved 01:16-48kS 10: 8-12kS 11: reserved	
0	I2S_DIVIDER_8	0	R/W	Bit 8 of I2S_DIVIDER (Reg. 1Ch) Please see master clock divider table	

Table 83 System Register

Name	Base	Default
System	**2-wire serial**	**E1h**

Offset: 20h		**System Settings Register** Controls the powering down conditions of the AFE. The IC can also be emergency shut down by a high level for 5.4sec (or 10.9sec see reg. 24h) at the PWRUP input pin This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Version <3:0>	1111	R	AFE number to identify the design version 1111: revision 7
3	HEARTBEAT_ON	0	R/W	Heartbeat (HBT) Watchdog The watchdog counter will be reset by a rising edge at the HBT input pin which has to occur at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. When start-up sequence #16-#25 is selected, no power down is performed but a reset invoked via the XRES output pin (pulse duration = 86µs typ., 60µs min) 0: HBT watchdog is disabled 1: HBT watchdog is enabled
2	JTEMP_OFF	0	R/W	Junction temperature supervision (level can be set in register 21h) 0: temperature supervision enabled 1: temperature supervision disabled
1	WATCHDOG_ON	0	R/W	2-wire serial interface watchdog To reset the watchdog counter a 2-wire serial read operation has to be performed at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. 0: watchdog is disabled 1: watchdog is enabled
0	PWR_HOLD	1	R/W	0: power up hold is cleared and AFE is powered down 1: set to on after power on

Table 84 Supervisor Register

Name		Base		Default
SUPERVISOR		**2-wire serial**		**00h**
Offset: 21h		**Supervisor Register** Sets the threshold levels of battery supply and junction temperature supervision. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	BVDD_SUP	000	R/W	Sets the threshold (brown-out voltage) at the BVDD input pin for an interrupt at low battery condition V_BrownOut=2.74+BVDD_Sup*60mV 000: 2.74V 001: 2.80V ... 110: 3.10V 111: 3.16V
4:0	JTEMP_SUP	00000	R/W	Sets the threshold for junction temperature emergency shutdown and junction temperature interrupt Invoke shutdown at: JTemp_SD=140-JTEMP_Sup*5°C Invoke interrupt at: JTemp_IRQ=120-JTEMP_Sup*5°C JT_Sup | IRQ | Shutdown **00000** | **120°C** | **140°C** 00001 | 115°C | 135°C . | . | . . | . | . 11110 | -30°C | -10°C 11111 | -35°C | -15°C

Table 85 Charger Register

Name		Base		Default
CHARGER		**2-wire serial**		**00h**
Offset: 22h		**Charger Control Register** Sets the charging current, end of charge voltage and battery temp. supervision. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BAT_TEMP_OFF	0	R/W	0: enables 15uA supply for external 100k NTC resistor 1: disables supply
6:4	CHG_I	000	R/W	set maximum charging current 111: 400 mA 110: 350 mA 101: 300 mA 100: 250 mA 011: 200 mA 010: 150 mA 001: 100 mA 000: 50 mA
3:1	CHG_V	000	R/W	set maximum charger voltage in 50mV steps 111: 4.25 V 110: 4.2 V .. 001: 3.95 V 000: 3.9 V
0	CHG_OFF	0	R/W	0: enables Charger 1: disables Charger

Table 86 First Interrupt Register

Name	Base	Default
IRQ_ENRD_0	**2-wire serial**	**00h**

Offset: 23h	**First Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.

Bit	Bit Name	Default	Access	Bit Description
7	CVDD2_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD2 occurs 0: disable 1: enable
	CVDD2_UNDER	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
6	CVDD2_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD2 0: disable 1: enable
	CVDD2_OVER	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
5	CVDD1_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD1 occurs 0: disable 1: enable
	CVDD1_UNDER	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
4	CVDD1_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD1 0: disable 1: enable
	CVDD1_OVER	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
3	PVDD2_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD2 occurs 0: disable 1: enable
	PVDD2_UNDER	x	R	This bit is set when a –5% under-voltage at PVDD2 occurs
2	PVDD2_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD2 0: disable 1: enable
	PVDD2_OVER	x	R	This bit is set when a +5% over-voltage at PVDD2 occurs
1	PVDD1_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD1 occurs 0: disable 1: enable
	PVDD1_UNDER	x	R	This bit is set when a –5% under-voltage at PVDD1 occurs
0	PVDD1_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD1 0: disable 1: enable
	PVDD1_OVER	x	R	This bit is set when a +5% over-voltage at PVDD1 occurs

Table 87 Second Interrupt Register

Name		Base		Default
IRQ_ENRD_1		**2-wire serial**		**00h**
Offset: 24h		**Second Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SD_TIME	0	R/W	Control bit which sets the emergency shut-down time from 5.4sec to 10.9sec. The shut-down of AS3517 is invoked by a high signal at the PWRUP input pin. 0: 5.4sec 1: 10.9sec
6		0	n/a	
5	PWRUP_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the PWRUP input pin occurs 0: disable 1: enable
		x	R	This bit is set whenever a high level of min. BVDD/3 at the PWRUP input pin occurs (PWRUP pin is commonly connected to the power-up button)
4	WAKEUP_IRQ	0	W	Enables interrupt which is invoked whenever a wake-up from RTC wake-up counter occurs 0: disable 1: enable
		X	R	This bit is set when a wake-up has been invoked by the RTC wake-up counter.
3	VOXM2_IRQ	0	W	Enables interrupt which is invoked by reaching a voltage threshold at MIC2 input (voice activation) 0: disable 1: enable
		x	R	This bit is set when a voltage threshold of $5mV_{RMS}$ (unfiltered) at MIC2 has been reached (voice activation)
2	VOXM1_IRQ	0	W	Enables interrupt which is invoked by reaching a voltage threshold at MIC1 input (voice activation) 0: disable 1: enable
		x	R	This bit is set when a voltage threshold of $5mV_{RMS}$ (unfiltered) at MIC1 has been reached (voice activation)
1	CVDD3_EN_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD2 occurs 0: disable 1: enable
	CVDD3_UNDER	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
0	CVDD3_EN_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD2 0: disable 1: enable
	CVDD3_OVER	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs

Table 88 Third Interrupt Register

Name		Base		Default
IRQ_ENRD_2		**2-wire serial**		**00h**
Offset: 25h		**Third Interrupt Register**		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BATTEMP_HIGH (level)	0	W	Battery over-temperature interrupt setting. 0: disable 1: enable interrupt if battery temperature exceeds 45°C The interrupt must not be enabled if the charger block and battery temperature supervision is disabled
		x	R	Battery over-temperature interrupt reading 0: battery temperature below 45°C 1: battery temperature was too high and the charger was turned off. The charger will be turned on again, when the temperature gets below 42°C
6	CHG_EOC (level)	0	W	Battery end of charge interrupt setting 0: disable 1: enable The interrupt must not be enabled if the charger block is disabled
		x	R	Battery end of charge interrupt reading 0: battery charging in progress 1: charging is complete, charging current is below 10% of nominal current, turn off charger To check end of charge again the charger has to be turned on.
5	CHG_STATUS	x	R	0: no charger input source connected 1: charger input source connected, also valid if charger is connected during wakeup
4	CHG_CHANGED (status change)	0	W	Charger input status change interrupt setting 0: disable 1: enables an interrupt on a low to high or high to low change of CHGIN pin.
		x	R	Charger input status change interrupt reading 0: charger input status not changed 1: charger input status changed, check CHG_STATUS
3	USB_STATUS	x	R	0: no USB input connected 1: USB input connected, also valid if USB is connected during wakeup. The threshold can be set in the USB_UTIL register (1Ah)
2	USB_CHANGED (status change)	0	W	USB input status change interrupt setting 0: disable 1: enables an interrupt on a low to high or high to low change of VBUS pin. The threshold can be set in the USB_UTIL register (1Ah)
		x	R	USB input status change interrupt reading 0: USB input status not changed 1: USB input status changed, check USB_STATUS

Name		Base		Default
IRQ_ENRD_2		**2-wire serial**		**00h**
Offset: 25h		**Third Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		

Bit	Bit Name	Default	Access	Bit Description
1	RVDD_LOW (level)	0	W	Real time clock supply (RVDD) under-voltage interrupt setting 0: disable 1: enable
		x	R	Real time clock supply interrupt reading 0: RTC supply o.k. 1: RTC supply (RVDD) was low, RTC not longer valid The interrupt gets set in hibernation or during power-up even if the interrupt is not enabled thus allowing to recognise a change of the battery connected to BVDDR during hibernation or shutdown. For a valid reading, the interrupt has to be enabled first.
0	BVDD_LOW (level)	0	W	BVDD under-voltage supervisor interrupt setting 0: disable 1: enable
		x	R	BVDD supervisor interrupt setting 0: BVDD is above brown out level 1: BVDD has reached brown out level The threshold can be set in the SUPERVISOR register (24h)

Table 89 Fourth Interrupt Register

Name	Base	Default
IRQ_ENRD_3	**2-wire serial**	**0x00**

Offset: 26h	**Fourth Interrupt Register**
	Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.

Bit	Bit Name	Default	Access	Bit Description
7	JTEMP_HIGH (level)	0	W	Supervisor junction over-temperature interrupt setting 0: disable 1: enable
		x	R	Supervisor junction over-temperature interrupt reading 0: chip temperature below threshold 1: chip temperature has reached the threshold The threshold can be set in the SUPERVISOR register (21h)
6		0	n/a	
5	HPH_OVC (level)	0	W	Headphone over-current interrupt setting 0: disable 1: enable The interrupt must not be enabled if the headphone block is disabled
		x	R	Headphone over-current interrupt reading 0: no over-current detected 1: headphone over-current detected, headphone amplifier was shut down. The current thresholds are 150mA at HPR / HPL pin or 300mA at HPCM pin. The shut-down time can be set in HPH_OUT_R register (0x02)
4	I2S_STATUS	x	R	0: no LRCK on I2S interface detected 1: LRCK on I2S interface present
3	I2S_CHANGED (status change)	0	W	I2S input status change interrupt setting 0: disable 1: enable
		x	R	I2S input status change interrupt reading 0: I2S input status not changed 1: I2S input status changed, check I2S_status
2	MIC2_CONNECT (level)	0	W	Microphone 2 connect detection interrupt setting 0: disable 1: enable
		x	R	Microphone 2 connect detection interrupt reading 0: no microphone connected to MIC input 1: microphone connected at MIC input. This interrupt is only invoked when the microphone stage is powered down. The IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current.
1	MIC1_CONNECT (level)	0	W	Microphone 1 connect detection interrupt setting 0: disable 1: enable
		x	R	Microphone 1 connect detection interrupt reading 0: no microphone connected to MIC input 1: microphone connected at MIC input. This interrupt is only invoked when the microphone stage is powered down. The IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current.

Name				Base	Default
IRQ_ENRD_3				**2-wire serial**	**0x00**
Offset: 26h		**Fourth Interrupt Register**			
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	HPH_CONNECT (level)	0	W	Headphone connect detection interrupt setting 0: disable 1: enable	
		x	R	Headphone connect detection interrupt reading 0: no headphone connected 1: headphone connected This interrupt is only invoked when the headphone stage is powered down. The IRQ will be released after enabling the headphone stage. Detecting a headphone during operation is not possible.	

Table 90 Fifth Interupt Register

Name		Base		Default
IRQ_ENRD_4		**2-wire serial**		**0x00**
Offset: 27h		**Fifth Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	T_DEB<1:0>	00	R/W	Sets the USB and Charger connect de-bounce time: 00: 340ms 01: 170ms 10: 85ms 11: 4ms
5	XIRQ_AH	0	R/W	Sets the active output state of the XIRQ line: 0: IRQ is active low 1: IRQ is active high
4	XIRQ_PP	0	R/W	Sets the XIRQ output buffer type: 0: IRQ output is open drain 1: IRQ output is push pull
3	REM2_DET (edge)	0	W	Microphone 2 remote key press detection interrupt setting 0: disable 1: enable
		x	R	Microphone 2 remote key press detection interrupt reading 0: no key press detected 1: Microphone 2 supply current got increased, remote key press detected -> measure MICS supply current
2	REM1_DET (edge)	0	W	Microphone 1 remote key press detection interrupt setting 0: disable 1: enable
		x	R	Microphone 1 remote key press detection interrupt reading 0: no key press detected 1: Microphone 1 supply current got increased, remote key press detected -> measure MICS supply current
1	RTC_UPDATE (edge)	0	W	RTC timer interrupt setting 0: disable 1: enable
		x	R	RTC timer interrupt reading 0: no RTC interrupt occurred 1: RTC timer interrupt occurred. Selecting minute or second interrupt can be done via RTCT register (29h)
0	ADC_EOC (edge)	0	W	ADC end of conversion interrupt setting 0: disable 1: enable
		x	R	ADC end of conversion interrupt reading 0: ADC conversion not finished 1: ADC conversion finished. Read out ADC_0 and ADC_1 register to get the result (2Eh & 2Fh)

Table 91 RTCV Register

Name				Base	Default
RTCV				**2-wire serial**	**23h**
Offset: 28h		**RTC Voltage Register**			
		This register is reset at a DVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	V_RVDD	0010	R/W	Selects the RVDD output voltage level (1V to 2.5V) Default: 1.2V RVDD= 1V + V_RVDD*0.1V	
3:2					
1	RTC_ON	1	R/W	RTC counter clock control: 0: Disable clock for RTC counter 1: Enables clock for RTC counter	
0	OSC32_ON	1	R/W	Switches the 32kHz oscillator ON A 32kHz watch crystal need to be connected to pins XIN32/XOUT32 0: Disable 32kHz oscillator 1: Enables 32kHz oscillator	

Table 92 RTCV Register

Name				Base	Default
RTCT				**2-wire serial**	**40h**
Offset: 29h		**RTC Timing Register**			
		This register is reset at a RVDD-POR.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	IRQ_MIN	0	R/W	0: generates an interrupt every second 1: generates an interrupt every minute The interrupt has to be enable in IRQ_ENRD_4 (27h)	
6:0	RTC_TBC<6:0>	1000000	R/W	These bits are used to correct the inaccuracy of the used 32kHz crystal. Trimming register for RTC, 128 steps @ 7.6ppm 000000: 1 (7.6ppm) 000001: 2 (15.2ppm) ... 100000: 64 (488ppm) ... 111110: 126 (960.8ppm) 111111: 127 (968.4ppm)	

Table 93 RTC_0 to RTC_3 Register

Name				Base	Default
RTC_0 to RTC_3				**2-wire serial**	**00 00 00 00h**
Offset: 2Ah to 2Dh		**RTC Time-base Seconds Register**			
		This register is reset at a RVDD-POR.			
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**	
2Ah	RTC_0	00h	R/W	QRTC<7:0>; RTC seconds bits 0 to 7	
2Bh	RTC_1	00h	R/W	QRTC<15:8>; RTC seconds bits 8 to 15	
2Ch	RTC_2	00h	R/W	QRTC<23:9>; RTC seconds bits 9 to 23	
2Dh	RTC_3	00h	R/W	QRTC<31:24>; RTC seconds bits 24 to 31	

Table 94 ADC_0 Register

Name			Base	Default
ADC_0			**2-wire serial**	**0000 00xx**
Offset: 2Eh		**First 10-bit ADC Register**		
		Writing to this register will start the measurement of the selected source. This register is reset at a DVDD-POR, exception are bit 8 and 9.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ADC_Source	00000000	R/W	Selects ADC input source 0000: CHGOUT 0001: BVDDR 0010: defined by DC_TEST in register 0x18 0011: CHGIN 0100: VBUS 0101: BatTemp 0110: MIC1S 0111: MIC2S 1000: VBE_1uA 1001: VBE_2uA 1010: I_MIC1S 1011: I_MIC1S 1100: RVDD 1101: reserved 1110: reserved 1101: reserved
3:2		00	n/a	
1:0	ADC<9:8>	xx	R/W	ADC result bit 9 to 8

Table 95 ADC_1 Register

Name			Base	Default
ADC_1			**2-wire serial**	**xxxx xxxx**
Offset: 2Fh		**Second 10-bit ADC Register**		
		This register is not reset.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ADC<7:0>	xxxx xxxx	R/W	ADC result bit 7 to 0

Table 96 UID_0 to UID_7 Register

Name			Base	Default
UID_0 to UID_7			**2-wire serial**	**n/a**
Offset: 38h to 3Fh		**Unique ID Register**		
		This register is read only and is not reset.		
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**
38h	UID_0	n/a	R	Unique ID byte 0
39h	UID_1	n/a	R	Unique ID byte 1
3Ah	UID_2	n/a	R	Unique ID byte 2
3Bh	UID_3	n/a	R	Unique ID byte 3
3Ch	UID_4	n/a	R	Unique ID byte 4
3Dh	UID_5	n/a	R	Unique ID byte 5
3Eh	UID_6	n/a	R	Unique ID byte 6
3Fh	UID_7	n/a	R	Unique ID byte 7

10 Typical Application

Figure 32 Typical Application Schematic 1

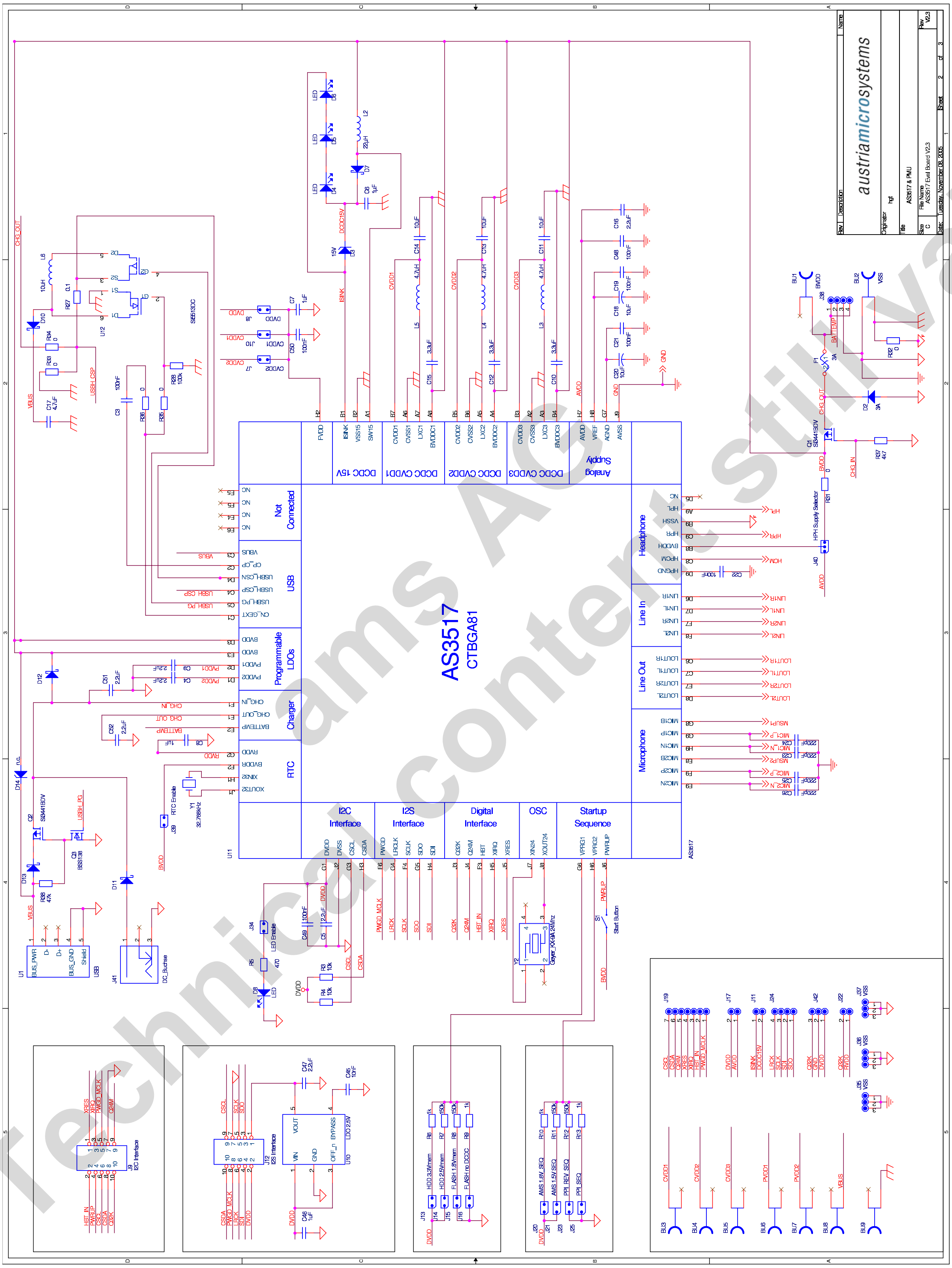
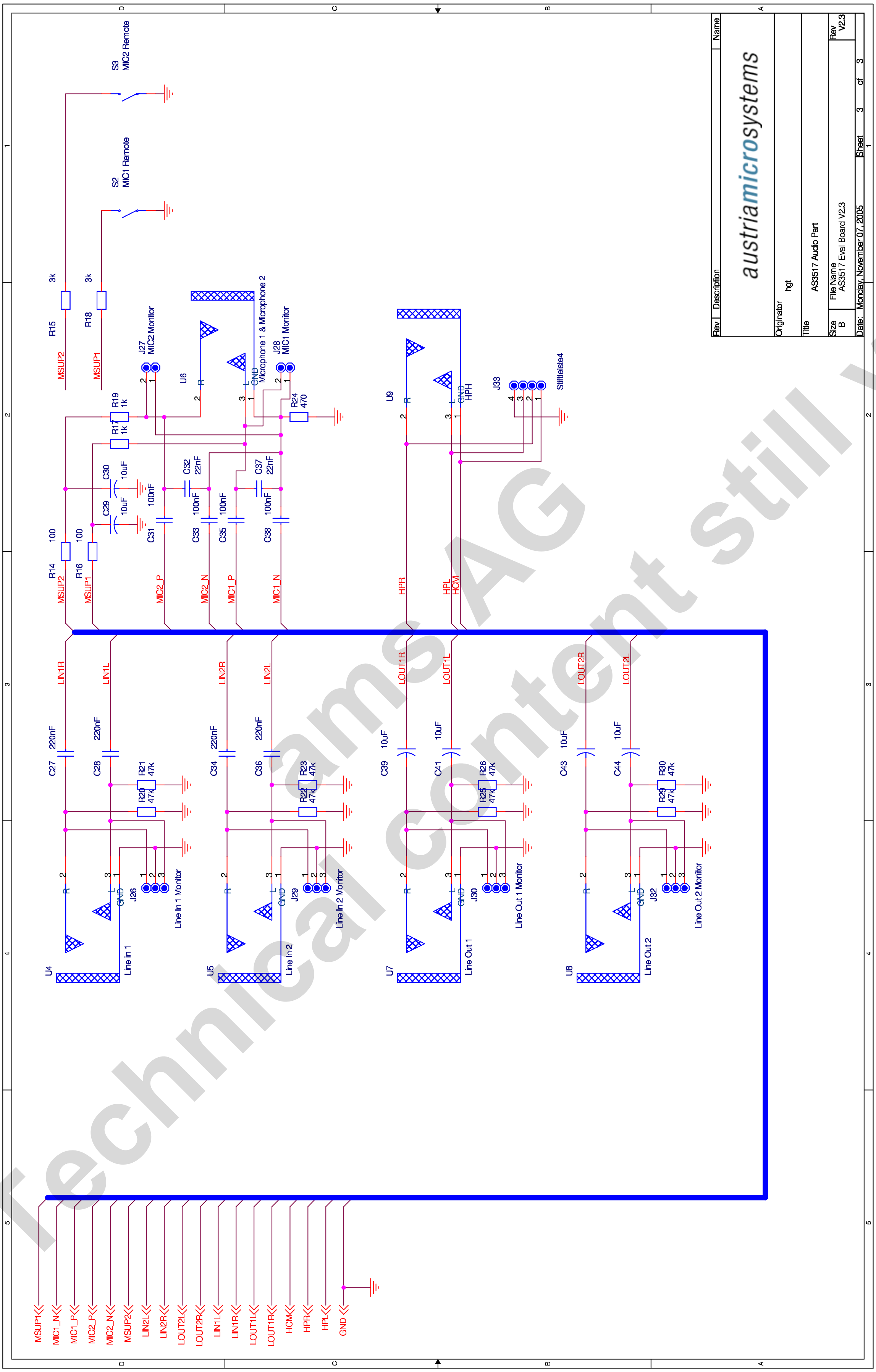


Figure 33 Typical Application Schematic 2



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