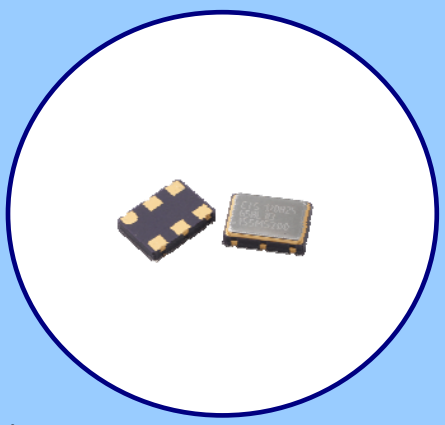
Model 353
HCMOS VCXO

FEATURES
- **Standard 5.0mm x 3.2mm 6-Pad Surface Mount Package**
- **HCMOS Output**
- **Low Jitter Performance**
- **Fundamental Crystal Designs**
- Frequency Range 1 – 80 MHz
- Operating Voltages +2.5Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS
Model 353 is ideal for applications such as broadband access, Ethernet/Gigabit Ethernet, SONET/SDH, xDSL, PCMIA, digital video, Picocells and base stations.

ORDERING INFORMATION

353 □ □ □ □ □ □ □ □ □

SUPPLY VOLTAGE
- N = +2.5 Vdc, Pin 2 Enable
- L = +3.3 Vdc, Pin 2 Enable
- S = +5.0 Vdc, Pin 2 Enable
- T = +2.5 Vdc, Pin 5 Enable
- V = +3.3 Vdc, Pin 5 Enable
- W = +5.0 Vdc, Pin 5 Enable

ABSOLUTE PULL RANGE [APR]
- B = ± 50 ppm APR

FREQUENCY STABILITY
- 6 = ± 20 ppm [2]
- 3 = ± 50 ppm
- 5 = ± 25 ppm

PACKAGING OPTIONS
- T - 1k pcs./reel
- R - 3k pcs./reel

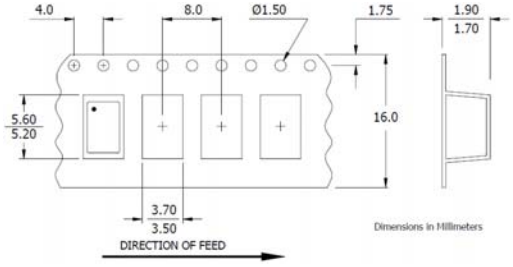
FREQUENCY
- Product Frequency Code [1]

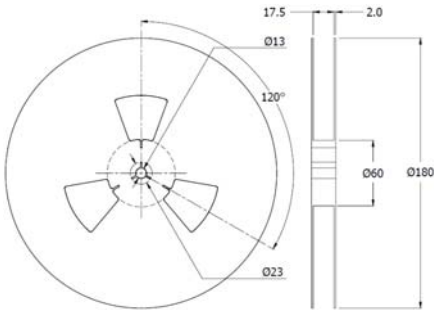
OPERATING TEMPERATURE RANGE
- A = -10°C to +60°C
- C = -20°C to +70°C
- I = -40°C to +85°C [2]

1] Refer to document 016-1454-0, Frequency Code Tables.
3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.
2] Consult factory for availability of 6I Stability/Temperature combination.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]
Device quantity is 1k pcs. maximum per 180mm reel.





ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL PARAMETERS	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
	Storage Temperature	T_{STG}	-	-40	-	+100	°C
	Frequency Range	f_O	-		1 - 80		MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_O$	-	-	-	20, 25 or 50	± ppm
	Absolute Pull Range (See Note 2 and Ordering Information)	APR	-	±50	-	-	ppm
	Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC} and V_C	-3	-	3	ppm
	Operating Temperature	T_A	-	-10	+25	+60	°C
				-20		+70	
				-40		+86	
	Supply Voltage	V_{CC}	Model 353N, 353T, ±5%	2.38	2.5	2.63	V
			Model 353L, 353V, ±5%	3.14	3.3	3.47	
			Model 353S, 353W, ±5%	4.75	5.0	5.25	
	Supply Current	I_{CC}	C_L = 15 pF				mA
			@ +2.5Vdc	-	-	25	
			@ +3.3Vdc	-	-	25	
			@ +5.0Vdc	-	-	30	
	Output Load	C_L	-	-	-	15	pF
	Control Voltage	V_C	Model 353N, 353T, V_{CC} = 2.5V	0.20	1.25	2.30	V
			Model 353L, 353V, V_{CC} = 3.3V	0.15	1.65	3.15	
			Model 353S, 353W, V_{CC} = 5.0V	0.50	2.50	4.50	
	Frequency Deviation	Δf	+25°C @ Time of Shipment, over V_C range	±100	-	-	ppm
	Linearity	L	Best Straight Line Fit	-	-	10	%
	Input Impedance	Z_{Vc}	-	10	-	-	kOhms
	Transfer Function	-	-		Positive		-
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Output Voltage Levels	V_{OH}	Logic '1' Level, CMOS Load	$0.9V_{CC}$	-	-	V
		V_{OL}	Logic '0' Level, CMOS Load	-	-	$0.1V_{CC}$	
	Rise and Fall Time	T_R, T_F	@ 20%/80% Levels	-	3	8.0	ns
	Start Up Time	T_S	Application of V_{CC}	-	5	10	ms
	Modulation Roll-off	-	@ -3dB	12	-	-	kHz
	Enable Function						V
	Enable Input Voltage	V_{IH}	Pin 2 or Pin 5 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	
	Disable Input Voltage	V_{IL}	Pin 2 or Pin 5 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	
	Enable Time	T_{PLZ}	Pin 2 or Pin 5 Logic '1'	-	-	100	ns
	Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	0.5	1	ps

1. Notes:
2. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1year aging. Minimum guaranteed frequency shift from f_O over variations in temperature, aging, power supply and load.

ENABLE TRUTH TABLE

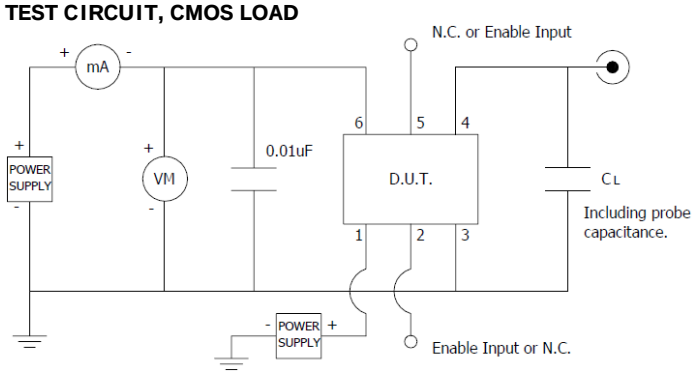
PIN 2 or Pin 5	PIN 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

SINGLE SIDE BAND PHASE NOISE (typical maximum)

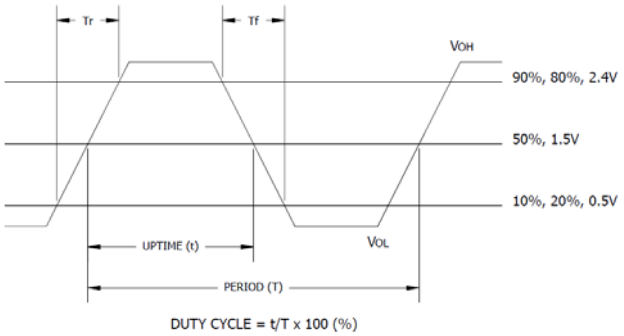
Frequency Offset	Phase Noise (dBc/Hz) *	Frequency Offset	Phase Noise (dBc/Hz) *
10 Hz	-60	10k Hz	-135
100 Hz	-90	100k Hz	-150
1k Hz	-120	>100k Hz	-150

* Results may vary depending on frequency.

TEST CIRCUIT, CMOS LOAD

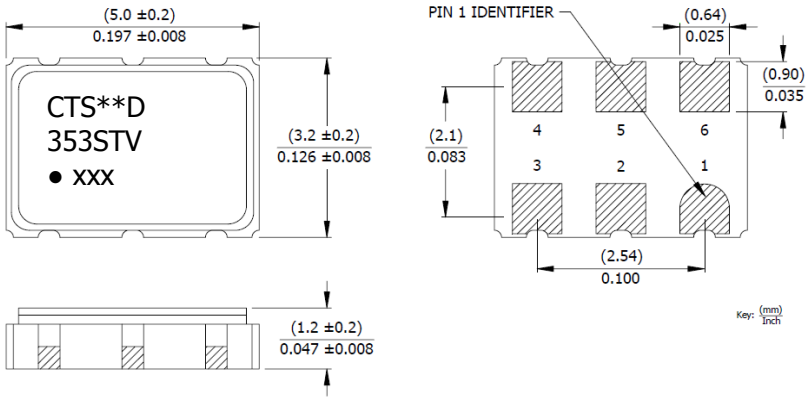


OUTPUT WAVEFORM, CMOS



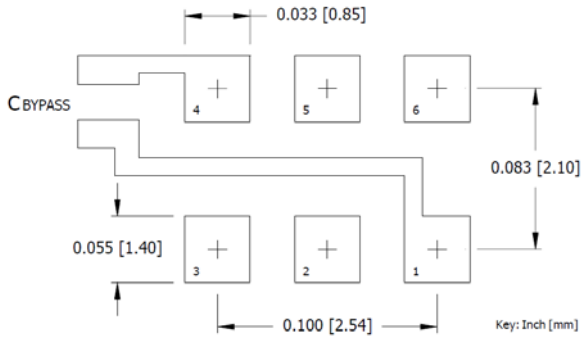
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. D – Date Code. See Table I for codes.
3. ST – Frequency stability/temperature code. [Refer to Ordering Information.]
4. V – Voltage code. N or T = 2.5V, L or V = 3.3V, S or W = 5.0V
5. xxx – Frequency Code. 3-digits, frequencies below 100MHz

Refer to document 016-1454-0, Frequency Code Tables.

NOTES

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
2. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
4. MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	V_C	Control Voltage
2	EOH or N.C.	Enable [std] or No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C. or EOH	No Connect or Enable [opt]
6	V_{CC}	Supply Voltage

TABLE I – DATE CODE

YEAR \ MONTH	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001 2005 2009 2013 2017	A	B	C	D	E	F	G	H	J	K	L	M
2002 2006 2010 2014 2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003 2007 2011 2015 2019	a	b	c	d	e	f	g	h	j	k	l	m
2004 2008 2012 2016 2020	n	p	q	r	s	t	u	v	w	x	y	z