SAF7167AHW

YUV-to-RGB digital-to-analog converter

Rev. 01 — 29 June 2004 Product data sheet

1. General description

The SAF7167AHW is a mixed-mode designed IC containing a video data path, keying control block, analog mixer, and a voltage output amplifier, capable of converting digital video data to analog RGB video, and then mixing video and external analog RGB inputs.

The video data path contains a data re-formatter, YUV-to-RGB colour space matrix as well as triple DACs for video data processing. An analog mixer performs multiplexing between DAC outputs of the video path and external analog RGB inputs.

The final analog outputs are buffered with built-in voltage output amplifiers to provide the direct driving capability for a 150 Ω load. See the overall block diagram.

The operation of SAF7167AHW is controlled via the I^{2}C-bus.

2. Features

- On-chip mixing of digital video data and analog RGB signals
- Supports video input format of YUV 4 : 2 : 2, 4 : 1 : 1, 2 : 1 : 1 and RGB 5 : 6 : 5
- Video input rate up to 66 MHz
- Allows for both binary and twos complement video input data
- Triple 8-bit DACs for video output
- Built-in voltage output amplifier
- Provides keying control with external key and internal 8-bit, 2 × 8-bit and 3 × 8-bit pixel colour key
- Programmable via the I^{2}C-bus
- 5 V CMOS device; HTQFP48 package.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
T_{amb}	ambient temperature		–40	-	+85	°C

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAF7167AHW	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-1

5. Block diagram

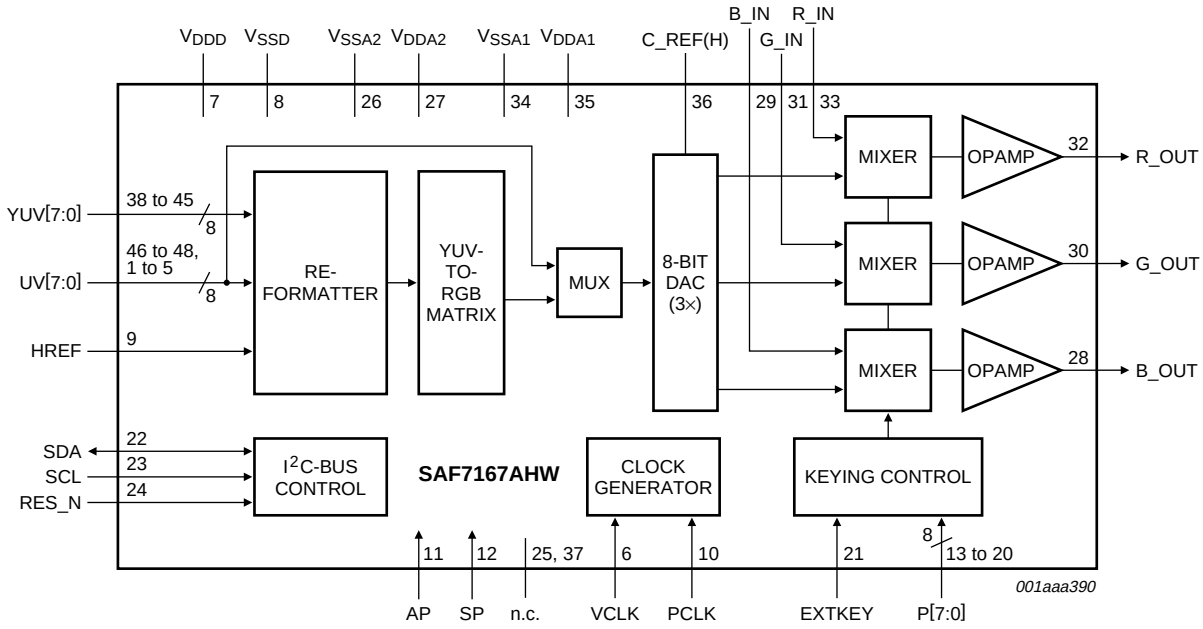


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

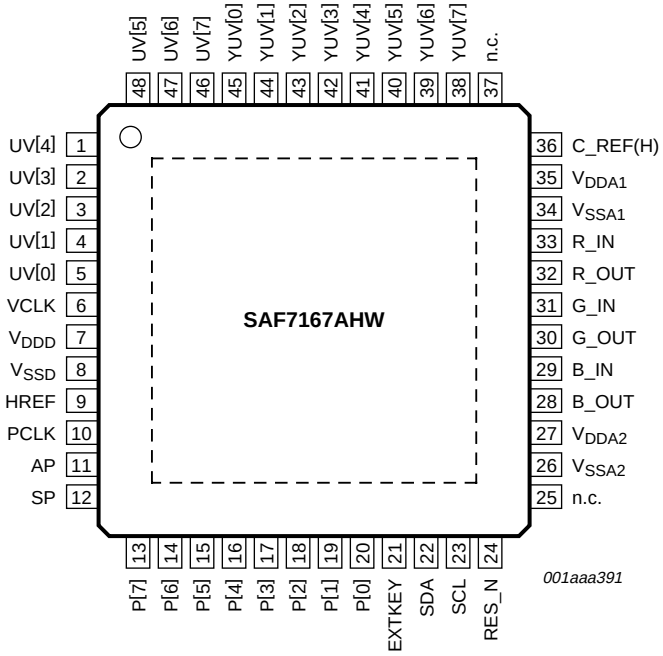


Fig 2. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Type [1]	Description
UV[4]	1	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[3]	2	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[2]	3	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[1]	4	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[0]	5	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
VCLK	6	I	video clock input
V_{DDD}	7	S	digital supply voltage
V_{SSD}	8	S	digital ground
HREF	9	I	horizontal reference input signal
PCLK	10	I	pixel clock input
AP	11	I	test pin, normally connected to ground
SP	12	I	test pin, normally connected to ground

Table 3: Pin description *...continued*

Symbol	Pin	Type [1]	Description
P[7]	13	I	pixel bus input 7 (for keying control)
P[6]	14	I	pixel bus input 6 (for keying control)
P[5]	15	I	pixel bus input 5 (for keying control)
P[4]	16	I	pixel bus input 4 (for keying control)
P[3]	17	I	pixel bus input 3 (for keying control)
P[2]	18	I	pixel bus input 2 (for keying control)
P[1]	19	I	pixel bus input 1 (for keying control)
P[0]	20	I	pixel bus input 0 (for keying control)
EXTKEY	21	I	external key signal input
SDA	22	I/O	I^2C-bus data line
SCL	23	I	I^2C-bus clock line
RES_N	24	I	resetting the I^2C-bus (active LOW)
n.c.	25	-	not connected
V_{SSA2}	26	S	analog ground 2
V_{DDA2}	27	S	analog supply voltage 2
B_OUT	28	O	analog blue signal output
B_IN	29	I	analog blue signal input
G_OUT	30	O	analog green signal output
G_IN	31	I	analog green signal input
R_OUT	32	O	analog red signal output
R_IN	33	I	analog red signal input
V_{SSA1}	34	S	analog ground 1
V_{DDA1}	35	S	analog supply voltage 1
C_REF(H)	36	S	de-coupling capacitor for internal reference voltage (2.25 V)
n.c.	37	-	not connected
YUV[7]	38	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[6]	39	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[5]	40	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[4]	41	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[3]	42	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[2]	43	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[1]	44	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data
YUV[0]	45	I	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data

Table 3: Pin description *...continued*

Symbol	Pin	Type [1]	Description
UV[7]	46	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[6]	47	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data
UV[5]	48	I	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data

[1] I = input; I/O = input or output; O = output; S = supply.

7. Functional description

The SAF7167AHW contains a video data path, 3 analog mixers and voltage output amplifiers for the RGB channels respectively, a keying control block as well as an I^2C-bus control block.

7.1 Video data path

The video data path includes a video data re-formatter, a YUV-to-RGB colour space conversion matrix, and triple 8-bit DACs.

7.1.1 Re-formatter

The re-formatter de-multiplexes the different video formats YUV 4 : 1 : 1, 4 : 2 : 2 or 2 : 1 : 1 to internal YUV 4 : 4 : 4, which can then be processed by the RGB matrix. The pixel byte sequences of those video input formats are shown in Table 4 to Table 7.

Table 4: Pixel byte sequence of 4 : 2 : 2

Input	Pixel byte sequence of 4 : 2 : 2					
YUV0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y data	0	1	2	3	4	5
UV data	0	0	2	2	4	4

Table 5: Pixel byte sequence of 4 : 1 : 1

Input	Pixel byte sequence of 4 : 1 : 1							
YUV0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	X	X	X	X	X	X	X	X
UV1	X	X	X	X	X	X	X	X
UV2	X	X	X	X	X	X	X	X
UV3	X	X	X	X	X	X	X	X
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y data	0	1	2	3	4	5	6	7
UV data	0	0	0	0	4	4	4	4

Table 6: Pixel byte sequence of 2 : 1 : 1

Input	Pixel byte sequence of 2 : 1 : 1							
YUV0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
YUV1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
YUV2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
YUV3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
YUV4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
YUV5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
YUV6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
YUV7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y data	X	0	X	2	X	4	X	6
UV data	0	X	0	X	4	X	4	X

Table 7: Pixel byte sequence of 5 : 6 : 5

Input	Pixel byte sequence of RGB 5 : 6 : 5			
UV7	G0	G0	G0	G0
UV6	R4	R4	R4	R4
UV5	R3	R3	R3	R3
UV4	R2	R2	R2	R2
UV3	R1	R1	R1	R1
UV2	R0	R0	R0	R0
UV1	G5	G5	G5	G5

Table 7: Pixel byte sequence of 5 : 6 : 5 *...continued*

Input	Pixel byte sequence of RGB 5 : 6 : 5			
UV0	G4	G4	G4	G4
YUV7	G3	G3	G3	G3
YUV6	G2	G2	G2	G2
YUV5	G1	G1	G1	G1
YUV4	B4	B4	B4	B4
YUV3	B3	B3	B3	B3
YUV2	B2	B2	B2	B2
YUV1	B1	B1	B1	B1
YUV0	B0	B0	B0	B0
RGB data	0	1	2	3

For RGB 5 : 6 : 5 video inputs, the video data are just directly bypassed to triple DACs.

The input video data can be selected to either twos complement (I^2C-bus bit DRP = 0) or binary offset (I^2C-bus bit DRP = 1). The video input format is selected by I^2C-bus bits FMTC[1:0].

The rising edge of HREF input defines the start of active video data. When HREF is inactive, the video output will be blanked.

7.1.2 YUV-to-RGB matrix

The matrix converts YUV data, in accordance with ITU-R BT.601, to RGB data with approximately 1.5 LSB deviation to the theoretical values for 8-bit resolution.

7.1.3 Triple 8-bit DACs

Three identical DACs for R, G and B video outputs are designed with voltage-drive architecture to provide high-speed operation of up to 66 MHz conversion data rate. Pin C_REF(H) is provided to allow for one external de-coupling capacitor to be connected between the internal reference voltage source and ground.

7.2 Analog mixers and keying control

The analog mixers are controlled to switch between the outputs from the video DACs and analog RGB inputs by a keying signal. The analog RGB inputs need to interface with analog mixers in the way of DC-coupling, also these RGB inputs are limited to RGB signals without a sync level pedestal. The keying control can be enabled by setting I^2C-bus bit KEN = 1. Two kinds of keying are possible to generate: one is external key (from EXTKEY pin when KMOD[2:0] are all logic 0), and the other is the internal pixel colour key (when KMOD[2:0] are not all logic 0) generated by comparing the input pixel data with the internal I^2C-bus register value KD[7:0]. Controlled by KMOD[2:0] bits, there are 4 ways to compare the pixel data (see Table 8).

Table 8: KMOD[2:0]

KMOD[2:0]	Pixel type	Remark
100	8-bit pixel	pseudo colour mode
101	2 × 8-bit pixel	high colour mode 1 with pixels given at both rising and falling edges of PCLK
110	2 × 8-bit pixel	high colour mode 2 with pixels given only at rising edges of PCLK
111	3 × 8-bit pixel	true colour mode

Since only one control register KD[7:0] provides the data value for pixel data comparison, when at 2 × 8-bit or 3 × 8-bit pixel input modes, it is presumed that all input bytes (lower, middle or higher) of each pixel must be the same as KD[7:0] in order to make graphics colour key active.

The polarity of EXTKEY can be selected with KINV. With KINV = 0, EXTKEY = HIGH switches analog mixers to select DAC outputs. Before the internal keying signal switches the analog multiplexers, it can be further delayed up to 7 PCLK cycles with the control bits KDLY[2:0].

7.3 Voltage output amplifiers

Before the analog input enters the analog mixers, it passes through voltage output amplifiers. Level shifters are used internally to provide an offset of 0.2 V and an amplifier gain of 2 for analog inputs to match with the output levels from DACs. After buffering with voltage output amplifiers, the final RGB outputs can drive a 150 Ω load directly (25 Ω internal resistor, 47 Ω external serial resistor, and 75 Ω load resistor) at the monitor side (see Figure 9).

The output voltage level of DAC ranges from the lowest level 0.2 V (zero code) to the highest level 1.82 V (all one code).

With the digital input YUV video data in accordance with ITU-R BT.601, the RGB output of 8-bit DAC actually ranges from the 16th step (black) to the 235th step (white). Therefore, after the voltage divider with external serial resistor and monitor load resistor, the output voltage range to a monitor is approximately 0.7 V (p-p).

7.4 I²C-bus control

Only one control byte is needed for the SAF7167AHW. The I²C-bus format is shown in Table 9.

Table 9: I²C-bus format

S [1]	SLAVE ADDRESS [2]	A [3]	SUBADDRESS [4]	A [3]	DATA [5]	A [3]	P [6]

[1] S = START condition.

[2] SLAVE ADDRESS = 1011 111X; X = R/$\overline{W}$ control bit. X = 0: order to write. X = 1: order to read (not used for SAF7167AHW).

[3] A = acknowledge; generated by the slave.

[4] SUBADDRESS = subaddress byte.

[5] DATA = data byte.

[6] P = STOP condition.

Table 10: Control data byte

Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
00	KMOD2	KMOD1	KMOD0	DRP	KEN	KINV	FMTC1	FMTC0
01	0	0	0	0	0	KDLY2	KDLY1	KDLY0
02	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

Table 11: Bit functions in data byte; Table note 1 and Table note 2

Bit	Description
FMTC[1:0]	video format control: 00: YUV 4 : 2 : 2 01: YUV 4 : 1 : 1 10: YUV 2 : 1 : 1/ITU-R BT.656 11: RGB 5 : 6 : 5
KINV	key polarity: KINV = 0: pin EXTKEY = HIGH for analog mixer to select DAC outputs KINV = 1: pin EXTKEY = HIGH for analog mixer to select analog RGB inputs
KEN	key enable: 0 = disable 1 = enable
DRP	UV input data code: 0 = twos complement 1 = binary offset
KMOD[2:0]	keying mode: 000: external key 100: 8-bit pixel colour key 101: 2 × 8-bit pixel colour key (with two-edge clock latching for pixel input) 110: 2 × 8-bit pixel colour key (with one-edge clock latching for pixel input) 111: 3 × 8-bit pixel colour key (with one-edge clock latching for pixel input) all other combinations are reserved
KDLY[2:0]	added keying delay cycles (from 0 to 7 PCLK cycles)
KD[7:0]	the data value compared for 8, 16 or 24-bit pixel colour key

[1] All I^2C-bus control bits are initialized to logic 0 after RES_N is activated.

[2] PCLK should be active in any event to allow for correct operation of I^2C-bus programming.

8. Limiting values

Table 12: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins and all supply pins connected together.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDD}	digital supply voltage		–0.5	+7.0	V
V_{DDA}	analog supply voltage		–0.5	+7.0	V
$V_{I(D)}$	digital input voltage		–0.5	+7.0	V
$V_{I(A)}$	analog input voltage		–0.5	+7.0	V
V_{diff}	voltage difference between V_{SS} pins		-	100	mV
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{esd}	electrostatic discharge voltage:				
	human body model	[1]	-	±2000	V
	machine model	[2]	-	±200	V

[1] Class 2 according to EIA/JESD22-114-B.

[2] Class B according to EIA/JESD22-115-A.

9. Thermal characteristics

Table 13: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	34 [1]	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAF7167AHW with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

10. Static characteristics

Table 14: Static characteristics

T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	f_{clk} = 27 MHz	-	130	-	mA
$V_{IH(SDA)}$	HIGH-level input voltage on pin SDA		3	-	V_{DDD} + 0.5	V
$V_{IL(SDA)}$	LOW-level input voltage on pin SDA		–0.5	-	+1.5	V
V_{IH}	HIGH-level digital input voltage		2	-	-	V
V_{IL}	LOW-level digital input voltage		-	-	0.8	V
V_i	full-scale analog RGB at input pins		-	0.7	-	V

Table 14: Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_o	full-scale analog RGB at output pins	with 125 Ω external load	1.250	1.375	1.500	V
DNL	differential non-linearity error of video output		-	-	1	LSB
INL	integral non-linearity error of video output		-	-	1	LSB

11. Dynamic characteristics

Table 15: Dynamic characteristics

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VCLK							
f_{clk}	video clock rate			-	-	66	MHz
δ	duty factor of VCLK			40	50	60	%
PCLK							
f_{clk}	pixel clock rate:						
	8-bit pixel colour key	see Figure 4		-	-	77.5	MHz
	2 × 8-bit pixel colour key; mode 1	see Figure 5		-	-	50	MHz
	2 × 8-bit pixel colour key; mode 2	see Figure 6		-	-	80	MHz
	3 × 8-bit pixel colour key	see Figure 7		-	-	77.5	MHz
δ	duty factor of PCLK			40	50	60	%
t_{su1}	digital input set-up time to VCLK rising edge			3	-	-	ns
t_{h1}	digital input hold time to VCLK rising edge			2	-	-	ns
t_{su2}	digital input set-up time to PCLK rising edge			0	-	-	ns
t_{h2}	digital input hold time to PCLK rising edge			4.2	-	-	ns
t_{su3}	digital input set-up time to PCLK falling edge			–1	-	-	ns
t_{h3}	digital input hold time to PCLK falling edge			6	-	-	ns
t_{sw}	switching time between video DAC outputs and analog inputs		[1]	-	-	15	ns
T_{group}	overall group delay from digital video inputs to analog outputs:						
	YUV video input mode	see Figure 8		-	$20T_{VCLK} + t_{PD}$	-	ns
	RGB video input mode	see Figure 8		-	$12T_{VCLK} + t_{PD}$	-	ns
t_r	DAC analog output rise time	see Figure 8	[2]	-	3.5	-	ns
t_f	DAC analog output fall time	see Figure 8	[2]	-	3.5	-	ns
t_s	DAC analog output settling time	see Figure 8	[3]	-	16.5	-	ns
t_{PD}	DAC analog output propagation delay	see Figure 8	[4]	-	20	-	ns

Table 15: Dynamic characteristics *…continued*

T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog outputs from analog inputs						
G_v	voltage gain		-	2.0	-	
B	bandwidth	at –3 dB	160	-	-	MHz
SR	slew rate		100	110	-	V/µs

[1] Switching time measured from the 50 % point of the EXTKEY transition edge to the 50 % point of the selected analog output transition.

[2] DAC output rise and fall times measured between the 10 % and 90 % points of full-scale transition.

[3] DAC settling time measured from the 50 % point of full-scale transition to the output remaining within ±1 LSB.

[4] DAC analog output propagation delay measured from the 50 % point of the rising edge of VCLK to the 50 % point of full-scale transition.

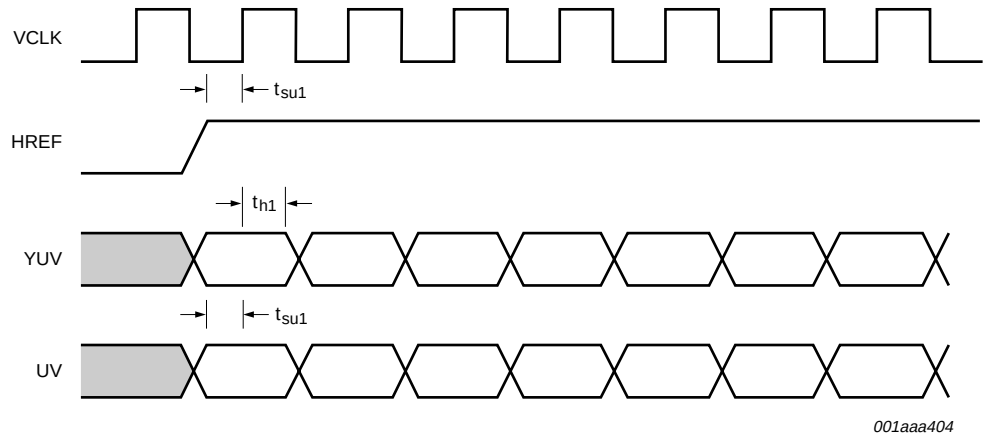


Fig 3. Video data input timing.

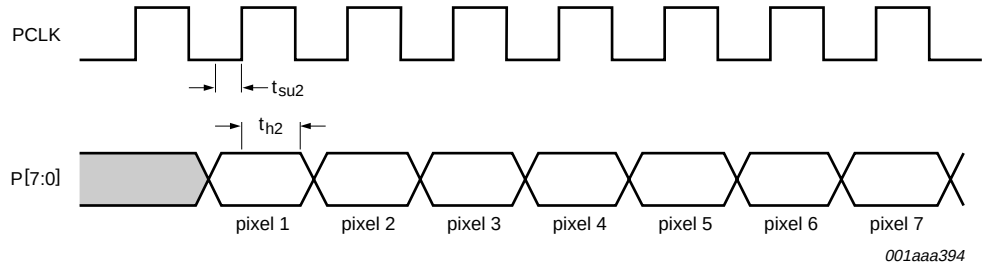


Fig 4. Pixel data input timing; 8-bit pixel colour key.

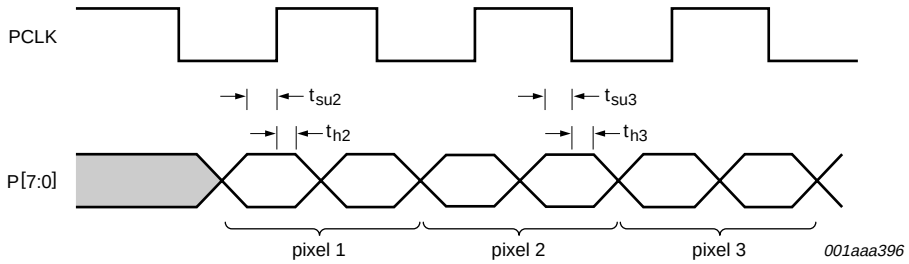


Fig 5. Pixel data input timing; 2 × 8-bit pixel colour key; mode 1.

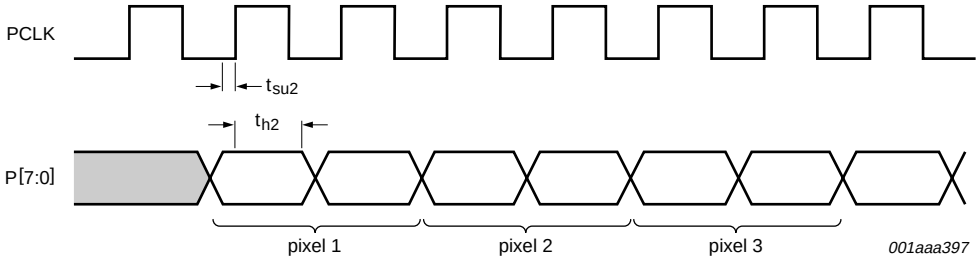


Fig 6. Pixel data input timing; 2 × 8-bit pixel colour key; mode 2.

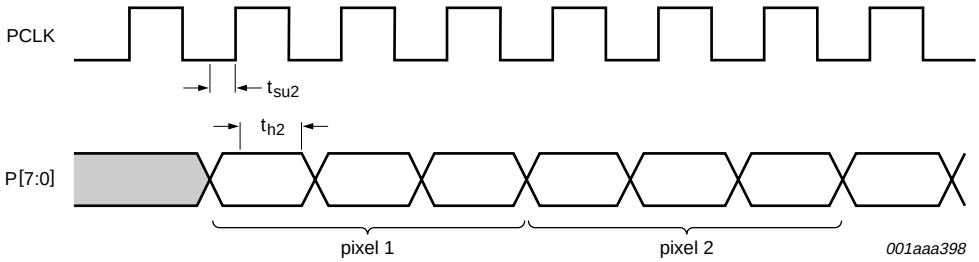


Fig 7. Pixel data input timing; 3 × 8-bit pixel colour key.

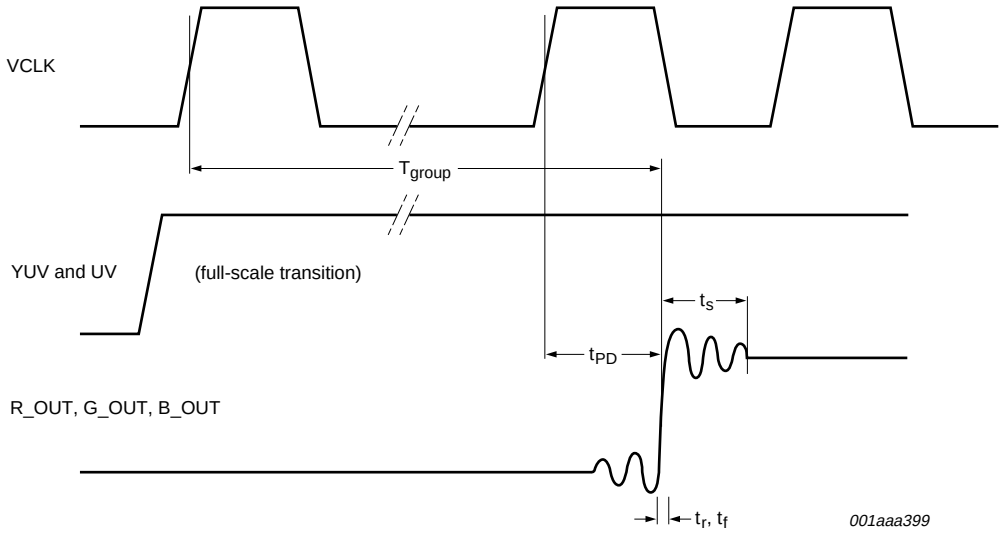


Fig 8. DAC output timing.

12. Application information

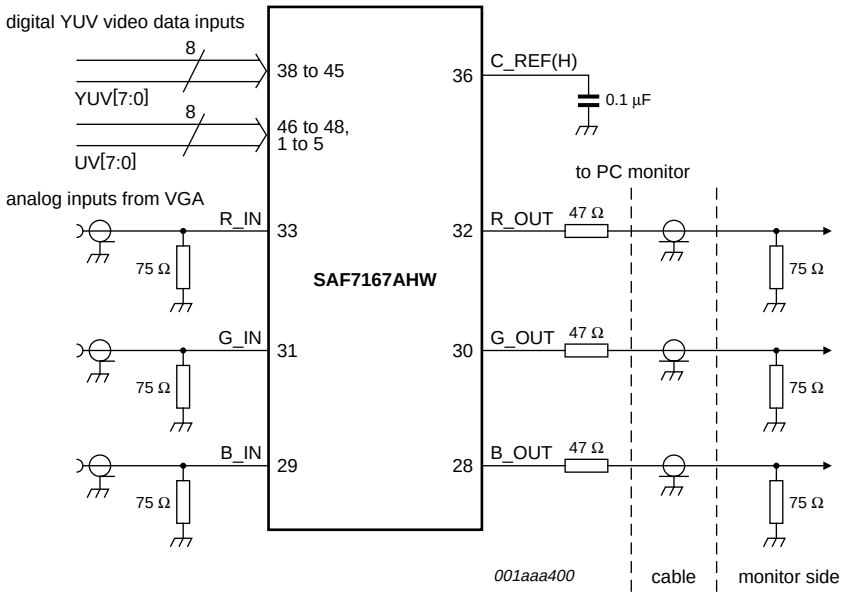
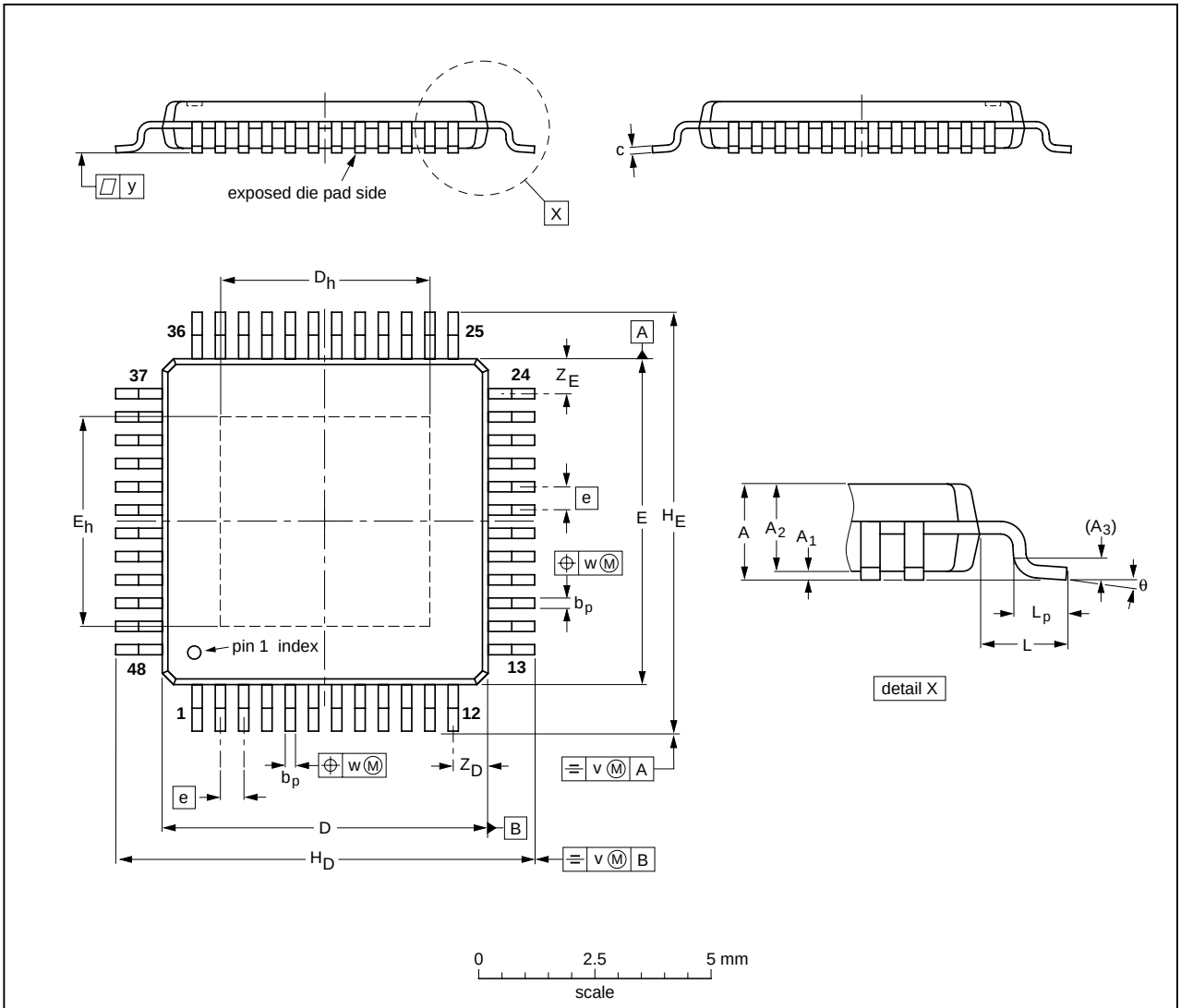


Fig 9. Typical application diagram for analog circuits.

13. Package outline

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad

SOT545-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.9 0.6	0.9 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2		MS-026				~~03-04-07~~ 04-01-29

Fig 10. Package outline diagram.

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 16: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Revision history

Table 17: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
SAF7167AHW_1	20040629	Product data	-	9397 750 12667	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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21. Contents

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