



Single/Dual/Quad, Low-Cost, SOT23, Micropower Rail-to-Rail I/O Op Amps

MAX4040-MAX4044

General Description

The MAX4040-MAX4044 family of micropower op amps operates from a single +2.4V to +5.5V supply or dual $\pm 1.2V$ to $\pm 2.75V$ supplies and have rail-to-rail input and output capabilities. These amplifiers provide a 90kHz gain-bandwidth product while using only 10 μA of supply current per amplifier. The MAX4041/MAX4043 have a low-power shutdown mode that reduces supply current to less than 1 μA and forces the output into a high-impedance state. The combination of low-voltage operation, rail-to-rail inputs and outputs, and ultra-low power consumption makes these devices ideal for any portable/battery-powered system.

These amplifiers have outputs that typically swing to within 10mV of the rails with a 100k Ω load. Rail-to-rail input and output characteristics allow the full power-supply voltage to be used for signal range. The combination of low input offset voltage, low input bias current, and high open-loop gain makes them suitable for low-power/low-voltage precision applications.

The MAX4040 is offered in a space-saving 5-pin SOT23 package. All specifications are guaranteed over the -40°C to +85°C extended temperature range.

Applications

Battery-Powered Systems	Strain Gauges
Portable/Battery-Powered Electronic Equipment	Sensor Amplifiers
Digital Scales	Cellular Phones
	Notebook Computers
	PDA's

Selector Guide

PART	NO. OF AMPS	SHUTDOWN	PIN-PACKAGE
MAX4040	1	—	5-pin SOT23, 8-pin μ MAX/SO
MAX4041	1	Yes	8-pin μ MAX/SO
MAX4042	2	—	8-pin μ MAX/SO
MAX4043	2	Yes	10-pin μ MAX/14-pin SO
MAX4044	4	—	14-pin SO

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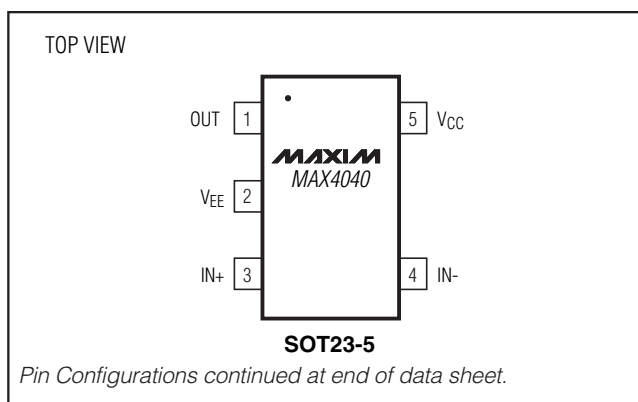
Features

- ◆ Single-Supply Operation Down to +2.4V
- ◆ Ultra-Low Power Consumption:
 - 10 μA Supply Current per Amplifier
 - 1 μA Shutdown Mode (MAX4041/MAX4043)
- ◆ Rail-to-Rail Input Common-Mode Range
- ◆ Outputs Swing Rail-to-Rail
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ 200 μV Input Offset Voltage
- ◆ Unity-Gain Stable for Capacitive Loads up to 200pF
- ◆ 90kHz Gain-Bandwidth Product
- ◆ Available in Space-Saving 5-Pin SOT23 and 8-Pin μ MAX[®] Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4040EUK-T	-40°C to +85°C	5 SOT23-5	ACGF
MAX4040EUA	-40°C to +85°C	8 μ MAX	—
MAX4040ESA	-40°C to +85°C	8 SO	—
MAX4041ESA	-40°C to +85°C	8 SO	—
MAX4041EUA	-40°C to +85°C	8 μ MAX	—
MAX4042EUA	-40°C to +85°C	8 μ MAX	—
MAX4042ESA	-40°C to +85°C	8 SO	—
MAX4043EUB	-40°C to +85°C	10 μ MAX	—
MAX4043ESD	-40°C to +85°C	14 SO	—
MAX4044ESD	-40°C to +85°C	14 SO	—

Pin Configurations



Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}).....+6V
 All Other Pins($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)
 Output Short-Circuit Duration to V_{CC} or V_{EE}Continuous
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....571mW
 8-Pin μMAX (derate 4.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....330mW
 8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....471mW

10-Pin μMAX (derate 5.6mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....444mW
 14-Pin SO (derate 8.33mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....667mW
 Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range -65°C to $+160^\circ\text{C}$
 Lead Temperature (soldering, 10s)..... $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS— $T_A = +25^\circ\text{C}$

($V_{CC} = +5.0V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC} / 2$, $\overline{\text{SHDN}} = V_{CC}$, $R_L = 100k\Omega$ tied to $V_{CC} / 2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply-Voltage Range	V_{CC}	Inferred from PSRR test		2.4		5.5	V
Supply Current per Amplifier	I_{CC}	$V_{CC} = 2.4V$			10		μA
		$V_{CC} = 5.0V$			14	20	
Shutdown Supply Current per Amplifier	$I_{CC}(\overline{\text{SHDN}})$	$\overline{\text{SHDN}} = V_{EE}$, MAX4041 and MAX4043 only	$V_{CC} = 2.4V$		1.0		μA
			$V_{CC} = 5.0V$		2.0	5.0	
Input Offset Voltage	V_{OS}	$V_{EE} \leq V_{CM} \leq V_{CC}$	MAX4044ESD		± 0.20	± 2.0	mV
			MAX404_EU_		± 0.25	± 2.5	
			All other packages		± 0.20	± 1.50	
Input Bias Current	I_B	(Note 1)			± 2	± 10	nA
Input Offset Current	I_{OS}	(Note 1)			± 0.5	± 3.0	nA
Differential Input Resistance	$R_{IN}(\text{DIFF})$	$ V_{IN+} - V_{IN-} < 1.0V$			45		$M\Omega$
		$ V_{IN+} - V_{IN-} > 2.5V$			4.4		$k\Omega$
Input Common-Mode Voltage Range	V_{CM}	Inferred from the CMRR test		V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} \leq V_{CM} \leq V_{CC}$			65	94	dB
		All other packages			70	94	
Power-Supply Rejection Ratio	PSRR	$2.4V \leq V_{CC} \leq 5.5V$		75	85		dB
Large-Signal Voltage Gain	A_{VOL}	$(V_{EE} + 0.2V) \leq V_{OUT} \leq (V_{CC} - 0.2V)$		$R_L = 100k\Omega$		94	dB
				$R_L = 25k\Omega$	74	85	
Output Voltage Swing High	V_{OH}	Specified as $ V_{CC} - V_{OH} $		$R_L = 100k\Omega$		10	mV
				$R_L = 25k\Omega$		60	
Output Voltage Swing Low	V_{OL}	Specified as $ V_{EE} - V_{OL} $		$R_L = 100k\Omega$		10	mV
				$R_L = 25k\Omega$		40	
Output Short-Circuit Current	$I_{OUT}(\text{SC})$	Sourcing			0.7		mA
		Sinking			2.5		
Channel-to-Channel Isolation		Specified at DC, MAX4042/MAX4043/MAX4044 only			80		dB

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MAX4040-MAX4044

ELECTRICAL CHARACTERISTICS— $T_A = +25^\circ\text{C}$ (continued)

($V_{CC} = +5.0\text{V}$, $V_{EE} = 0\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = V_{CC} / 2$, $\overline{\text{SHDN}} = V_{CC}$, $R_L = 100\text{k}\Omega$ tied to $V_{CC} / 2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current in Shutdown	$I_{OUT(\overline{\text{SHDN}})}$	$\overline{\text{SHDN}} = V_{EE} = 0$, MAX4041/MAX4043 only (Note 2)		20	100	nA
$\overline{\text{SHDN}}$ Logic Low	V_{IL}	MAX4041/MAX4043 only		0.3 x V_{CC}		V
$\overline{\text{SHDN}}$ Logic High	V_{IH}	MAX4041/MAX4043 only	0.7 x V_{CC}			V
$\overline{\text{SHDN}}$ Input Bias Current	I_{IH}, I_{IL}	MAX4041/MAX4043 only		40	120	nA
Gain Bandwidth Product	GBW			90		kHz
Phase Margin	Φ_m			68		degrees
Gain Margin	G_m			18		dB
Slew Rate	SR			40		V/ms
Input Voltage Noise Density	e_n	$f = 1\text{kHz}$		70		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density	i_n	$f = 1\text{kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Capacitive-Load Stability		$A_{VCL} = +1\text{V/V}$, no sustained oscillations		200		pF
Power-Up Time	t_{ON}			200		μs
Shutdown Time	$t_{\overline{\text{SHDN}}}$	MAX4041 and MAX4043 only		50		μs
Enable Time from Shutdown	t_{EN}	MAX4041 and MAX4043 only		150		μs
Input Capacitance	C_{IN}			3		pF
Total Harmonic Distortion	THD	$f_{IN} = 1\text{kHz}$, $V_{OUT} = 2\text{V}_{p-p}$, $A_v = +1\text{V/V}$		0.05		%
Settling Time to 0.01%	t_s	$A_v = +1\text{V/V}$, $V_{OUT} = 2V_{STEP}$		50		μs

ELECTRICAL CHARACTERISTICS— $T_A = T_{MIN}$ to T_{MAX}

($V_{CC} = +5.0\text{V}$, $V_{EE} = 0\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = V_{CC} / 2$, $\overline{\text{SHDN}} = V_{CC}$, $R_L = 100\text{k}\Omega$ tied to $V_{CC} / 2$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply-Voltage Range	V_{CC}	Inferred from PSRR test	2.4		5.5	V
Supply Current per Amplifier	I_{CC}				28	μA
Shutdown Supply Current per Amplifier	$I_{CC(\overline{\text{SHDN}})}$	$\overline{\text{SHDN}} = V_{EE}$, MAX4041 and MAX4043 only			6.0	μA
Input Offset Voltage	V_{OS}	$V_{EE} \leq V_{CM} \leq V_{CC}$	MAX4044ESA		± 4.5	mV
			MAX4044_EU_		± 5.0	
			All other packages		± 3.5	
Input Offset Voltage Drift	TC_{VOS}			2		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	(Note 1)			± 20	nA
Input Offset Current	I_{OS}	(Note 1)			± 8	nA

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ELECTRICAL CHARACTERISTICS— $T_A = T_{MIN}$ to T_{MAX} (continued)

($V_{CC} = +5.0V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC} / 2$, $\overline{SHDN} = V_{CC}$, $R_L = 100k\Omega$ tied to $V_{CC} / 2$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Inferred from the CMRR test	V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} \leq V_{CM} \leq V_{CC}$	MAX404_EU_	60		dB
			All other packages	65		
Power-Supply Rejection Ratio	PSRR	$2.4V \leq V_{CC} \leq 5.5V$	70			dB
Large-Signal Voltage Gain	A_{VOL}	$(V_{EE} + 0.2V) \leq V_{OUT} \leq (V_{CC} - 0.2V)$, $R_L = 25k\Omega$	68			dB
Output Voltage Swing High	V_{OH}	Specified as $ V_{CC} - V_{OH} $, $R_L = 25k\Omega$			125	mV
Output Voltage Swing Low	V_{OL}	Specified as $ V_{EE} - V_{OL} $, $R_L = 25k\Omega$			75	mV

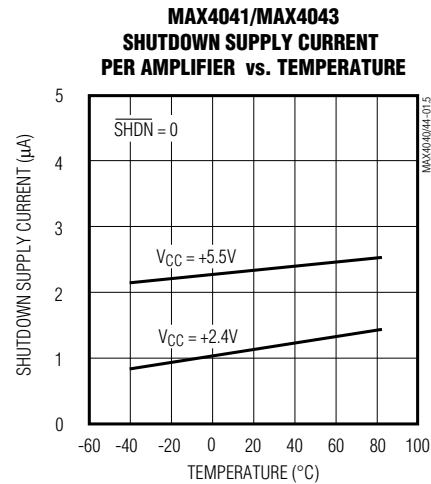
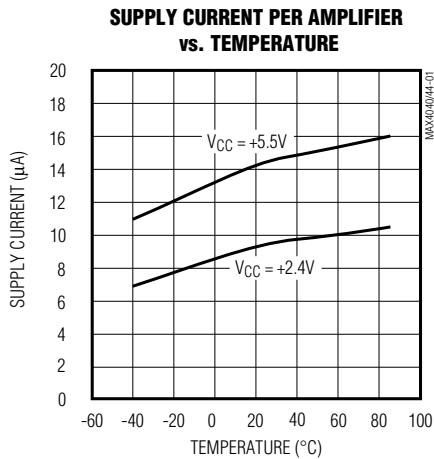
Note 1: Input bias current and input offset current are tested with $V_{CC} = +5.0V$ and $+0.5V \leq V_{CM} \leq +4.5V$.

Note 2: Tested for $V_{EE} \leq V_{OUT} \leq V_{CC}$. Does not include current through external feedback network.

Note 3: All devices are 100% tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

Typical Operating Characteristics

($V_{CC} = +5.0V$, $V_{EE} = 0$, $V_{CM} = V_{CC} / 2$, $\overline{SHDN} = V_{CC}$, $R_L = 100k\Omega$ to $V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

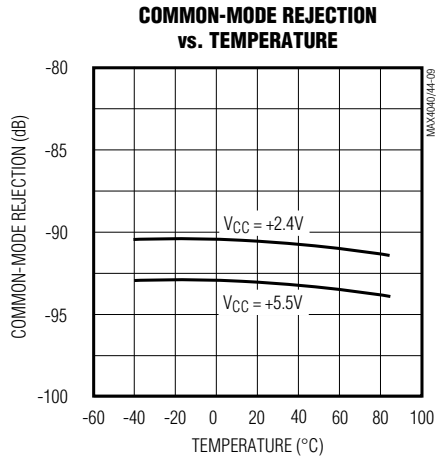
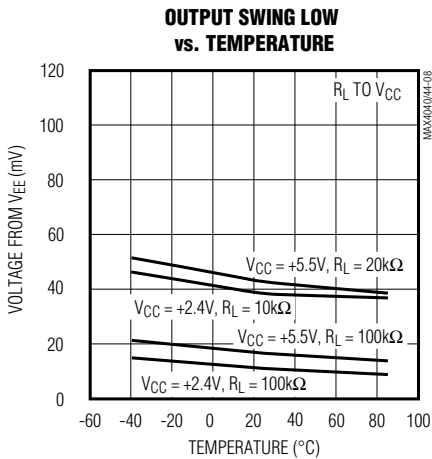
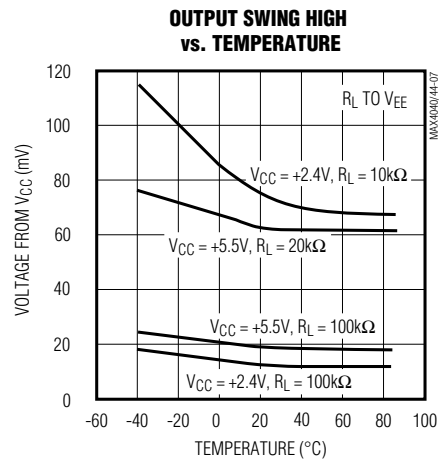
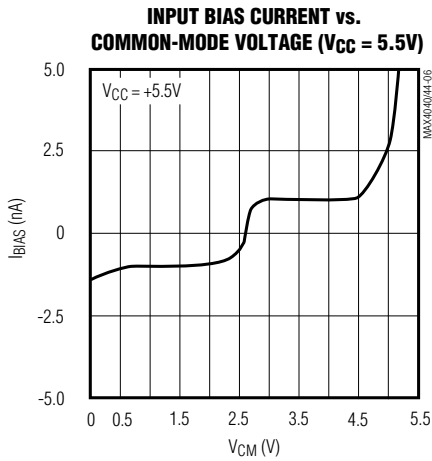
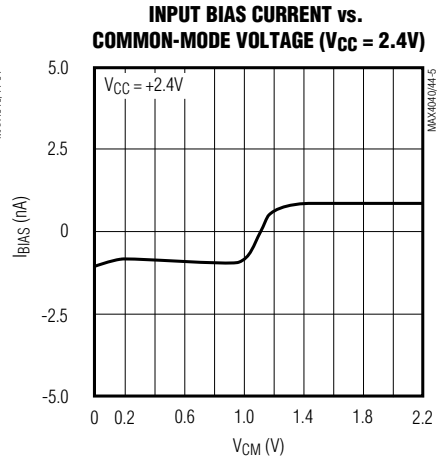
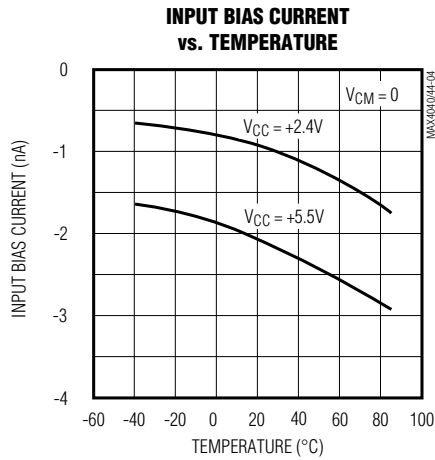
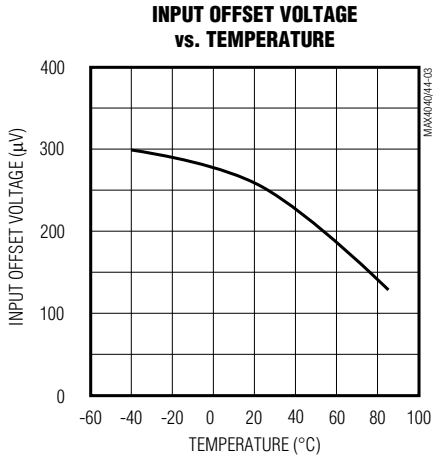


Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

MAX4040-MAX4044

Typical Operating Characteristics (continued)

($V_{CC} = +5.0V$, $V_{EE} = 0$, $V_{CM} = V_{CC} / 2$, $\overline{SHDN} = V_{CC}$, $R_L = 100k\Omega$ to $V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

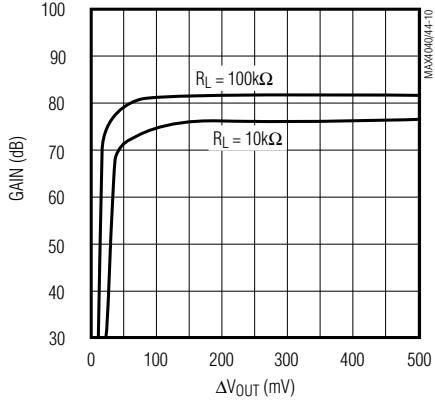


Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

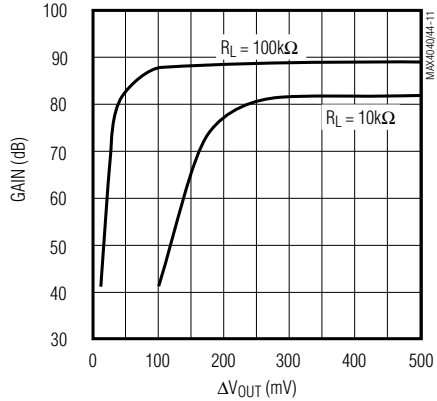
Typical Operating Characteristics (continued)

($V_{CC} = +5.0V$, $V_{EE} = 0$, $V_{CM} = V_{CC} / 2$, $\overline{SHDN} = V_{CC}$, $R_L = 100k\Omega$ to $V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

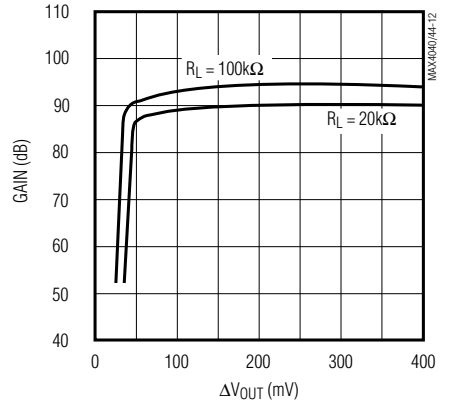
OPEN-LOOP GAIN vs. OUTPUT SWING LOW
($V_{CC} = +2.4V$, R_L TIED TO V_{CC})



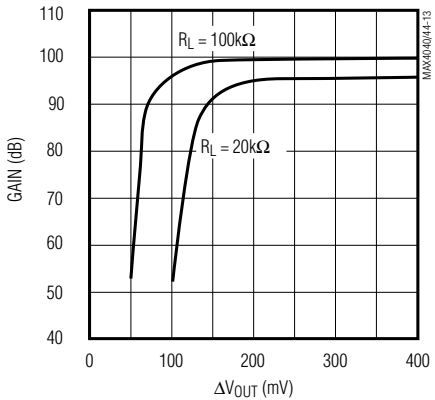
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH
($V_{CC} = +2.4V$, R_L TIED TO V_{EE})



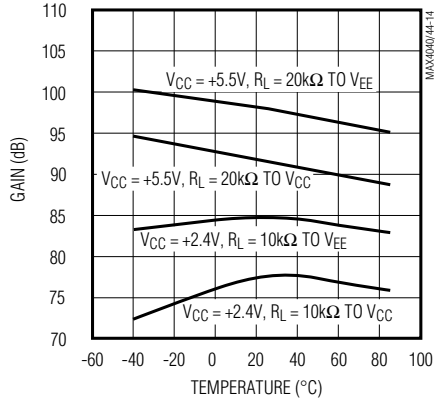
OPEN-LOOP GAIN vs. OUTPUT SWING LOW
($V_{CC} = +5.5V$, R_L TIED TO V_{CC})



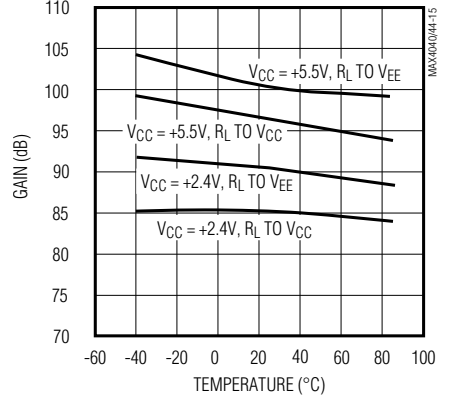
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH
($V_{CC} = +5.5V$, R_L TIED TO V_{EE})



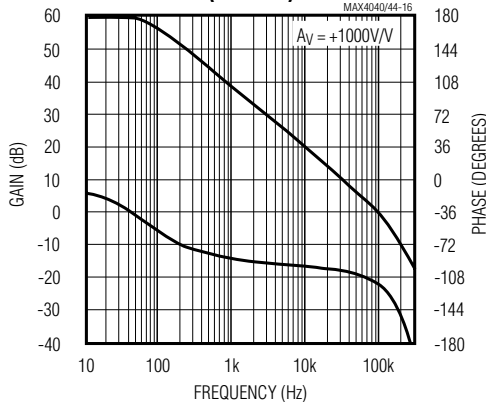
OPEN-LOOP GAIN vs. TEMPERATURE



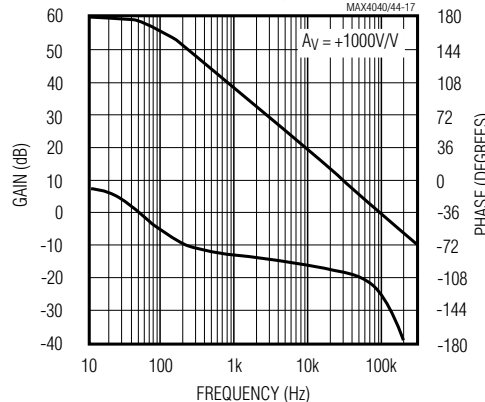
OPEN-LOOP GAIN vs. TEMPERATURE



GAIN AND PHASE vs. FREQUENCY
(NO LOAD)



GAIN AND PHASE vs. FREQUENCY
($C_L = 100pF$)



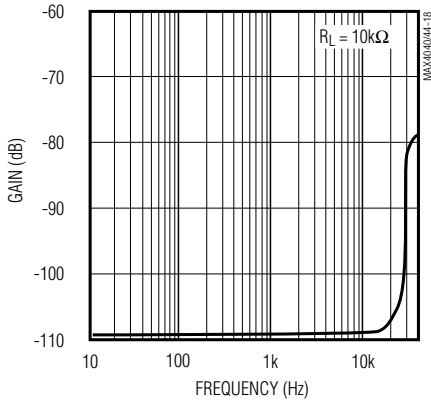
Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

MAX4040-MAX4044

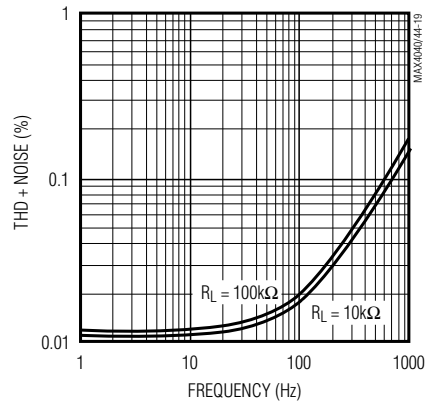
Typical Operating Characteristics (continued)

($V_{CC} = +5.0V$, $V_{EE} = 0$, $V_{CM} = V_{CC} / 2$, $\overline{SHDN} = V_{CC}$, $R_L = 100k\Omega$ to $V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

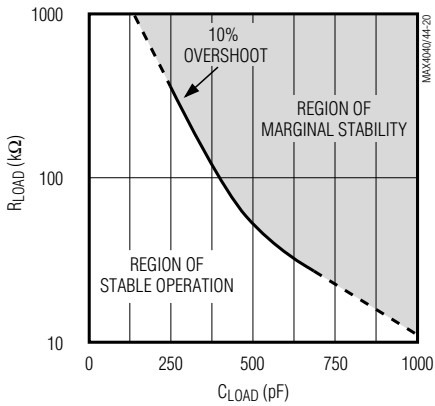
**MAX4042/MAX4043/MAX4044
CROSSTALK vs. FREQUENCY**



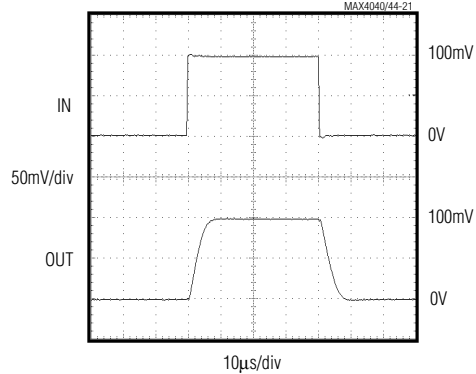
**TOTAL HARMONIC DISTORTION PLUS NOISE
vs. FREQUENCY**



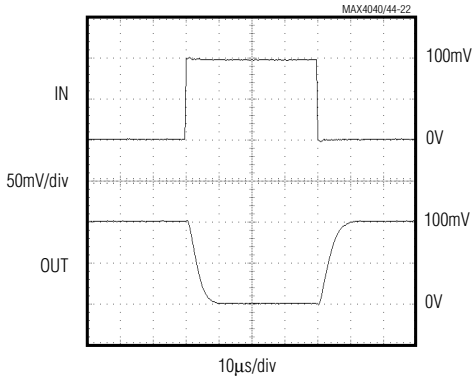
**LOAD RESISTOR vs.
CAPACITIVE LOAD**



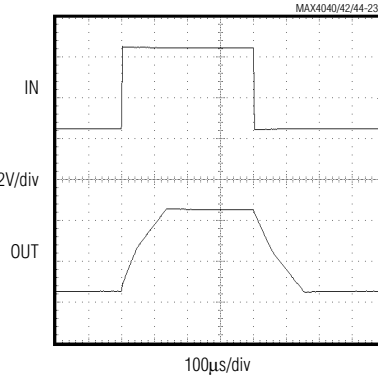
**SMALL-SIGNAL TRANSIENT RESPONSE
(NONINVERTING)**



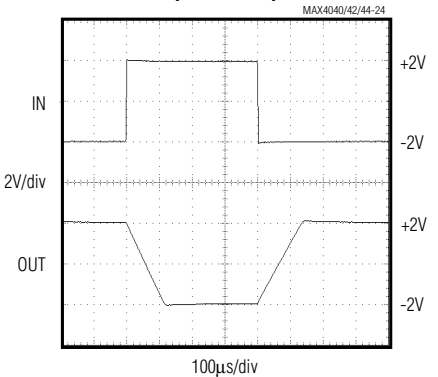
**SMALL-SIGNAL TRANSIENT RESPONSE
(INVERTING)**



**LARGE-SIGNAL TRANSIENT RESPONSE
(NONINVERTING)**



**LARGE-SIGNAL TRANSIENT RESPONSE
(INVERTING)**



Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

Pin Description

MAX4040		PIN				MAX4044	NAME	FUNCTION
SOT23-5	SO/ μ MAX	MAX4041	MAX4042	μ MAX	SO			
1	6	6	—	—	—	—	OUT	Amplifier Output. High impedance when in shutdown mode.
2	4	4	4	4	4	11	VEE	Negative Supply. Tie to ground for single-supply operation.
3	3	3	—	—	—	—	IN+	Noninverting Input
4	2	2	—	—	—	—	IN-	Inverting Input
5	7	7	8	10	14	4	VCC	Positive Supply
—	1, 5, 8	1, 5	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	—	8	—	—	—	—	$\overline{\text{SHDN}}$	Shutdown Input. Drive high, or tie to VCC for normal operation. Drive to VEE to place device in shutdown mode.
—	—	—	1, 7	1, 9	1, 13	1, 7	OUTA, OUTB	Outputs for Amplifiers A and B. High impedance when in shutdown mode.
—	—	—	2, 6	2, 8	2, 12	2, 6	INA-, INB-	Inverting Inputs to Amplifiers A and B
—	—	—	3, 5	3, 7	3, 11	3, 5	INA+, INB+	Noninverting Inputs to Amplifiers A and B
—	—	—	—	5, 6	6, 9	—	$\overline{\text{SHDNA}}$, $\overline{\text{SHDNB}}$	Shutdown Inputs for Amplifiers A and B. Drive high, or tie to VCC for normal operation. Drive to VEE to place device in shutdown mode.
—	—	—	—	—	—	8, 14	OUTC, OUTD	Outputs for Amplifiers C and D
—	—	—	—	—	—	9, 13	INC-, IND-	Inverting Inputs to Amplifiers C and D
—	—	—	—	—	—	10, 12	INC+, IND+	Noninverting Inputs to Amplifiers C and D

Detailed Description

Rail-to-Rail Input Stage

The MAX4040-MAX4044 have rail-to-rail inputs and rail-to-rail output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between VCC and VEE. The input offset voltage is typically 200 μ V. Low operating supply voltage, low supply current, rail-to-rail common-mode input range, and rail-to-rail outputs make this family of operational amplifiers

an excellent choice for precision or general-purpose, low-voltage battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedances (Figures 1a and 1b). The combination of high source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that produces an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

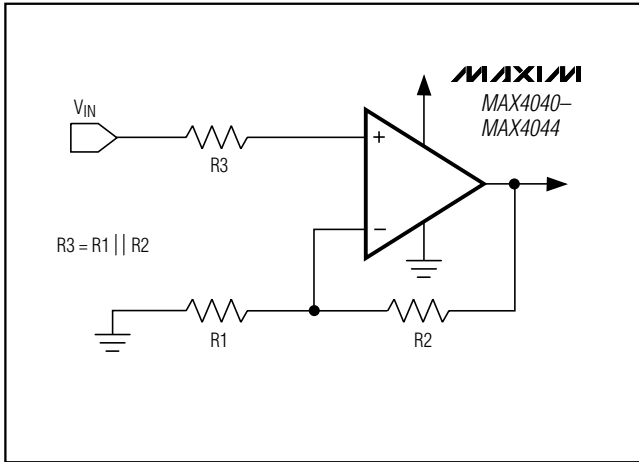


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

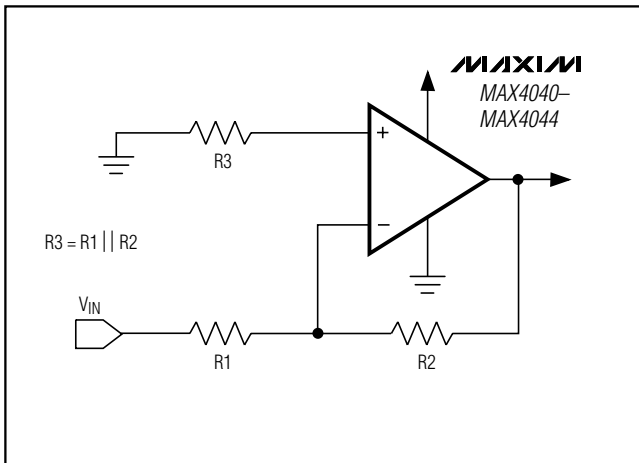


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

The MAX4040–MAX4044 family’s inputs are protected from large differential input voltages by internal 2.2kΩ series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential input voltages (much less than 1.8V), input resistance is typically 45MΩ. For differential input voltages greater than 1.8V, input resistance is around 4.4kΩ, and the input bias current can be approximated by the following equation:

$$I_{BIAS} = (V_{DIFF} - 1.8V) / 4.4k\Omega$$

In the region where the differential input voltage approaches 1.8V, the input resistance decreases exponentially from 45MΩ to 4.4kΩ as the diode block begins conducting. Conversely, the bias current increases with the same curve.

Rail-to-Rail Output Stage

The MAX4040–MAX4044 output stage can drive up to a 25kΩ load and still swing to within 60mV of the rails. Figure 3 shows the output voltage swing of a MAX4040 configured as a unity-gain buffer, powered from a single +4.0V supply voltage. The output for this setup typically swings from (VEE + 10mV) to (VCC - 10mV) with a 100kΩ load.

Applications Information

Power-Supply Considerations

The MAX4040–MAX4044 operate from a single +2.4V to +5.5V supply (or dual ±1.2V to ±2.75V supplies) and consume only 10μA of supply current per amplifier. A high power-supply rejection ratio of 85dB allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

Power-Up Settling Time

The MAX4040–MAX4044 typically require 200μs to power up after VCC is stable. During this start-up time, the output is indeterminate. The application circuit should allow for this initial delay.

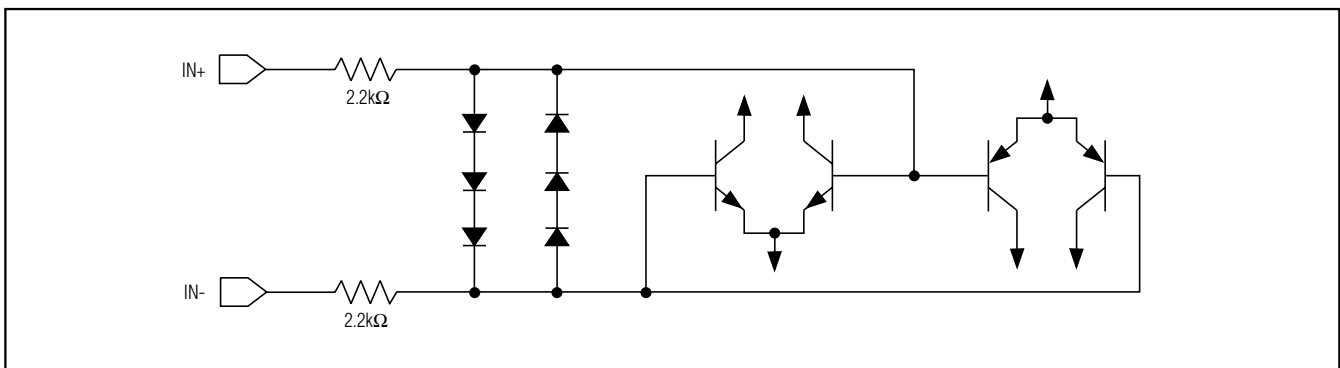


Figure 2. Input Protection Circuit

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

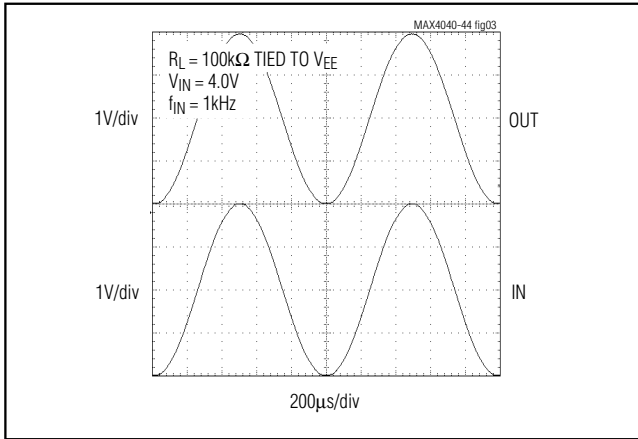


Figure 3. Rail-to-Rail Input/Output Voltage Range

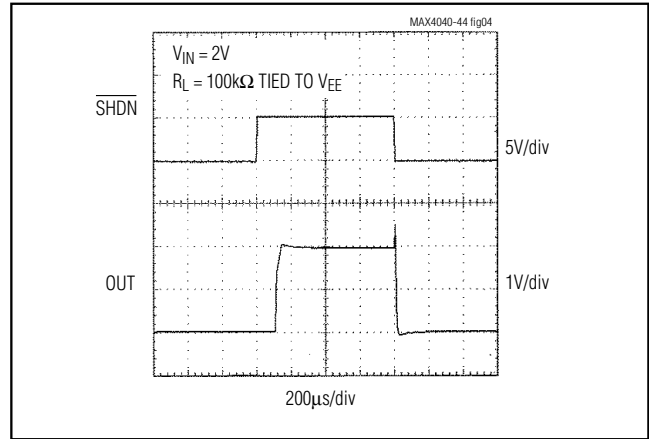


Figure 4. Shutdown Enable/Disable Output Voltage

Shutdown Mode

The MAX4041 (single) and MAX4043 (dual) feature a low-power shutdown mode. When the shutdown pin (SHDN) is pulled low, the supply current drops to 1µA per amplifier, the amplifier is disabled, and the outputs enter a high-impedance state. Pulling SHDN high or leaving it floating enables the amplifier. Take care to ensure that parasitic leakage current at the SHDN pin does not inadvertently place the part into shutdown mode when SHDN is left floating. Figure 4 shows the output voltage response to a shutdown pulse. The logic threshold for SHDN is always referred to $V_{CC} / 2$ (not to GND). When using dual supplies, pull SHDN to V_{EE} to enter shutdown mode.

Load-Driving Capability

The MAX4040-MAX4044 are fully guaranteed over temperature and supply voltage to drive a maximum resistive load of $25k\Omega$ to $V_{CC} / 2$, although heavier loads can be driven in many applications. The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward V_{CC} , and as a current sink when driving the load toward V_{EE} . The magnitude of this current source/sink varies with supply voltage, ambient temperature, and lot-to-lot variations of the units.

Figures 5a and 5b show the typical current source and sink capability of the MAX4040-MAX4044 family as a function of supply voltage and ambient temperature. The contours on the graph depict the output current value, based on driving the output voltage to within 50mV, 100mV, and 200mV of either power-supply rail.

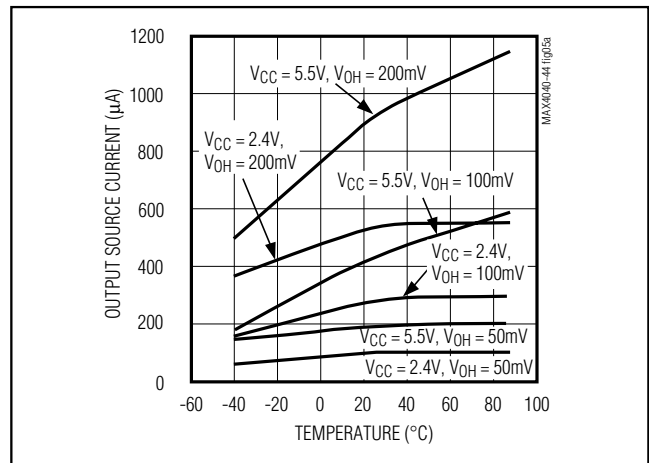


Figure 5a. Output Source Current vs. Temperature

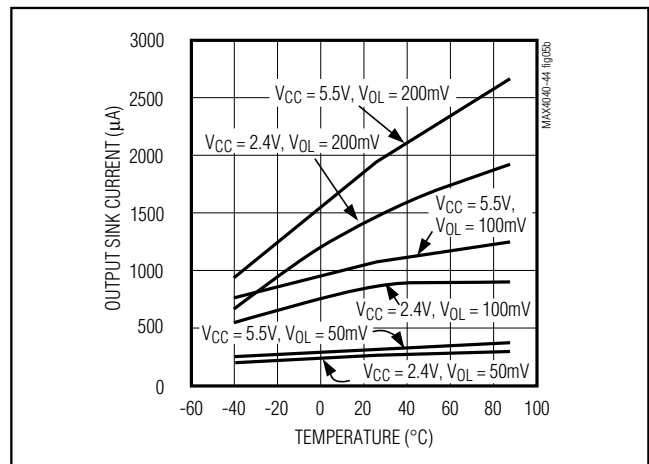


Figure 5b. Output Sink Current vs. Temperature

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

MAX4040-MAX4044

For example, a MAX4040 running from a single +2.4V supply, operating at $T_A = +25^\circ\text{C}$, can source $240\mu\text{A}$ to within 100mV of V_{CC} and is capable of driving a $9.6\text{k}\Omega$ load resistor to V_{EE} :

$$R_L = \frac{2.4\text{V} - 0.1\text{V}}{240\mu\text{A}} = 9.6\text{k}\Omega \text{ to } V_{EE}$$

The same application can drive a $4.6\text{k}\Omega$ load resistor when terminated in $V_{CC} / 2$ (+1.2V in this case).

Driving Capacitive Loads

The MAX4040-MAX4044 are unity-gain stable for loads up to 200pF (see Load Resistor vs. Capacitive Load graph in *Typical Operating Characteristics*). Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load (Figures 6a-6c). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the load resistor.

Power-Supply Bypassing and Layout

The MAX4040-MAX4044 family operates from either a single +2.4V to +5.5V supply or dual $\pm 1.2\text{V}$ to $\pm 2.75\text{V}$ supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to V_{EE} (in this case GND). For dual-supply operation, both the V_{CC} and V_{EE} supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths by placing external components as close as possible to the op amp. Surface-mount components are an excellent choice.

Using the MAX4040-MAX4044 as Comparators

Although optimized for use as operational amplifiers, the MAX4040-MAX4044 can also be used as rail-to-rail I/O comparators. Typical propagation delay depends on the input overdrive voltage, as shown in Figure 7. External hysteresis can be used to minimize the risk of output oscillation. The positive feedback circuit, shown in Figure 8, causes the input threshold to change when the output voltage changes state. The two thresholds create a hysteresis band that can be calculated by the following equations:

$$V_{HYST} = V_{HI} - V_{LO}$$

$$V_{LO} = V_{IN} \times R_2 / (R_1 + (R_1 \times R_2 / R_{HYST}) + R_2)$$

$$V_{HI} = [(R_2 / R_1 \times V_{IN}) + (R_2 / R_{HYST}) \times V_{CC}] / (1 + R_1 / R_2 + R_2 / R_{HYST})$$

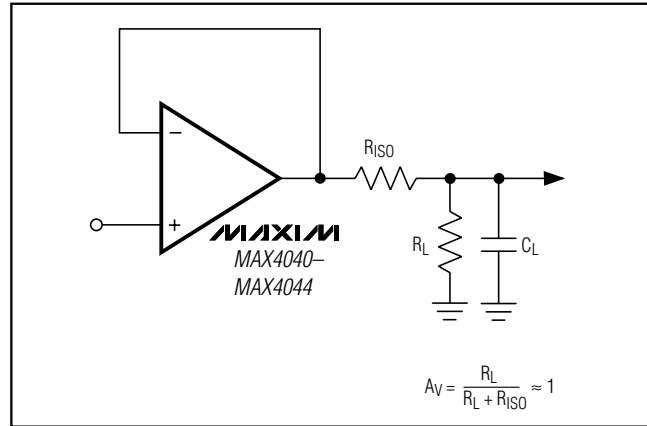


Figure 6a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

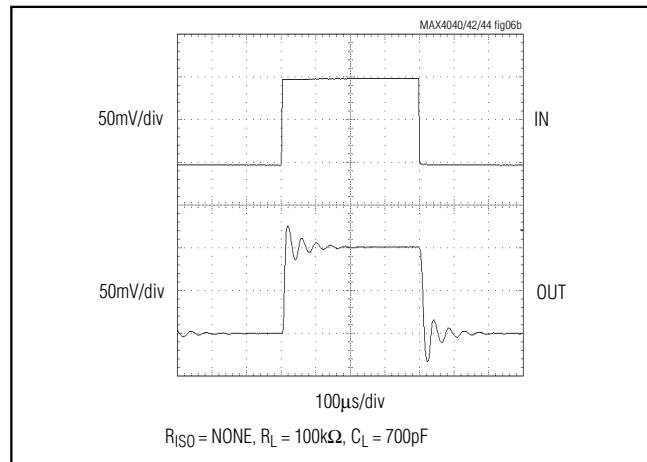


Figure 6b. Pulse Response without Isolating Resistor

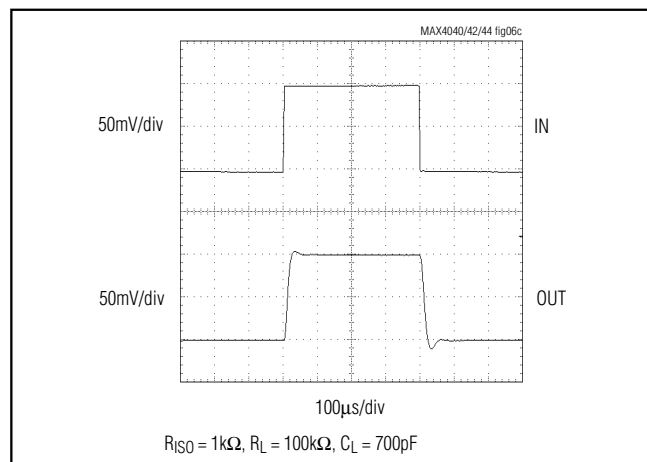


Figure 6c. Pulse Response with Isolating Resistor

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

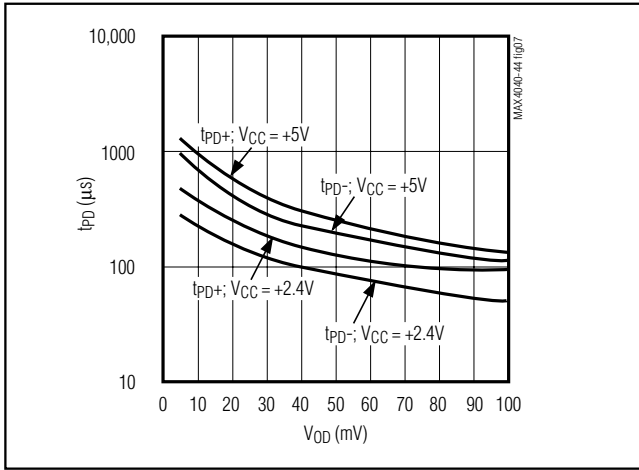


Figure 7. Propagation Delay vs. Input Overdrive

The MAX4040-MAX4044 contain special circuitry to boost internal drive currents to the amplifier output stage. This maximizes the output voltage range over which the amplifiers are linear. In an open-loop comparator application, the excursion of the output voltage is so close to the supply rails that the output stage transistors will saturate, causing the quiescent current to increase from the normal 10µA. Typical quiescent currents increase to 35µA for the output saturating at VCC and 28µA for the output at VEE.

Using the MAX4040-MAX4044 as Ultra-Low-Power Current Monitors

The MAX4040-MAX4044 are ideal for applications powered from a battery stack. Figure 9 shows an application circuit in which the MAX4040 is used for monitoring the current of a battery stack. In this circuit, a current load is applied, and the voltage drop at the battery terminal is sensed.

The voltage on the load side of the battery stack is equal to the voltage at the emitter of Q1, due to the feedback loop containing the op amp. As the load current increases, the voltage drop across R1 and R2 increases. Thus, R2 provides a fraction of the load current (set by the ratio of R1 and R2) that flows into the emitter of the PNP transistor. Neglecting PNP base current, this current flows into R3, producing a ground-referenced voltage proportional to the load current. Scale R1 to give a voltage drop large enough in comparison to VOS of the op amp, in order to minimize errors.

The output voltage of the application can be calculated using the following equation:

$$V_{OUT} = [I_{LOAD} \times (R1 / R2)] \times R3$$

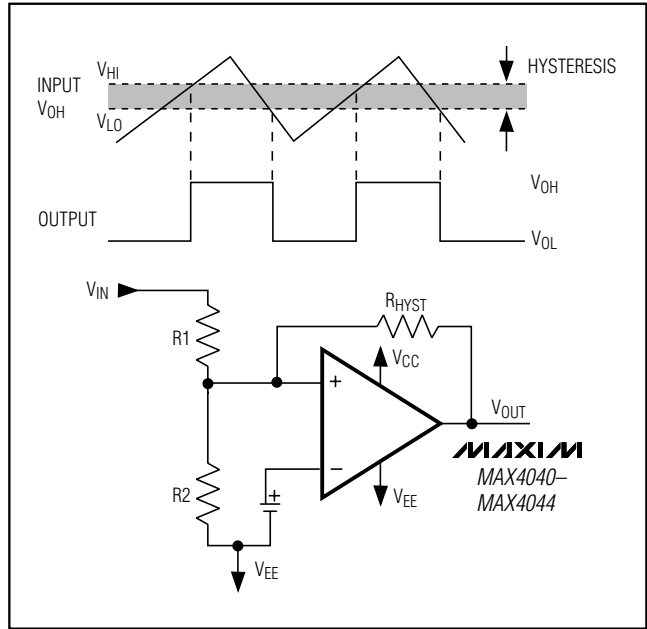


Figure 8. Hysteresis Comparator Circuit

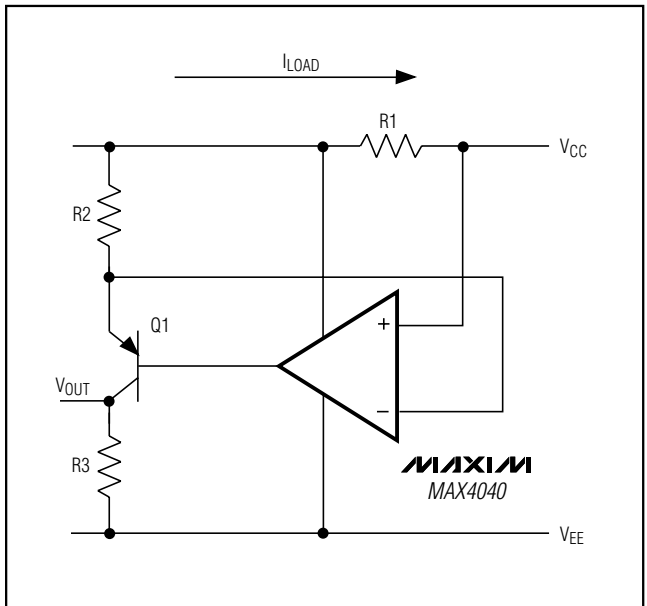


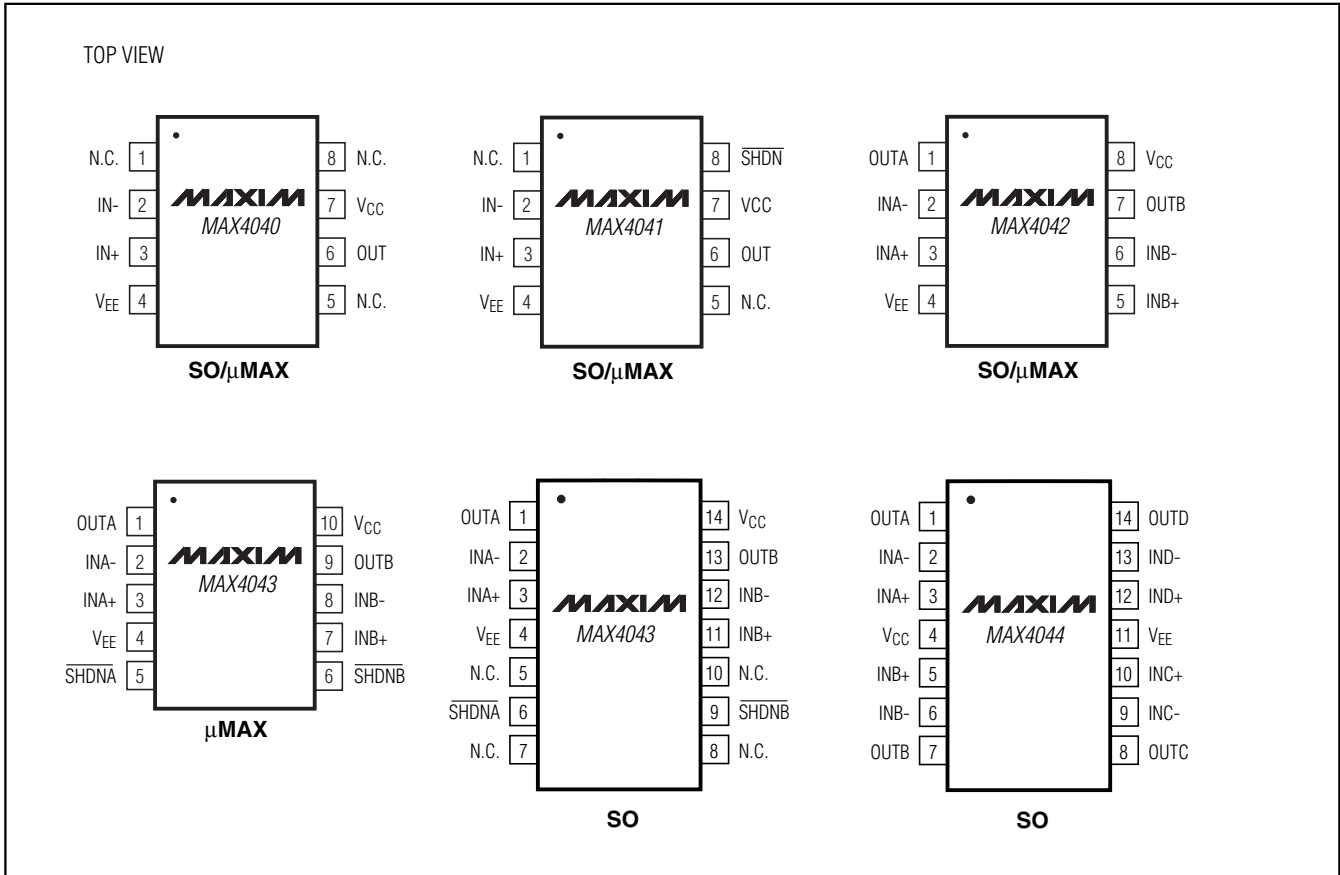
Figure 9. Current Monitor for a Battery Stack

For a 1V output and a current load of 50mA, the choice of resistors can be R1 = 2Ω, R2 = 100kΩ, R3 = 1MΩ. The circuit consumes less power (but is more susceptible to noise) with higher values of R1, R2, and R3.

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

Pin Configurations (continued)

MAX4040-MAX4044



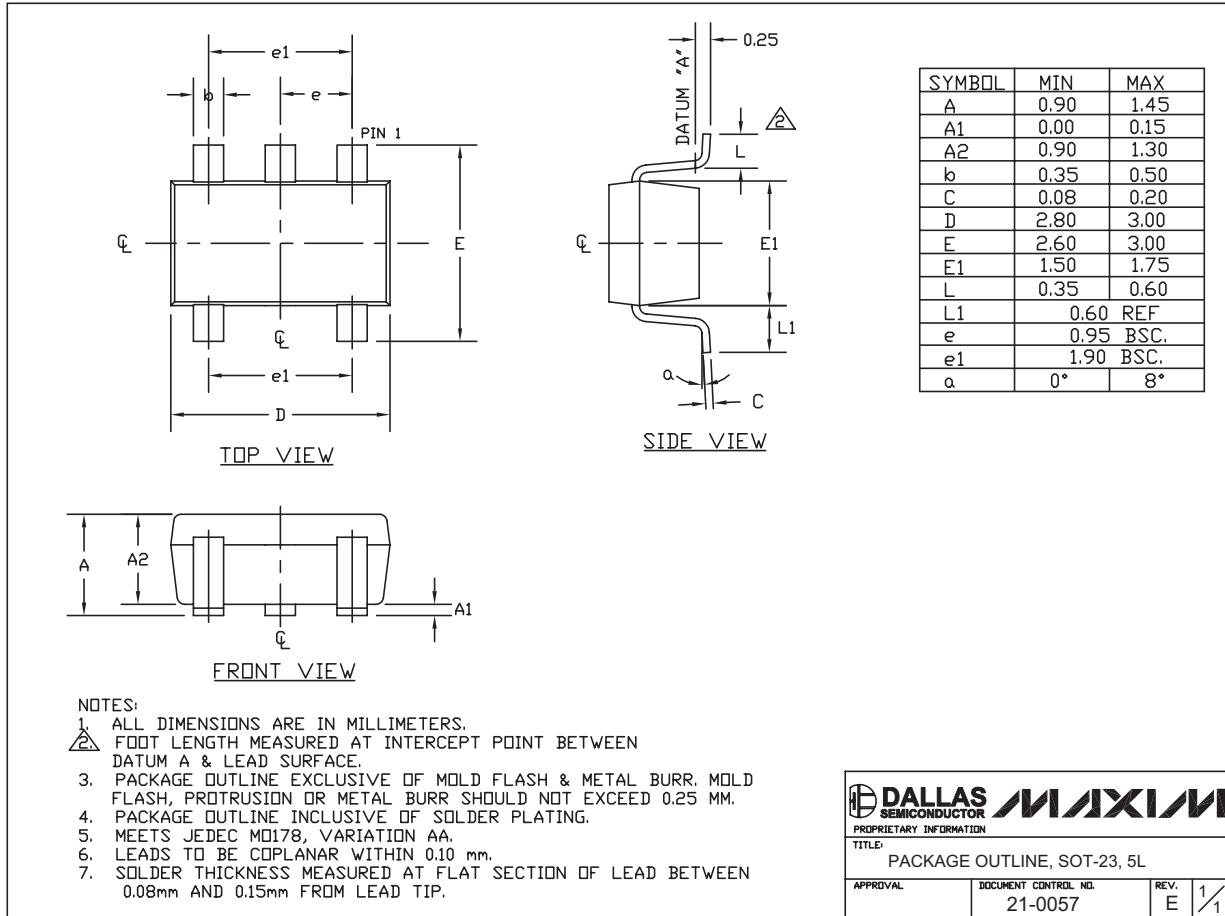
Chip Information

MAX4040/MAX4041 TRANSISTOR COUNT: 234
 MAX4042/MAX4043 TRANSISTOR COUNT: 466
 MAX4044 TRANSISTOR COUNT: 932
 SUBSTRATE CONNECTED TO VEE

Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



SOT-23, 5L, EPS

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO. 21-0057	REV. E	1/1
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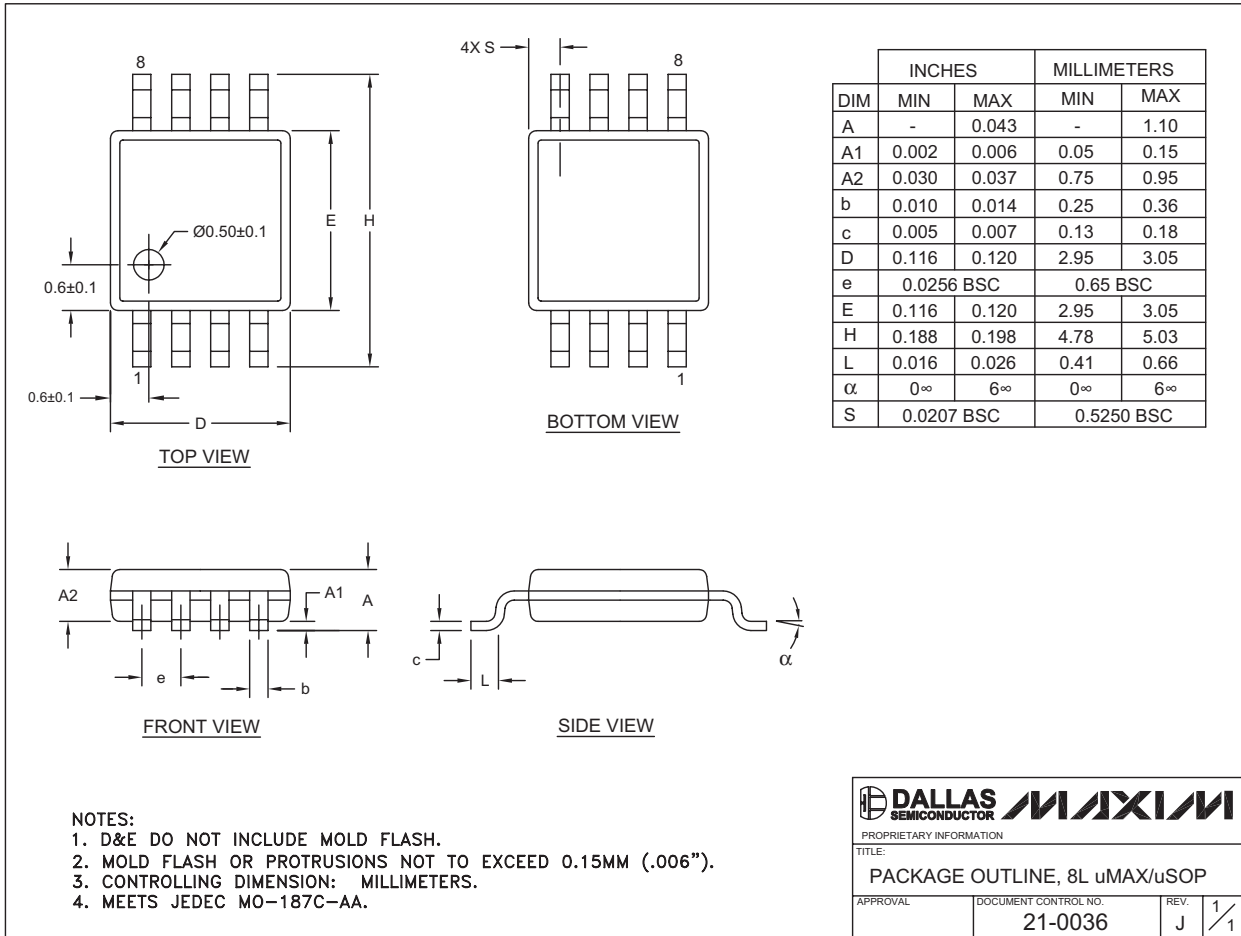
Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

Package Information (continued)

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MAX4040-MAX4044

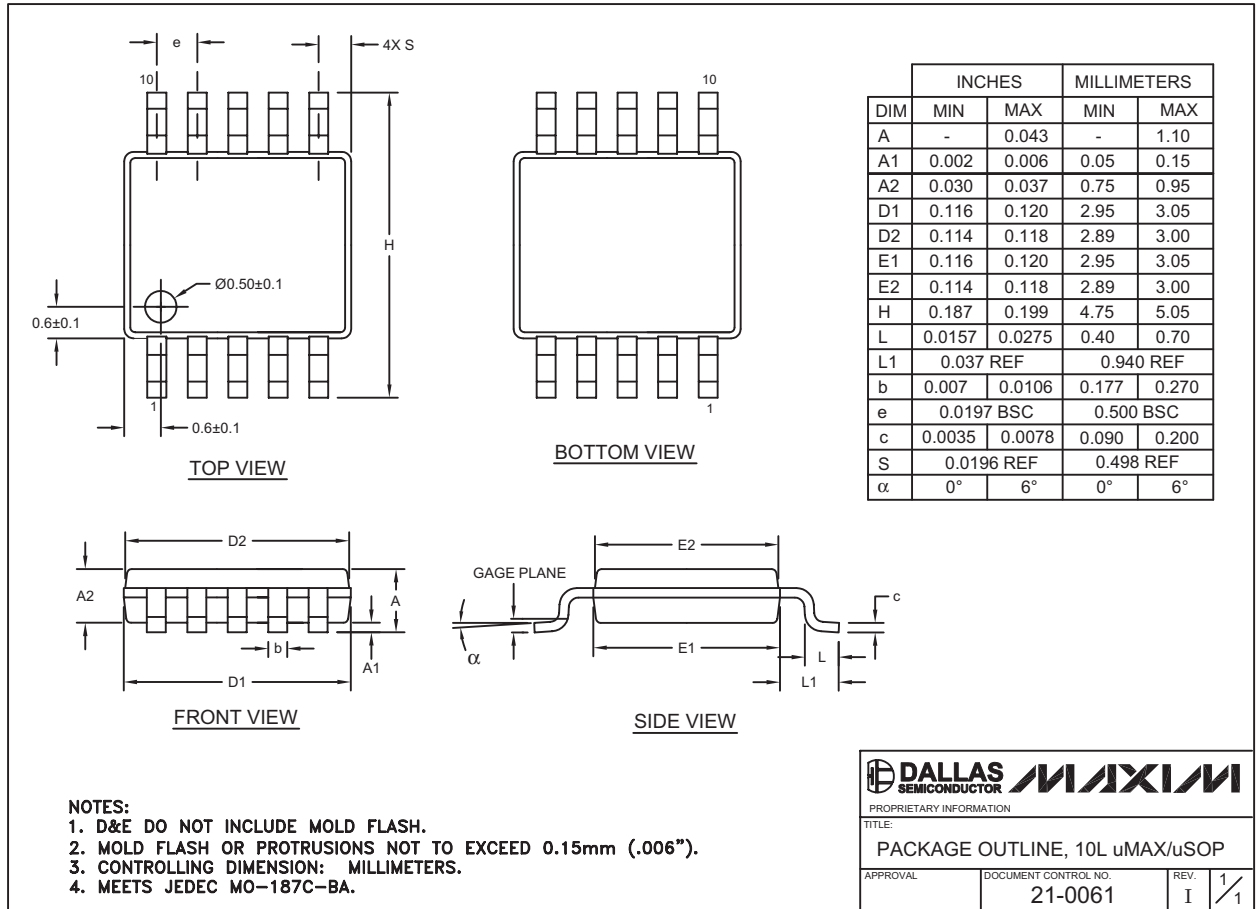
8LUMAXD.EPS



Single/Dual/Quad, Low-Cost, SOT23, Micropower, Rail-to-Rail I/O Op Amps

Package Information (continued)

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10L uMAX uEPS

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