Ordering number : ENA1915A

LB11868V

ON Semiconductor®

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Monolithic Digital IC

For Fan Motor
Variable Speed Single-phase Full-wave Pre-driver

Overview

LB11868V is a single-phase bipolar driving motor pre-driver with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved. This product is best suited for driving of the server requiring large air flow and large current and the fan motor of consumer appliances.

Features

- Single-phase full-wave driving pre-driver
- Variable speed control possible with external PWM input
- Current limiting circuit incorporated
- Reactive current cut circuit incorporated
- Minimum speed setting pin
- Soft start setting pin
- Start setting pin of on time
- Pch-FET kickback absorption setting pin
- Lock protection and automatic reset circuits incorporated
- FG (rotational speed detection) output, RD (lock detection) output
- Thermal shutdown circuit incorporated

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} pin maximum supply voltage	V_{CC} max		18	V
OUTN pin maximum current	$I_{OUT}N$ max		30	mA
OUTN pin output withstand voltage	$V_{OUT}N$ max		18	V
OUTP pin maximum Sink current	$I_{OUT}P$ max		30	mA
Maximum inflow current at OUTP pin OFF	$I_{OUT}P$ off max	DUTY8% under	10	mA
OUTP pin output withstand voltage	$V_{OUT}P$ max	*1	19	V
VTH/RMI pins withstand voltage	VVTH/VRMI max		7	V
S-S pin withstand voltage	V_{S-S} max		7	V
OTS pin withstand voltage	V_{OTS} max		7	V
KBSET pin withstand voltage	V_{KBSET} max		7	V
FG/RD pin withstand voltage	$V_{FG/RD}$ max		19	V
FG/RD pin maximum Sink current	$I_{FG/RD}$ max		10	mA
REG pin maximum output current	I_{REG} max		10	mA
HB pin maximum output current	I_{HB} max		10	mA
Allowable power dissipation	Pd max	with specified substrate *2	800	mW
Operating temperature	Topr	*3	-30 to 95	°C
Storage temperature	Tstg		-55 to 150	°C

*1 The direct input from the power supply is improper. There must be resistance between OUTP and the power side power supply.

*2 Specified substrate: 114.3mm×76.1mm×1.6mm, glass epoxy board.

*3 Tj max=150°C must not be exceeded.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} Supply voltage	V_{CC}		4.0 to 16	V
VTH/RMI input voltage range	$V_{TH/RMI}$		0 to 4.0	V
Hall input voltage range	V_{ICM}		0.2 to 1.8	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC}1$	During drive	7.5	9.0	10.5	mA
	$I_{CC}2$	During lock protection	6.0	7.6	9.0	mA
REG voltage	V_{REG}	I_{REG} = 5mA	3.65	3.80	3.95	V
HB voltage	V_{HB}	I_{HB} = 5mA	1.14	1.24	1.34	V
Current limiting voltage	V_{LIM}		195	215	235	mV
CPWM pin “H” level voltage	$V_{CPWM}H$		2.35	2.50	2.65	V
CPWM pin “L” level voltage	$V_{CPWM}L$		0.65	0.80	0.95	V
CPWM pin charge current	$I_{CPWM}1$	V_{CPWM} = 0.5V	19	24	29	µA
CPWM pin discharge current	$I_{CPWM}2$	V_{CPWM} = 2.8V	19.5	24.5	29.5	µA
CPWM Oscillation frequency	FPWM	C = 220PF		32		kHz
CT pin “H” level voltage	$V_{CT}H$		2.35	2.50	2.65	V
CT pin “L” level voltage	$V_{CT}L$		0.65	0.80	0.95	V
CT pin charge current	$I_{CT}1$	V_{CT} = 0.5V	1.6	2.0	2.4	µA
CT pin discharge current	$I_{CT}2$	V_{CT} = 2.8V	0.16	0.20	0.24	µA
CT pin charge/discharge ratio	R_{CT}	$I_{CT}1/I_{CT}2$	8	10	12	times
S-S pin discharge current	I_{S-S}	V_{S-S} = 1V	0.35	0.45	0.55	µA
OTS pin charge current	$I_{OTS}1$	V_{OTS}=0.5V	0.65	0.85	1.05	µA
OTS pin discharge current	$I_{OTS}2$	V_{OTS}=0.5V	50	58	66	µA
OTS pin threshold voltage	V_{OTS}		1.2	1.3	1.4	V
OUTN output H-level voltage	V_ONH	I_O = 1mA		V_{CC}-0.9	V_{CC}-1.0	V
		I_O = 10mA		V_{CC}-1.9	V_{CC}-2.1	V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
OUTN output L-level voltage	V_ONL	IO = 10mA		0.9	1.05	V
OUTP output L-level voltage	V_OPL	IO = 10mA		0.4	0.55	V
Hall input sensitivity	V_{HN}	IN+, IN- differential voltage (including offset and hysteresis)		±10	±20	mV
FG/RD output L-level voltage	$V_{FG}L/_{RD}L$	$I_{FG/RD}$ = 5mA		0.2	0.3	V
FG/RD pin leakage current	$I_{FG}L/_{RD}L$	$V_{FG/RD}$ = 19V			10	μA
VTH/RMI pin bias current	I_{VTH}/I_{RMI}	CPWM = 2V, $V_{TH/RMI}$ = 1V			0.3	μA

Truth table

(1) Drive lock CPWM=H VTH, RMI, S-S=L

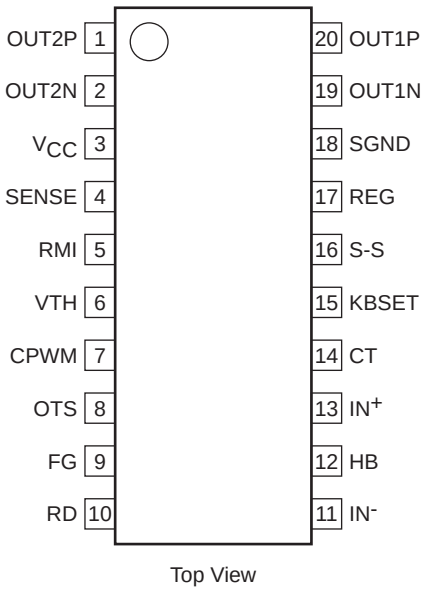
IN^-	IN^+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	RD	Mode
H	L	L	L	L	OFF	H	L	L	OUT1 → 2 drive
L	H		OFF	H	L	L	OFF	L	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	OFF	Lock protection
L	H		OFF	H	OFF	L	OFF	OFF	

(2) Speed control CT, S-S=L

VTH, RMI	CPWM	OTS	IN^-	IN^+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	L	H	L	L	L	OFF	H	OUT1 → 2 drive
			L	H	OFF	H	L	L	OUT2 → 1 drive
H	L		H	L	OFF	L	OFF	H	Regeneration mode
			L	H	OFF	H	OFF	L	
H	L	H	H	L	OFF	L	OFF	L	Standby mode
			L	H	OFF	L	OFF	L	

For VTH, RMI, and S-S pins, refer to the timing chart.

Pin Assignment

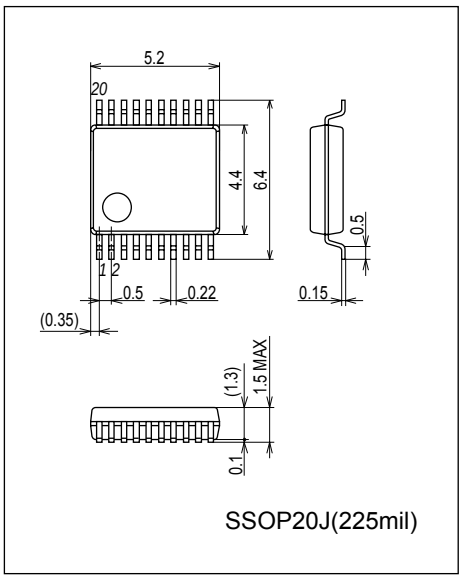


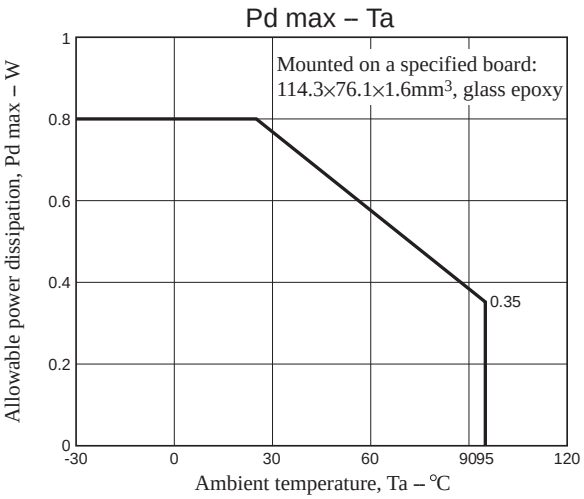
Top View

Package Dimensions

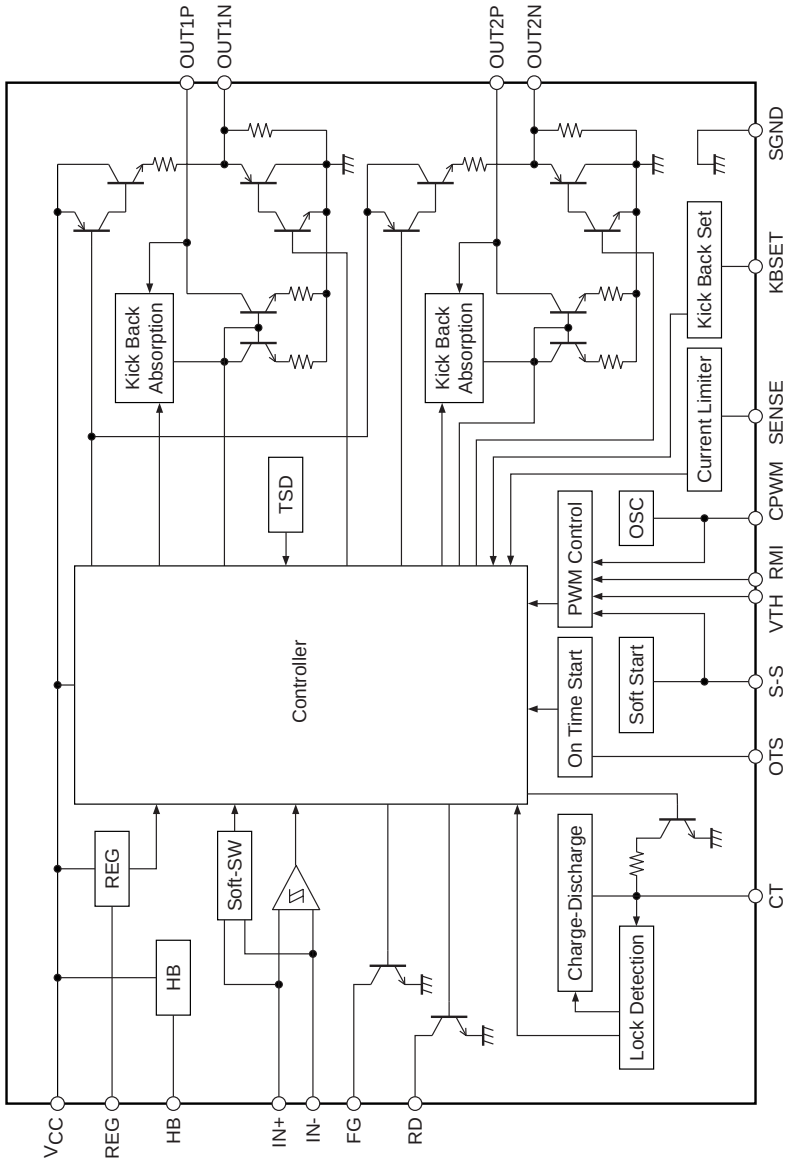
unit : mm (typ)

3360

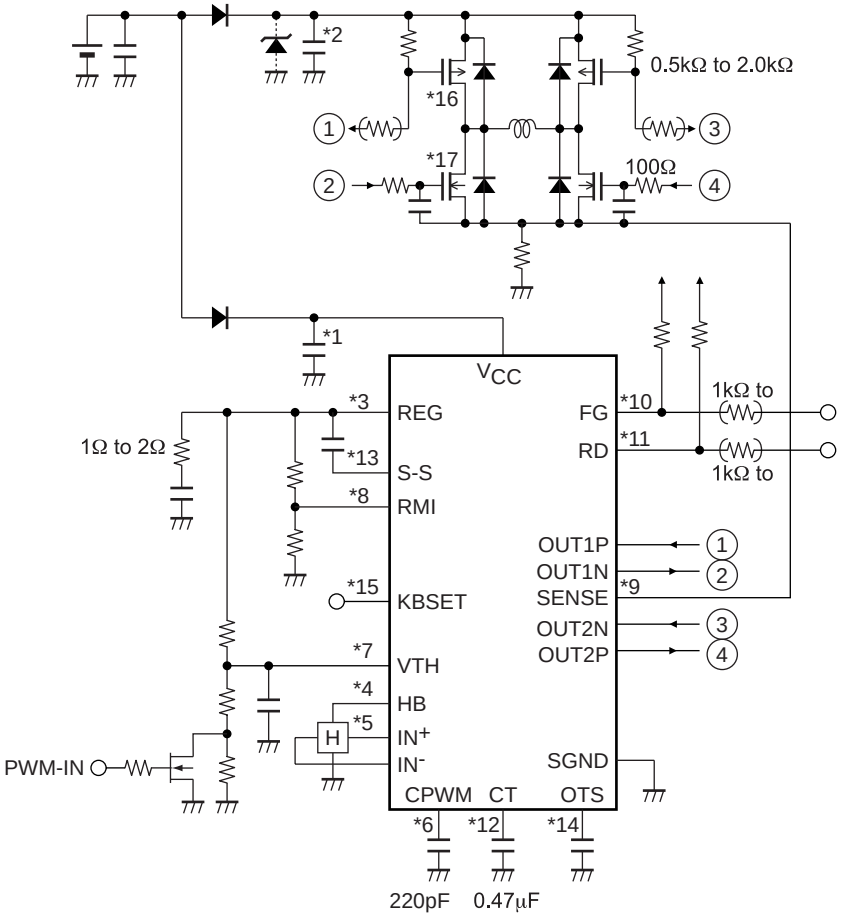




Block Diagram



Application Circuit Example



*1. Power stabilization capacitor
For the power stabilization capacitor on the signal side, use the capacitance of 1μF or more.
Connect V_{CC} and SGND with a thick and shortest pattern.

*2. Power stabilization capacitor on the power side
For the power stabilization capacitor on the power side, use the capacitance of 1μF or more.
Connect the power supply on the power side and GND with a thick and shortest pattern.
When the IC is used for a fan with a high current level, insert a zener diode between the power supply on the power side and GND.

*3. REG pin
3.8V constant-voltage output pin. For the REG oscillation prevention and stabilization, use a capacitor with capacitance of 1μF or more. Connect the REG pin and SGND with a thick and shortest pattern.

*4. HB pin
Used for Hall device bias purposes.

*5. IN^+, IN^- pins
Hall signal input pin.
Wiring should be short to prevent carrying of noise.
If noise is carried, insert the capacitor between IN^+ and IN^- pins.
The Hall input circuit functions as a comparator with hysteresis (15mV).
This also has a soft switch section with ±30mV (input signal differential voltage).
It is also recommended that the Hall input level is minimum 100mV (p-p).

*6. CPWM pin

Pin to connect the capacitor for generation of the PWM basic frequency
The use of CP = 220pF causes oscillation at f = 30kHz (typical), which is the basic frequency of PWM.
As this is used also for the current limiting canceling signal, ON-time start function and Soft start function, be sure to connect the capacitor even when the speed control is not made.

*7. RMI pin

Minimum speed setting pin.
Perform pull-up with REG when this pin is not to be used.
If the IC power supply is likely to be turned OFF first when the pin is used with external power supply, be sure to insert the current limiting resistor to prevent inflow of large current. (The same applies to the VTH pin.)

*8. VTH pin

Speed control pin.
Connect this pin to GND when it is not used (at full speed).
For the control method, refer to the timing chart.
For control with pulse input, insert the current limiting resistor and use the pin with the frequency of 20kHz to 100kHz (20kHz to 50kHz recommended).

*9. SENSE pin

Current limiting detection pin.
When the pin voltage exceeds VLIM, the current is limited and the operation enters the lower regeneration mode.
Connect this pin to GND when it is not to be used.

*10. FG pin

Rotational speed detection pin.
Open collector output that can detect rotational speeds by the FG output in response to the phase switching signal.
Keep this pin open when it is not to be used.
It is recommended that a current-limiting resistor with a resistance of 1kΩ or more be inserted in order to protect the pin during unplugging and plugging the connector or when mistakes are made in connection.

*11. RD pin

Lock detection pin
In open collector output, L upon rotation and H when locked (using pull-up resistance).
Keep this pin open when it is not to be used.

*12. CT pin

Pin to connect the lock detection capacitor.
The constant-current charge and discharge circuits incorporated cause locking when the pin voltage becomes VCTH and unlocking when it is VCTL.
Connect the pin to GND when it is not to be used (locking not necessary).

*13. S-S pin

Pin to connect the soft-start setting capacitor.
Connect the capacitor between REG and S-S pin.
This pin enables setting of the soft start time according to the capacity of the capacitor.
See the timing char.
Connect the pin to GND when it is not to be used.

*14. OTS pin

Pin to connect the ON-time start setting capacitor.
A constant-current charging circuit and a discharging circuit based on the control duty ratio are incorporated, and when the pin voltage exceeds VOTS, the CT pin is discharged and the S-S pin is charged.
Connect the pin to GND when it is not to be used (when the lowest speed setting is used).

*15. KBSET pin

Pch kickback absorption circuit setting pin.
Open: The kickback absorption circuit is activated at a VCC voltage of 7.4V (typ) or above.
Pull-down to GND: Always OFF
Pull-up to REG: Always ON (but when the IC power is OFF, the kickback absorption circuit is OFF)
If the Pch load is to be reduced due to the large fan current, short the KBSET pin to GND, and use a zener diode between the power supply on the power side and GND.
Kickback absorption circuit ON: At OUTPOFF, the OUTP voltage is clamped at VCC + 0.85V (at room temperature and inflow current 5mA (typ)).
Kickback absorption circuit OFF: At OUTPOFF, the OUTP voltage is clamped at 18V or so (at room temperature and inflow current 5mA (typ)) in order to protect the pin.
At OUTPOFF, the maximum inflow current must not be exceeded.

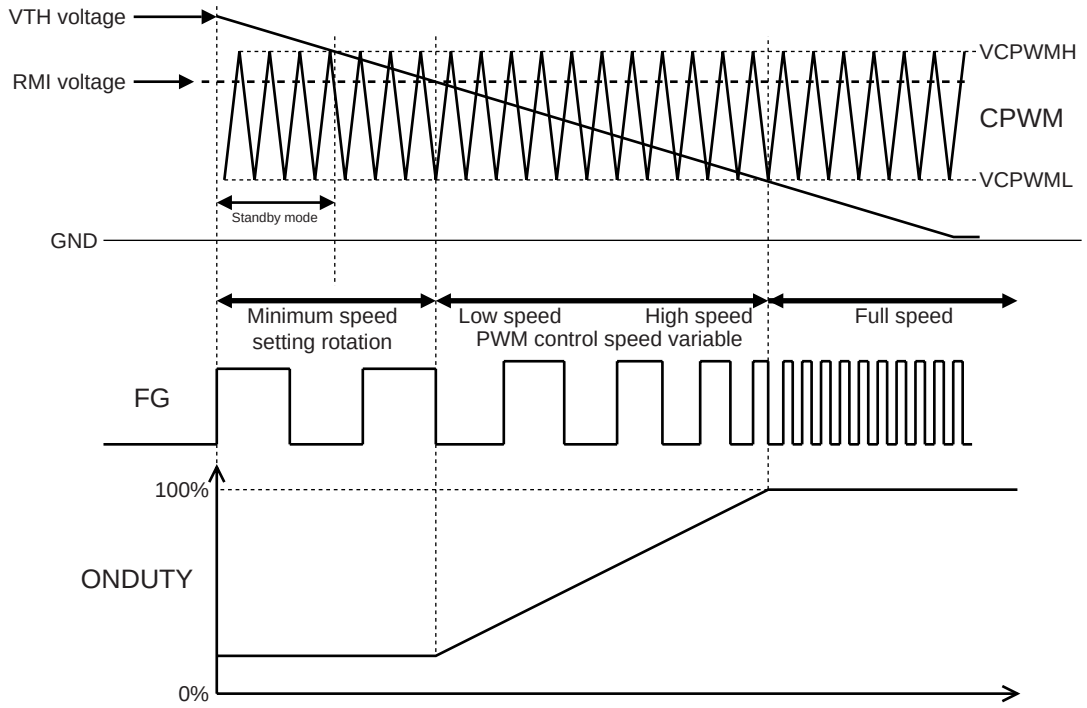
*16. Pch FET

If the Pch kickback absorption circuit is activated and a zener diode between the power supply and GND is not used, the kickback during phase switching is absorbed by Pch.
Since the circuit is activated with a high voltage difference between the drain and source, select a FET with sufficiently high capability.

*17. Nch FET

If the Nch gate voltage fluctuates significantly due to the effects of switching, insert a capacitor between the gate and GND.
Since an Nch diode is used during coil current regeneration, select a FET with sufficiently high capability.

Control timing chart (Speed control)



(1) Minimum speed setting (standby) mode

The low-speed fan rotation occurs at the minimum speed set with the RMI pin.
When the minimum speed is not set (RMI pin pulled up to REG), the motor stops.
If the VHT voltage rises when the lowest speed is not set (RMI pin is pulled up to REG), the fan stops running, and if the OTS pin capacitor is used, the standby mode is established.
Details of the standby mode are given in the section “Control timing chart (ON-time start, Lock protection).

(2) Low speed⇔high speed

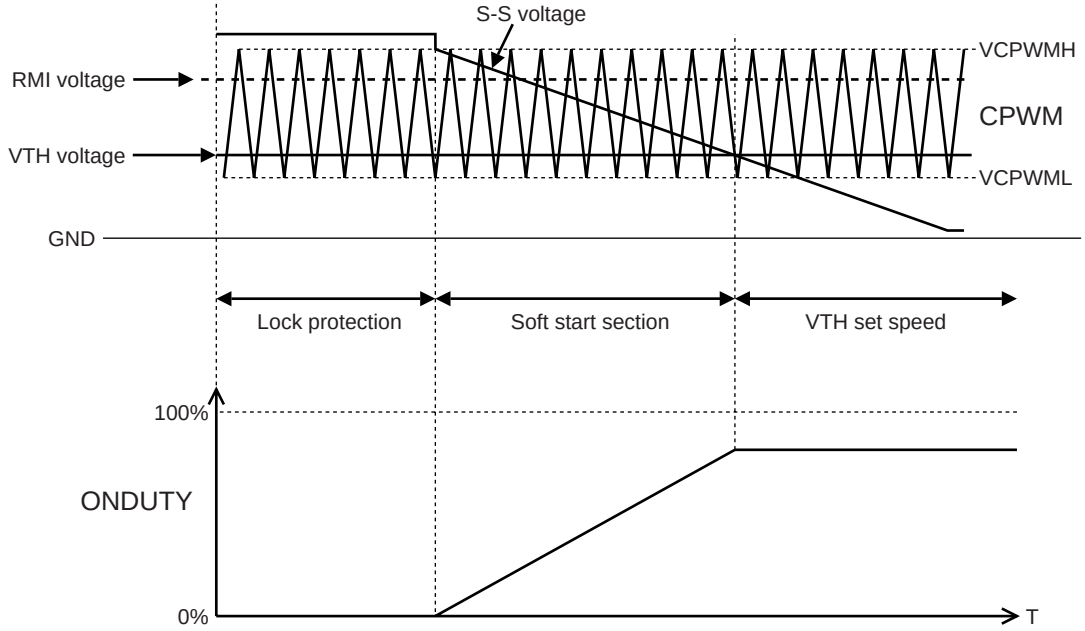
PMW control is made by comparing the CPWM oscillation voltage (VCPWML⇔VCPEMH) and VTH voltage.
The drive mode is established when the VTH voltage is low.
Both upper and lower output FET are turned ON when the VTH voltage is low.
When the VTH voltage is high, Pch is turned off, and the coil current is regenerated inside the lower FET. Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing an increase in the coil current and raising the motor rotation speed.
The upper output Pch is turned OFF when the VTH voltage is high, regenerating the coil current in the lower TR. Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing increase in the coil current, raising the motor rotation speed.
The rotational speed can be monitored using the FG output.

(3) Full speed mode

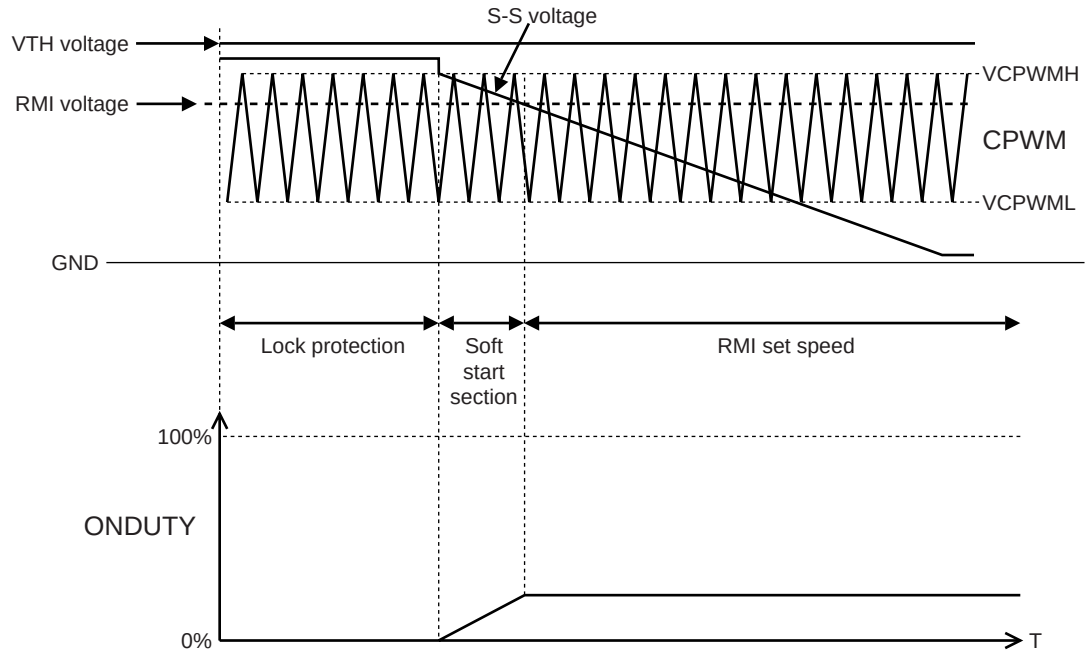
The full speed mode becomes effective when the VTH voltage is VCPWML or less. (Set VTH = GND when the speed control is not to be made.)

Control timing chart (Soft start)

(1)At VTH < RMI voltage



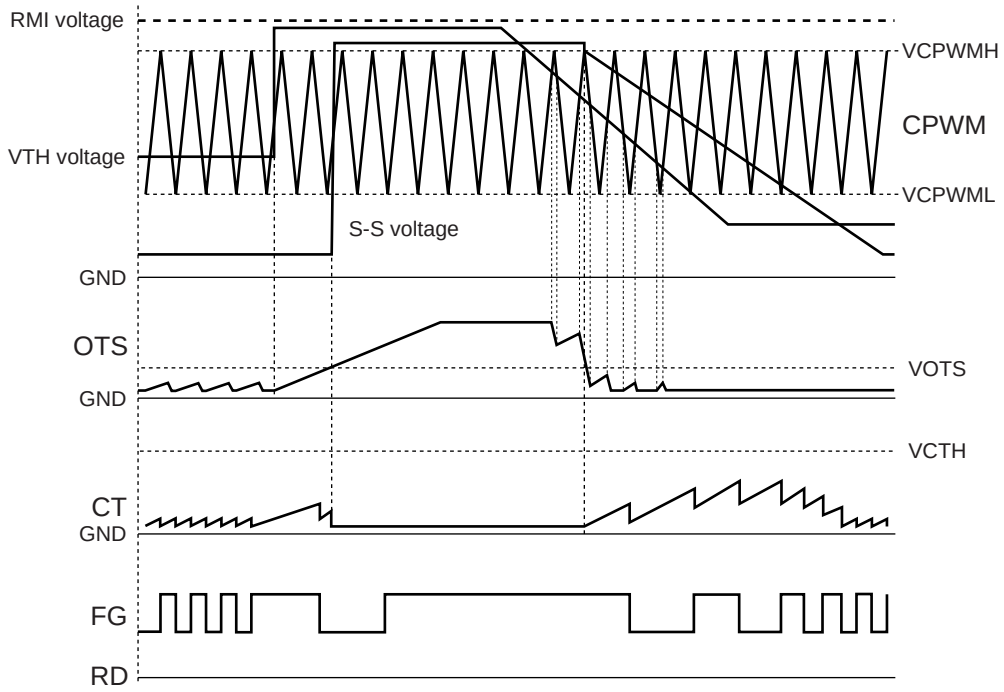
(2) At VTH > RMI voltage



Adjust the S-S pin voltage gradient by means of the capacitance of the capacitor between the S-S pin and REG..
Recommended capacitor: 0.1μ to 1μF

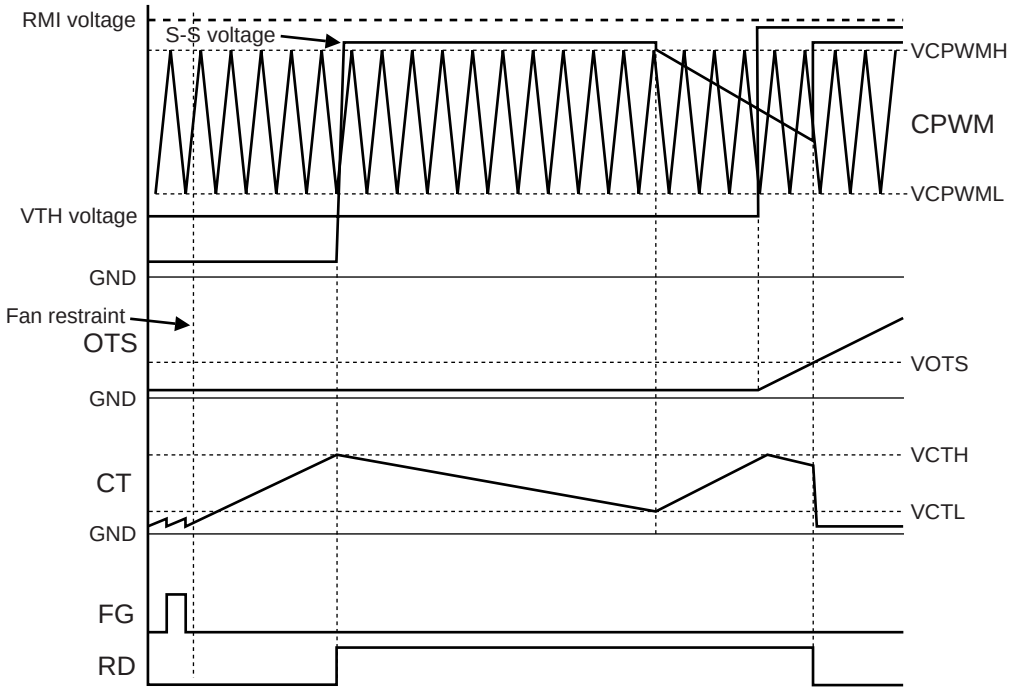
Control timing chart (ON-time start, Lock protection)

(1) When a stop signal based on the VTH voltage has been input during normal rotation



When the output duty ratio based on the VTH/RMI input drops to below 1% or so, the OTS voltage rises, and when it reaches VOTS, the standby mode is established, the CT pin discharges, and the S-S pin is charged. In the standby mode, if the drive mode has been established again by the VTH/RMI input, the rotation is started immediately with soft start. The CT pin discharges at the same time as the switching of FG. For details on lock protection, refer to (2).

(2) When a stop signal based on the VTH voltage has been input while the fan is constrained



When the fan is constrained, the CT pin voltage rises, and when it reaches VCTH, the lock protection mode is established, and OUTP is set to OFF and RD is set to OFF.
When the lock protection mode is established, the CT pin discharges, and when VCTL is reached, restart (soft start) is initiated. When rotation is started and the FG signal is switched, RD is set to low.
Note: RD is also set to low when the standby mode is established when locked.