

System motor driver for CD/DVD Player

4ch System Motor Driver for Car Audio

BD8266EFV-M

●General Description

BD8266EFV-M is BTL driver of 5 inputs and 4 outputs for Car CDs developed for SPINDLE motor (CH1), SLED/LOADING motor (CH2) and coil drive for actuator(CH3:TRAKING CH4:FOCUS). It can drive motor and coil of the CD/DVD drive.

●Features

- Drive at PowVCC=5V and 8V with wide Maximum Output Amplitude .
- Switches SLED/LOADING input by CNT terminal.
- Incorporates mute function by CNT terminal and MUTE terminal.
- Preventing the overcurrent to the load by the FOCUS Over Current Protection (OCP) function.
- Built-in TSD, UVLO.
- PowVCC1 and PowVCC2 are independent, and an efficient drive is possible.
PowVCC1 : for SPINDLE&SLED/LOADING.
PowVCC2 : for TRAKING & FOCUS.
- AEC-Q100 Qualified

●Applications

- Car Audio

●Key Specifications

- Input voltage range: 4.5V to 10.0V
- Operating temperature range -40°C to +85°C

PowVCC1=PowVCC2=8V, RL=8Ω

- Maximum Output Amplitude (CH1) 6.5V(Typ.)
- Maximum Output Amplitude (CH2) 7.0V(Typ.)
- Maximum Output Amplitude (CH3,CH4) 6.0V(Typ.)

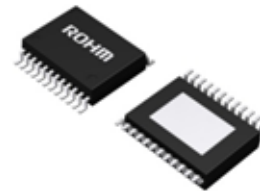
PowVCC1=PowVCC2=5V, RL=8Ω

- Maximum Output Amplitude (CH1) 4.1V(Typ.)
- Maximum Output Amplitude (CH2) 4.5V(Typ.)
- Maximum Output Amplitude (CH3,CH4) 3.8V(Typ.)

●Package

HTSSOP-B24

W(Typ.) D(Typ.) H(Max.)
7.80mm x 7.60mm x 1.00mm



HTSSOP-B24

●Typical Application Circuit

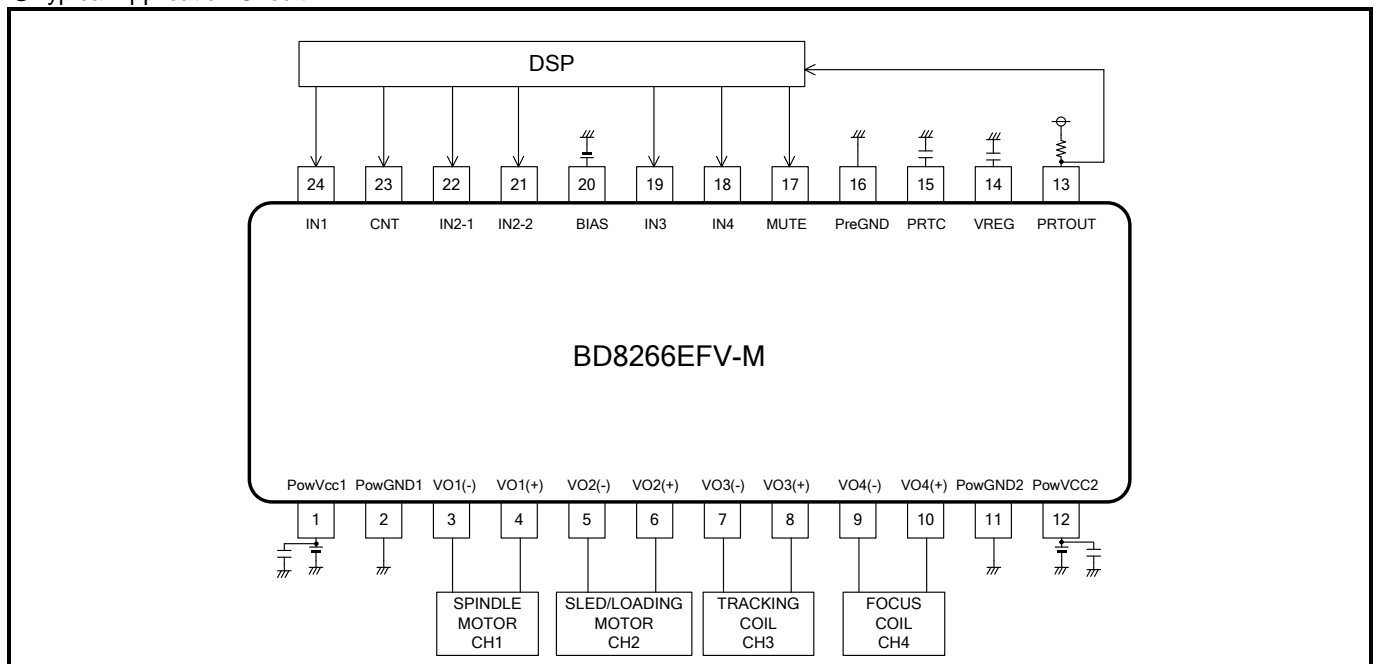


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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●Pin Configuration (TOPVIEW)

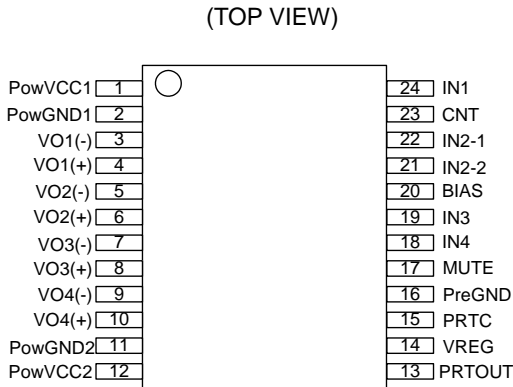


Figure 2. Pin Configuration

●Pin Description

| NO. | Signal | Function |
|-----|---------|---|
| 1 | PowVCC1 | CH1,2 Power Supply Input |
| 2 | PowGND1 | Power GND1 |
| 3 | VO1(-) | Driver CH1 negative output |
| 4 | VO1(+) | Driver CH1 positive output |
| 5 | VO2(-) | Driver CH2 negative output |
| 6 | VO2(+) | Driver CH2 positive output |
| 7 | VO3(-) | Driver CH3 negative output |
| 8 | VO3(+) | Driver CH3 positive output |
| 9 | VO4(-) | Driver CH4 negative output |
| 10 | VO4(+) | Driver CH4 positive output |
| 11 | PowGND2 | Power GND2 |
| 12 | PowVCC2 | CH3,4 Power Supply Input |
| 13 | PRTOUT | Output overcurrent protection flag |
| 14 | VREG | Power output for internal logic |
| 15 | PRTC | Overcurrent protection function ON time setting |
| 16 | PreGND | Pre part GND |
| 17 | MUTE | Mute |
| 18 | IN4 | CH4 (FC:FOCUS) input |
| 19 | IN3 | CH3 (TK:TRACKING) input |
| 20 | BIAS | BIAS input |
| 21 | IN2-2 | CH2-2 (LD:LOADING) input |
| 22 | IN2-1 | CH2-1 (SL:SLED)input |
| 23 | CNT | Control input |
| 24 | IN1 | IN1 (SP:SPINDLE)input |

●Block Diagram

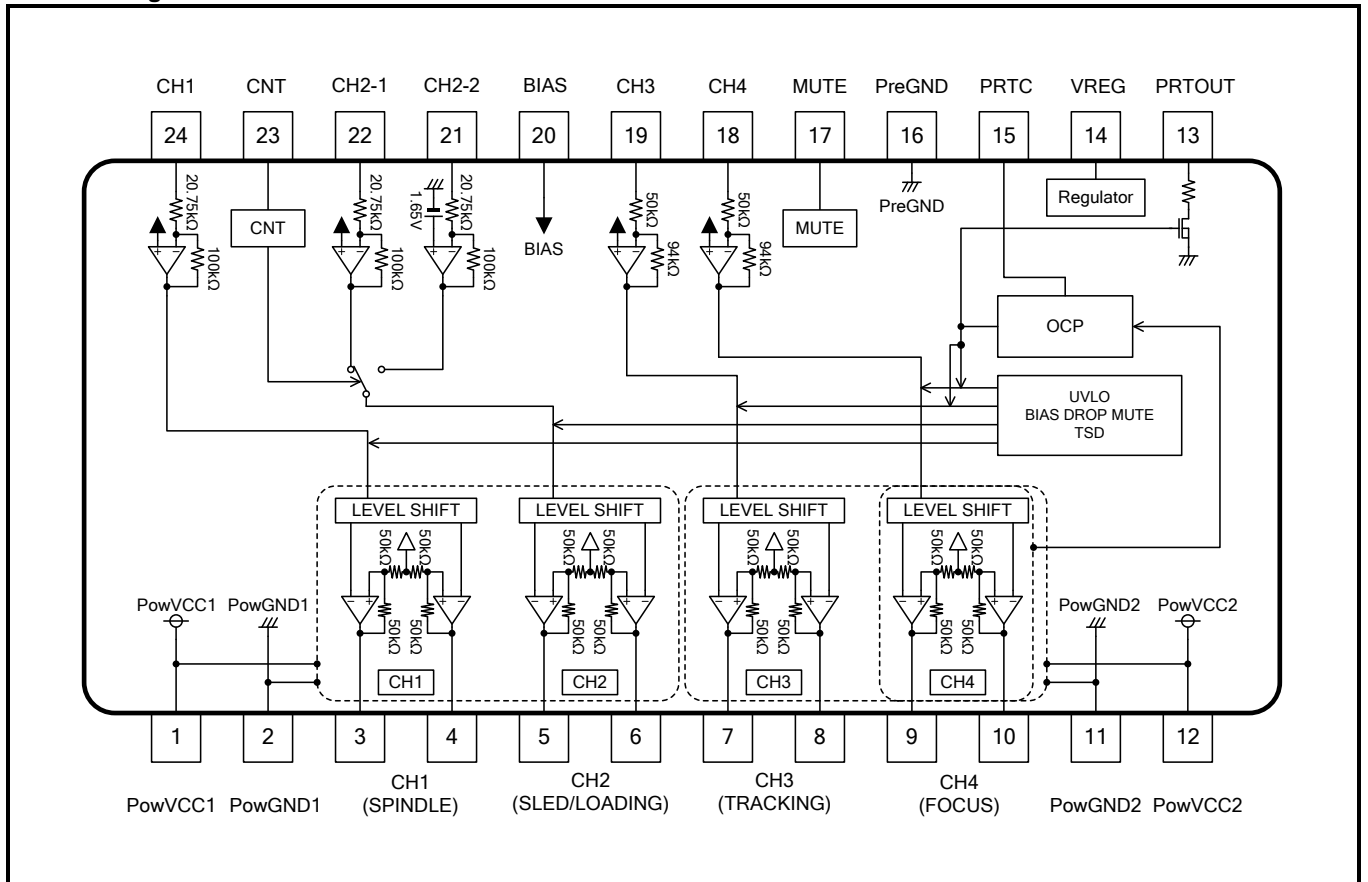


Figure 3. Block Diagram

● Absolute Maximum Ratings (Ta=25°C)

| Parameters | Symbol | Value | Units |
|-----------------------------|---------------------|-------------------|-------|
| Power Supply | PowVCC1 PowVCC2 | 15 | V |
| Input Terminal Voltage 1 | VIN1 ^{*1} | PowVCC1 | V |
| Input Terminal Voltage 2 | VIN2 ^{*2} | 7 | V |
| Output Terminal Voltage 1 | VOUT1 ^{*3} | PowVCC1 | V |
| Output Terminal Voltage 2 | VOUT2 ^{*4} | 7 | V |
| Power dissipation | Pd | 1.1 ^{*5} | W |
| | | 4.0 ^{*6} | |
| Operating temperature range | Topr | -40 to +85 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |
| Junction temperature | Tjmax | +150 | °C |

*1 VIN1 Application terminal: CNT, MUTE

*2 VIN2 Application terminal: IN1, IN2-1, IN2-2, IN3, IN4, BIAS, PRTC

*3 VOUT1 Application terminal: PRTOU1.

*4 VOUT2 Application terminal: VREG.

*5 70mm×70mm×1.6mm, occupied copper foil is less than 3%, one layer substrate (back copper foil 0mm×0mm)
Reduce power by 8.8mW for each degree above 25°C

*6 70mm×70mm×1.6mm, occupied copper foil is less than 3%, four layer substrate (back copper foil 70mm×70mm)
Reduce power by 32.0mW for each degree above 25°C.

● Operating conditions (Ta=-40 to+85°C)

| Parameters | Symbol | Min. | Typ. | Max. | Units |
|---|------------|------|------|---------|-------|
| Pre-block power supply voltage | PowVCC1 | 4.5 | 8.0 | 10.0 | V |
| Spindle driver power-block power supply voltage ^{*7} | | | | | |
| Loading/Sled driver power-block power supply voltage ^{*7} | PowVCC2 | 4.5 | 8.0 | PowVCC1 | V |
| Actuator system power supply ^{*7} | | | | | |
| Voltage difference between PowVCC1 and PowVCC2 (PowVCC1-PowVCC2) | DiffPowVCC | 0 | - | 3.5 | V |

*7 Please decide the power supply voltage after considering power dissipation.

●Electrical Characteristics (Unless otherwise noted, Ta=25°C, PowVCC1=PowVCC2=8V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---------------------------------|---------|--------|-------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Quiescent Current | IQ | — | 16 | 40 | mA | At no-load, MUTE=High |
| < Driver > | | | | | | |
| Output Offset (CH1,2) | VOOF1 | -100 | 0 | 100 | mV | |
| Output Offset (CH3,4) | VOOF2 | -50 | 0 | 50 | mV | |
| Maximum Output Amplitude (CH1) | VOM1 | 5.8 | 6.5 | — | V | RON(total)=1.7Ω (Typ.) Equivalent |
| Maximum Output Amplitude (CH2) | VOM2 | 6.4 | 7.0 | — | V | RON(total)=0.9Ω (Typ.) Equivalent |
| Maximum Output Amplitude(CH3,4) | VOM34 | 5.3 | 6.0 | — | V | RON(total)=2.5Ω (Typ.) Equivalent |
| Closed Loop Gain (CH1,2) | GV12 | 24.0 | 25.7 | 27.4 | dB | |
| Closed Loop Gain (CH3,4) | GV34 | 15.5 | 17.5 | 19.5 | dB | |
| Input Impedance (CH1,2) | INRCH12 | 15 | 20.75 | 27 | kΩ | |
| Input Impedance (CH3,4) | INRCH34 | 38 | 50 | 62 | kΩ | |
| MUTE Low Level Voltage | VML | — | — | 0.5 | V | |
| MUTE High Level Voltage | VMH | 2.0 | — | — | V | |
| MUTE Input Current | IMUTE | 32 | 52 | 74 | μA | MUTE=3.3V |
| CNT Low Level Voltage | VCNTL | — | — | 0.5 | V | |
| CNT High Level Voltage | VCNTH | 2.0 | — | — | V | |
| CNT Input Current | ICNT | 32 | 52 | 74 | μA | CNT=3.3V |
| BIAS Drop Mute | VBD | 0.5 | 0.7 | 0.9 | V | |
| BIAS Input Current | IBD | 32 | 52 | 74 | μA | BIAS=1.65V |
| LDIN Voltage (SLED is input) | VLDIN | — | 0.1 | 0.3 | V | CNT=Low |
| Internal Bias Voltage | VBIN | 1.53 | 1.65 | 1.77 | V | CNT=High |
| UVLO Release Voltage | UVLOR | 3.8 | 4.0 | 4.2 | V | |
| UVLO Detection Voltage | UVLOD | 3.6 | 3.8 | 4.0 | V | |
| VREG Voltage | VREG | — | 5.0 | — | V | CVREG=0.1μF |

●Electrical Characteristics (Unless otherwise noted, Ta=25°C, PowVCC1=PowVCC2=8V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|--|----------|--------|------|------|------|---------------------------|
| | | Min. | Typ. | Max. | | |
| < Focus overcurrent protection function > | | | | | | |
| PRTC Default Voltage | VPRTREF | — | 0 | 0.3 | V | At no-load |
| PRTC Protection Detection Voltage | VPRTDET | 2.7 | 3.0 | 3.3 | V | |
| PRTC Protection Release Voltage | VPRTOFF | 0.7 | 1.0 | 1.3 | V | |
| PRTOUT Low Output Voltage | VPOL | — | 0.1 | 0.3 | V | PRTOUT : 3.3V,33kΩ pullup |
| OCP Detection Current | IOCP | — | 470 | — | mA | |
| PRTC SINK Current | IPTCSINK | — | 43 | — | μA | PRTC=1V |

●Electrical Characteristics (Ta=25°C, PowVCC1=PowVCC2=5V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---------------------------------|--------|--------|------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Maximum Output Amplitude (CH1) | VOM1 | 3.7 | 4.1 | — | V | RON(total)=1.7Ω (Typ.) Equivalent |
| Maximum Output Amplitude (CH2) | VOM2 | 4.1 | 4.5 | — | V | RON(total)=0.9Ω (Typ.) Equivalent |
| Maximum Output Amplitude(CH3,4) | VOM34 | 3.4 | 3.8 | — | V | RON(total)=2.5Ω (Typ.) Equivalent |

●Electrical Characteristics (Unless otherwise noted, Ta=-40 to 85°C, PowVCC1=PowVCC2=8V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---------------------------------|---------|--------|-------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Quiescent Current | IQ | — | 16 | 44 | mA | At no-load, MUTE=High |
| < Driver > | | | | | | |
| Output Offset (CH1,2) | VOOF1 | -100 | 0 | 100 | mV | |
| Output Offset (CH3,4) | VOOF2 | -50 | 0 | 50 | mV | |
| Maximum Output Amplitude (CH1) | VOM1 | 5.5 | 6.5 | — | V | RON(total)=1.7Ω (Typ.) Equivalent |
| Maximum Output Amplitude (CH2) | VOM2 | 6.4 | 7.0 | — | V | RON(total)=0.9Ω (Typ.) Equivalent |
| Maximum Output Amplitude(CH3,4) | VOM34 | 4.8 | 6.0 | — | V | RON(total)=2.5Ω (Typ.) Equivalent |
| Closed Loop Gain (CH1,2) | GV12 | 24.0 | 25.7 | 27.4 | dB | |
| Closed Loop Gain (CH3,4) | GV34 | 15.5 | 17.5 | 19.5 | dB | |
| Input Impedance (CH1,2) | INRCH12 | 11 | 20.75 | 29 | kΩ | |
| Input Impedance (CH3,4) | INRCH34 | 34 | 50 | 66 | kΩ | |
| MUTE Low Level Voltage | VML | — | — | 0.4 | V | MUTE=3.3V |
| MUTE High Level Voltage | VMH | 2.0 | — | — | V | |
| MUTE Input Current | IMUTE | 22 | 52 | 108 | μA | |
| CNT Low Level Voltage | VCNTL | — | — | 0.4 | V | CNT=3.3V |
| CNT High Level Voltage | VCNTH | 2.0 | — | — | V | |
| CNT Input Current | ICNT | 22 | 52 | 108 | μA | BIAS=1.65V |
| BIAS Drop Mute | VBD | 0.3 | 0.7 | 1.1 | V | CNT=Low |
| BIAS Input Current | IBD | 22 | 52 | 108 | μA | CNT=High |
| LDIN Voltage (SLED is input) | VLDIN | — | 0.1 | 0.3 | V | |
| Internal Bias Voltage | VBIN | 1.45 | 1.65 | 1.85 | V | |
| UVLO Release Voltage | UVLOR | 3.7 | 4.0 | 4.3 | V | |
| UVLO Detection Voltage | UVLOD | 3.5 | 3.8 | 4.1 | V | |
| VREG Voltage | VREG | — | 5.0 | — | V | CVREG=0.1μF |

●Electrical Characteristics (Unless otherwise noted, Ta=-40 to 85°C, PowVCC1=PowVCC2=8V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|--|----------|--------|------|------|------|---------------------------|
| | | Min. | Typ. | Max. | | |
| < Focus overcurrent protection function > | | | | | | |
| PRTC Default Voltage | VPRTREF | — | 0 | 0.3 | V | At no-load |
| PRTC Protection Detection Voltage | VPRTDET | 2.5 | 3.0 | 3.5 | V | |
| PRTC Protection Release Voltage | VPRTOFF | 0.5 | 1.0 | 1.5 | V | |
| PRTOUT Low Output Voltage | VPOL | — | 0.1 | 0.4 | V | PRTOUT : 3.3V,33kΩ pullup |
| OCP Detection Current | IOCP | — | 470 | — | mA | |
| PRTC SINK Current | IPTCSINK | — | 43 | — | μA | PRTC=1V |

●Electrical Characteristics (Unless otherwise noted, Ta=-40 to 85°C, PowVCC1=PowVCC2=5V, BIAS=1.65V, RL=8Ω)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---------------------------------|--------|--------|------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Maximum Output Amplitude (CH1) | VOM1 | 3.7 | 4.1 | — | V | RON(total)=1.7Ω (Typ.) Equivalent |
| Maximum Output Amplitude (CH2) | VOM2 | 4.1 | 4.5 | — | V | RON(total)=0.9Ω (Typ.) Equivalent |
| Maximum Output Amplitude(CH3,4) | VOM34 | 3.4 | 3.8 | — | V | RON(total)=2.5Ω (Typ.) Equivalent |

● Typical Performance Curves

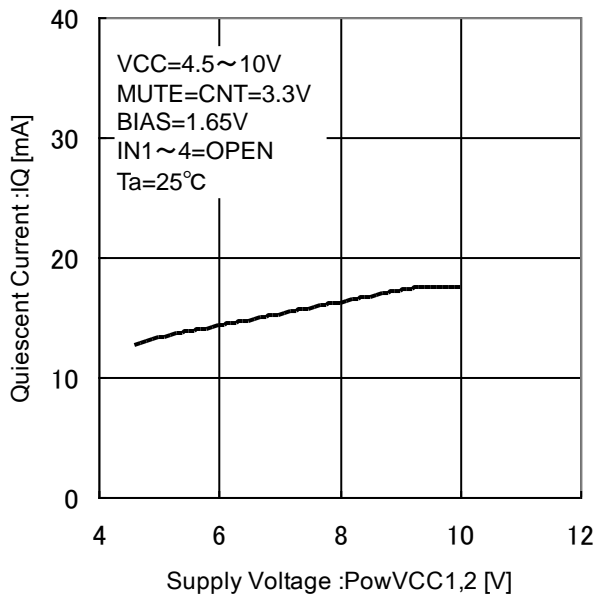


Figure 4. Quiescent Current

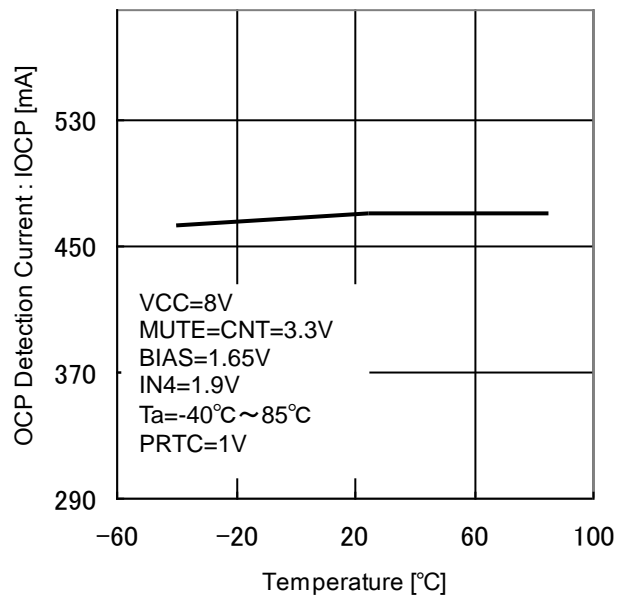


Figure 5. OCP Detection Current

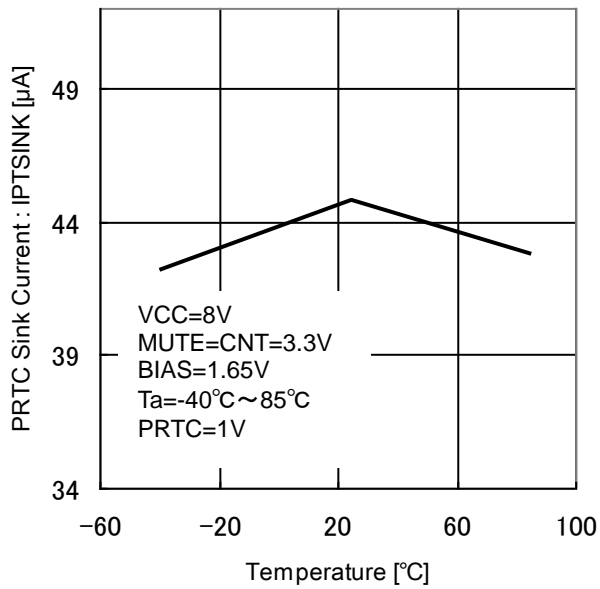


Figure 6. PRTC Sink Current

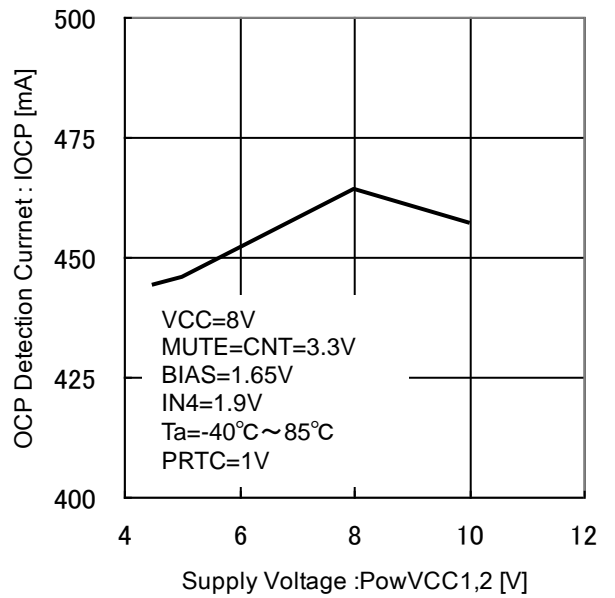


Figure 7. OCP Detection Current

● Typical Performance Curves

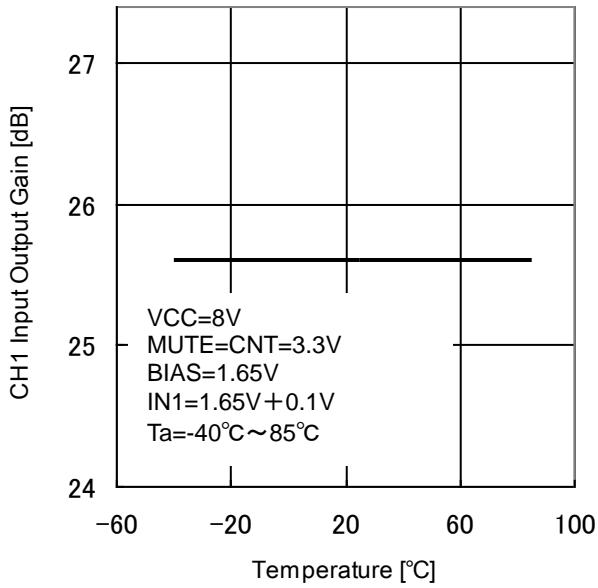


Figure 8. CH1 Closed Loop Gain

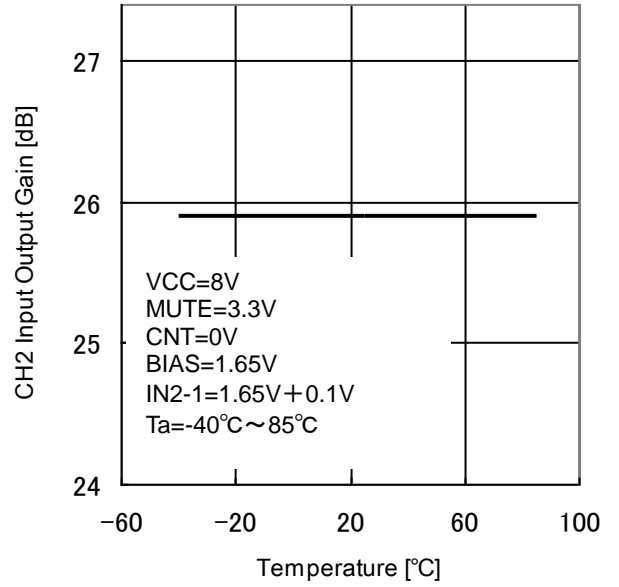


Figure 9. CH2 Closed Loop Gain

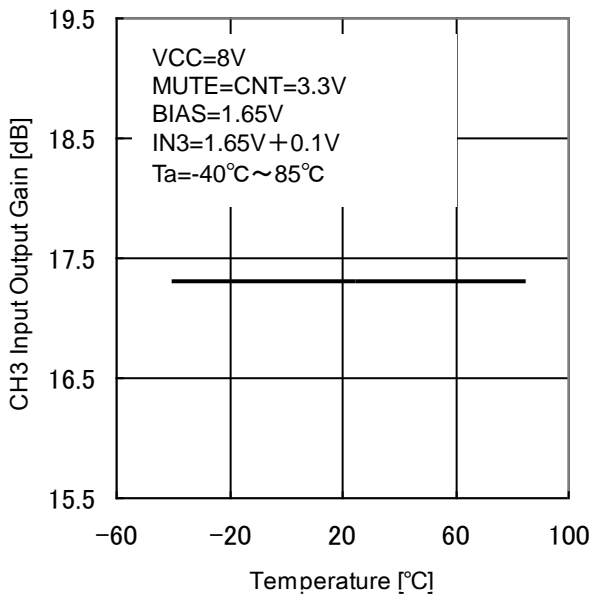


Figure 10. CH3 Closed Loop Gain

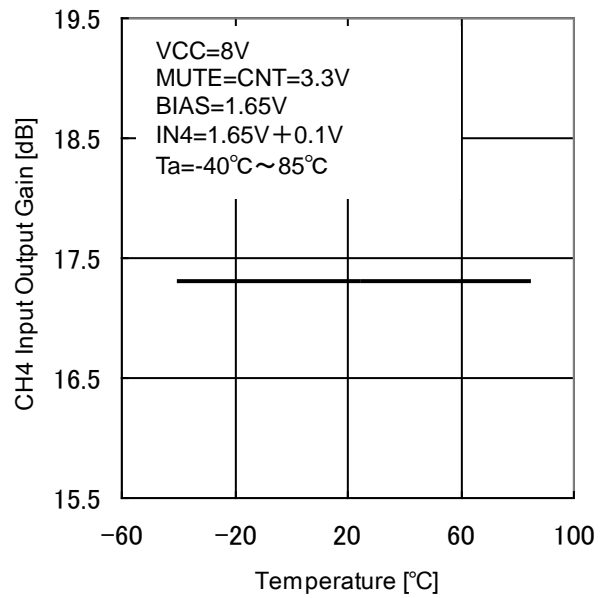


Figure 11. CH4 Closed Loop Gain

● Typical Performance Curves

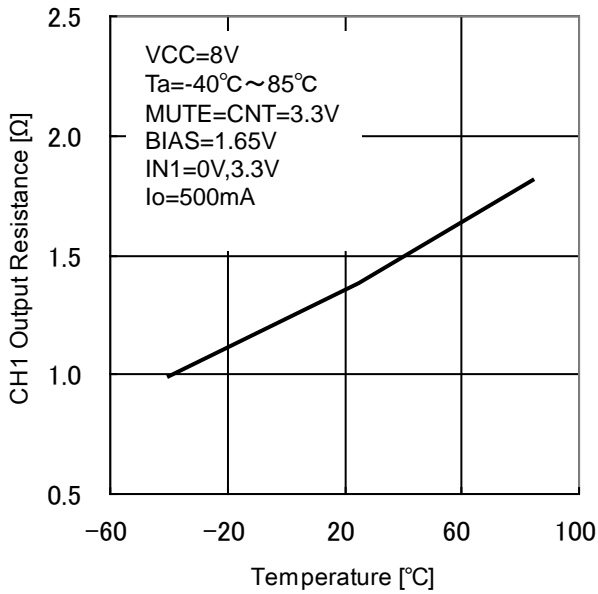


Figure 12. CH1 Output ON resistance characteristic

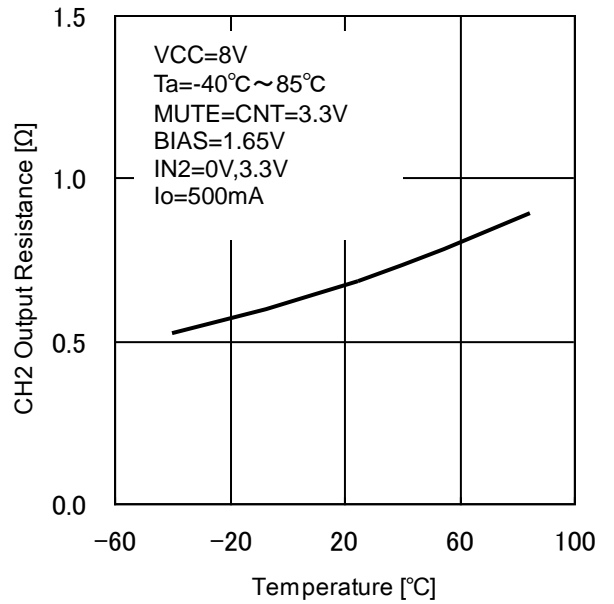


Figure 13. CH2 Output ON resistance characteristic

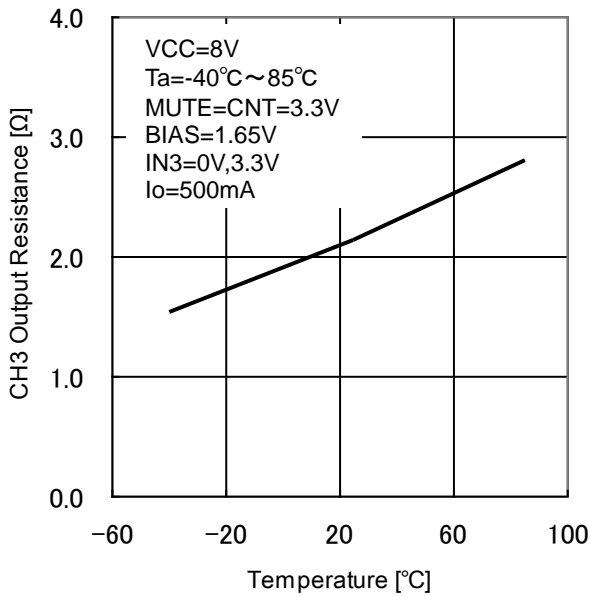


Figure 14. CH3 Output ON resistance characteristic

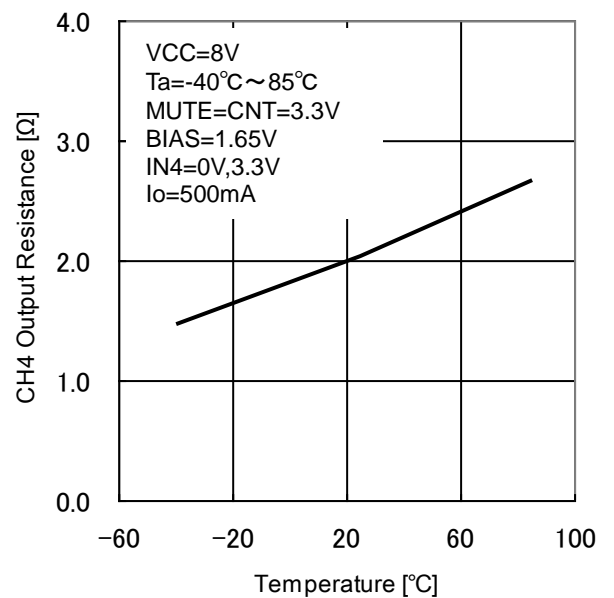


Figure 15. CH4 Output ON resistance characteristic

● Typical Performance Curves

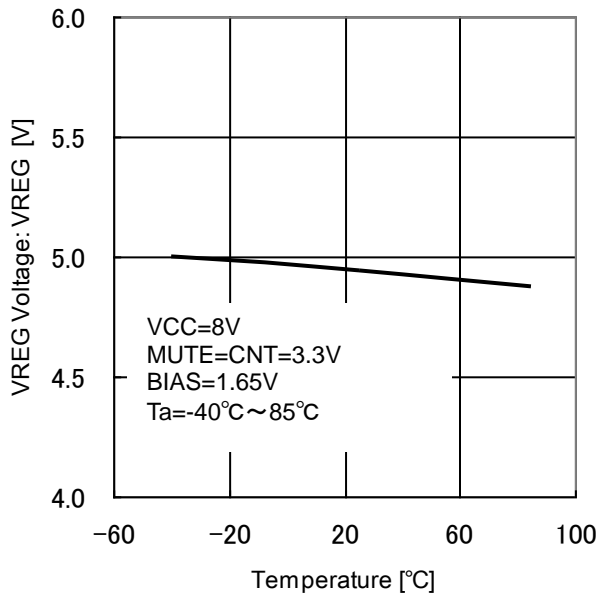


Figure 16. VREG Voltage

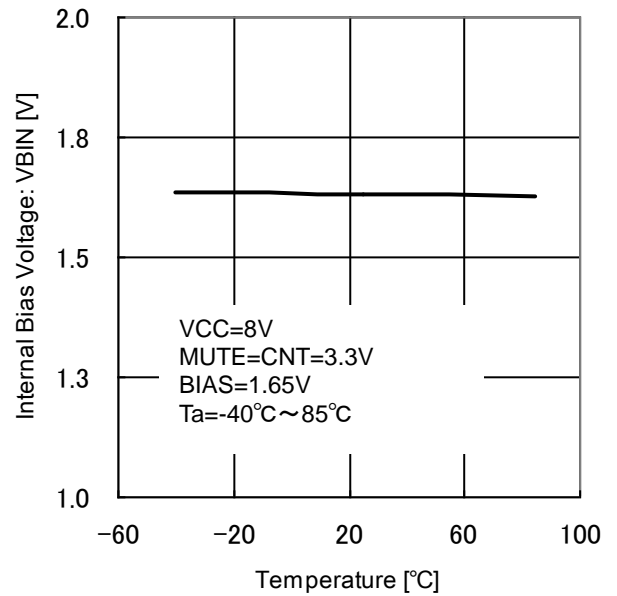


Figure 17. Internal Bias Voltage

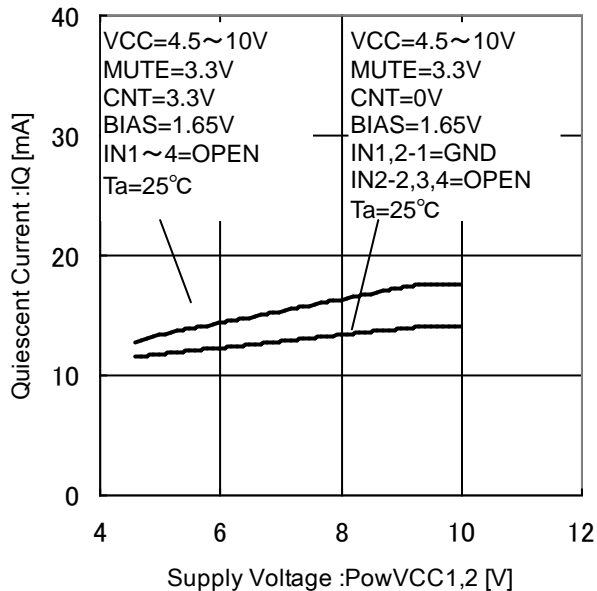


Figure 18. Quiescent Current at IN1~4=OPEN, Circuit Current at IN1=IN2-1=GND

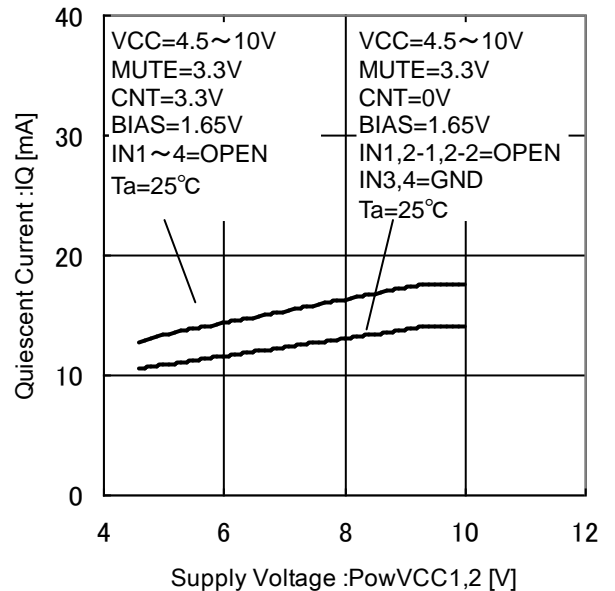


Figure 19. Quiescent Current at IN1~4=OPEN, Circuit Current at IN3=IN4=GND

●Operation description

- The driver can put the mute by switching the terminal MUTE and the terminal CNT to High level and Low level. The table below shows the logic.

▼Driver logic (Normally operation)

| State | Input | | | Output *8*9 | | | | |
|-------|-------|-----|------|-------------|-----------|-----------|---------|---------|
| | MUTE | CNT | BIAS | CH1(SP) | CH2-1(SL) | CH2-2(LD) | CH3(TK) | CH4(FC) |
| 1 | H | H | H | Active | MUTE | Active | Active | Active |
| 2 | H | L | H | Active | Active | MUTE | Active | Active |
| 3 | L | H | H | MUTE | MUTE | Active | MUTE | MUTE |
| 4 | L | L | H | MUTE | MUTE | MUTE | MUTE | MUTE |
| 5 | H | H | L | MUTE | MUTE | Active | MUTE | MUTE |
| 6 | H | L | L | MUTE | MUTE | MUTE | MUTE | MUTE |
| 7 | L | H | L | MUTE | MUTE | Active | MUTE | MUTE |
| 8 | L | L | L | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

▼Driver logic (OCP Protected operation)

| State | Input | | | Output *8*9 | | | | |
|-------|-------|-----|------|-------------|-----------|-----------|---------|---------|
| | MUTE | CNT | BIAS | CH1(SP) | CH2-1(SL) | CH2-2(LD) | CH3(TK) | CH4(FC) |
| 9 | H | H | H | Active | MUTE | Active | MUTE | MUTE |
| 10 | H | L | H | Active | Active | MUTE | MUTE | MUTE |
| 11 | L | H | H | MUTE | MUTE | Active | MUTE | MUTE |
| 12 | L | L | H | MUTE | MUTE | MUTE | MUTE | MUTE |
| 13 | H | H | L | MUTE | MUTE | Active | MUTE | MUTE |
| 14 | H | L | L | MUTE | MUTE | MUTE | MUTE | MUTE |
| 15 | L | H | L | MUTE | MUTE | Active | MUTE | MUTE |
| 16 | L | L | L | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

▼Driver logic (UVLO,TSD Protected operation)

| State | Input | | | Output *8*9 | | | | |
|-------|------------------|-----|------|-------------|-----------|-----------|---------|---------|
| | MUTE | CNT | BIAS | CH1(SP) | CH2-1(SL) | CH2-2(LD) | CH3(TK) | CH4(FC) |
| 17 | L | L | L | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 18 | The others state | | | MUTE | MUTE | MUTE | MUTE | MUTE |

*8 MUTE : Both positive and negative output voltages become PowVCC/2.

*9 Hi-Z : Both positive and negative outputs become Hi-Z.

- BIAS drop mute function
BIAS terminal (Pin20) put the mute by 0.7V(Typ.) or less. Please make it to 1.3V or more in the normally operation.
- UVLO function
Output current put the mute when PowVCC1 voltage becomes 3.8V(Typ.) or less. The driver part circuit stands up when rising to 4.0V(typ.) again.
- Voltage reference(VREG)
5V (Typ.) is generated from the PowVCC1 input voltage. Connect a capacitor (CVREG = 0.1μF Typ.) to the VREG terminal for phase compensation. Operation may become unstable if CVREG is not connected.

5. Focus overcurrent protection function

It is a function to turn off the actuator output when detecting the FOCUS(CH4) over current state more than set time. When the load current that flows to FOCUS (CH4) output NMOS exceeds 470mA (Typ.), the current proportional to the load current value is charged to the capacitor. The time to protection is decided depending on the capacitor value connected with the terminal PRTC. The default value of the terminal PRTC is 0V (Typ.).

It protects with 3.0V (Typ.). (Please note that protection operates when the potential of 3.0V or more remains in the terminal PRTC when the power supply starts, and the standby is released. It is likely to protect when the power supply is started up in the slew rate of 1ms or less, and please start up the power supply in the slew rate of 1ms or more.)When the terminal PRTC is 1.0V (Typ.) or less, protection is released.

Please delete C of the terminal PRTC and short-circuited with GND when the overcurrent function unused.

| PRTC | PRTOUT (OUTPUT) | CH3(TRAKING)Output CH4(FOCUS)Output |
|-------|-----------------|--|
| >3.0V | H | MUTE (Protection state) |
| <3.0V | L | Active |

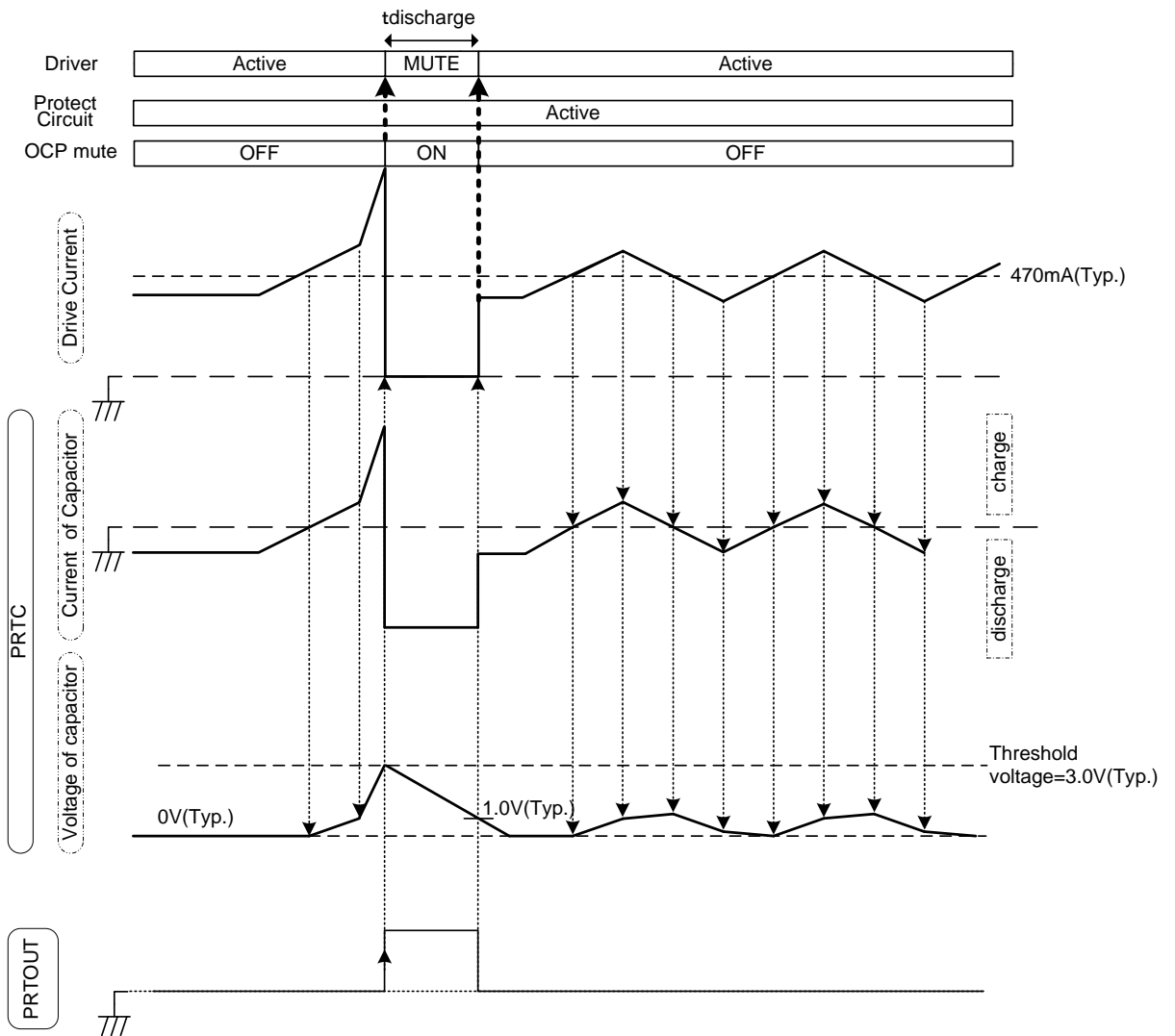


Figure 20. OCP Timing Chart

▼ Focus overcurrent protection circuit (OCP) setting

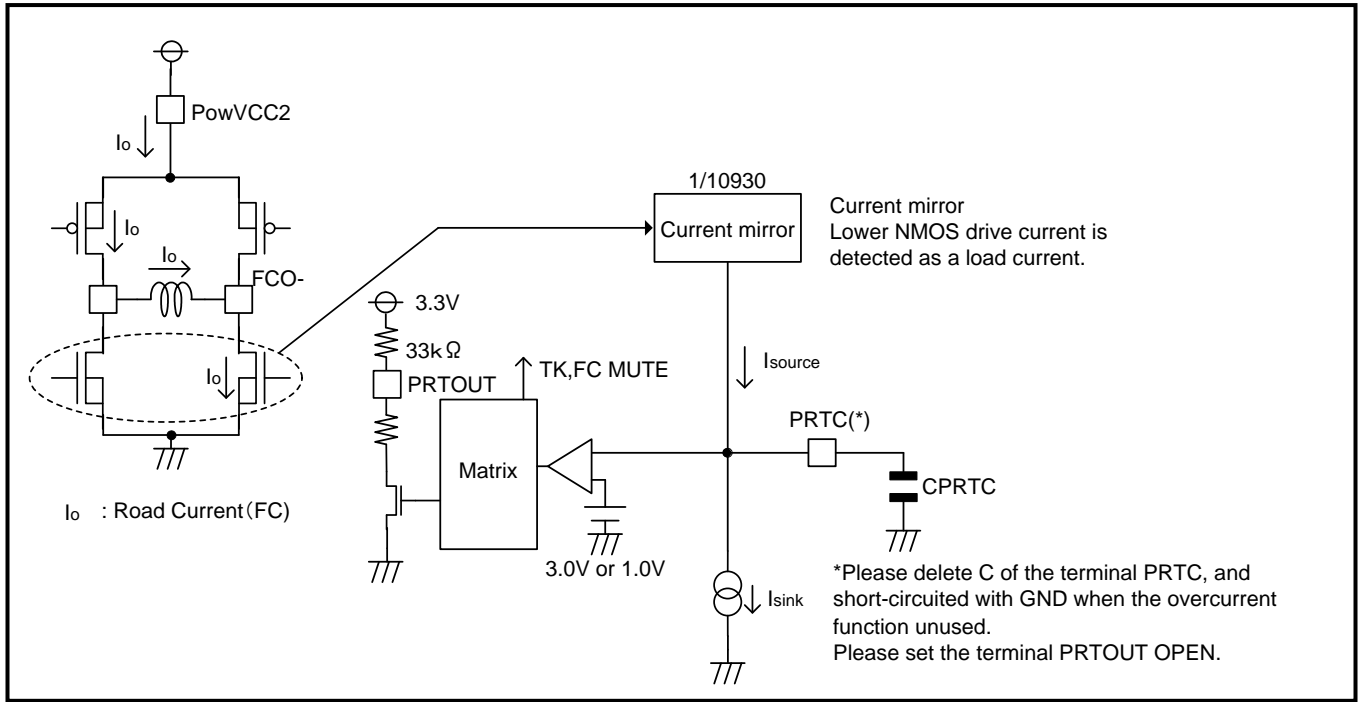


Figure 21. OCP Setting

PowVCC1=PowVCC2=8V, Ta=25°C

$$I_{sink} = 43\mu A(Typ.) \dots\dots ①$$

$$I_{source} = \frac{I_o}{10930} \dots\dots ②$$

Load current that begins to be detected I_t as over current (Threshold current) : $I_t = 43\mu A \times 10930 = 470mA(Typ.)$

Error detection flag output time $t_{detective}$: The charge is started to CPRTC reaches 3.0V from 0V, and the time to becoming PRTOUT =High.

$$CPRTC \times VRTDET = (I_{source} - I_{sink}) \times t_{detective} \quad (VRTDET = 3.0V(Typ.))$$

$$\therefore t_{detective} = \frac{CPRTC \times VRTDET}{I_{source} - I_{sink}}$$

$$\therefore t_{detective} = \frac{CPRTC \times VRTDET}{\frac{I_o}{10930} - 43\mu A} \dots\dots ③ (*: ①, ②)$$

When assuming $t_{detective} = 0.5s$, $I_o = 500mA$ as an example

$$③ \quad CPRTC = \frac{t_{detective}}{VRTDET} \times \left(\frac{I_o}{10930} - 43\mu A \right) = \frac{0.5s}{3.0V} \times \left(\frac{500mA}{10930} - 43\mu A \right) = 0.46\mu F$$

MUTE release time $t_{discharge}$: Electricity is discharged from CPRTC after it becomes PRTOUT =High and time until the PRTC voltage drops from 3.0V to 1.0V.

$$CPRTC \times (VRTDET - VRTOFF) = I_{sink} \times t_{discharge}$$

$$\therefore t_{discharge} = \frac{CPRTC \times (VRTDET - VRTOFF)}{I_{sink}}$$

$$\therefore t_{discharge} = \frac{0.46\mu A \times (3.0V - 1.0V)}{43\mu A} = 21ms$$

6. Output Amplitude calculation

P) SPINDLE,SLED/LOADING

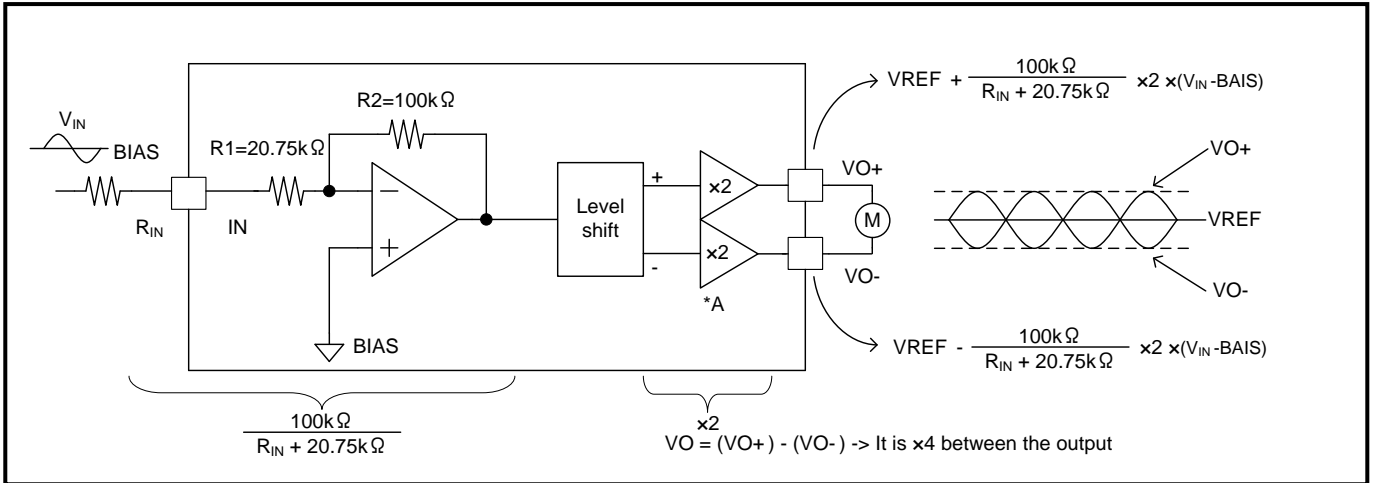


Figure 22. SPINDLE,SLED/LOADING Closed Loop Gain calculation

$$\text{Gain} = \frac{VO}{V_{IN}} = \frac{100k\Omega}{R_{IN} + 20.75k\Omega} \times 2 \times 2$$

Example $R_{IN} = 0k\Omega$

$$\text{Gain} = \frac{100k\Omega}{20.75k\Omega} \times 2 \times 2 = 25.7\text{dB}$$

*Please consider component dispersion
 $R1 = 20.75k\Omega \pm 18\%$
 $R2 = 100k\Omega \pm 18\%$
 $R2/R1 = 4.82 \pm 2.5\%$
 $*A = 2 \pm 18\%, 2 - 16\%$

ii) FOCUS, TACKING

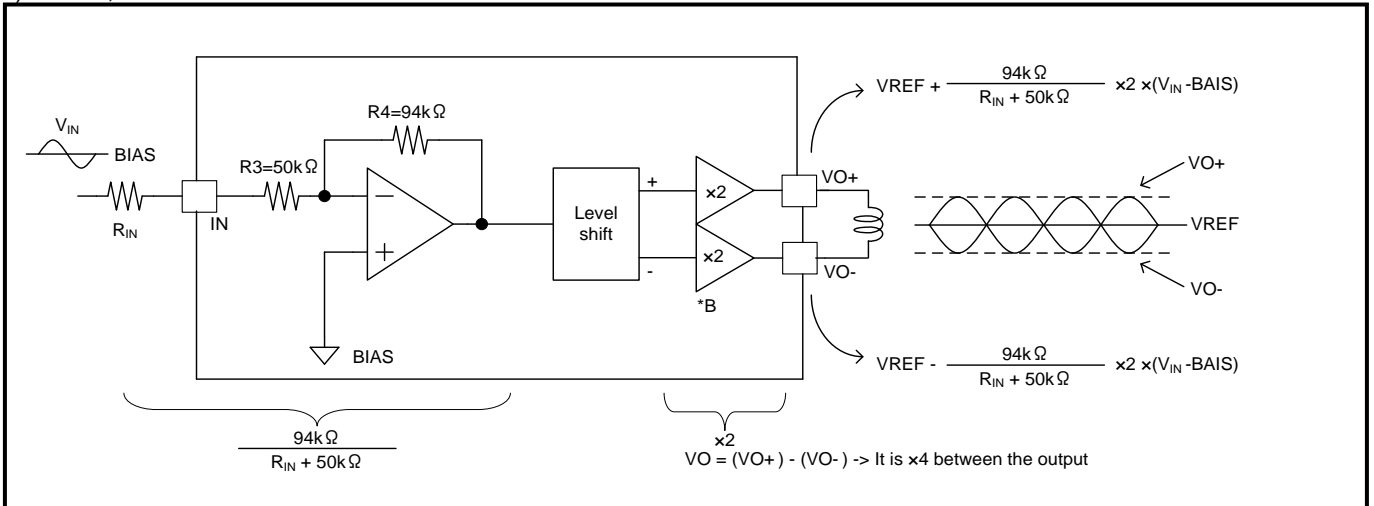


Figure 23. FOCUS, TRACKING Closed Loop Gain calculation

$$\text{Gain} = \frac{VO}{V_{IN}} = \frac{94k\Omega}{R_{IN} + 50k\Omega} \times 2 \times 2$$

Example $R_{IN} = 0k\Omega$

$$\text{Gain} = \frac{VO}{V_{IN}} = \frac{94k\Omega}{50k\Omega} \times 2 \times 2 = 17.5\text{dB}$$

*Please consider component dispersion
 $R3 = 50k\Omega \pm 18\%$
 $R4 = 94k\Omega \pm 18\%$
 $R4/R3 = 1.88 \pm 2.5\%$
 $*B = 2 \pm 22\%, 2 - 19\%$

● Typical Application Circuit

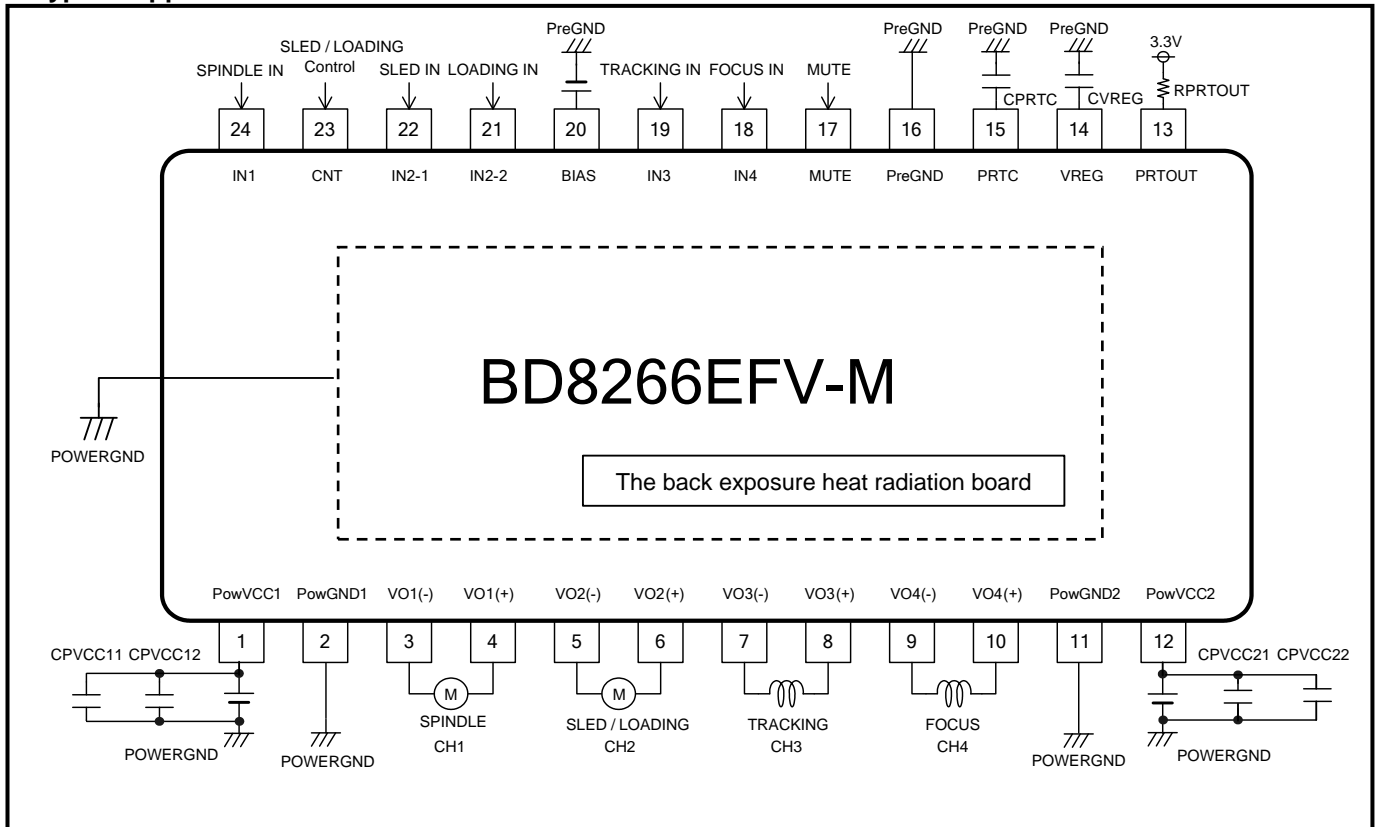


Figure 24. Typical Application Circuit Example

▼ Channel example

| | |
|-----|--------------|
| CH1 | SPINDLE |
| CH2 | SLED/LOADING |
| CH3 | TRACKING |
| CH4 | FOCUS |

▼ External part list

| Component name | Component value | Product name | Manufacturer |
|----------------|-----------------|-------------------|--------------|
| CPVCC11 | 0.1μF | GCM188R11H104KA42 | murata |
| CPVCC12 | 47μF | UCD1E470MCL | Nichicon |
| CPVCC21 | 0.1μF | GCM188R11H104KA42 | murata |
| CPVCC22 | 47μF | UCD1E470MCL | Nichicon |
| CPRTC | 0.1μF~1μF | GCM188R11HxxxKA42 | murata |
| CVREG | 0.1μF | GCM188R11H104KA42 | murata |
| RPRTOUT | 33kΩ | MCR03 Series | Rohm |

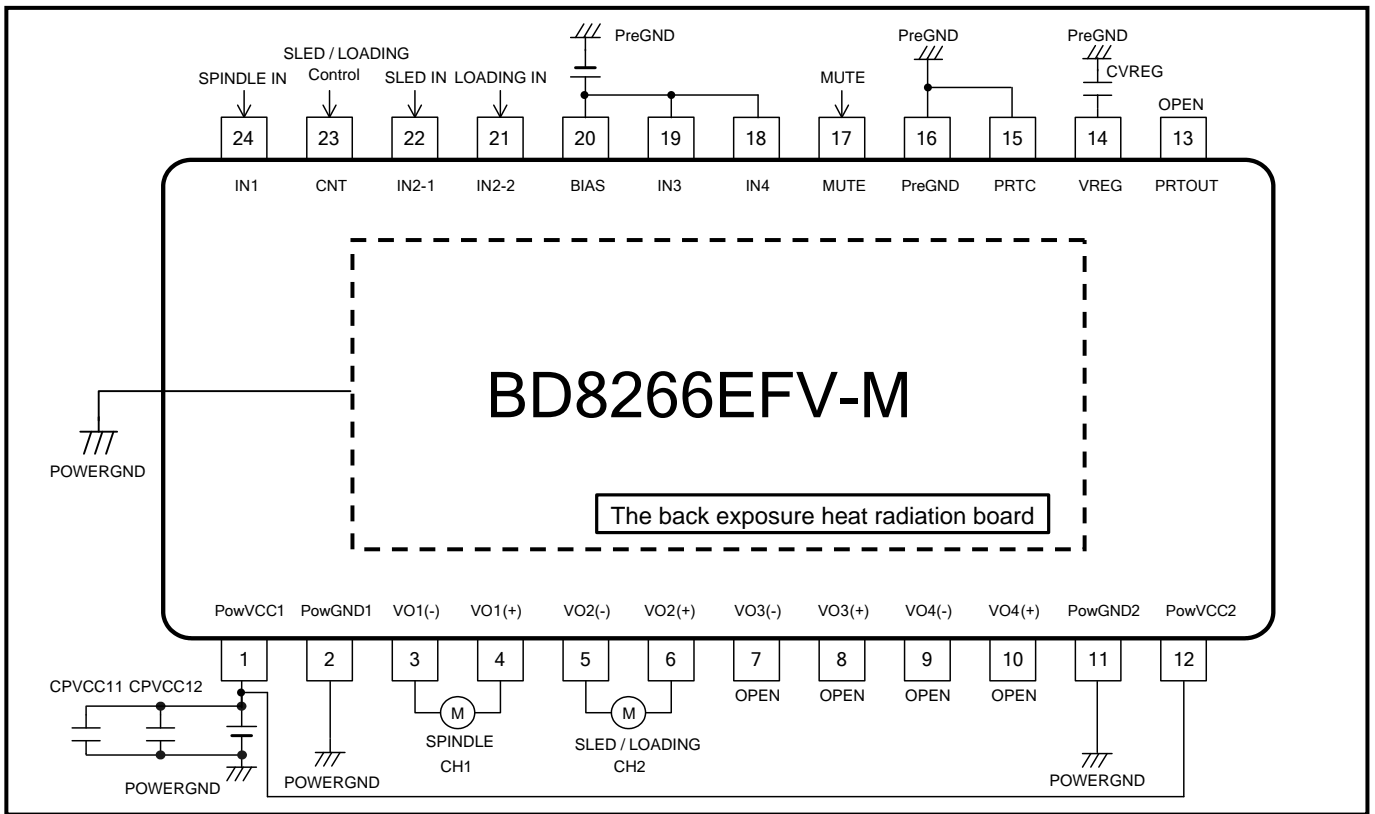


Figure 25. Application Circuit Example : CH1,CH2 are used, and CH3,CH4 are not used

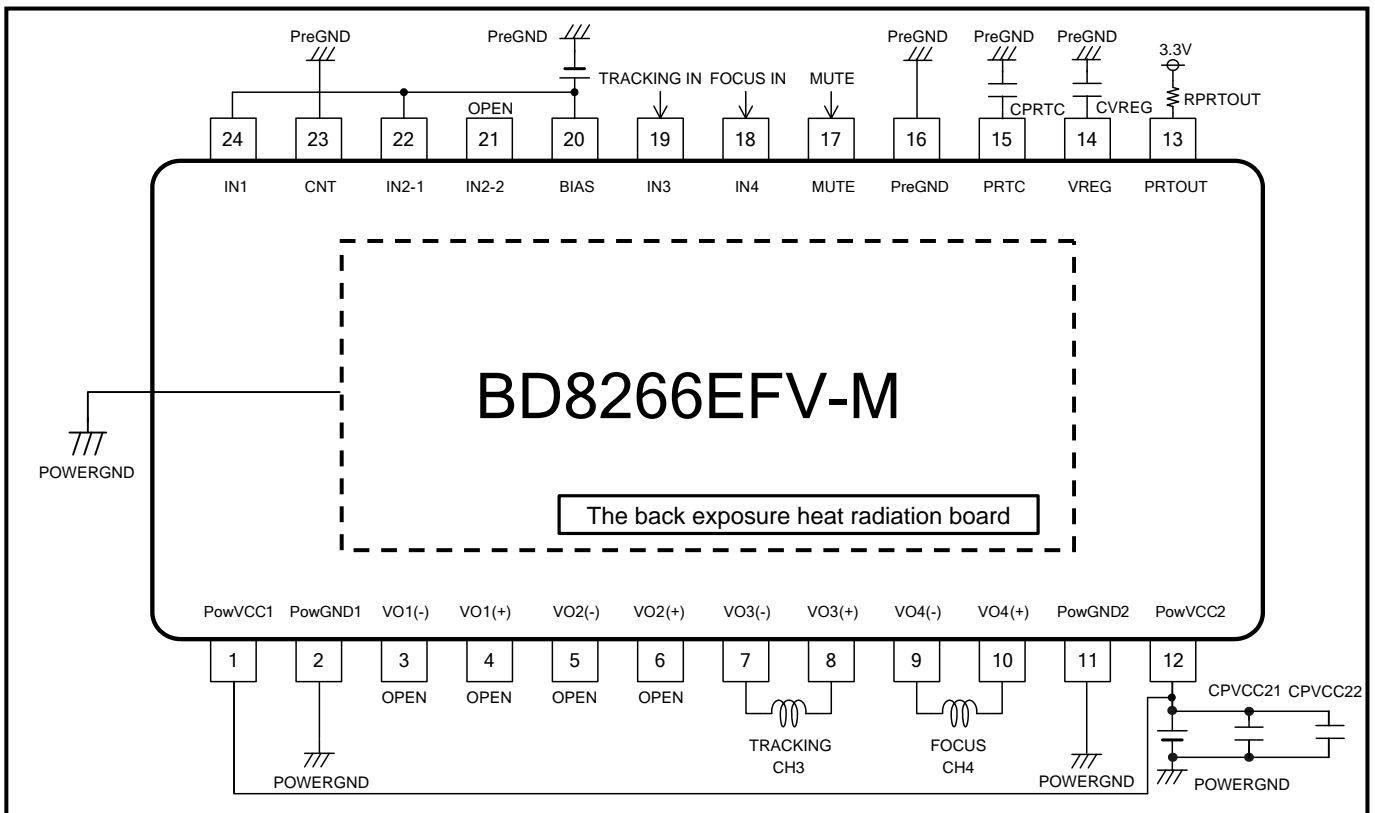


Figure 26. Application Circuit Example : CH1,CH2 are not used, and CH3,CH4 are used

● Power dissipation

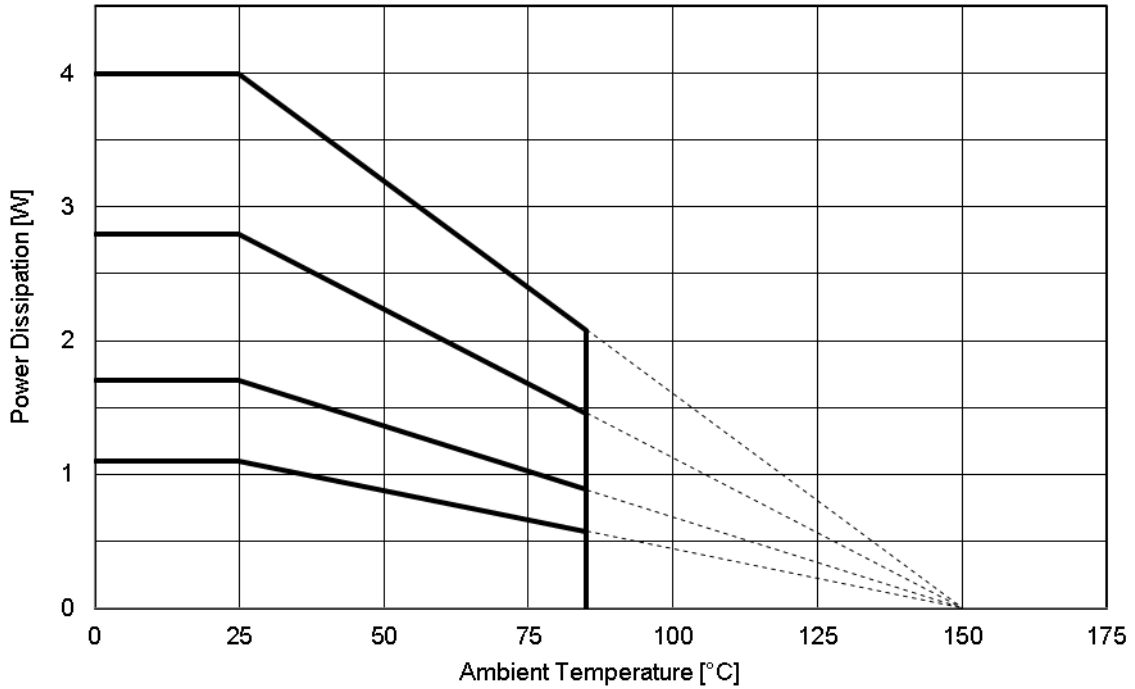


Figure 27. Power Dissipation

70mm×70mm×1.6mm, occupied copper foil is less than 3%, glass epoxy substrate,

The board and the back exposure heat radiation board part of package are connected with solder.

- Board (1) : 1 layer board (copper foil 0mm × 0mm)
- Board (2) : 2 layer board (copper foil 15mm × 15mm)
- Board (3) : 2 layer board (copper foil 70mm × 70mm)
- Board (4) : 4 layer board (copper foil 70mm × 70mm)

- Board (1) : $\theta_{ja} = 113.6 \text{ }^\circ\text{C/W}$
- Board (2) : $\theta_{ja} = 73.5 \text{ }^\circ\text{C/W}$
- Board (3) : $\theta_{ja} = 44.6 \text{ }^\circ\text{C/W}$
- Board (4) : $\theta_{ja} = 31.3 \text{ }^\circ\text{C/W}$

Under Ambient Temperature is 85°C

- Board (1) : Pd =0.57W
- Board (2) : Pd =0.88W
- Board (3) : Pd =1.46W
- Board (4) : Pd =2.08W

CAUTION: Pd depends on number of the PCB layer and area.
This value is measurement value.

● I/O equivalence circuit

| | | |
|--|---|-------------------|
| <p>3. VO1- 4. VO1+ 5. VO2- 6. VO2+</p> | <p>7. VO3- 8. VO3+ 9. VO4- 10. VO4+</p> | <p>13. PRTOUT</p> |
| | | |
| <p>14. VREG</p> | <p>15. PRTC</p> | <p>17. MUTE</p> |
| | | |
| <p>18. IN4 19. IN3</p> | <p>20. BIAS</p> | <p>21. IN2-2</p> |
| | | |
| <p>23. CNT</p> | <p>22. IN2-1 24. IN1</p> | |
| | | |

※Values is typical .

●Operational Note

- 1) Absolute maximum ratings
We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum ratings, such as impressed voltages or the operating temperature range, is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.
- 2) Reverse polarity connection
Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line and motor coil line. Power supply line
- 3) Power supply Line
Due to return of regenerative current by reverse electromotive force, using electrolytic and ceramic suppress filter capacitors (0.1 μ F) close to the IC power input terminals (electric power supply and GND) are recommended. Please note the electrolytic capacitor value decreases at lower temperatures and examine to dispense physical measures for safety. And, for ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.
- 4) GND line
Please keep the GND line the lowest potential always, and check the GND voltage when transient voltages are connected to the IC.
- 5) Thermal design
Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins. This product has exposed the frame to the back side of the package, but please note that it is assumed to use heat radiation efficiency by the heat radiation for this part. Please take the heat radiation pattern on not only the surface of the substrate but also the back of the substrate widely.
- 6) Short circuit mode between terminals and wrong mounting
Do not mount the IC in the wrong direction and displacement, and be careful about the reverse-connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GND.
- 7) Radiation
Strong electromagnetic radiation can cause operation failures.
- 8) ASO (Area of Safety Operation)
Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.
- 9) TSD (Thermal Shut-Down)
The TSD is activated when the junction temperature (Tj) exceeds 175°C, and the output terminal is switched to OPEN. This protection have 25°C(Typ.) hysteresis. The guarantee and protection of set are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.
- 10) Capacitor between output driver and GND
If a large capacitor is connected between the output driver and GND, this IC might be destroyed when Vcc becomes 0V or GND, because the electric charge accumulated in the capacitor flows to the output driver. Please set said capacitor to smaller than 0.1 μ F.
- 11) Inspection by the set circuit board
The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, when attaching or detaching from jig in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC, and vice versa. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

12) Input terminal

This IC is a monolithic IC, and has P⁺ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is formed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminal A on the resistor, at Terminal B on the transistor, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the interference of circuit operation, then the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND (P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.

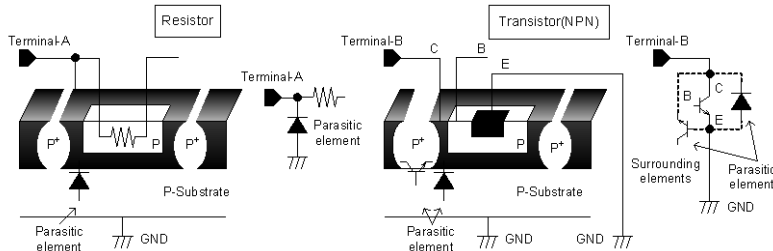


Figure 28. Example of IC Structure

13) Earth wiring pattern

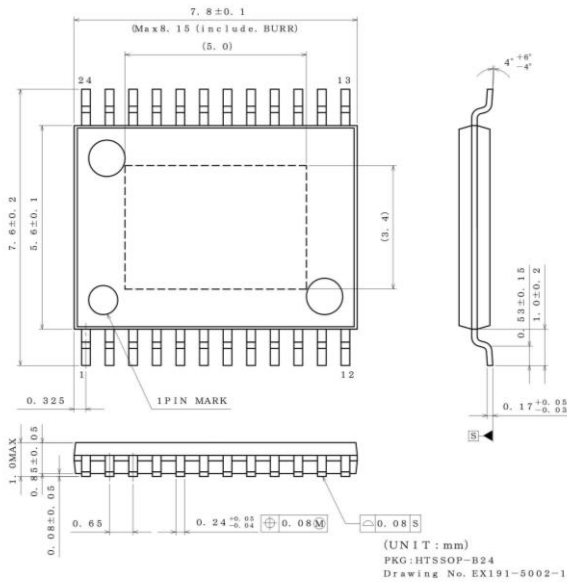
If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

● Ordering Information

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | D | 8 | 2 | 6 | 6 | E | F | V | - | M | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

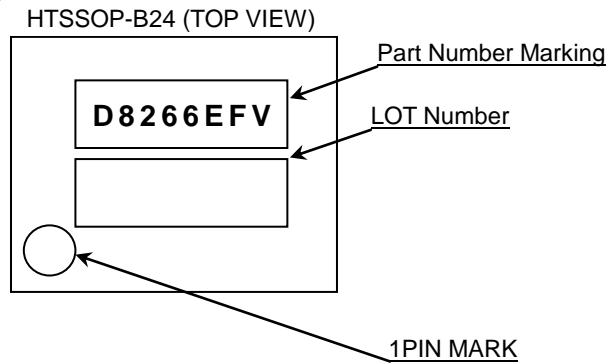
| | | |
|-------------|----------------------------|--|
| Part Number | Package EFV: HTSSOP-B24 | Packaging M: high reliability E2: Embossed carrier tape (HTSSOP-B24) |
|-------------|----------------------------|--|

● Physical Dimension Tape and Reel Information



| <Tape and Reel information> | |
|-----------------------------|---|
| Tape | Embossed carrier tape (with dry pack) |
| Quantity | 2000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

● Marking Diagram (TOP VIEW)



●Revision History

| Date | Revision | Changes |
|-------------|----------|---|
| 30.May.2012 | 001 | New Release |
| 30.Aug.2012 | 005 | <p>Page addition P6-7 Electrical Characteristic for -40°C to 85°C P8-11 Typical Performance Curves P15 Gain calculation</p> <p>Revise P1 Typical Application Circuit P2 Pin Description & Block Diagram P4 Term addition in Electrical Characteristic(s) P5 Term addition in Electrical Characteristic(s) P12 Additional table for Driver logic (OPU Protected operation) P12 VREG explanation P13-14 Constant symbol P16 Block Diagram P16 Table addition for Channel example and External constant P17 Power dissipation at 85°C P22 Revision History</p> |
| 8.Nov.2012 | 006 | <p>Revise Input resistant (IN1,IN2-1,IN2-2)21kΩ -> 20.75 kΩ Input resistant (IN3,IN4)47kΩ -> 50kΩ</p> <p>P4,P6 Symbol of BIAS Input Current change VBD ->IBD P14 Equation ③ unit change μA -> μF P15 Revise equation VO of Figure 20. And Figure 21. P16 External part list change P20 VCC-> electric power supply and add T.S.D explanation</p> <p>Change Symbol 'H' ->High 'L' ->Low u ->μ typ. ->Typ.</p> |
| 13.Jun.2013 | 007 | Revise P.21 Physical Dimension |
| 27.Aug.2013 | 008 | Revise P.12 Change the name OPU -> OCP P.14 Add the parenthesis and CPRTC in the calculation. |
| 24.Apr.2014 | 009 | Revise P.1 Add the sentence of AEC-Q100 Qualified at the features P.20 Delete the sentence of status of this document |
| 17.Aug.2016 | 010 | Revise P.3 Add DiffPowVCC at operating conditions P.11 Add Figure18, 19 P.17 Add Figure25, 26 Update of figure number Correction of other errors |

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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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