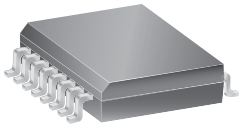
DMOS Full-Bridge Motor Driver

Features and Benefits

- Single supply operation
- Very small outline package
- Low $R_{DS(ON)}$ outputs
- Sleep function
- Internal UVLO
- Crossover current protection
- Thermal shutdown protection

Packages:



Package LB, 16-pin SOIC
with internally fused pins

Not to scale

Description

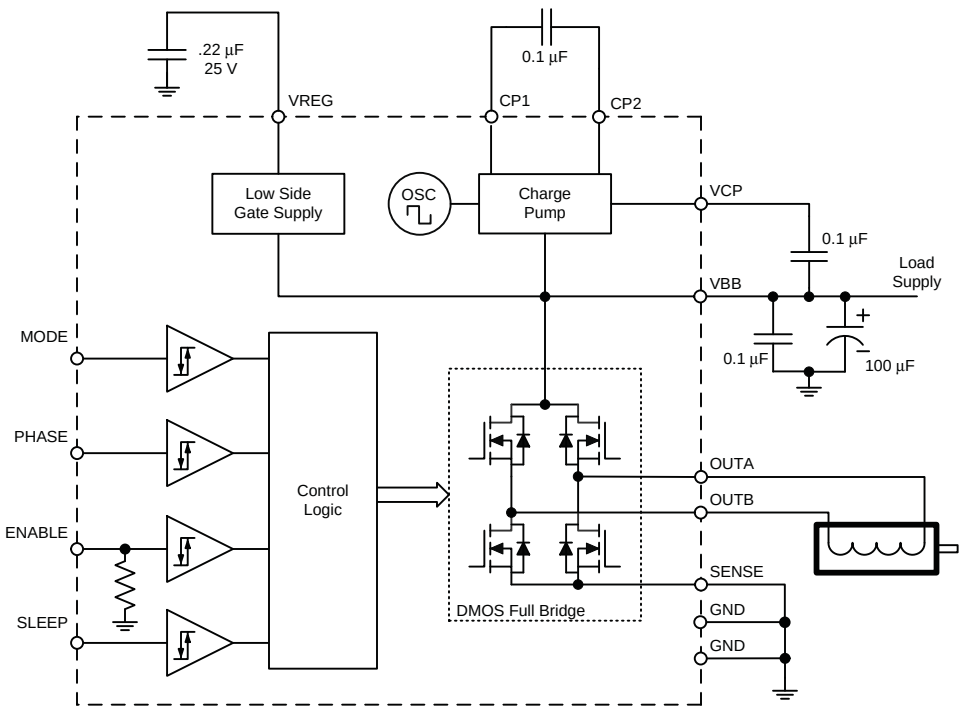
Designed for PWM (pulse width modulated) control of DC motors, the A3949 is capable of peak output currents to ±2.8 A and operating voltages to 36 V.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of V_{BB} and V_{CP}, and crossover current protection.

The A3949 is supplied in a power package, a 16-pin plastic SOIC with a copper batwing tab (part number suffix *LB*). The packages are lead (Pb) free, with 100% matte tin leadframes.

Functional Block Diagram



Selection Guide

Part Number	Package	Packing
A3949SLBTR-T	16-pin, SOIC	1000 per reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		36	V
		Peak < 2 µs	38	V
Logic Input Voltage	V_{IN}		–0.3 to 7	V
Sense Voltage	V_{SENSE}		0.5	V
Output Current, Repetitive	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, DO NOT exceed the specified I_{OUT} or T_J.	±2.8	A
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Package Thermal Characteristics*

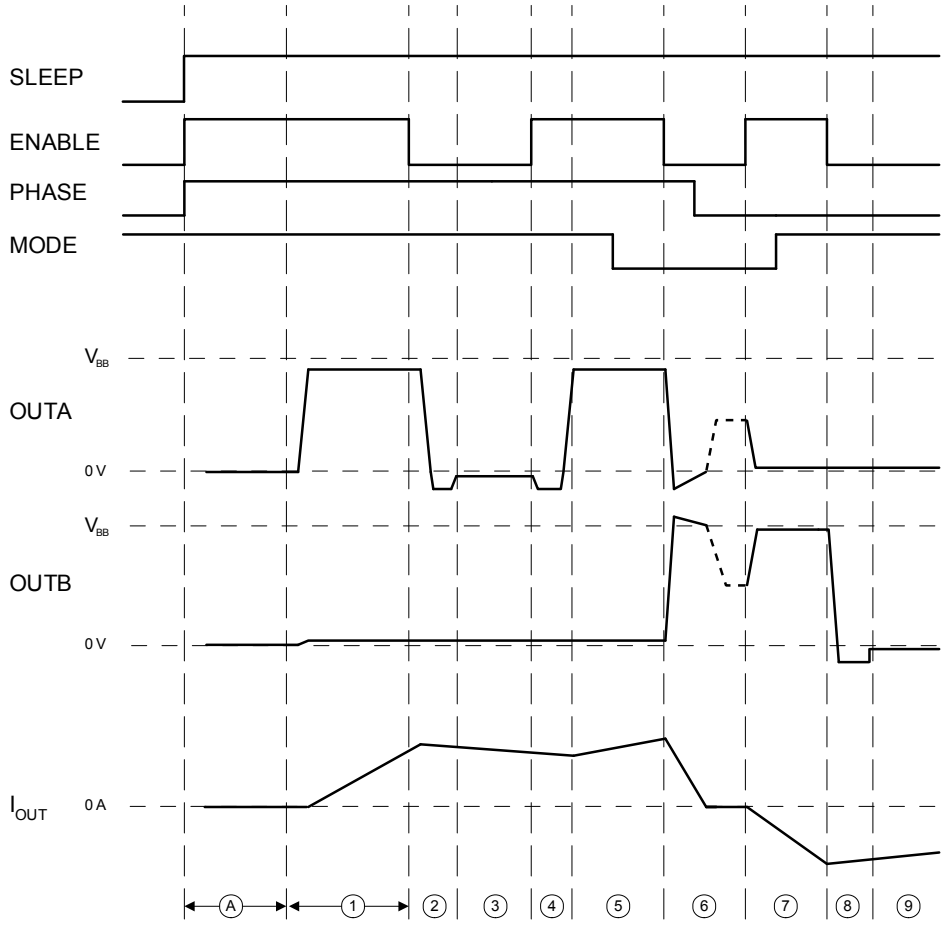
Characteristic	Symbol	Note	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Measured on 2-layer PCB with 2 in.^{2} 2-oz. copper each side	52	°C/W

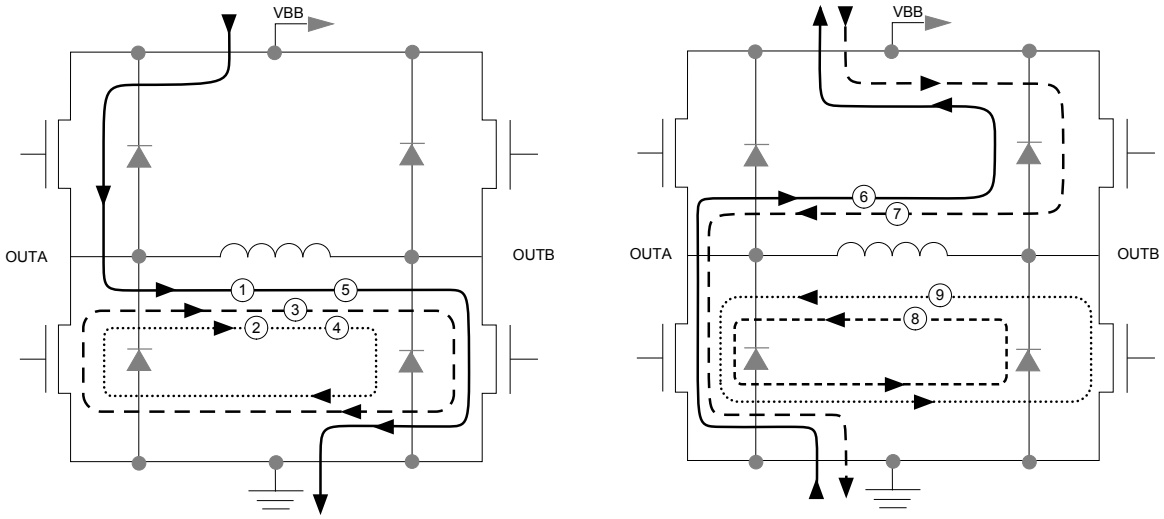
*Additional information is available on the Allegro website.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 8 V to 36 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output-On Resistance	R_{DSON}	Source driver, I_{OUT} = –2.8 A, T_J= 25°C	–	.4	.48	Ω
		Source driver, I_{OUT} = –2.8 A, T_J= 125°C	–	.68	–	Ω
		Sink driver, I_{OUT} = 2.8 A, T_J= 25°C	–	.3	.43	Ω
		Sink driver, I_{OUT} = –2.8 A, T_J= 125°C	–	.576	–	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = –2.8 A	–	1.1	1.3	V
		Sink diode, I_F = 2.8 A	–	1	1.3	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	6	8.5	mA
		Charge pump turned on; outputs disabled	–	3	4.5	mA
		Sleep mode	–	–	10	µA
Logic Input Voltage PHASE, ENABLE, MODE	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Voltage SLEEP	$V_{IN(1)}$		2.7	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current PHASE, MODE pins	$I_{IN(1)}$	V_{IN} = 2.0 V	–	< 1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	< –2.0	–20	µA
Logic Input Current ENABLE pin	$I_{IN(1)}$	V_{IN} = 2.0 V	–	40	100	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	16	40	µA
Logic Input Current SLEEP pin	$I_{IN(1)}$	V_{IN} = 2.7 V	–	27	50	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	< 1	10	µA
Propagation Delay Times	t_{pd}	From PWM change to source or sink turn on	–	600	–	ns
		From PWM change to source or sink turn off	–	100	–	ns
Crossover Delay	t_{COD}		–	500	–	ns
Protection Circuitry						
UVLO Enable Threshold		VBB rising	–	6	–	V
UVLO Hysteresis			–	250	–	mV
Thermal Shutdown Temp.	T_J		–	170	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C

PWM Control Timing Diagram





(A) Charge pump and VREG power-up delay (approximately 200 us)

Functional Description

VREG. This supply voltage is used to operate the sink-side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The VREG pin should be decoupled with a 0.22 µF capacitor to ground.

Charge Pump. The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1 uF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 uF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high side DMOS devices. The VCP voltage is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on VCP or VREG, the outputs of the device are disabled until the fault condition is removed. At power-up, the UVLO circuit disables the drivers.

Sleep Mode. Control input SLEEP is used to minimize power consumption when the A3949 is not in use. This disables much of the internal circuitry, including the low-side gate supply and the charge pump. A logic low on this pin puts the device into Sleep mode. A logic high allows normal operation. After coming out of Sleep mode, the user should wait 1 ms before applying PWM signals, to allow the charge pump to stabilize.

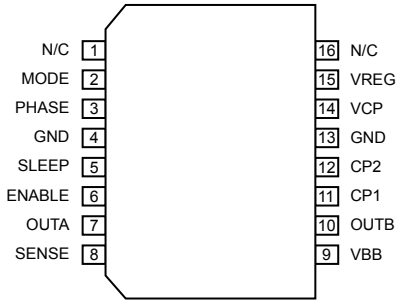
Braking. The braking function is implemented by driving the device in slow decay mode via the MODE pin, and applying an enable chop command. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF, as long as the enable chop mode is asserted on the ENABLE pin. The maximum current can be approximated by V_{BEMF} / R_L. Care should be taken to insure that the maximum ratings of the device are not exceeded in worse case braking situations of high speed and high inertial loads.

Control Logic Table

PHASE	ENABLE	MODE	SLEEP	OUTA	OUTB	Function
1	1	X	1	H	L	Forward
0	1	X	1	L	H	Reverse
X	0	1	1	L	L	Brake (slow decay)
1	0	0	1	L	H	Fast decay SR*
0	0	0	1	H	L	Fast decay SR*
X	X	X	0	Hi-Z	Hi-Z	Sleep mode

* To prevent reversal of current during fast decay SR (synchronous rectification), the outputs go to the high impedance state as the current approaches zero.

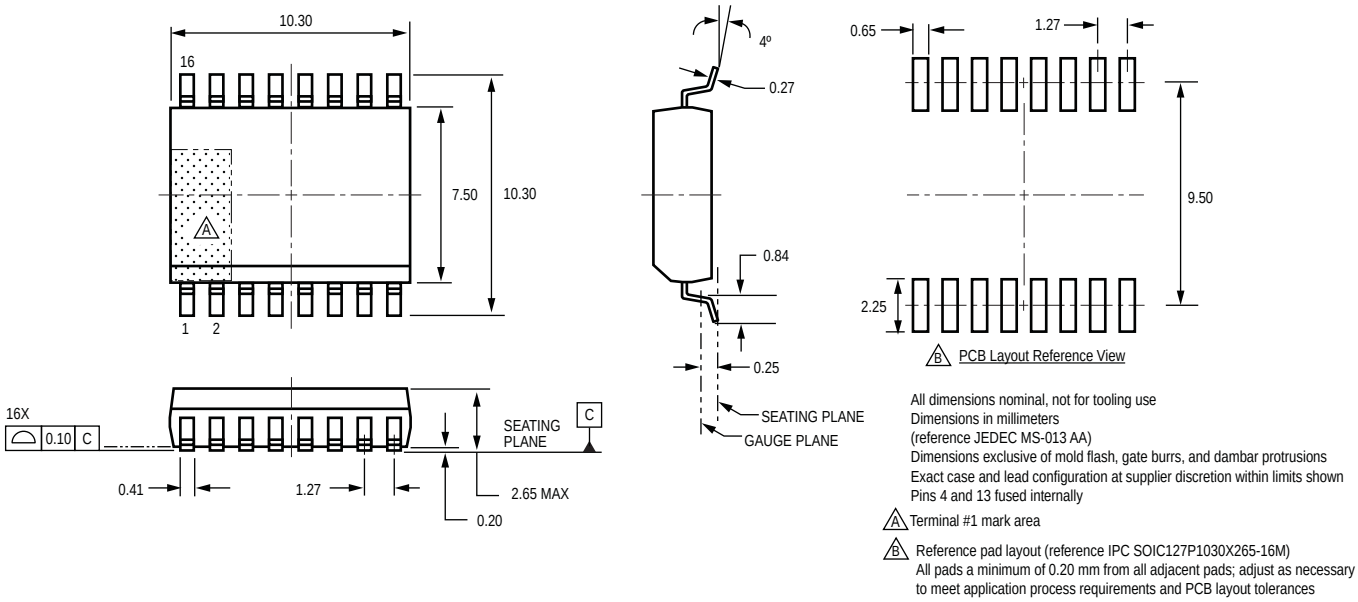
LB Package



Name	Description	Number
N/C	Not used	1
MODE	Logic input	2
PHASE	Logic input for direction control	3
GND	Ground	4*
SLEEP	Logic input	5
ENABLE	Logic input	6
OUTA	Output A for full bridge	7
SENSE	Power return	8
VBB	Load supply voltage	9
OUTB	Output B for full bridge	10
CP1	Charge pump capacitor	11
CP2	Charge pump capacitor	12
GND	Ground	13*
VCP	Reservoir capacitor	14
VREG	Low side gate supply decoupler	15
N/C	Not used	16

*These pins are internally connected.

LB 16-Pin SOICW



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