

Low Harmonic Distortion, 24-Channel SPST High Voltage Analog Switch

Features

- 24 Channels of high voltage analog switch
- 3.3 or 5.0V CMOS input logic level
- 24 Channel SPST configuration
- 20 MHz data shift clock frequency
- HVCMOS technology for high performance
- Very low quiescent power dissipation-10 μ A
- Low parasitic capacitance
- DC to 50 MHz analog signal frequency
- -60dB typical OFF-isolation at 5.0 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages
- Integrated bleed resistors on outputs (HV2762 only)

Applications

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Inkjet printer heads
- Optical MEMS modules

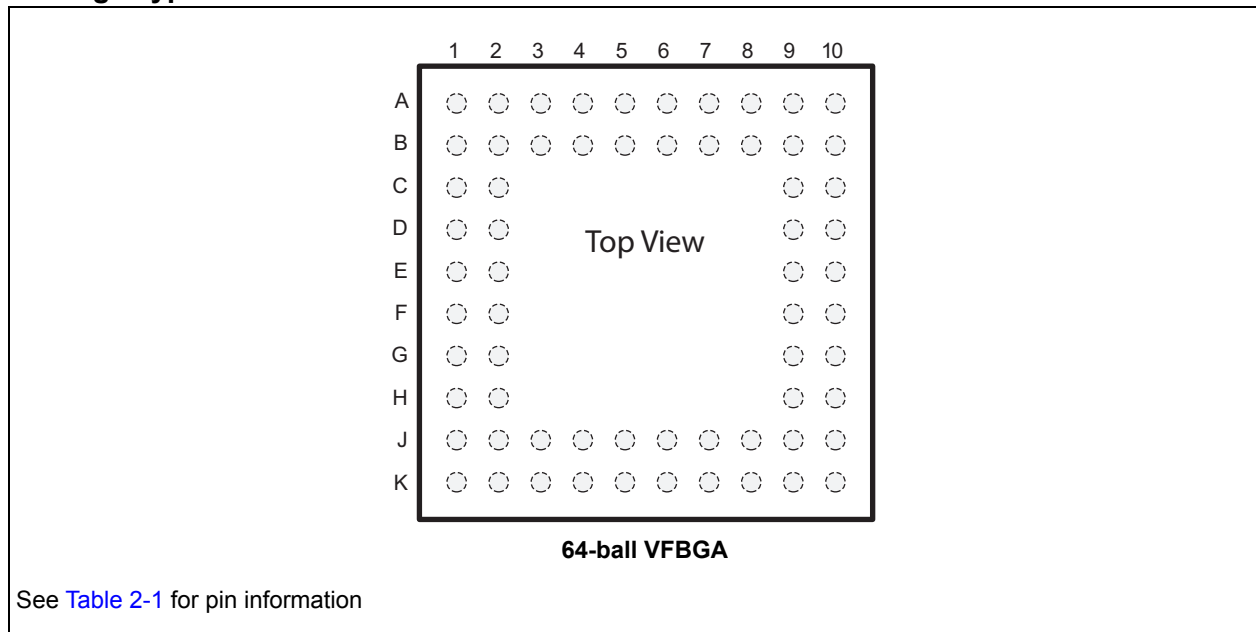
Description

HV2662/HV2762 are low-charge injection, 24-channel, high-voltage analog switch integrated circuits (ICs). These ICs excel in applications requiring high-voltage switching controlled by low-voltage control signals such as medical ultrasound imaging, piezoelectric transducer driver, and printers. HV2762 provides integrated bleed resistors that eliminate voltage build-up on capacitive loads such as piezoelectric transducers. HV2662 does not have integrated bleed resistors.

HV2662/HV2762 shift input data into a 24-bit shift register that can then be retained in a 24-bit latch. To reduce any possible clock feed through noise, the latch-enable bar should be left high until all bits are clocked in during the rising edge of the clock. Using High Voltage CMOS technology, these ICs combine high-voltage, bilateral DMOS switches and low-power CMOS logic to provide efficient control of high voltage analog signals.

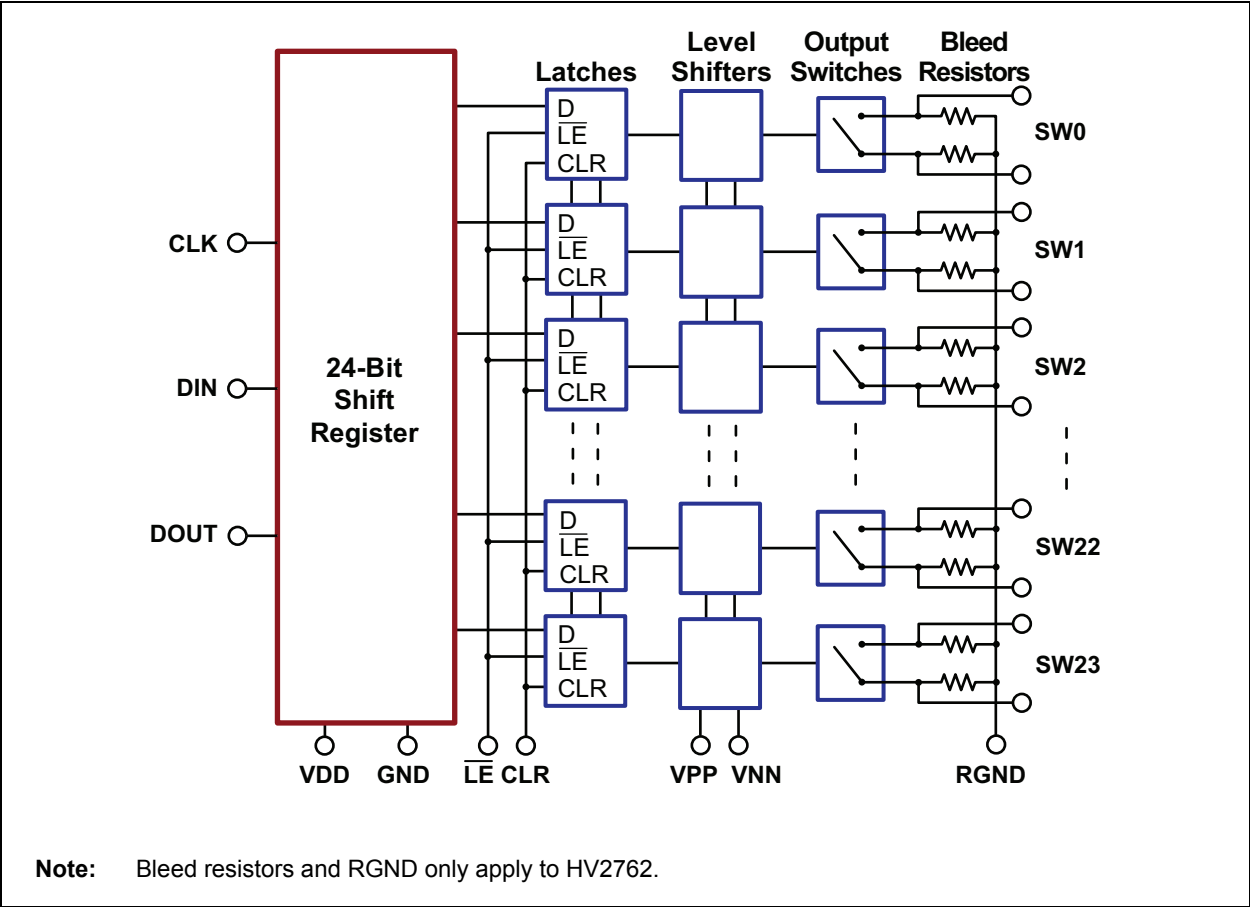
The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Package Types



HV2662 / HV2762

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

| | |
|---|--------------------------|
| V_{DD} logic supply | -0.50 to +6.5V |
| $V_{PP} - V_{NN}$ differential supply | 220V |
| V_{PP} positive supply | -0.5 to $V_{NN} + 200V$ |
| V_{NN} negative supply | +0.5 to -200V |
| Logic input voltage | -0.5V to $V_{DD} + 0.3V$ |
| Analog signal range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 2.0A |
| Storage temperature | -65°C to +150°C |
| Power dissipation | 1.0W |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Notes 1– 3)

| Symbol | Parameter | Value |
|-----------|------------------------------------|---|
| V_{DD} | Logic power supply voltage | 3.0V to 5.5V (Note 2) |
| V_{PP} | Positive high voltage supply | +40V to $V_{NN} + 200V$ (Note 2) |
| V_{NN} | Negative high voltage supply | -40V to -160V (Note 2) |
| V_{IH} | High level input voltage | $0.9V_{DD}$ to V_{DD} |
| V_{IL} | Low level input voltage | 0V to $0.1 V_{DD}$ |
| V_{SIG} | Analog signal voltage peak-to-peak | $V_{NN} + 10V$ to $V_{PP} - 10V$ (Note 3) |
| T_A | Operating free air temperature | 0°C to 70°C |

- Note 1:** Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2: Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.
3: V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise specified.
 See test circuits [Figure 3-2](#)

| Parameter | Symbol | 0°C | | 25°C | | | 70°C | | Units | Conditions |
|--|------------------|-----|-----|------|-----|-----|------|-----|------------|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| Small signal switch ON-resistance | R_{ONS} | - | - | - | 26 | - | - | - | Ω | $I_{SIG} = 5.0mA$, $V_{PP} = +40V$, $V_{NN} = -160V$ |
| | | - | - | - | 22 | - | - | - | | |
| | | - | - | - | 22 | - | - | - | | $I_{SIG} = 5.0mA$, $V_{PP} = +100V$, $V_{NN} = -100V$ |
| | | - | - | - | 18 | - | - | - | | |
| | | - | - | - | 20 | - | - | - | | $I_{SIG} = 5.0mA$, $V_{PP} = +160V$, $V_{NN} = -40V$ |
| | | - | - | - | 16 | - | - | - | | |
| Small signal switch ON-resistance matching | ΔR_{ONS} | - | 20 | - | 5.0 | 20 | - | 20 | % | $I_{SIG} = 5.0mA$, $V_{PP} = +100V$, $V_{NN} = -100V$ |
| Large signal switch ON-resistance | R_{ONL} | - | - | - | 30 | - | - | - | Ω | $V_{SIG} = V_{PP} - 10V$, $I_{SIG} = 1A$ (Note 1) |
| Output-switch shunt resistance (HV2762 only) | R_{INT} | - | - | 20 | 35 | 50 | - | - | K Ω | Output switch to R_{GND} , $I_{RINT} = 0.5 mA$ |

HV2662 / HV2762

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical Specifications: Over recommended operating conditions unless otherwise specified. See test circuits Figure 3-2 | | | | | | | | | | | |
|--|-------------------|------|-----|------|------|-----|------|-----|-------|--|---|
| Parameter | Symbol | 0°C | | 25°C | | | 70°C | | Units | Conditions | |
| | | Min | Max | Min | Typ | Max | Min | Max | | | |
| Switch OFF-leakage per switch | I _{SOL} | - | 5.0 | - | 1.0 | 10 | - | 15 | μA | V _{SIG} = V _{PP} -10V, V _{NN} +10V | |
| DC offset switch OFF | V _{OS} | - | 300 | - | 100 | 300 | - | 300 | mV | No load for HV2762. R _{LOAD} = 100 kΩ for HV2662 | |
| DC offset switch ON | | - | 500 | - | 100 | 500 | - | 500 | | | |
| Quiescent V _{PP} supply current | I _{PPQ} | - | - | - | 10 | 50 | - | - | μA | All switches OFF | |
| Quiescent V _{NN} supply current | I _{NNQ} | - | - | - | -10 | -50 | - | - | | | |
| Quiescent V _{PP} supply current | I _{PPQ} | - | - | - | 10 | 50 | - | - | μA | All switches ON, I _{SW} = 5.0mA | |
| Quiescent V _{NN} supply current | I _{NNQ} | - | - | - | -10 | -50 | - | - | | | |
| Switch output peak current | I _{SW} | - | - | - | 2.0 | 1.3 | - | - | A | V _{SIG} duty cycle < 0.1% (Note 1) | |
| Output switching frequency | f _{SW} | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% (Note 1) | |
| Average V _{PP} supply current | I _{PP} | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | V _{PP} = +40V, V _{NN} = -160V | All output switches are turning ON and OFF at 50 kHz with no load |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +100V, V _{NN} = -100V | |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +160V, V _{NN} = -40V | |
| Average V _{NN} supply current | I _{NN} | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | V _{PP} = +40V, V _{NN} = -160V | All output switches are turning ON and OFF at 50 kHz with no load |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +100V, V _{NN} = -100V | |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +160V, V _{NN} = -40V | |
| Average V _{DD} supply current | I _{DD} | - | 8.0 | - | - | 8.0 | - | 8.0 | mA | f _{CLK} = 5.0MHz, V _{DD} = 5.0V | |
| Quiescent V _{DD} supply current | I _{DDQ} | - | 10 | - | - | 10 | - | 10 | μA | All logic inputs are static | |
| Data out source current | I _{SOR} | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | V _{OUT} = V _{DD} -0.7V | |
| Data out sink current | I _{SINK} | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | V _{OUT} = 0.7V | |
| Logic input capacitance | C _{IN} | - | 10 | - | - | 10 | - | 10 | pF | (Note 2) | |

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise specified.
See test circuits [Figure 3-2](#)

| Parameter | Symbol | 0°C | | 25°C | | | 70°C | | Units | Conditions |
|---------------------------------------|-------------------|-----|-----|------|-----|-----|------|-----|---------|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| Set up time before LE rises | t_{SD} | 25 | - | 25 | - | - | 25 | - | ns | (Note 1) |
| Time width of LE | t_{WLE} | 56 | - | 56 | - | - | 56 | - | ns | $V_{DD} = 3.0V$ (Note 1) |
| | | 12 | - | 12 | - | - | 12 | - | | $V_{DD} = 5.0V$ (Note 1) |
| Clock delay time to data out | t_{DO} | 9.0 | 40 | 9.0 | - | 40 | 9.0 | 40 | ns | $V_{DD} = 3.0V$ (Note 1) |
| | | 8.0 | 30 | 8.0 | - | 30 | 8.0 | 30 | | $V_{DD} = 5.0V$ (Note 1) |
| Time width of CLR | t_{WCLR} | 55 | - | 55 | - | - | 55 | - | ns | (Note 1) |
| Set up time data to clock | t_{SU} | 21 | - | 21 | - | - | 21 | - | ns | $V_{DD} = 3.0V$ (Note 1) |
| | | 7.0 | - | 7.0 | - | - | 7.0 | - | | $V_{DD} = 5.0V$ (Note 1) |
| Hold time data from clock | t_H | 5.0 | - | 5.0 | - | - | 5.0 | - | ns | $V_{DD} = 3.0V$ (Note 1) |
| | | 5.0 | - | 5.0 | - | - | 5.0 | - | | $V_{DD} = 5.0V$ (Note 1) |
| Clock frequency | f_{CLK} | - | 8 | - | - | 8 | - | 8 | MHz | $V_{DD} = 3.0V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{DD} = 5.0V$ (Note 1) |
| Clock rise and fall times | t_R, t_F | - | 50 | - | - | 50 | - | 50 | ns | (Note 1) |
| Turn ON time | t_{ON} | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V$, $R_{LOAD} = 10k\Omega$ |
| Turn OFF time | t_{OFF} | - | 5.0 | - | - | 5.0 | - | 5.0 | | |
| Maximum V_{SIG} slew rate | dv/dt | - | 20 | - | - | 20 | - | 20 | V/ns | $V_{PP} = +40V, V_{NN} = -160V$ (Note 1) |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +100V, V_{NN} = -100V$ (Note 1) |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +160V, V_{NN} = -40V$ (Note 1) |
| OFF isolation | K_O | -30 | - | -30 | -33 | - | -30 | - | dB | $f = 5.0$ MHz, 1.0 k Ω /15 pF load (Note 1) |
| | | -58 | - | -58 | -60 | - | -58 | - | | $f = 5.0$ MHz, 50 Ω load (Note 1) |
| Switch crosstalk | K_{CR} | -60 | - | -60 | -70 | - | -60 | - | dB | $f = 5.0$ MHz, 50 Ω load (Note 1) |
| Output switch isolation diode current | I_{ID} | - | 300 | - | - | 300 | - | 300 | mA | 300 ns pulse width, 2.0% duty cycle (Note 1) |
| OFF capacitance SW to GND | $C_{SG(OFF)}$ | - | 14 | - | 9.0 | 14 | - | 14 | pF | $V_{SIG} = 0V, f = 1.0$ MHz (Note 1) |
| ON capacitance SW to GND | $C_{SG(ON)}$ | - | 17 | - | 12 | 17 | - | 17 | | |
| Output voltage spike (per switch) | +V _{SPK} | - | - | - | - | 150 | - | - | mV | $V_{PP} = +40V, V_{NN} = -160V$ $R_{LOAD} = 50\Omega$ (Note 1) |
| | -V _{SPK} | - | - | - | - | 150 | - | - | | |
| | +V _{SPK} | - | - | - | - | 150 | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ $R_{LOAD} = 50\Omega$ (Note 1) |
| | -V _{SPK} | - | - | - | - | 150 | - | - | | |
| | +V _{SPK} | - | - | - | - | 150 | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ $R_{LOAD} = 50\Omega$ (Note 1) |
| | -V _{SPK} | - | - | - | - | 150 | - | - | | |
| Charge injection (per switch) | QC | - | - | - | 820 | - | - | - | pC | $V_{PP} = +40V, V_{NN} = -160V$ (Note 1) |
| | | - | - | - | 600 | - | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ (Note 1) |
| | | - | - | - | 350 | - | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ (Note 1) |

Note 1: Specification is obtained by characterization and is not 100% tested.

HV2662 / HV2762

TEMPERATURE SPECIFICATIONS

| Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$ | | | | | | |
|---|---------------|-----|-----|-----|--------------------|------------|
| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
| Temperature Ranges | | | | | | |
| Storage Temperature | T_A | -65 | – | 150 | $^\circ\text{C}$ | |
| Package Thermal Resistances | | | | | | |
| Thermal Resistance, 64-Ball VFBGA | θ_{ja} | – | 36 | – | $^\circ\text{C/W}$ | |

2.0 PIN DESCRIPTION

The locations of the balls are listed in [Package Types](#).

TABLE 2-1: BALL DESCRIPTION 64-BALL VFBGA

| Pin # | HV2662 | HV2762 | Description |
|-------|------------------------|------------------------|---------------------------------------|
| A1 | SW22B | SW22B | Analog switch 22 terminal B |
| A2 | V _{NN} | V _{NN} | Negative supply voltage |
| A3 | SW21B | SW21B | Analog switch 21 terminal B |
| A4 | SW20B | SW20B | Analog switch 20 terminal B |
| A5 | SW19B | SW19B | Analog switch 19 terminal B |
| A6 | SW18B | SW18B | Analog switch 18 terminal B |
| A7 | SW17B | SW17B | Analog switch 17 terminal B |
| A8 | SW16B | SW16B | Analog switch 16 terminal B |
| A9 | SW15B | SW15B | Analog switch 15 terminal B |
| A10 | SW15A | SW15A | Analog switch 15 terminal A |
| B1 | SW23B | SW23B | Analog switch 23 terminal B |
| B2 | SW23A | SW23A | Analog switch 23 terminal A |
| B3 | SW22A | SW22A | Analog switch 22 terminal A |
| B4 | SW21A | SW21A | Analog switch 21 terminal A |
| B5 | SW20A | SW20A | Analog switch 20 terminal A |
| B6 | SW19A | SW19A | Analog switch 19 terminal A |
| B7 | SW18A | SW18A | Analog switch 18 terminal A |
| B8 | SW17A | SW17A | Analog switch 17 terminal A |
| B9 | SW16A | SW16A | Analog switch 16 terminal A |
| B10 | SW14B | SW14B | Analog switch 14 terminal B |
| C1 | NC | NC | No connect |
| C2 | V _{PP} | V _{PP} | Positive supply voltage |
| C9 | SW14A | SW14A | Analog switch 14 terminal A |
| C10 | SW13B | SW13B | Analog switch 13 terminal B |
| D1 | CLR | CLR | Latch clear logic input |
| D2 | NC | RGND | No connect/ Ground for bleed resistor |
| D9 | V _{NN} | V _{NN} | Negative supply voltage |
| D10 | SW13A | SW13A | Analog switch 13 terminal A |
| E1 | $\overline{\text{LE}}$ | $\overline{\text{LE}}$ | Latch-enable logic input, low active |
| E2 | CLK | CLK | Clock logic input for shift register |
| E9 | SW12B | SW12B | Analog switch 12 terminal B |
| E10 | SW12A | SW12A | Analog switch 12 terminal A |
| F1 | V _{DD} | V _{DD} | Logic supply voltage |
| F2 | GND | GND | Ground |
| F9 | SW11B | SW11B | Analog switch 11 terminal B |
| F10 | SW11A | SW11A | Analog switch 11 terminal A |
| G1 | D _{IN} | D _{IN} | Data-in logic input |
| G2 | D _{OUT} | D _{OUT} | Data-out logic output |
| G9 | SW10B | SW10B | Analog switch 10 terminal B |
| G10 | V _{NN} | V _{NN} | Negative supply voltage |
| H1 | NC | RGND | No connect/ Ground for bleed resistor |
| H2 | V _{PP} | V _{PP} | Positive supply voltage |

HV2662 / HV2762

TABLE 2-1: BALL DESCRIPTION 64-BALL VFBGA (CONTINUED)

| Pin # | HV2662 | HV2762 | Description |
|-------|-----------------|-----------------|-----------------------------|
| H9 | SW10A | SW10A | Analog switch 10 terminal A |
| H10 | SW9B | SW9B | Analog switch 9 terminal B |
| J1 | SW0A | SW0A | Analog switch 0 terminal A |
| J2 | SW0B | SW0B | Analog switch 0 terminal B |
| J3 | SW1B | SW1B | Analog switch 1 terminal B |
| J4 | SW2B | SW2B | Analog switch 2 terminal B |
| J5 | SW3B | SW3B | Analog switch 3 terminal B |
| J6 | SW4B | SW4B | Analog switch 4 terminal B |
| J7 | SW5B | SW5B | Analog switch 5 terminal B |
| J8 | SW6B | SW6B | Analog switch 6 terminal B |
| J9 | SW7B | SW7B | Analog switch 7 terminal B |
| J10 | SW9A | SW9A | Analog switch 9 terminal A |
| K1 | SW1A | SW1A | Analog switch 1 terminal A |
| K2 | V _{NN} | V _{NN} | Negative supply voltage |
| K3 | SW2A | SW2A | Analog switch 2 terminal A |
| K4 | SW3A | SW3A | Analog switch 3 terminal A |
| K5 | SW4A | SW4A | Analog switch 4 terminal A |
| K6 | SW5A | SW5A | Analog switch 5 terminal A |
| K7 | SW6A | SW6A | Analog switch 6 terminal A |
| K8 | SW7A | SW7A | Analog switch 7 terminal A |
| K9 | SW8A | SW8A | Analog switch 8 terminal A |
| K10 | SW8B | SW8B | Analog switch 8 terminal B |

3.0 FUNCTIONAL DESCRIPTION

FIGURE 3-1: LOGIC TIMING WAVEFORMS

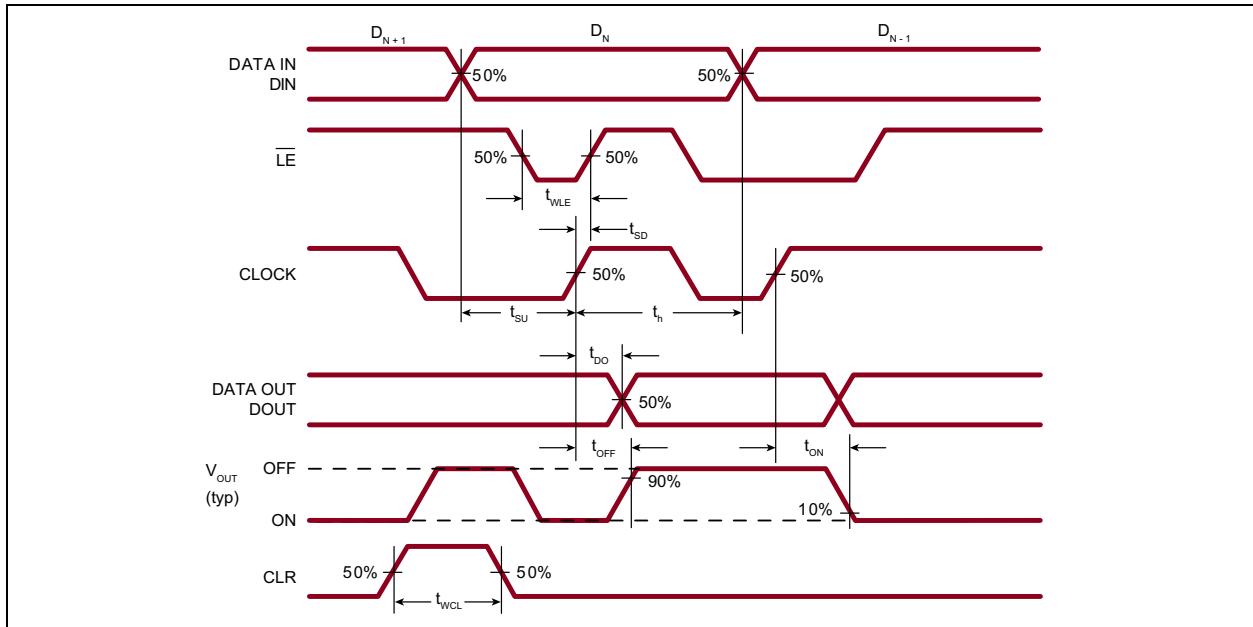


TABLE 3-1: TRUTH TABLE

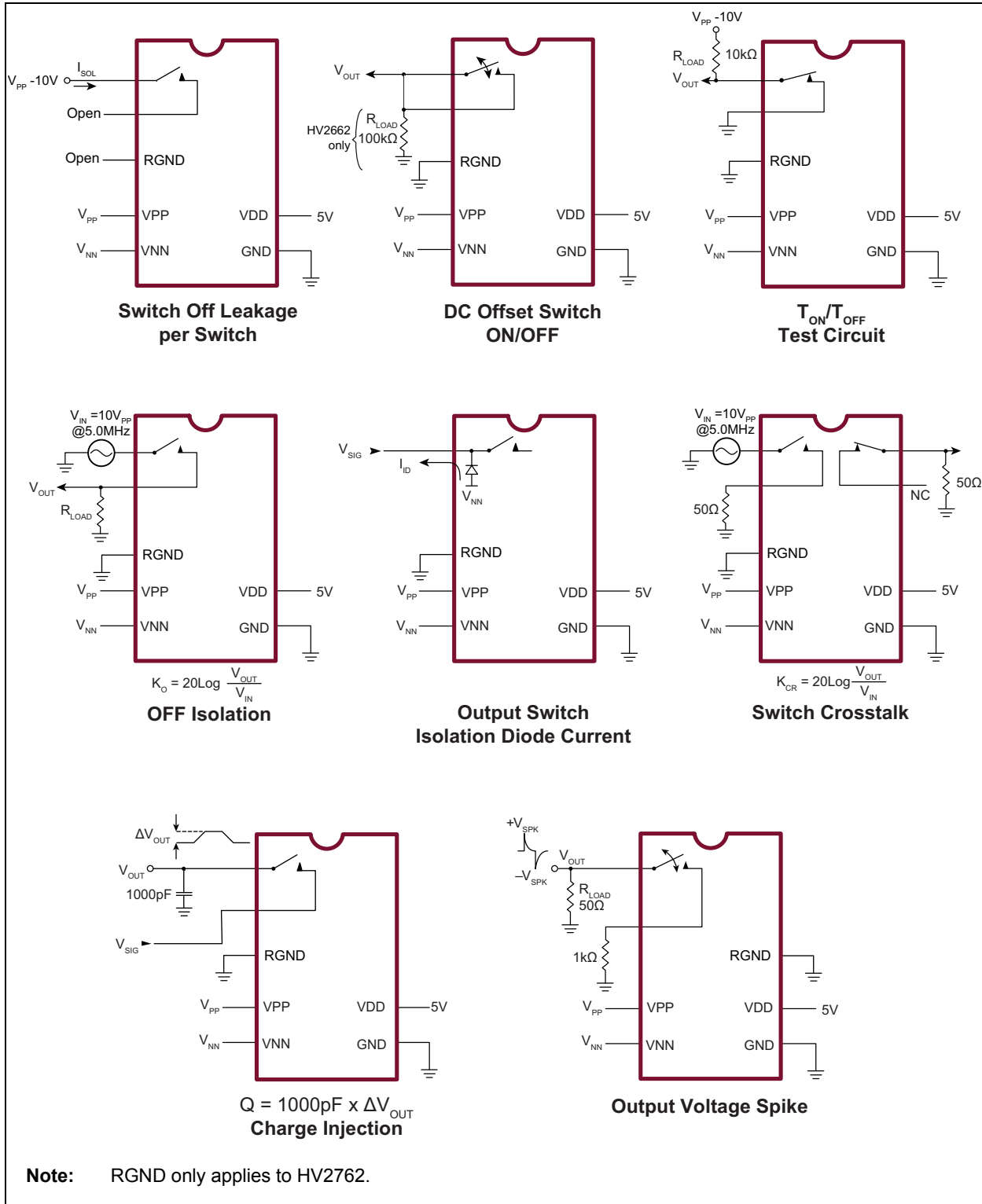
| D0 ¹ | D1 | ... | D15 | D16 | ... | D23 ² | \overline{LE} ³ | CLR ⁴ | SW0 ^{5,6} | SW1 | ... | SW15 | SW16 | ... | SW23 |
|-----------------|----|-----|-----|-----|-----|------------------|------------------------------|------------------|---------------------|-----|-----|------|------|-----|------|
| L | - | | - | - | | - | L | L | OFF | - | | - | - | | - |
| H | - | | - | - | | - | L | L | ON | - | | - | - | | - |
| - | L | | - | - | | - | L | L | - | OFF | | - | - | | - |
| - | H | | - | - | | - | L | L | - | ON | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | L | - | | - | L | L | - | - | | OFF | - | | - |
| - | - | | H | - | | - | L | L | - | - | | ON | - | | - |
| - | - | ... | - | L | ... | - | L | L | - | - | ... | - | OFF | ... | - |
| - | - | | - | H | | - | L | L | - | - | | - | ON | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | L | L | L | - | - | | - | - | | OFF |
| - | - | | - | - | | H | L | L | - | - | | - | - | | ON |
| X | X | X | X | X | X | X | H | L | HOLD PREVIOUS STATE | | | | | | |
| X | X | X | X | X | X | X | X | H | ALL SWITCHES OFF | | | | | | |

- Note 1:** Serial data is clocked in on the L to H transition of the CLK
- 2:** DOUT is high when data in the register 23 is high.
- 3:** Shift registers clocking has no effect on the switch states if LE is high.
- 4:** The CLR clear input overrides all other inputs.
- 5:** The 24 switches operate independently.
- 6:** All 24 switches go to a state retaining their latched condition at the rising edge of \overline{LE} . When \overline{LE} is low, the shift registers data flow through the latch.

HV2662 / HV2762

3.1 Application Information

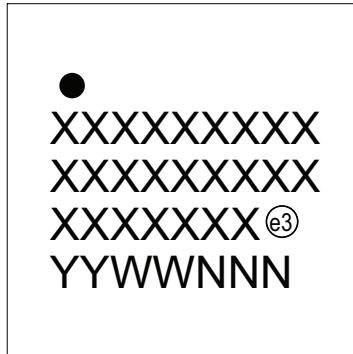
FIGURE 3-2: TEST CIRCUITS



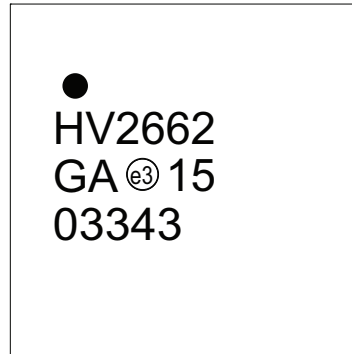
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

64-Ball VFBGA



Example



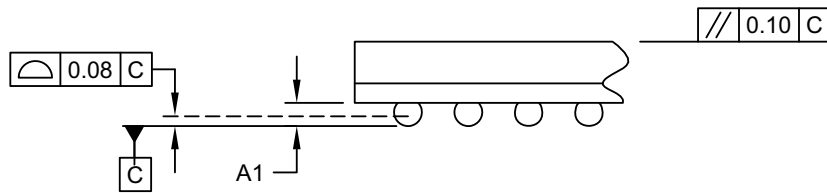
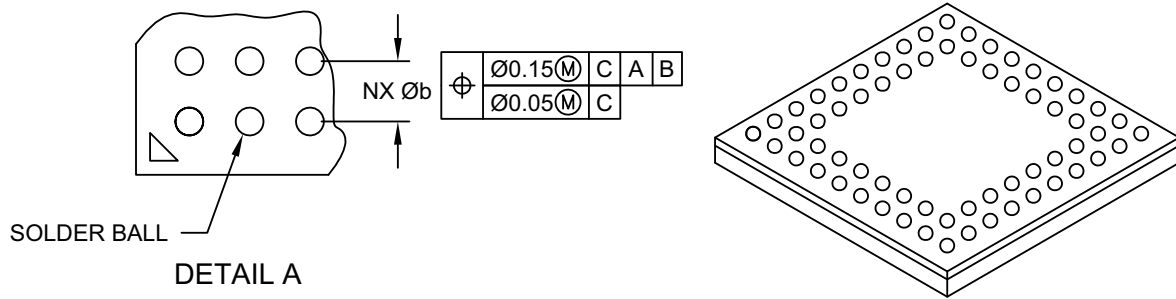
| | | |
|----------------|--------|--|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

HV2662 / HV2762

64-Ball Very Thin Fine Pitch Ball Grid Array (GA) - 7x7x1.0 mm Body [VFBGA] Supertex Legacy

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A

| | | Units | MILLIMETERS | | |
|----------------------|----|-------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | | |
| Pitch | e | | 0.65 BSC | | |
| Overall Height | A | - | - | - | 1.00 |
| Standoff | A1 | 0.16 | - | - | 0.25 |
| Molded Cap Thickness | A3 | | 0.45 REF | | |
| Overall Width | E | | 7.00 BSC | | |
| Overall Ball Pitch | E1 | | 5.85 BSC | | |
| Overall Length | D | | 7.00 BSC | | |
| Overall Ball Pitch | D1 | | 5.85 BSC | | |
| Ball Diameter | Øb | 0.25 | 0.30 | 0.35 | |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-370-GA Rev A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (May 2016)

- Converted Supertex Docs #'s DSFP-2662 and DSFP-HV2762 to Microchip DS20005372A.
- Merged HV2662 and HV2762 into one document.
- Updated “**Product Identification System**”.
Removed parts with a package code of “LA”;
Added package “GA”.
- EOL of 64-Ball LFGA package (LB).per PCN JAON-20WQKC840.
- Added information for 64-Ball VFBGA (GA) throughout.
- Minor text changes throughout.

HV2662 / HV2762

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>XX</u> | - | <u>X</u> | - | <u>X</u> |
|--|---|---|---------------|---|---------------|
| Device | Package Options | | Environmental | | Media Type |
| Device: Package: Environmental Media Type: | HV2662 = 24-Channel, HV Analog Switch HV2762 = 24-Channel, HV Analog Switch with Bleed Resistors GA = 64-ball VFBGA G = Lead (Pb)-free/RoHS-compliant package (blank) = 120/Tray for GA package | | | | |
| Examples: a) HV2662GA-G: 64-ball VFBGA package, 120/Tray b) HV2762GA-G: 64-ball VFBGA package, 120/Tray | | | | | |

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