

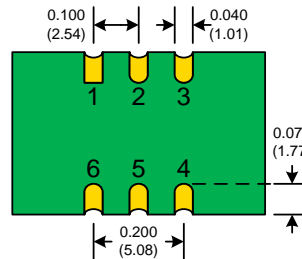
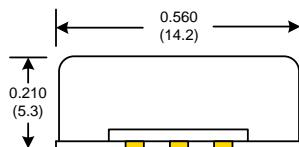
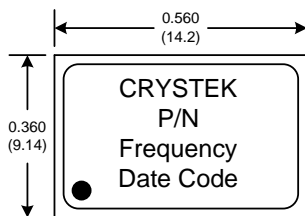
# Differential LVPECL Voltage Controlled Crystal Oscillator

## CVPD-920 Model 9x14 mm SMD, 3.3V, LVPECL

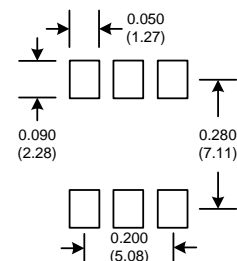
<b>Frequency Range:</b>	50 MHz to 125 MHz
<b>Frequency Pulling:</b>	±20ppm APR Min
<b>Temperature Range:</b>	0°C to 70°C
	(Option X)
	-40°C to 85°C
<b>Storage:</b>	-45°C to 90°C
<b>Input Voltage:</b>	3.3V ±0.3V
<b>Control Voltage:</b>	1.65V ±1.65V
<b>Input Current:</b>	88mA Max
<b>Output:</b>	Differential LVPECL
	Symmetry: 45/55% Max @ 50% Vcc
	Rise/Fall Time: 1ns Max @ 20% to 80% Vcc
	Linearity: ±10% Max
	Logic: Terminated to Vcc-2V into 50 ohms
	"0" = Vcc-1.85V Min, Vcc-1.62V Max
	"1" = Vcc-1.02V Min, Vcc-0.81V Max
	200ns
	Disable Time: 1ms Typical, 2ms Max
	Start-up Time: 1ms Typical, 2ms Max
<b>Phase Jitter:</b>	12kHz to 80MHz 0.5psec Typical, 1psec RMS Max
<b>Phase Noise:</b>	10Hz -65 dBc/Hz Typical
	100Hz -98 dBc/Hz Typical
	1kHz -125 dBc/Hz Typical
	10kHz -140 dBc/Hz Typical
	100kHz -145 dBc/Hz Typical
<b>Aging:</b>	<3ppm 1 <sup>st</sup> year, <1ppm every year thereafter



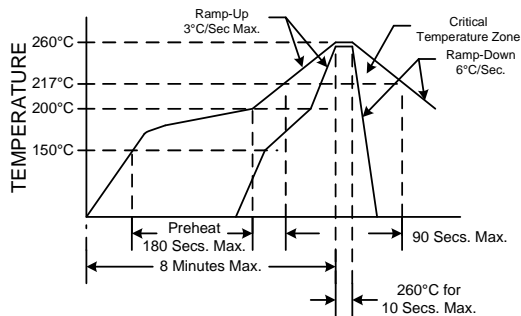
Designed to meet today's requirements for 3.3V Differential LVPECL applications. The CVPD-920 is produced using our cost saving FR5 PCB and UM-1 overtone crystal technology. This design offers considerable cost savings over other HFF VCXO products when broad frequency pulling is not required. Also available in 14 pin dip fully hermetic package.



### SUGGESTED PAD LAYOUT



### RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

PIN	Function
1	Control Volt
2	E/D
3	GND
4	OUT
5	COU
6	Vcc

### Crystek Part Number Guide

#### CVPD-920 X - 100.000

#1	#2	#3	#4
#1 Crystek 9x14 SMD PECL VCXO			
#2 Model 920			
#3 Temp. Range: Blank = 0/70°C, X = -40/85°C			
#4 Frequency in MHz: 3 or 6 decimal places			

Example:  
CVPD-920X-100.000 = 3.3V, 45/55, -40/85°C, 100.000 MHz

### Enable/Disable Function

Pin 2	Output Pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State: Pin 4 will assume a fixed level of logic "0" Pin 5 will assume a fixed level of logic "1"	

Specifications subject to change without notice.

TD-030701 Rev. G