FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

# 74AC257 • 74ACT257
# Quad 2-Input Multiplexer with 3-STATE Outputs

## General Description

The AC/ACT257 is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

## Features

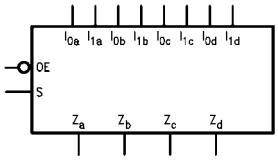
- $I_{CC}$ and $I_{OZ}$ reduced by 50%
- Multiplexer expansion by tying outputs together
- Noninverting 3-STATE outputs
- Outputs source/sink 24 mA
- ACT257 has TTL-compatible inputs

## Ordering Code:

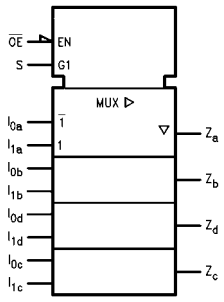
| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC257SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74AC257SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC257MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC257PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT257SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74ACT257SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT257MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT257PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

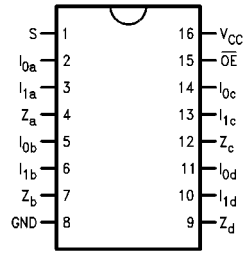
## Logic Symbols




**IEEE/IEC**




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| S | Common Data Select Input |
| $\overline{OE}$ | 3-STATE Output Enable Input |
| $I_{0a}$–$I_{0d}$ | Data Inputs from Source 0 |
| $I_{1a}$–$I_{1d}$ | Data Inputs from Source 1 |
| $Z_a$–$Z_d$ | 3-STATE Multiplexer Outputs |

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## Functional Description

The AC/ACT257 is quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the $I_{0x}$ inputs are selected and when Select is HIGH, the $I_{1x}$ inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are as follows:

$$Z_a = \overline{OE} \bullet (1_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_b = \overline{OE} \bullet (1_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{OE} \bullet (1_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{OE} \bullet (1_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

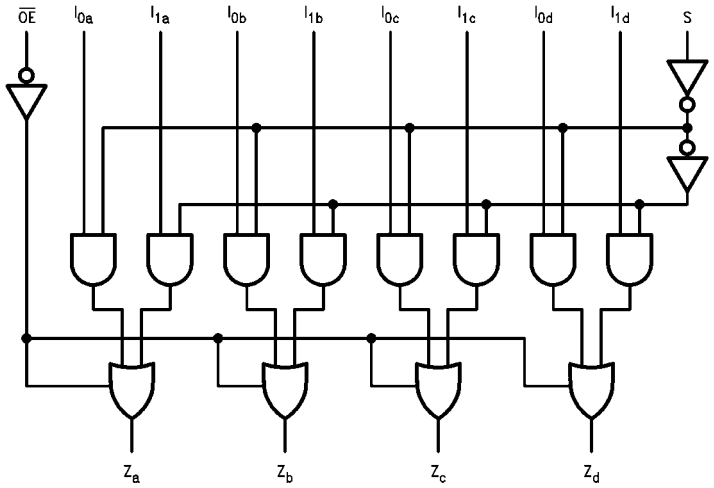
When the Output Enable ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

## Truth Table

| Output Enable | Select Input | Data Inputs | | Outputs |
|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | Z |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ +0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ +0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source ort | |
| Sink Curren ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| Per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| AC Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate (ΔV/Δt) | |
| ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | (V) | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level | 3.0 | 1.5 | 2.1 | 2.1 | | $V_{OUT}$ = 0.1V |
| | Voltage Input | 4.5 | 2.25 | 3.15 | 3.15 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.9 | 0.9 | | $V_{OUT}$ = 0.1V |
| | Voltage Input | 4.5 | 2.25 | 1.35 | 1.35 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level | 3.0 | 2.99 | 2.9 | 2.9 | | |
| | Voltage Output | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | | $I_{OH}$ = −12 mA |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level | 3.0 | 0.002 | 0.1 | 0.1 | | |
| | Voltage Output | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ (Note 4) | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE | | | | | | $V_I$ (OE) = $V_{IL}$, $V_{IH}$ |
| | Leakage Current | 5.5 | | ±0.25 | ±2.5 | μA | $V_I$ = $V_{CC}$, GND |
| | | | | | | | $V_O$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic (Note 3) | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 4) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50\ \mu A$ |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OH} = -24$ mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH} = -24$ mA (Note 5) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50\ \mu A$ |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OL} = 24$ mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL} = 24$ mA (Note 5) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I = V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE Leakage Current | 5.5 | | ± 0.5 | ± 5.0 | μA | $V_I = V_{IL}$, $V_{IH}$<br>$V_O = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | Dynamic Output Current | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max |
| $I_{OHD}$ | Minimum (Note 6) | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND |

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 7) | $T_A = +25°C$, $C_L = 50$ pF Min | Typ | Max | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay $I_n$ to $Z_n$ | 3.3 | 1.5 | 5.0 | 8.5 | 1.0 | 9.0 | ns |
| | | 5.0 | 1.5 | 4.0 | 6.0 | 1.0 | 7.0 | |
| $t_{PHL}$ | Propagation Delay $I_n$ to $Z_n$ | 3.3 | 1.5 | 6.0 | 8.5 | 1.0 | 9.0 | ns |
| | | 5.0 | 1.5 | 4.5 | 6.0 | 1.0 | 7.0 | |
| $t_{PLH}$ | Propagation Delay S to $Z_n$ | 3.3 | 1.5 | 7.0 | 10.5 | 1.5 | 11.5 | ns |
| | | 5.0 | 1.5 | 5.0 | 7.5 | 1.0 | 8.5 | |
| $t_{PHL}$ | Propagation Delay S to $Z_n$ | 3.3 | 1.5 | 7.5 | 10.5 | 1.5 | 11.5 | ns |
| | | 5.0 | 1.5 | 5.5 | 7.5 | 1.0 | 8.5 | |
| $t_{PZH}$ | Output Enable Time | 3.3 | 1.5 | 6.5 | 9.5 | 1.0 | 10.5 | ns |
| | | 5.0 | 1.5 | 5.0 | 7.5 | 1.0 | 8.5 | |
| $t_{PZL}$ | Output Enable Time | 3.3 | 1.5 | 5.5 | 9.0 | 1.0 | 10.0 | ns |
| | | 5.0 | 1.5 | 5.0 | 8.5 | 1.0 | 9.5 | |
| $t_{PHZ}$ | Output Disable Time | 3.3 | 1.5 | 5.5 | 10.0 | 1.0 | 11.0 | ns |
| | | 5.0 | 1.5 | 5.0 | 9.0 | 1.0 | 10.0 | |
| $t_{PLZ}$ | Output Disable Time | 3.3 | 1.5 | 5.5 | 9.0 | 1.0 | 10.0 | ns |
| | | 5.0 | 1.5 | 5.0 | 8.0 | 1.0 | 9.0 | |

**Note 7:** Voltage Range 3.3 is 3.0V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

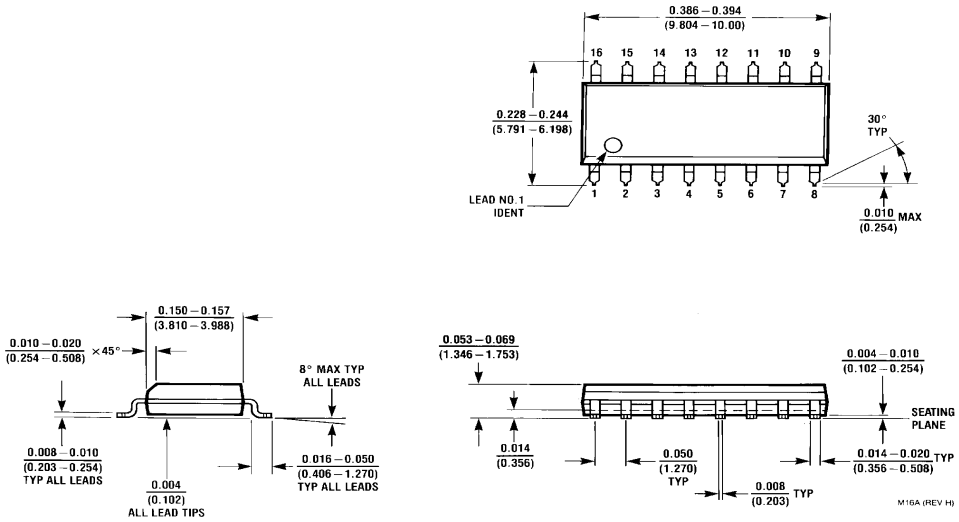
| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 1.5 | 5.0 | 7.0 | 1.0 | 7.5 | ns |
| $t_{PHL}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 2.0 | 6.0 | 7.5 | 1.5 | 8.5 | ns |
| $t_{PLH}$ | Propagation Delay S to $Z_n$ | 5.0 | 2.0 | 7.0 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PHL}$ | Propagation Delay S to $Z_n$ | 5.0 | 2.5 | 7.0 | 10.5 | 2.0 | 11.5 | ns |
| $t_{PZH}$ | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.5 | 9.0 | ns |
| $t_{PZL}$ | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.5 | 9.0 | ns |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 2.5 | 6.5 | 9.0 | 1.5 | 10.0 | ns |
| $t_{PLZ}$ | Output Disable Time | 5.0 | 2.0 | 6.0 | 7.5 | 1.5 | 8.5 | ns |

**Note 8:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

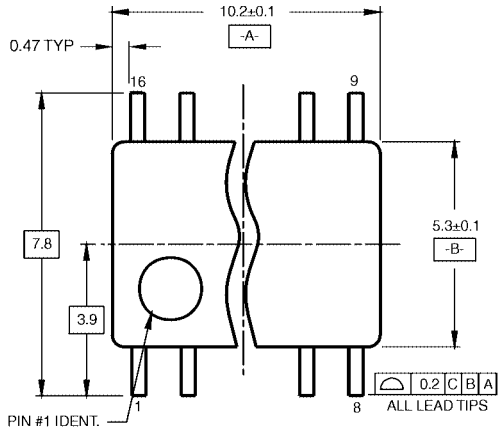
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 50.0 | pF | $V_{CC}$ = 5.0V |

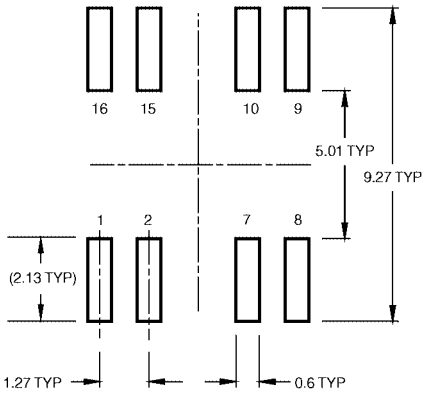
## Physical Dimensions inches (millimeters) unless otherwise noted



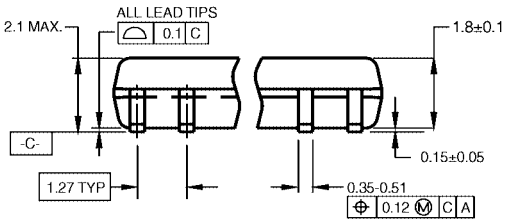

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body**
**Package Number M16A**

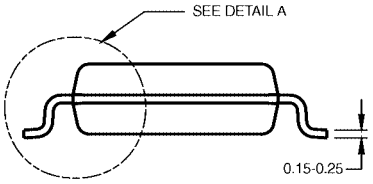
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



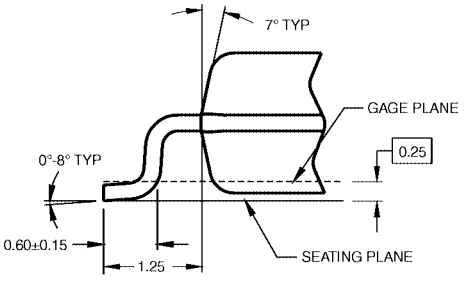




LAND PATTERN RECOMMENDATION




DIMENSIONS ARE IN MILLIMETERS




DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

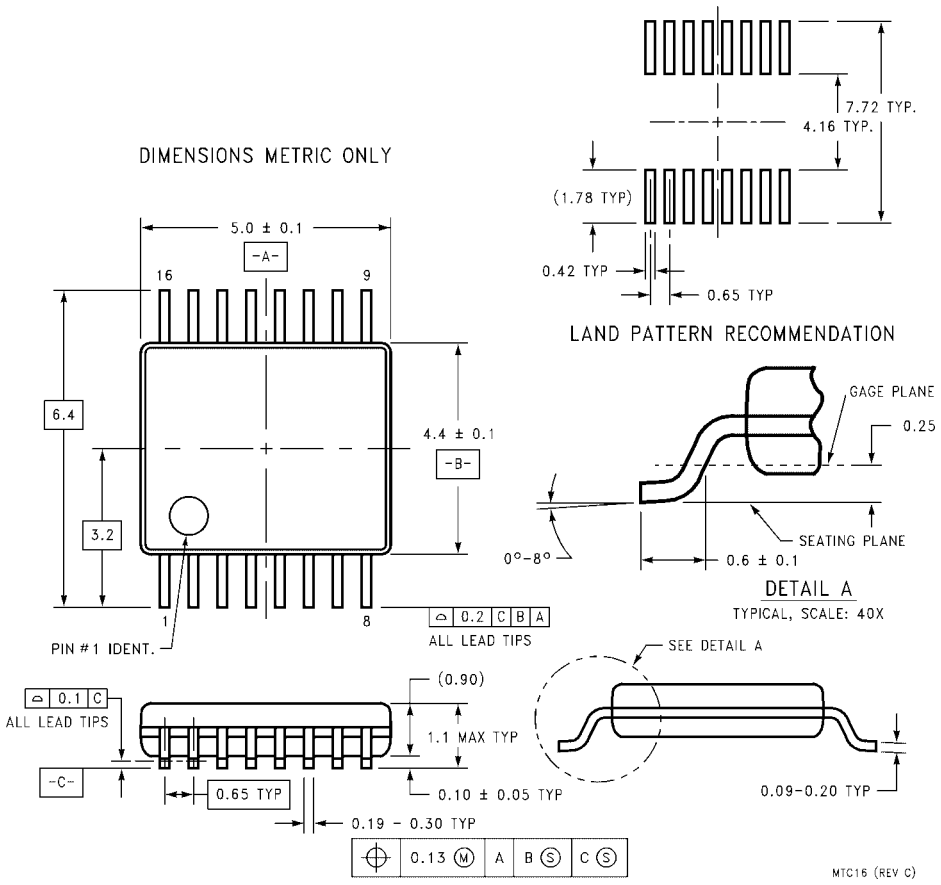
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

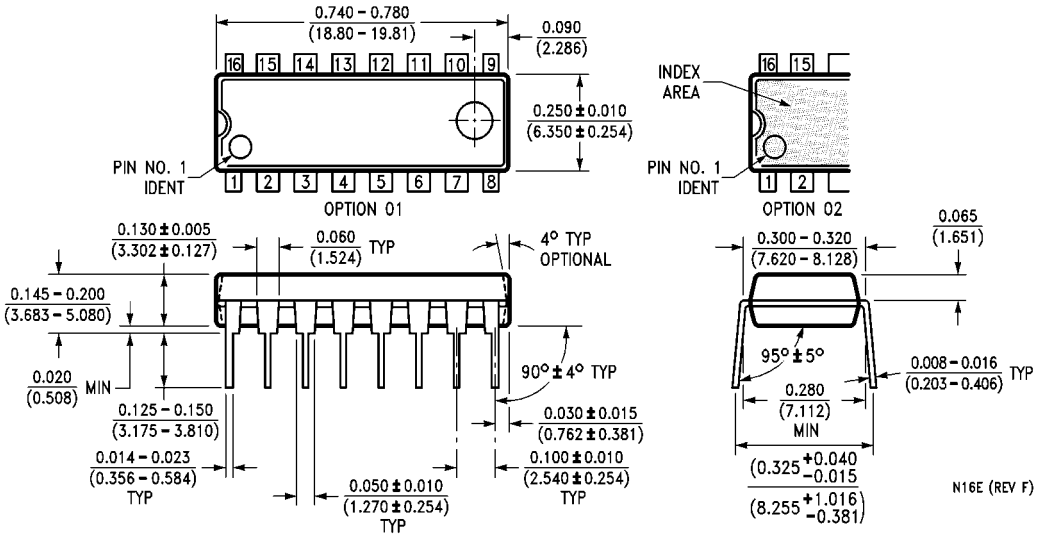
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**