## General Description

The 8430S10I-02 is a PLL-based clock generator specifically designed for Cavium Networks SoC processors. This high performance device is optimized to generate the processor core reference clock, the DDR reference clocks, the PCI/PCI-X bus clocks, and the clocks for both the Gigabit Ethernet MAC and PHY. The clock generator offers ultra low-jitter, low-skew clock outputs, and edge rates that easily meet the input requirements for the CN30XX/CN31XX/CN38XX/CN58XX processors. The output frequencies are generated from a 25MHz external input source or an external 25MHz parallel resonant crystal. The extended temperature range of the 8430S10I-02 supports telecommunication, networking, and storage requirements.

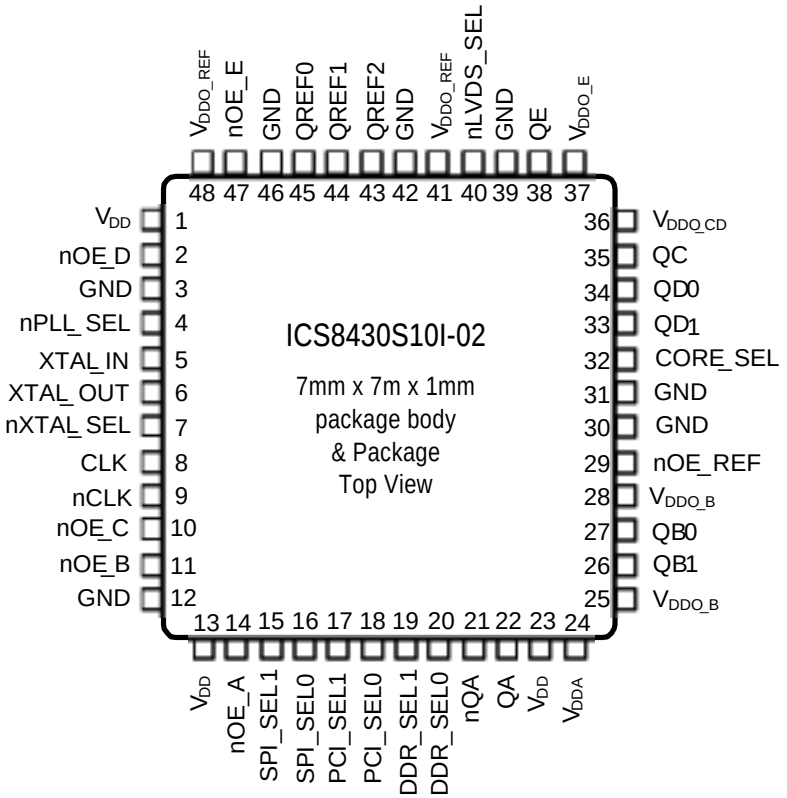
## Features

- One selectable differential output pair for DDR 533/400/667, LVPECL, LVDS interface levels
- Nine LVCMOS/ LVTTL outputs, 20Ω typical output impedance
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential input pair (CLK, nCLK) accepts LVPECL, LVDS, SSTL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Power output supply modes
  LVDS and LVPECL – full 3.3V
  LVCMOS – full 3.3V or mixed 3.3V core/2.5V output
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

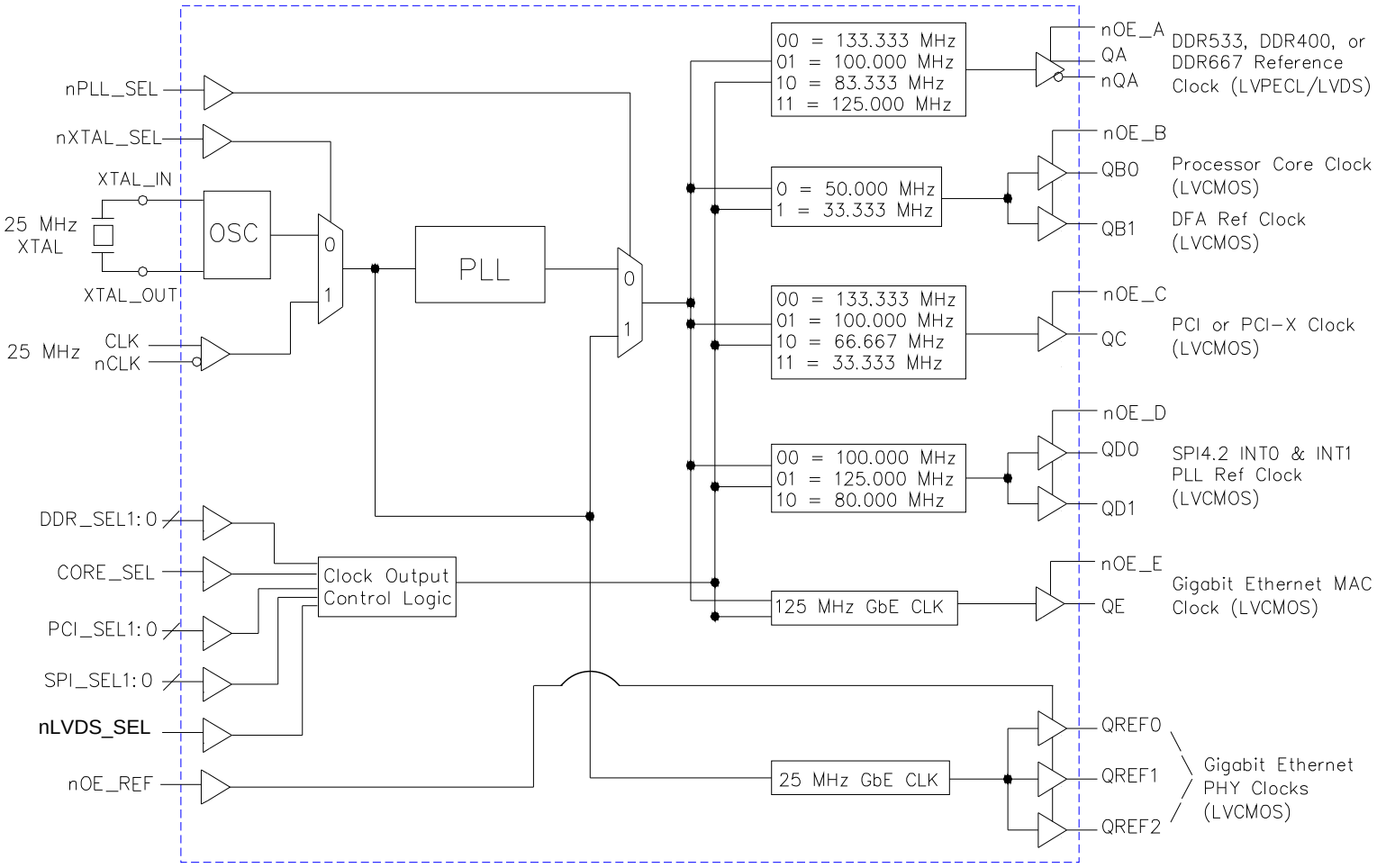
## Applications

- Systems using Cavium Processors
- CPE Gateway Design
- Home Media Servers
- 802.11n AP or Gateway
- Soho Secure Gateway
- Soho SME Gateway
- Wireless Soho and SME VPN Solutions
- Wired and Wireless Network Security
- Web Servers and Exchange Servers

## Pin Assignment



## Block Diagram



## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 13, 23 | $V_{DD}$ | Power | | Core supply pins. |
| 2 | nOE_D | Input | Pulldown | Active LOW output enable for Bank D outputs. When logic HIGH, the outputs are in high impedance (HI-Z). When logic LOW, the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 3, 12, 30, 31, 39, 42, 46 | GND | Power | | Power supply ground. |
| 4 | nPLL_SEL | Input | Pulldown | PLL bypass. When LOW, PLL is enable. When HIGH, PLL is bypassed. LVCMOS/LVTTL interface levels. |
| 5, 6 | XTAL_IN, XTAL_OUT | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 7 | nXTAL_SEL | Input | Pulldown | Selects XTAL inputs when LOW. Selects differential clock (CLK, nCLK) input when HIGH. LVCMOS/LVTTL interface levels. |
| 8 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 9 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. Internal resistor bias to $V_{DD}/2$. |
| 10 | nOE_C | Input | Pulldown | Active LOW output enable for Bank C output. When logic HIGH, the output is in high impedance (HI-Z). When logic LOW, QC output is enabled. LVCMOS/LVTTL interface levels. |
| 11 | nOE_B | Input | Pulldown | Active LOW output enable for Bank B outputs. When logic HIGH, the outputs are in high impedance (HI-Z). When logic LOW, the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 14 | nOE_A | Input | Pulldown | Active LOW output enable for Bank A outputs. LVCMOS/LVTTL interface levels. |
| 15, 16 | SPI_SEL1, SPI_SEL0 | Input | Pulldown | Selects the SPI PLL clock reference frequency. See Table 3D. |
| 17, 18 | PCI_SEL1, PCI_SEL0 | Input | Pulldown | Selects the PCI, PCI-X reference clock output frequency. See Table 3C. LVCMOS/LVTTL interface levels. |
| 19, 20 | DDR_SEL1, DDR_SEL0 | Input | Pulldown | Selects the DDR reference clock output frequency. See Table 3B. LVCMOS/LVTTL interface levels. |
| 21, 22 | nQA, QA | Output | | Differential output pair. Selectable between LVPECL and LVDS interface levels. |
| 24 | $V_{DDA}$ | Power | | Analog supply pin. |
| 25, 28 | $V_{DDO\_B}$ | Power | | Bank B output supply pins. 3.3 V or 2.5V supply. |
| 26, 27 | QB1, QB0 | Output | | Single-ended Bank B outputs. LVCMOS/LVTTL interface levels. |
| 29 | nOE_REF | Input | Pulldown | Active LOW output enable. When logic HIGH, the QREF[2:0] outputs are in high impedance (HI-Z). When logic LOW, the QREF[2:0] outputs are enabled. LVCMOS/ LVTTL interface levels. |
| 32 | CORE_SEL | Input | Pulldown | Selects the processor core clock output frequency. The output frequency is 50MHz when LOW, and 33.333MHz when HIGH. See Table 3A. LVCMOS/LVTTL interface levels. |
| 33, 34 | QD1, QD0 | Output | | Single-end Bank D outputs. LVCMOS/LVTTL interface levels. |
| 35 | QC | Output | | Single-end Bank C output. LVCMOS/LVTTL interface levels. |
| 36 | $V_{DDO\_CD}$ | Power | | Bank C and Bank D output supply pin. 3.3 V or 2.5V supply. |

Pin descriptions continue on the next page.

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 37 | $V_{DDO\_E}$ | Power | | Bank E output supply pin. 3.3 V or 2.5V supply. |
| 38 | QE | Output | | Single-end Bank E output. LVCMOS/LVTTL interface levels. |
| 40 | nLVDS_SEL | Input | Pulldown | Selects between LVDS and LVPECL interface levels on differential output pair QA and nQA. When LOW, LVDS interface levels are selected. When HIGH, LVPECL is selected. See Table 3E. |
| 41, 48 | $V_{DDO\_REF}$ | Power | | Bank QREF output supply pins. 3.3 V or 2.5V supply. |
| 43, 44, 45 | QREF2, QREF1, QREF0 | Output | | Single-ended reference clock outputs. LVCMOS/LVTTL interface levels. |
| 47 | nOE_E | Input | Pulldown | Active LOW output enable for Bank E outputs. When logic HIGH, the outputs are in high impedance (HI-Z). When logic LOW, the outputs are enabled. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | | $V_{DD}$, $V_{DDO\_X}$ = 3.465V | | 10 | | pF |
| | | | $V_{DD}$ = 3.465V, $V_{DDO\_X}$ = 2.625V | | 5 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | QB[0:1], QC, QD[0:1], QE QREF[0:2] | $V_{DDO\_X}$ = 3.465V | | 20 | | Ω |
| | | QB[0:1], QC, QD[0:1], QE QREF[0:2] | $V_{DDO\_X}$ = 2.625V | | 25 | | Ω |

NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_E}$ and $V_{DDO\_REF}$.

# Function Tables

**Table 3A. Control Input Function Table**

| Input | Output Frequency |
|---|---|
| CORE_SEL | QB[0:1] |
| 0 | 50MHz (default) |
| 1 | 33.333MHz |

**Table 3B. Control Input Function Table**

| Inputs | | Output Frequency |
|---|---|---|
| DDR_SEL1 | DDR_SEL0 | QA, nQA |
| 0 | 0 | 133.333MHz (default) |
| 0 | 1 | 100.000MHz |
| 1 | 0 | 83.333MHz |
| 1 | 1 | 125.000MHz |

**Table 3C. Control Input Function Table**

| Inputs | | Output Frequency |
|---|---|---|
| PCI_SEL1 | PCI_SEL0 | QC |
| 0 | 0 | 133.333MHz (default) |
| 0 | 1 | 100.000MHz |
| 1 | 0 | 66.6667MHz |
| 1 | 1 | 33.333MHz |

**Table 3D. Control Input Function Table**

| Inputs | | Output Frequency |
|---|---|---|
| SPI_SEL1 | SPI_SEL0 | QD[0:1] |
| 0 | 0 | 100.000MHz (default) |
| 0 | 1 | 125.000MHz |
| 1 | 0 | 80.000MHz |

**Table 3E. Control Input Function Table**

| Input | Output Levels |
|---|---|
| nLVDS_SEL | QA, nQA |
| 0 | LVDS (default) |
| 1 | LVPECL |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge Current | <br>10mA<br>15mA |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 33.1°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. LVCMOS Power Supply DC Characteristics,** $V_{DD}$ = $V_{DDO\_X}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.25 | 3.3 | $V_{DD}$ | V |
| $V_{DDO\_X}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 180 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 25 | mA |
| $I_{DDO\_X}$ | Output Supply Current | No Load, CLK selected | | | 60 | mA |

NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$ and $V_{DDO\_REF}$.

**Table 4B. LVCMOS Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.25 | 3.3 | $V_{DD}$ | V |
| $V_{DDO\_X}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | | 102 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 25 | mA |
| $I_{DDO\_X}$ | Output Supply Current | No Load, CLK selected | | | 42 | mA |

NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$ and $V_{DDO\_REF}$.

**Table 4C. LVPECL Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.25 | 3.3 | $V_{DD}$ | V |
| $I_{EE}$ | Power Supply Current | nLVDS_SEL = 1 | | | 180 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 25 | mA |

**Table 4D. LVDS Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.25 | 3.3 | $V_{DD}$ | V |
| $I_{DD}$ | Power Supply Current | nLVDS_SEL = 0 | | | 192 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 25 | mA |

**Table 4E. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | DDR_SEL[0:1], nPLL_SEL, nLVDS_SEL, PCI_SEL[0:1], nOE_REF, SPI_SEL[0:1], nOE_[A:E], nXTAL_SEL, CORE_SEL | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | DDR_SEL[0:1], nPLL_SEL, nLVDS_SEL, PCI_SEL[0:1], nOE_REF, SPI_SEL[0:1], nOE_[A:E], nXTAL_SEL, CORE_SEL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| $V_{OH}$ | Output High Voltage | | $V_{DDO\_X}$ = 3.465V, $I_{OH}$ = -12mA | 2.6 | | | V |
| | | | $V_{DDO\_X}$ = 2.625V, $I_{OH}$ = -12mA | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage | | $V_{DDO\_X}$ = 3.465V, $I_{OL}$ = 12mA | | | 0.65 | V |
| | | | $V_{DDO\_X}$ = 2.625V, $I_{OL}$ = 12mA | | | 0.55 | V |

NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_E}$ and $V_{DDO\_REF}$.

**Table 4F. Differential DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK, nCLK | $V_{DD} = V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| | | nCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | 1.2 | | $V_{DD}$ | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as $V_{IH}$.

**Table 4G. LVPECL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DD}$ – 1.4 | | $V_{DD}$ – 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{DD}$ – 2.0 | | $V_{DD}$ – 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.55 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DD}$ – 2V.

**Table 4H. LVDS DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 300 | 500 | 600 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.04 | 1.14 | 1.24 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

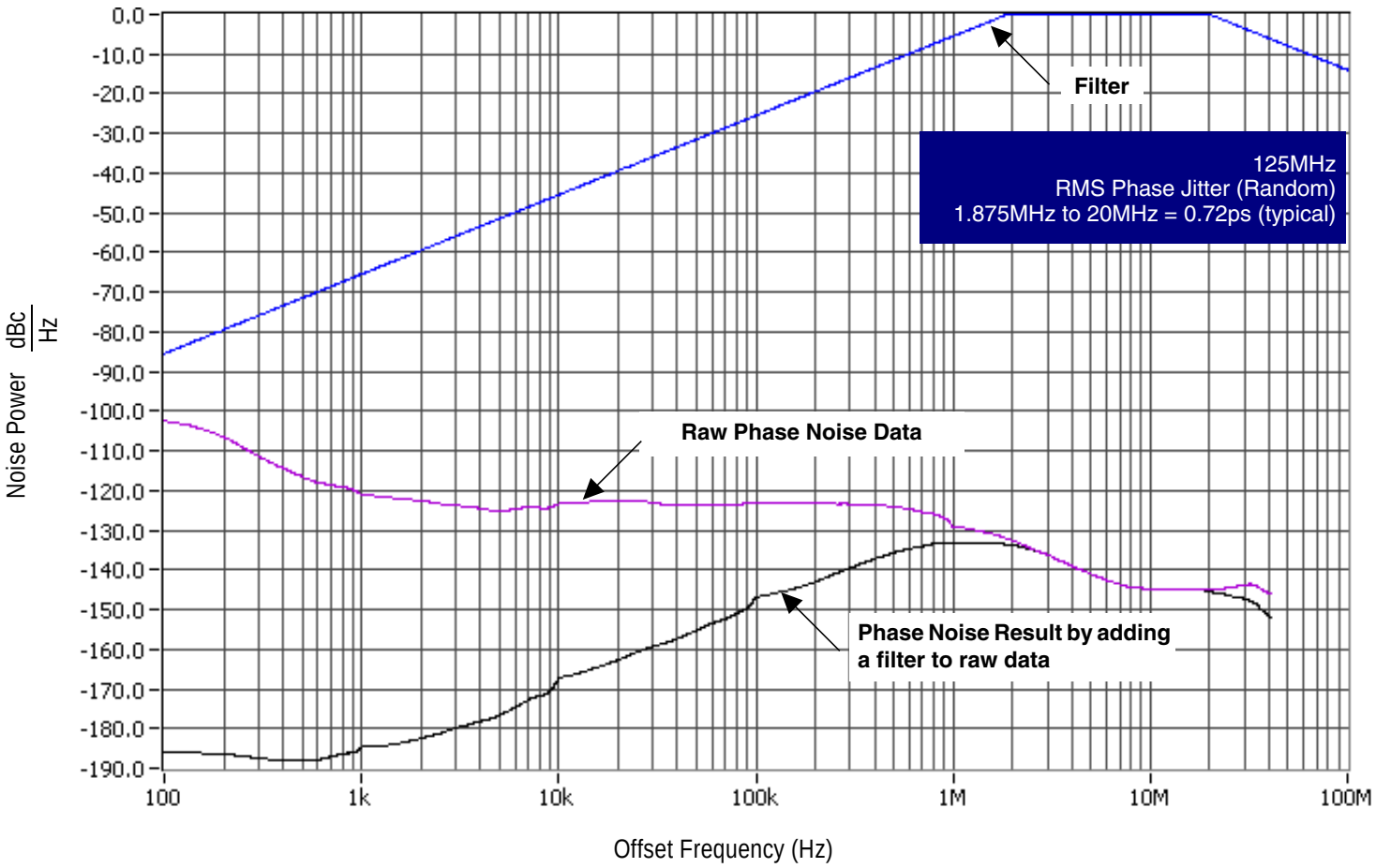
## AC Electrical Characteristics

**Table 6. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO\_X}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

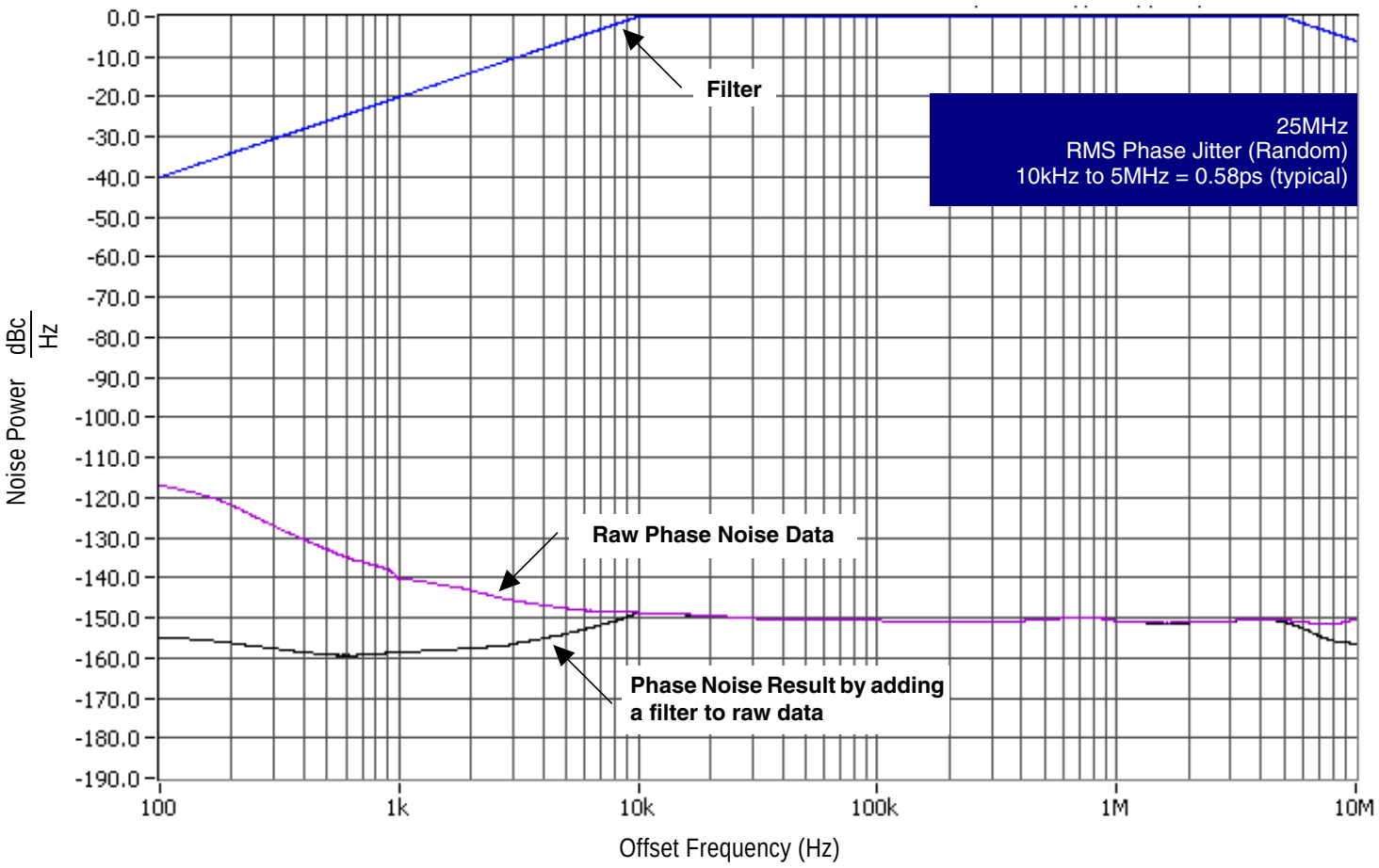
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | QA, nQA | DDR_SEL[1:0] = 00 | | 133.333 | | MHz |
| | | QA, nQA | DDR_SEL[1:0] = 01 | | 100 | | MHz |
| | | QA, nQA | DDR_SEL[1:0] = 10 | | 83.333 | | MHz |
| | | QA, nQA | DDR_SEL[1:0] = 11 | | 125 | | MHz |
| | | QBx | CORE_SEL = 0 | | 50 | | MHz |
| | | QBx | CORE_SEL = 1 | | 33.333 | | MHz |
| | | QC | PCI_SEL[1:0] = 00 | | 133.333 | | MHz |
| | | QC | PCI_SEL[1:0] = 01 | | 100 | | MHz |
| | | QC | PCI_SEL[1:0] = 10 | | 66.667 | | MHz |
| | | QC | PCI_SEL[1:0] = 11 | | 33.333 | | MHz |
| | | QDx | SPI_SEL[1:0] = 00 | | 100 | | MHz |
| | | QDx | SPI_SEL[1:0] = 01 | | 125 | | MHz |
| | | QDx | SPI_SEL[1:0] = 10 | | 80 | | MHz |
| | | QE | | | 125 | | MHz |
| | | QREFx | | | 25 | | MHz |
| *t*sk(b) | Bank Skew; NOTE 2, 4 | QREFx | | | | 30 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | QREFx | | | | 200 | ps |
| tjit(cc) | Cycle-to-Cycle Jitter | QA, nQA | measured at crosspoint | | | 60 | ps |
| | | QBx, QC, QDx | | | | 115 | ps |
| | | QE | | | | 120 | ps |
| tjit(per) | RMS Period Jitter | QA, nQA | measured at crosspoint | | | 40 | ps |
| tjit(hper) | RMS Half-period Jitter | QA, nQA | measured at crosspoint | | | 50 | ps |
| tjit(Ø) | RMS Phase Jitter, (Random); NOTE 1 | QREFx | 25MHz (10kHz to 5MHz) | | 0.58 | | ps |
| | | QE | 125MHz (1.875MHz to 20MHz) | | 0.72 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | QA, nQA | 20% to 80% | 100 | | 300 | ps |
| | | QBx, QC, QDx, QE, QREFx | | 400 | | 1200 | ps |
| odc | Output Duty Cycle | QA, nQA | | 48 | | 52 | % |
| | | QBx, QC, QDx, QE, QREFx | | 40 | | 60 | % |
| $t_{LOCK}$ | Lock Time | | | | | 100 | ms |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at maximum $f_{OUT}$ unless noted otherwise.
NOTE: $V_{DDO\_X}$ denotes $V_{DDO\_B}$, $V_{DDO\_CD}$, $V_{DDO\_E}$ and $V_{DDO\_REF}$.
NOTE 1: Refer to the phase noise plot.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO\_REF}$/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

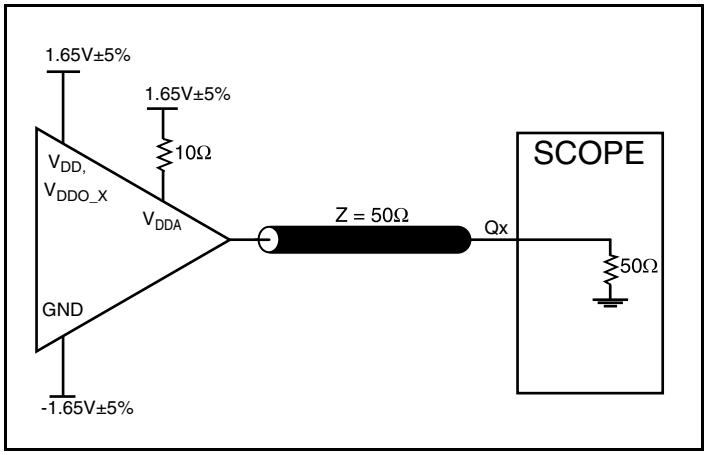
## Typical Phase Noise at 125MHz (QE output)



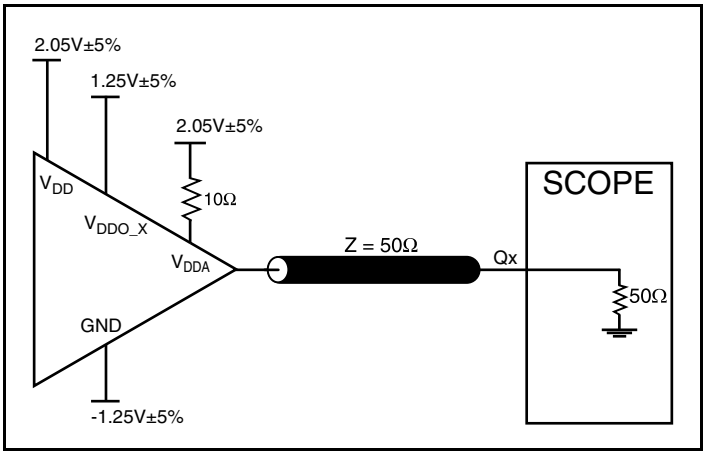
## Typical Phase Noise at 25MHz (QREF output)



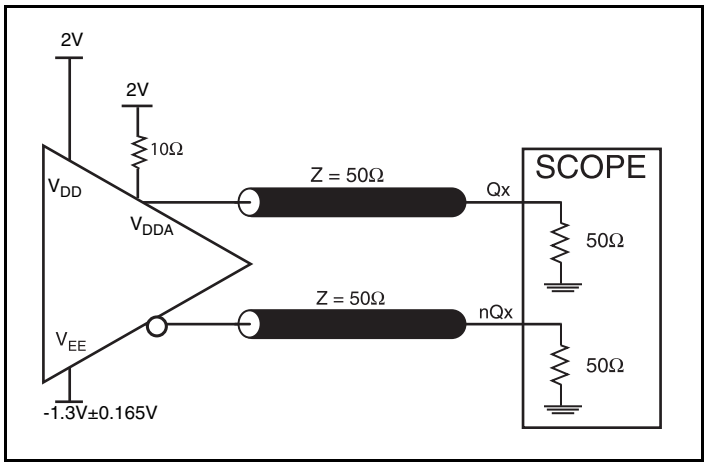
## Parameter Measurement Information



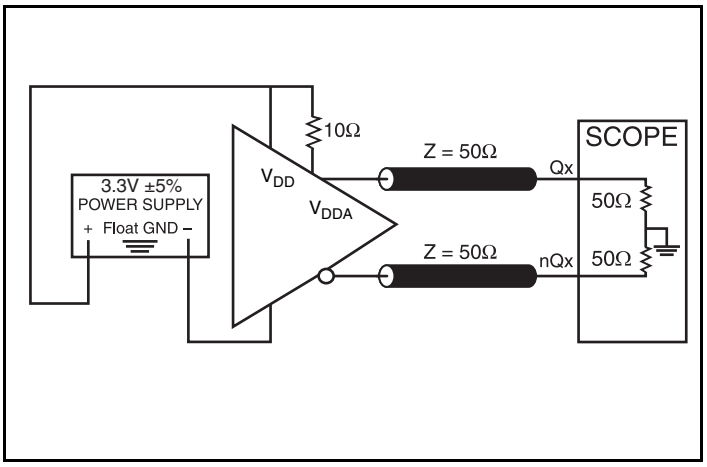

**3.3V Core/3.3V LVCMOS Output Load AC Test Circuit**



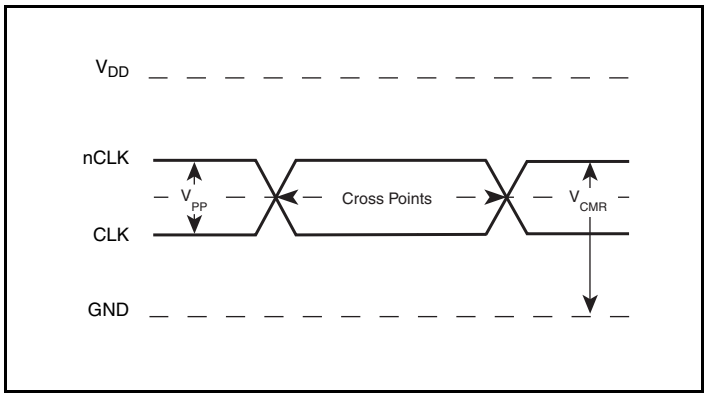

**3.3V Core/2.5V LVCMOS Output Load AC Test Circuit**



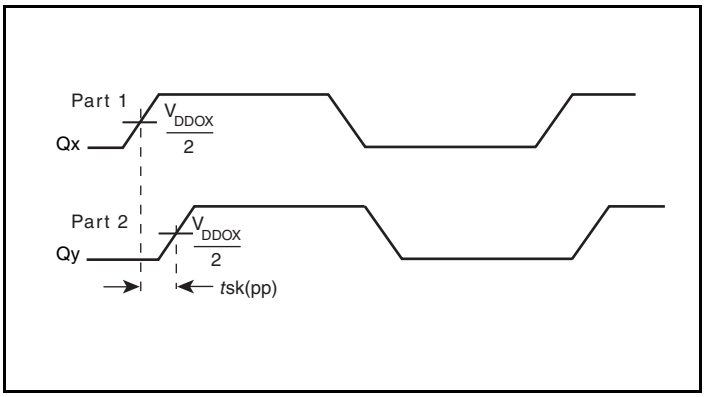

**3.3V Core/3.3V LVPECL Output Load AC Test Circuit**




**3.3V Core/3.3V LVDS Output Load AC Test Circuit**

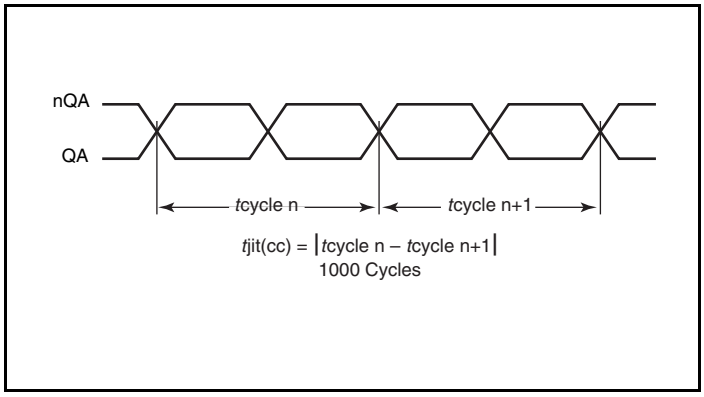



**Differential Input Level**

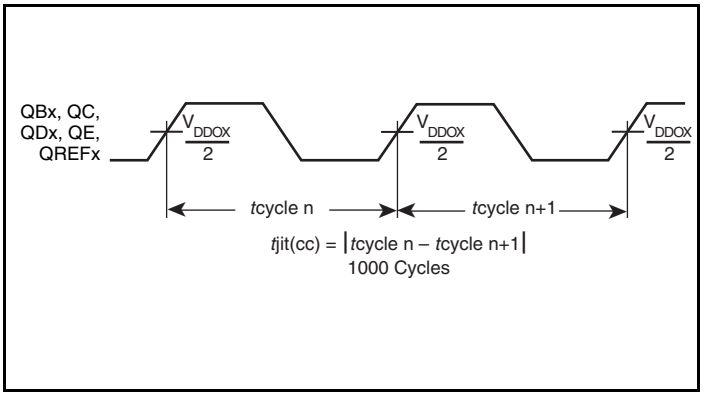



**LVCMOS Part-to-Part Skew**

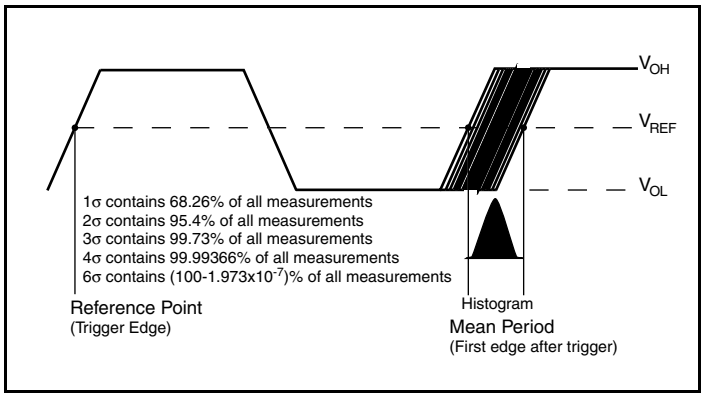
# Parameter Measurement Information, continued



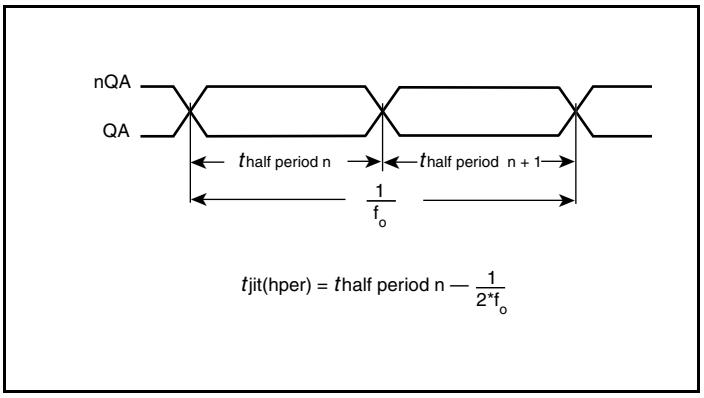

**Differential Cycle-to-Cycle Jitter**



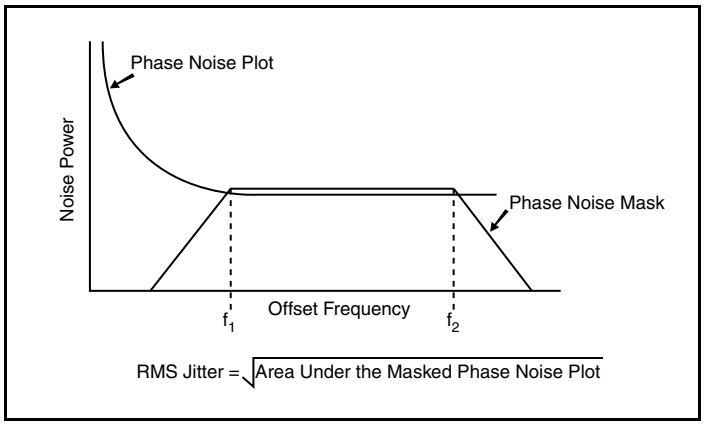

**LVCMOS Cycle-to-Cycle Jitter**



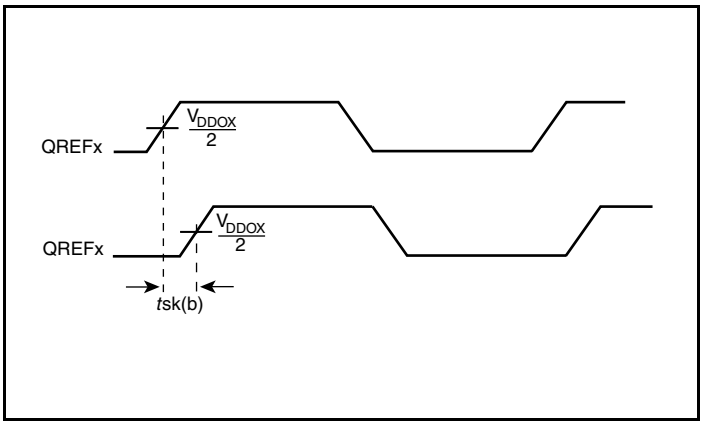

**Period Jitter**




**Half Period Jitter**

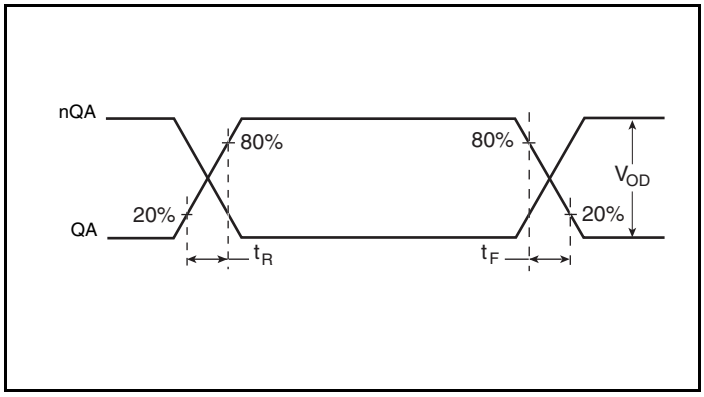



**RMS Phase Jitter**

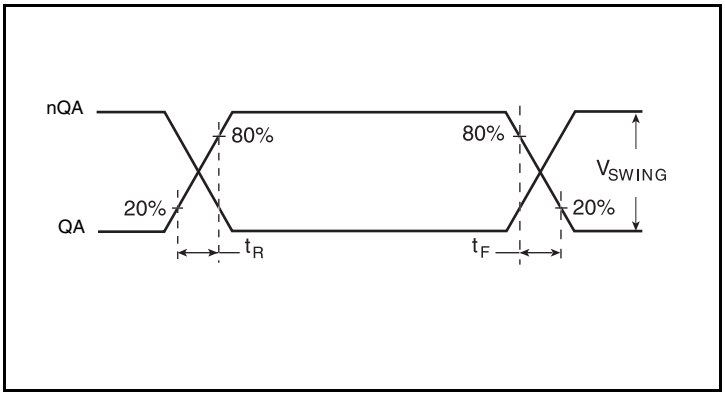



**LVCMOS Bank Skew (where X denotes QREF0 1, or 2)**

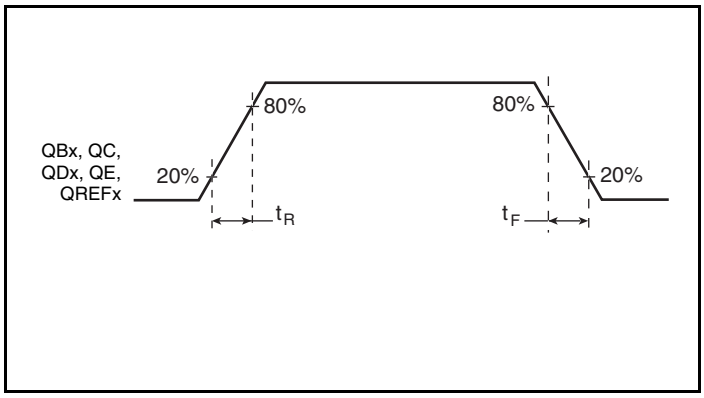
## Parameter Measurement Information, continued



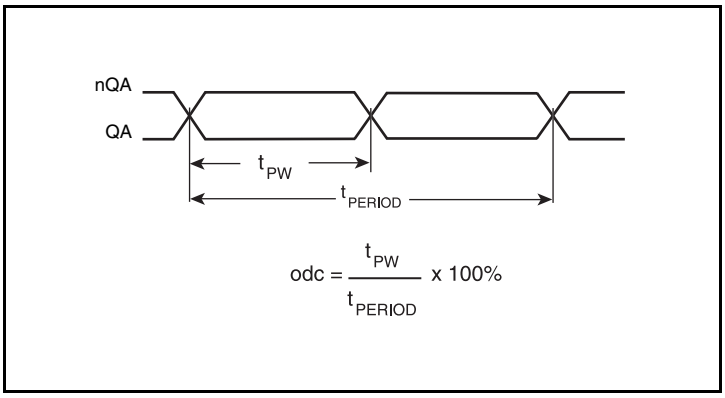

**LVDS Output Rise/Fall Time**



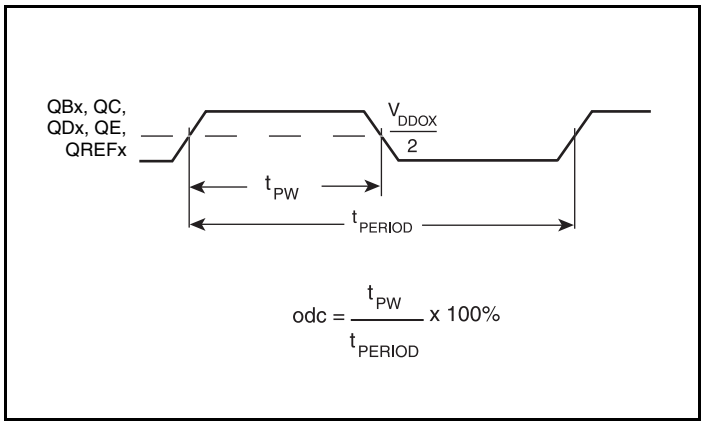

**LVPECL Output Rise/Fall Time**



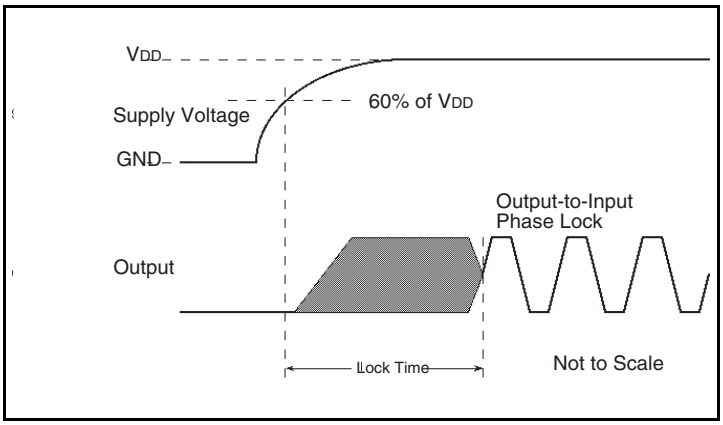

**LVCMOS Output Rise/Fall Time**




**Differential Output Duty Cycle/Pulse Width/Period**

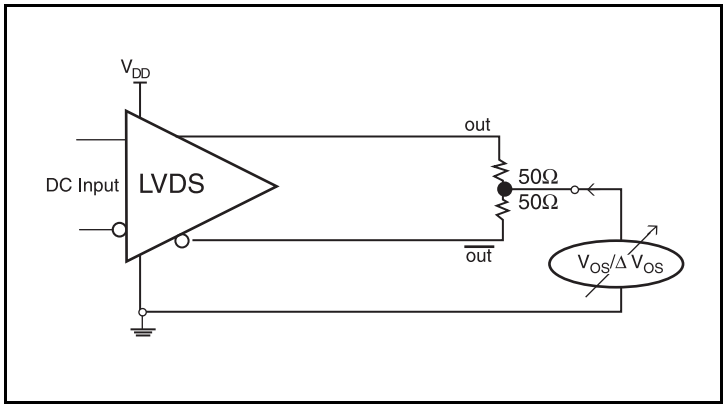



**LVCMOS Output Duty Cycle/Pulse Width/Period**

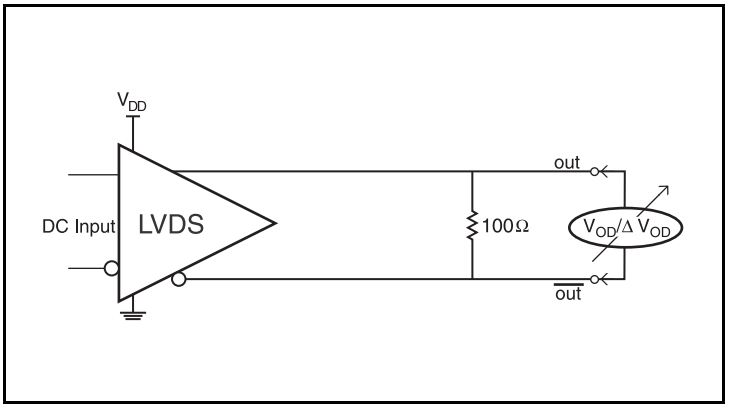



**Lock Time**

## Parameter Measurement Information, continued




**Offset Voltage Setup**




**Differential Output Voltage Setup**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_{REF}$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_{REF}$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

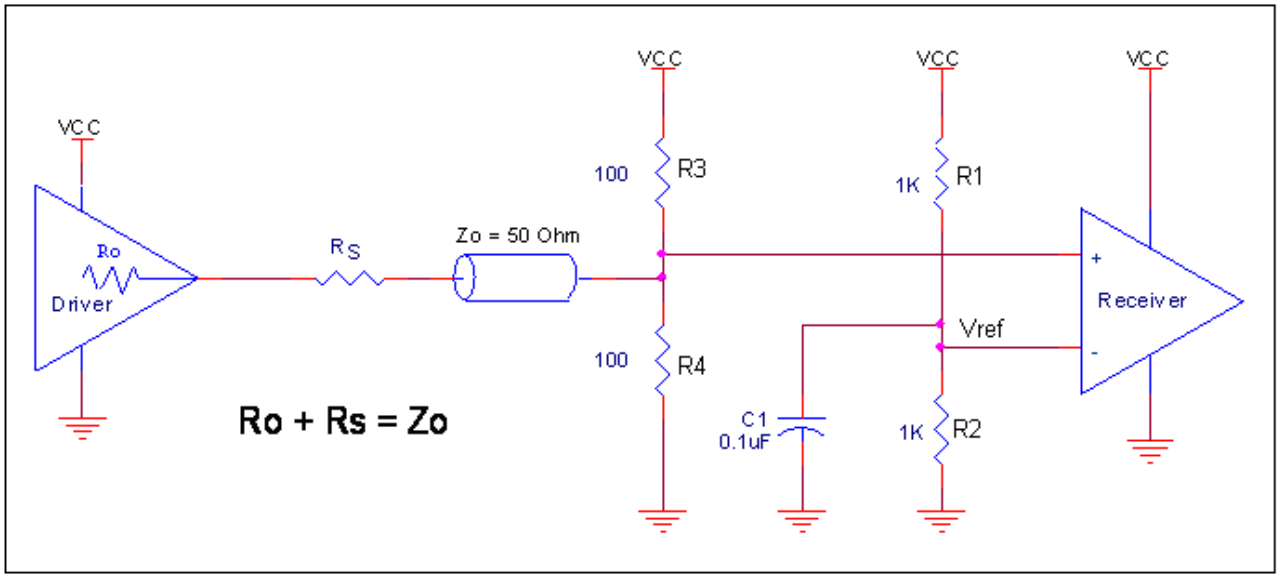



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, SSTL, and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. If the driver is from another vendor, use their termination recommendation.

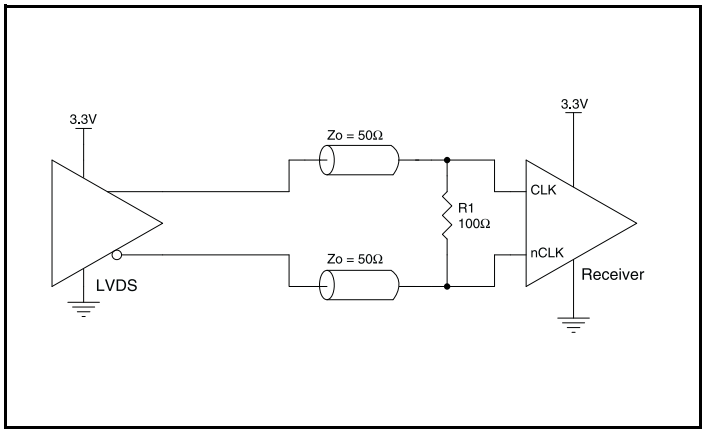



**Figure 2A. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

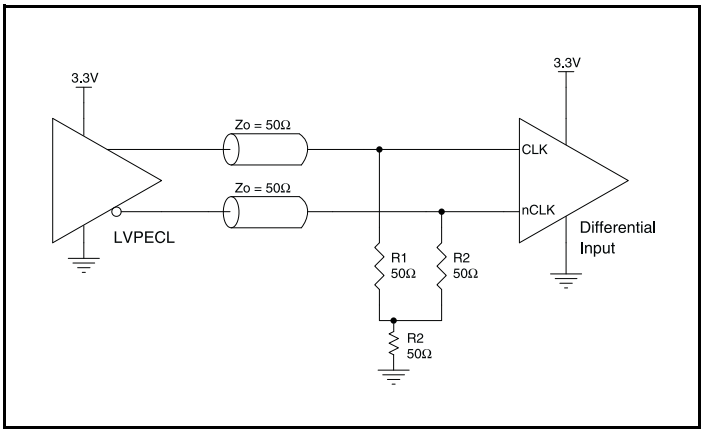



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

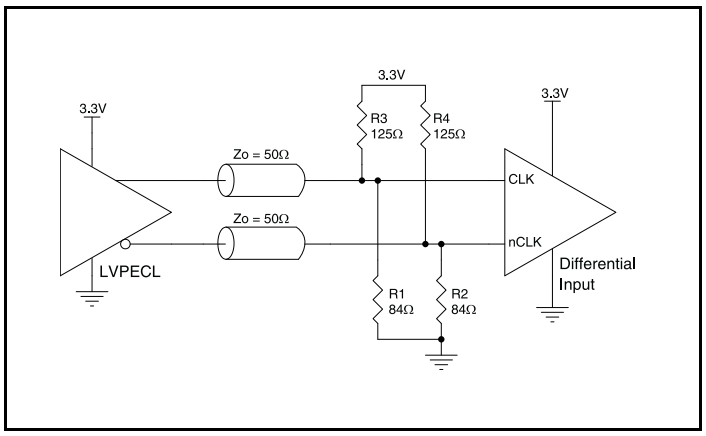



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

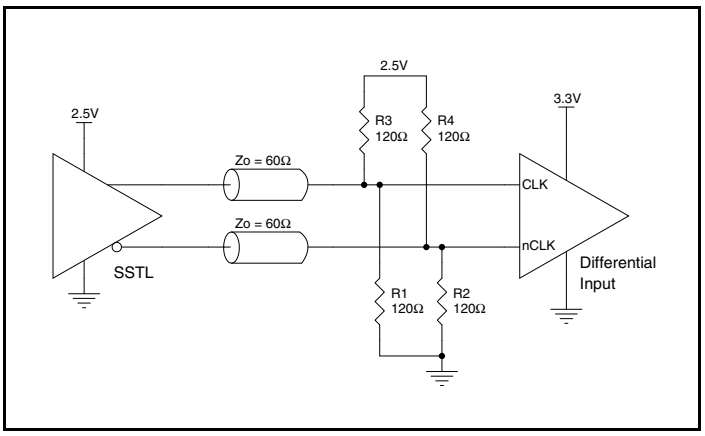



**Figure 2D. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

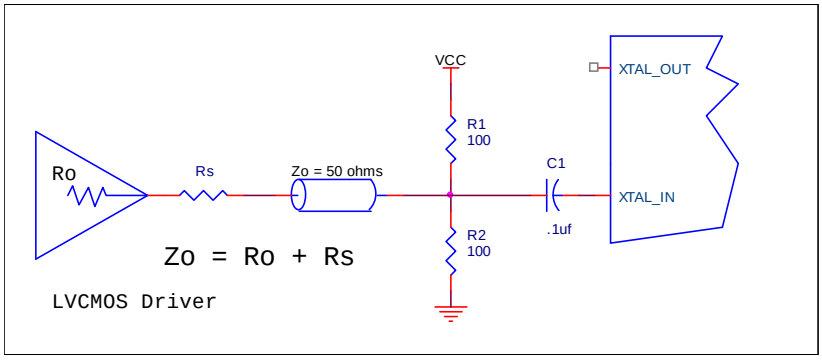



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

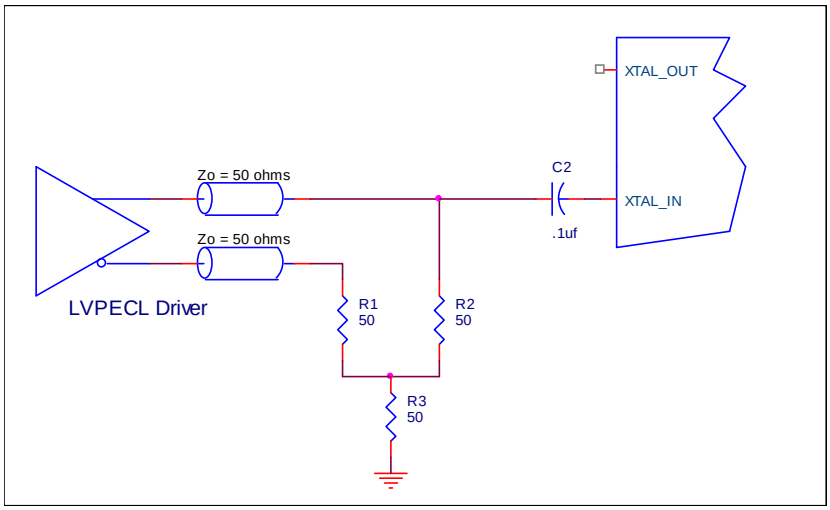



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.
The differential output pair is low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

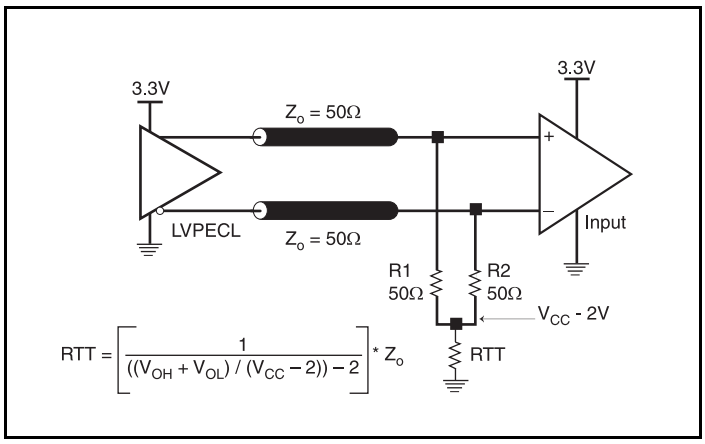



**Figure 4A. 3.3V LVPECL Output Termination**

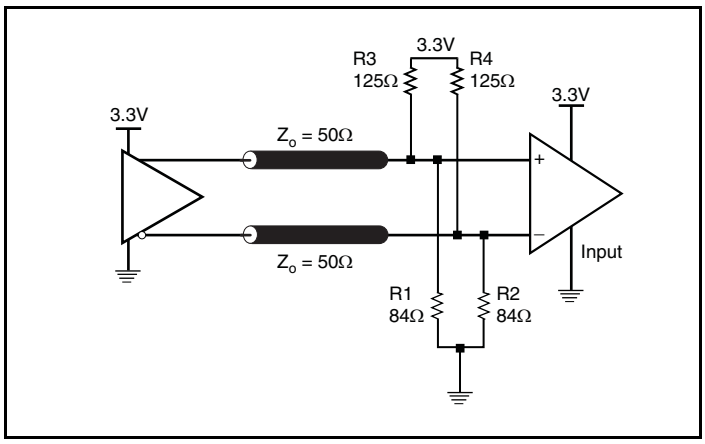



**Figure 4B. 3.3V LVPECL Output Termination**

## LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 5 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

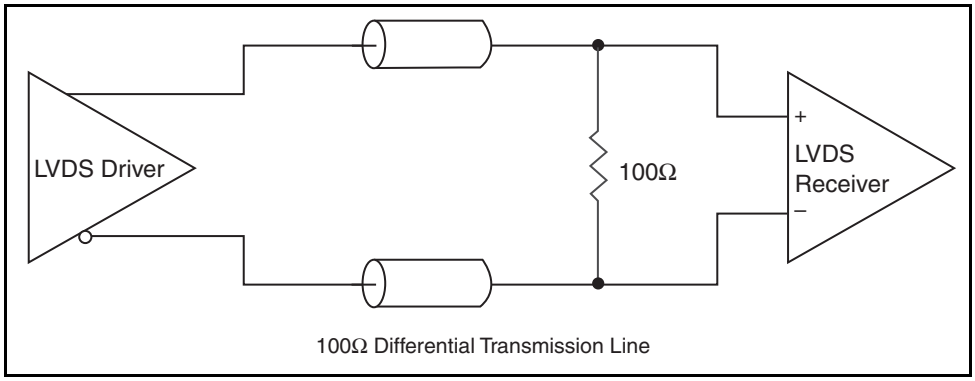



**Figure 5. Typical LVDS Driver Termination**

## EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

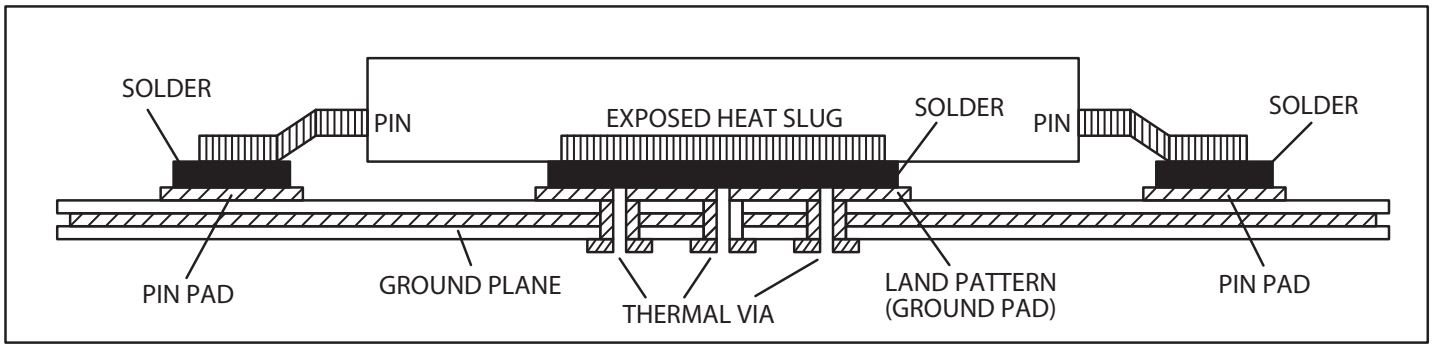



**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

#### LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

## Schematic Example

*Figure 7* shows an example of 8430S10I-02 application schematic. In this example, the device is operated at $V_{DD}$ = $V_{DDO\_B}$ = $V_{DDO\_CD}$ = $V_{DDO\_E}$ = $V_{DDO\_REF}$ = 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 18pF and C2 = 18pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 8430S10I-02 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

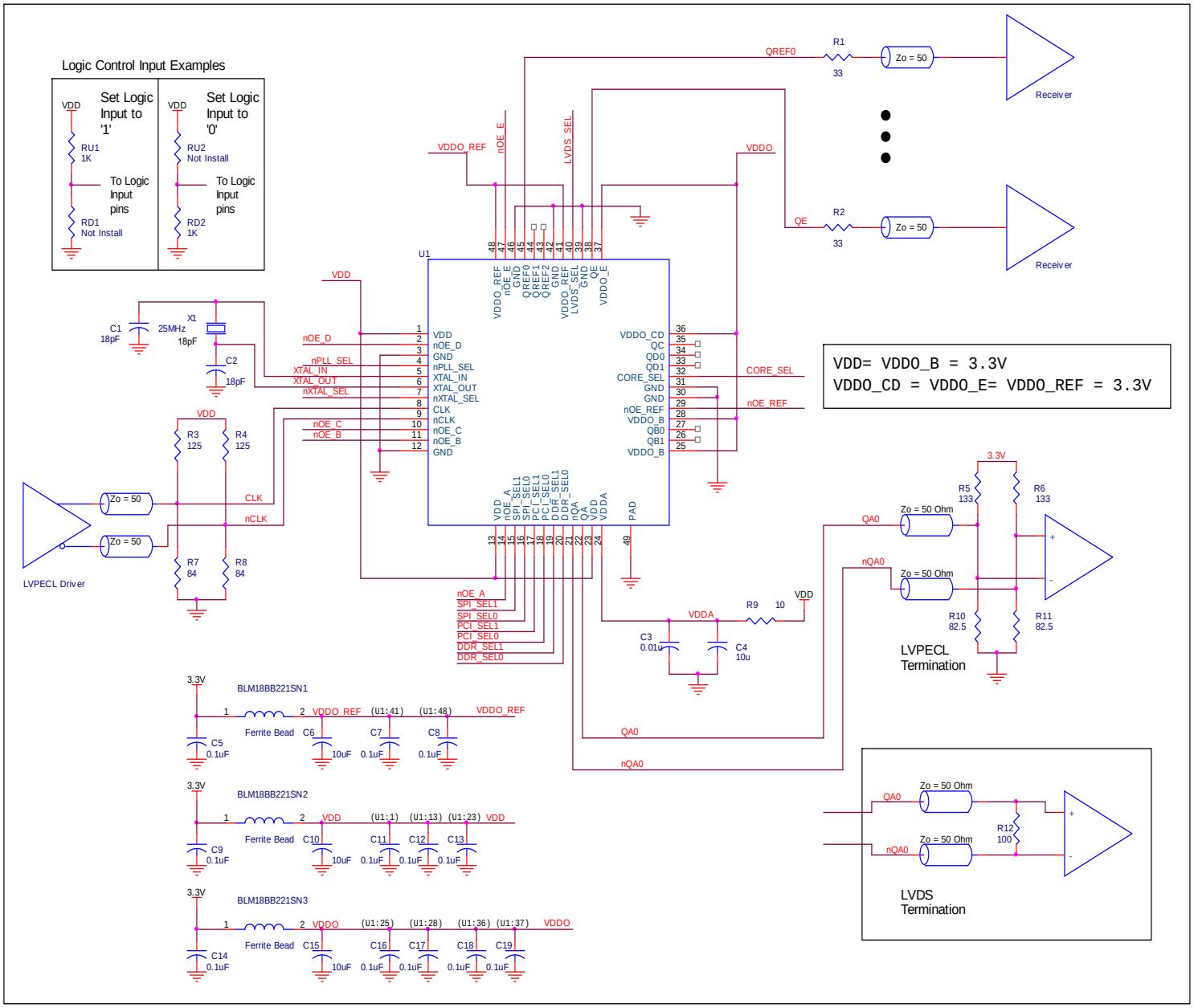



**Figure 7. 8430S10I-02 Layout Example**

# Power Considerations (LVCMOS/LVDS Outputs)

This section provides information on power dissipation and junction temperature for the 8430S10I-02.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8430S10I-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

**Core and LVDS Output Power Dissipation**

- Power (core, LVDS) = $V_{DD\_MAX}$ * ($I_{DD}$ + $I_{DDA}$) = 3.465V * (192mA + 25mA) = **751.9mW**

**LVCMOS Output Power Dissipation**

- Output Impedance $R_{OUT}$ Power Dissipation due to Loading 50Ω to $V_{DDO}$/2
  Output Current $I_{OUT}$ = $V_{DDO\_MAX}$ / [2 * (50Ω + $R_{OUT}$)] = 3.465V / [2 * (50Ω + 20Ω)] = **24.80mA**
- Power Dissipation on the $R_{OUT}$ per LVCMOS output
  Power ($R_{OUT}$) = $R_{OUT}$ * ($I_{OUT}$)$^2$ = 20Ω * (24.80mA)$^2$ = **12.3mW per output**
- Total Power Dissipation on the $R_{OUT}$
  **Total Power ($R_{OUT}$)** = 12.3mW * 9 = **110.7mW**
- Dynamic Power Dissipation at 133MHz
  Power (133MHz) = $C_{PD}$ * Frequency * ($V_{DDO}$)$^2$ = 10pF * 133MHz * (3.465V)$^2$ = **16mW per output**
  **Total Power** (133MHz) = 16mW * 6 = **96mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = $C_{PD}$ * Frequency * ($V_{DDO}$)$^2$ = 10pF * 25MHz * (3.465)$^2$ = **3mW per output**
  **Total Power** (25MHz) = 3mW * 3 **= 9mW**

**Total Power Dissipation**

- **Total Power**
  = Power (core, LVDS) + Total Power ($R_{OUT}$) + Total Power (133MHz) + Total Power (25MHz)
  = 751.9mW + 110.7mW + 96mW + 9mW
  **= 967.6mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.968W * 33.1°C/W = 117°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7A. Thermal Resistance $\theta_{JA}$ for 48 Lead TQFP, EPAD Forced Convection**

| $\theta_{JA}$ Vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 27.2°C/W | 25.7°C/W |

# Power Considerations (LVCMOS/LVPECL Outputs)

This section provides information on power dissipation and junction temperature for the 8430S10I-02.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8430S10I-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

**Core and LVPECL Output Power Dissipation**

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 180mA = **623.7mW**
- Power (output)$_{MAX}$ = **30mW/Loaded Output Pair**

**LVCMOS Output Power Dissipation**

- Output Impedance $R_{OUT}$ Power Dissipation due to Loading 50Ω to $V_{DDO}$/2
  Output Current $I_{OUT}$ = $V_{DDO\_MAX}$ / [2 * (50Ω + $R_{OUT}$)] = 3.465V / [2 * (50Ω + 20Ω)] = **24.80mA**
- Power Dissipation on the $R_{OUT}$ per LVCMOS output
  Power ($R_{OUT}$) = $R_{OUT}$ * ($I_{OUT}$)$^2$ = 20Ω * (24.80mA)$^2$ = **12.3mW per output**
- Total Power Dissipation on the $R_{OUT}$
  **Total Power ($R_{OUT}$)** = 12.3mW * 9 = **110.7mW**
- Dynamic Power Dissipation at 133MHz
  Power (133MHz) = $C_{PD}$ * Frequency * ($V_{DDO}$)$^2$ = 10pF * 133MHz * (3.465V)$^2$ = **16mW per output**
  **Total Power** (133MHz) = 16mW * 6 = **96mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = $C_{PD}$ * Frequency * ($V_{DDO}$)$^2$ = 10pF * 25MHz * (3.465)$^2$ = **3mW per output**
  **Total Power** (25MHz) = 3mW * 3 **= 9mW**

**Total Power Dissipation**

- **Total Power**
  = Power (core) + Power (LVPECL output) + Total Power ($R_{OUT}$) + Total Power (133MHz) + Total Power (25MHz)
  = 623.7mW + 30mW + 110.7mW + 96mW + 9mW
  **= 869.4mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.869W * 33.1°C/W = 113.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7B. Thermal Resistance $\theta_{JA}$ for 48 Lead TQFP, EPAD Forced Convection**

| $\theta_{JA}$ Vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 27.2°C/W | 25.7°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

The LVPECL output driver circuit and termination are shown in *Figure 8.*

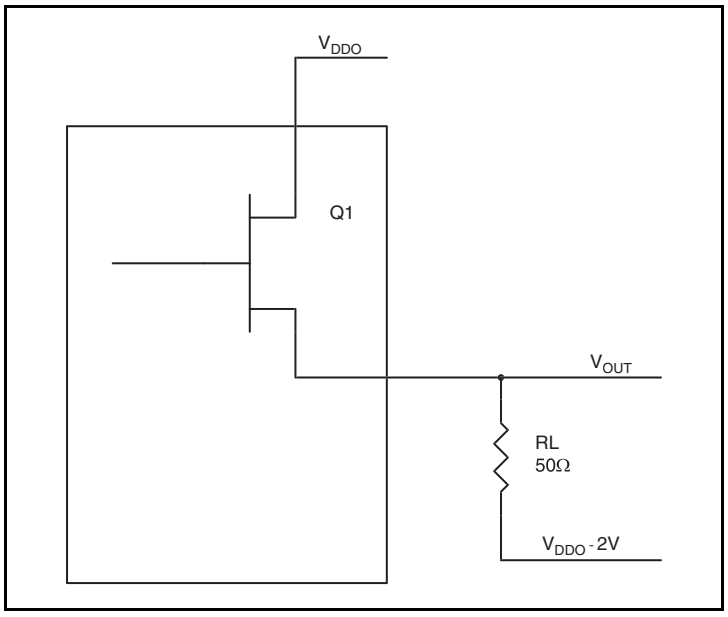



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{DDO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DDO\_MAX} – 0.9V}$
  $(V_{DDO\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DDO\_MAX} – 1.7V}$
  $(V_{DDO\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{DDO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 48 Lead TQFP, EPAD**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 27.2°C/W | 25.7°C/W |

## Transistor Count

The transistor count for 8430S10I-02 is: 10,871

# Package Outline and Package Dimensions

## Package Outline - Y Suffix for 48 Lead TQFP, EPAD

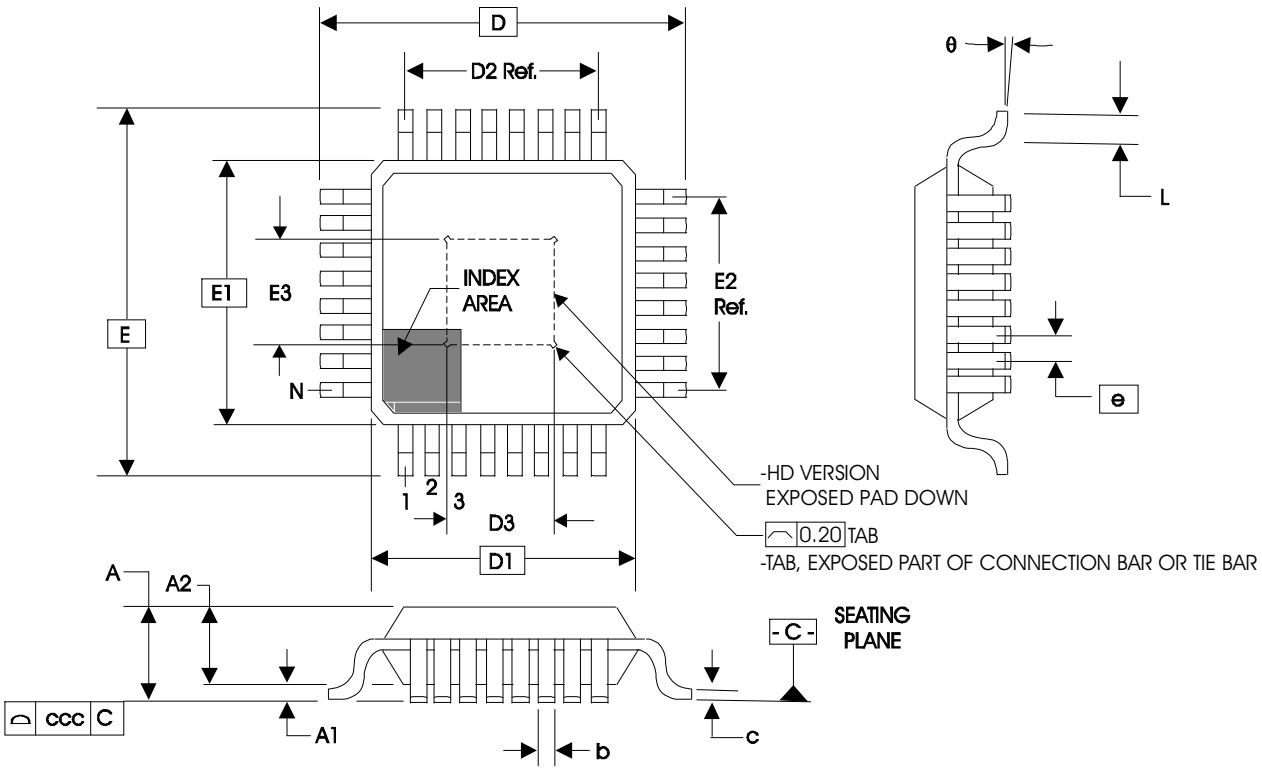



**Table 9. Package Dimensions 48L TQFP, EPAD**

| JEDEC Variation: ABC - HD<br>All Dimensions in Millimeters | | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| **N** | | 48 | |
| **A** | | | 1.20 |
| **A1** | 0.05 | 0.10 | 0.15 |
| **A2** | 0.95 | 1.00 | 1.05 |
| **b** | 0.17 | 0.22 | 0.27 |
| **c** | 0.09 | | 0.20 |
| **D & E** | | 9.00 Basic | |
| **D1 & E1** | | 7.00 Basic | |
| **D2 & E2** | | 5.50 Ref. | |
| **D3 & E3** | | 3.5 | |
| **e** | | 0.5 Basic | |
| **L** | 0.45 | 0.60 | 0.75 |
| θ | 0° | | 7° |
| **ccc** | | | 0.08 |

Reference Document: JEDEC Publication 95, MS-026

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8430S10BYI-02LF | ICS0S10BI02L | “Lead-Free” 48 TQFP, EPAD | Tray | -40°C to 85°C |
| 8430S10BYI-02LFT | ICS0S10BI02L | “Lead-Free” 48 TQFP, EPAD | Tape & Reel | -40°C to 85°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| B | T6 | 9<br>15 | AC Characteristics Table - added Lock Time parameter.<br>Added Lock Time measurement drawing. | 11/2/09 |
| C | T4F | 1<br>2<br>8<br>16<br>17<br>18<br>19<br>21 | Features section - corrected Differential Input bullet (deleted HCSL and LVHSTL levels).<br>Block Diagram - corrected naming convention for SPI4_SEL1:0 to SPI_SEL1:0.<br>Differential DC Characteristics Table - corrected VCMR levels from 0.5V min / $V_{DD}$ - 0.85V max to 1.2V min / $V_{DD}$ max.<br>Deleted *Power Supply Filtering Technique* application note (see Schematic Example). Updated *Wiring the Differential Input to Accept Single-ended Levels* application note.<br>Corrected *Differential Clock Input Interface* application note (deleted HCSL and LVHSTL levels).<br>Deleted *Crystal Input Interface* application note (see Schematic Example). Updated *Overdriving the XTAL Interface* application note.<br>Updated *LVDS Driver Termination* application note.<br>Updated *Schematic Example* application note and diagram. | 1/17/11 |
| | T9 | 28 | Corrected D3/E3 dimensions. Updated Package Outline. | |
| C | T10 | 29 | Ordering Information - Removed quantity in tape and reel. Deleted LF note below table.<br>Removed ICS from part number where needed.<br>Updated header and footer. | 10/4/16 |

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