

NXQ1TXA5

One-chip 5 V Qi wireless transmitter

Rev. 1.2 — 10 September 2015

Product short data sheet

1. General description

The NXQ1TXA5 is a controller/driver IC for a 5 V Qi-certified/compliant low-power wireless charger. It offers a fully integrated solution that includes a 5 V full-bridge power stage, as defined in Wireless Power Consortium (WPC) 5 V Qi standards A5, A11, A12 and A16.

The NXQ1TXA5 uses dedicated analog ping circuitry to detect devices, according to the Qi standard, achieving extremely low standby power consumption. If a Qi-compliant receiver is detected, the NXQ1TXA5 starts to communicate with it. If the receiver is recognized, it safely initiates wireless power transfer from the transmitter to the receiver, while monitoring for fault conditions such as overheating or interference from metal objects. The device is optimized to operate from a USB power supply and uses Smart Power Limiting (SPL) to adjust the output power automatically to compensate for power-limited supplies. The device supports Foreign Object Detection (FOD).

LED outputs and a buzzer output are available for the user interface. The LED outputs feature a number of blinking modes. Static Power Reduction (SPR) allows multiple NXQ1TXA5-based transmitters to operate from a single USB power supply by limiting power consumption per device.

The NXQ1TXA5 is available in a 5 mm × 5 mm, 32-pin HVQFN package.

2. Features and benefits

- One-chip WPC 1.1.2 Qi-compliant device for A5/A11/A12/A16 5 V single-coil low-power transmitter
- Operates from 5 V supply
- Integrated high-efficiency full-bridge power stage with low EMI radiation meeting EN55022 radiated and conducted emission limits
- Very few external components required, minimizing cost and board space
- Extremely low-power receiver detection circuitry; standby power 10 mW (typical)
- Power stage fully protected against overcurrents and overtemperature
- Fully integrated accurate coil current measurement
- Demodulates and decodes communication packages from Qi-compliant receivers
- PID regulation for closed-loop power drive and control
- Internal 1.8 V digital supply generation
- LED (×2) and buzzer outputs
- NTC input for external temperature check and protection
- On-chip thermal protection
- Small HVQFN 32-pin package (5 × 5 mm) with 0.5 mm pitch



- FOD with automatic switching between V1.1 and V1.0 for legacy receiver support
- FOD levels can be adjusted using external resistors to compensate for application differences to meet Qi certification requirements
- Smart Power Limiting (SPL) function to adapt to power-limited 5 V supplies
- Static Power Reduction (SPR) function to limit power consumption
- Supports Near Field Communication (NFC) TAG applications with delayed start-up

3. Applications

- Wireless Power Consortium (WPC) certified/compliant Qi wireless power transmitters

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DDP}	power supply voltage	on pins VDDP1 and VDDP2	3.5	-	5.25	V
I _{DDP}	power supply current	on pins VDDP1 and VDDP2				
		Ping mode (average current)	-	2	2.8	mA
		Power_Transfer mode (no load)	-	15	-	mA
		Power_Transfer mode (with load)	-	-	5	A

5. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
NXQ1TXA5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

5.1 Ordering options

Table 3. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum ordering quantity	Temperature
NXQ1TXA5	NXQ1TXA5/404J	HVQFN32	reel 7" Q1/T1, *standard mark SMD non-dry-pack	1500	T _{amb} = -20 °C to +85 °C

6. Block diagram

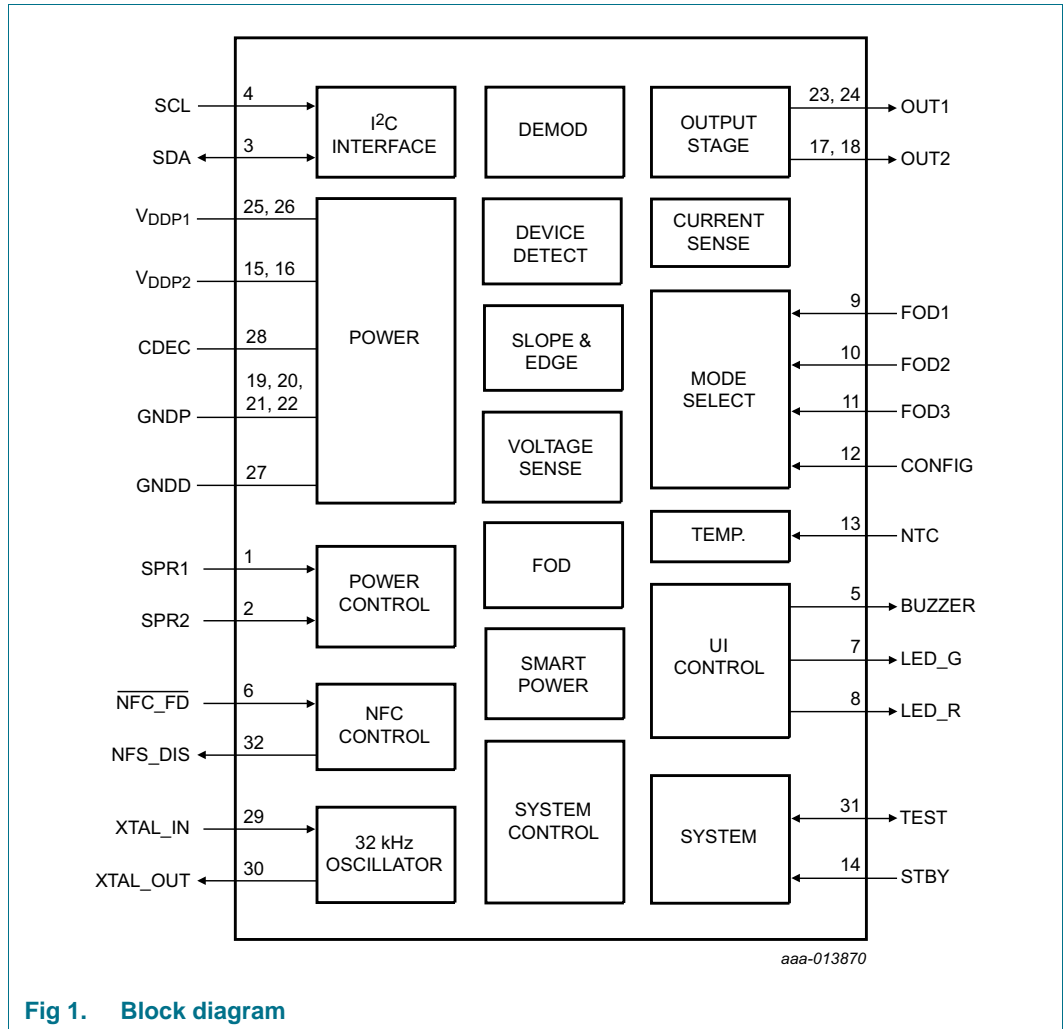
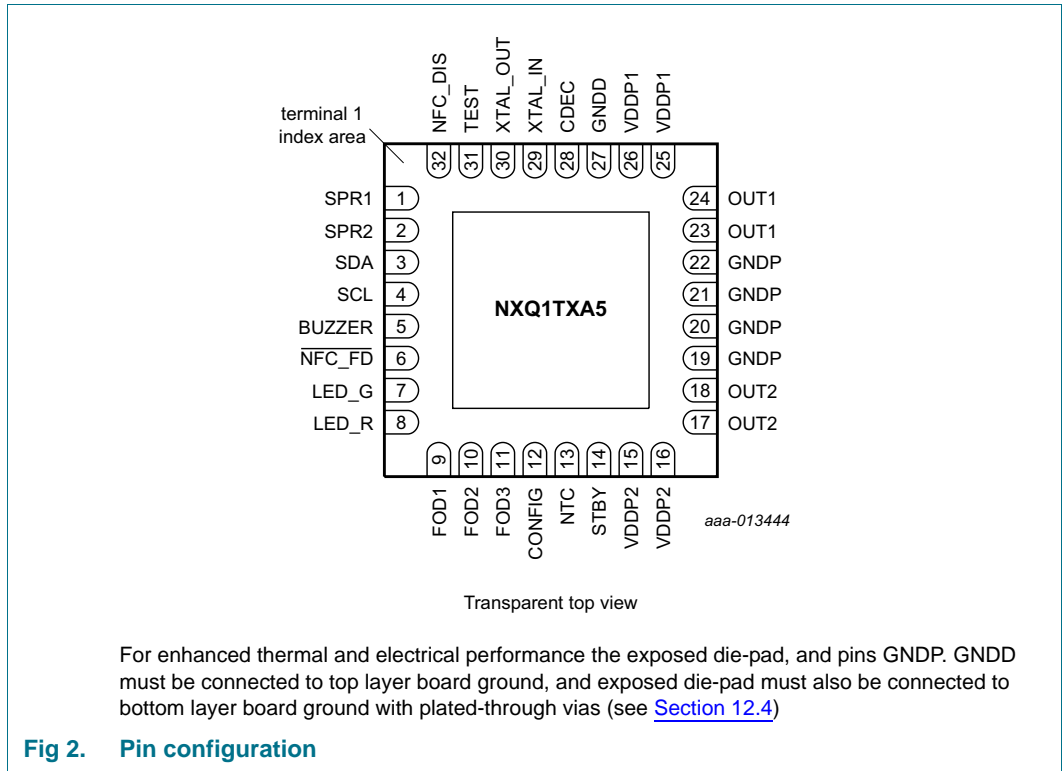


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
SPR1	1	I	static power reduction 1
SPR2	2	I	static power reduction 2
SDA	3	I/O	I ² C-bus data input/output; should be left open or grounded under normal operating conditions (I ² C-bus included for test purposes)
SCL	4	I	I ² C-bus clock input; should be left open or grounded under normal operating conditions (I ² C-bus included for test purposes)
BUZZER	5	O	buzzer output
NFC_FD	6	I	NFC field detect input (active LOW)
LED_G	7	O	green LED output
LED_R	8	O	red LED output
FOD1	9	I	FOD level configuration
FOD2	10	I	FOD loss configuration 1
FOD3	11	I	FOD loss configuration 2
CONFIG	12	I	LED and buzzer configuration
NTC	13	I	temperature measurement using NTC
STBY	14	I	standby function; connect to ground when not used

Table 4. Pin description^[1]...continued

Symbol	Pin	Type	Description
VDDP2	15, 16	P	power supply pin 2
OUT2	17, 18	O	transmitter output 2
GNDP ^[1]	19, 20, 21, 22	P	power ground
OUT1	23, 24	O	transmitter output 1
VDDP1	25, 26	P	power supply pin 1
GNDD ^[1]	27	P	digital ground
CDEC	28	P	decoupling connection for internal LDO
XTAL_IN	29	I	crystal input
XTAL_OUT	30	O	crystal output
TEST	31	I/O	test pin; connect to ground
NFC_DIS	32	O	NFC disable function

[1] For enhanced thermal and electrical performance, the exposed die-pad, and pins GNDP, GNDD must be connected to top layer board ground. The exposed die-pad must also be connected to bottom layer board ground with plated-through vias (see [Section 12.4](#)).

8. Functional description

8.1 Device operation

The NXQ1TXA5 is a 5 V wireless charger with an integrated full-bridge power stage. It integrates all the functions required to control the power transfer between a WPC-compliant Qi transmitter and a WPC-compliant Qi receiver efficiently. It can deliver up to 8 W continuous power into the WPC-compliant Qi type A5, A11, A12 or A16 transmitter coil.

A block diagram of the NXQ1TXA5 is shown in [Figure 1](#). It is operational when a 5 V supply is connected and pin STBY is LOW. Internal 1.8 V biasing is activated and the NXQ1TXA5 starts checking for a device on the transmitter base station. Power consumption is extremely low (typically 10 mW) during this phase. When a device is detected, the low-power DSP core starts up and sets up communications with the detected device. Power transfer is initiated if the device is identified as a WPC-compliant Qi receiver. The NXQ1TXA5 ensures that the correct power transfer level is maintained with frequency and duty cycle control according to the WPC Qi specifications.

The power transfer can be monitored via the LED and BUZZER outputs. The external temperature can be monitored via the NTC input to protect the application from overheating when charging Qi-V1.0 receivers that do not support Foreign Object Detection (FOD).

Additional inputs are provided to select the LED mode, configure FOD according to the application design and coil/capacitor selection, set the SPR level and enable/disable SPL.

8.2 Protection mechanisms

The following protection circuits are included in the NXQ1TXA5:

- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Foreign Object Detection (FOD)
- Negative Temperature Coefficient (NTC)

8.2.1 OverTemperature Protection (OTP)

8.2.1.1 Software OTP

A temperature protection circuit embedded in the NXQ1TXA5 keeps track of the temperature inside the device. If the temperature exceeds 110 °C, the output power is limited to prevent the device from being damaged. Normal power transfer is resumed when the temperature drops below 80 °C.

8.2.1.2 Hardware OTP

Additional hardware OTP is triggered when the junction temperature exceeds the temperature protection threshold of between 125 °C and 140 °C. When this happens, the output stages are set floating. Because the software OTP mechanism reacts at lower temperatures, it is expected that this additional hardware OTP is only triggered under abnormal load conditions. It acts as an extra safety mechanism.

8.2.2 OverCurrent Protection (OCP)

In the NXQ1TXA5, the power stages are protected against excessive currents. If the output current exceeds the maximum OCP threshold of 5 A, the output current is limited by reversing the current in the output stage that is drawing excessive current.

8.2.3 Foreign Object Detection (FOD)

The NXQ1TXA5 features FOD functionality according to the Qi 1.1.2 standard. If the received power level reported by the receiver is not in line with the transmitted power level measured by the NXQ1TXA5, the NXQ1TXA5 switches to FOD mode.

If the difference between reported (as perceived by the receiver) and transmitted power level is greater than the selected FOD threshold, the NXQ1TXA5 enters FOD mode. To avoid the heating up of metal objects placed between the transmitter and the receiver, power transfer is suspended in FOD mode.

8.2.4 Negative Temperature Coefficient (NTC)

The NTC input is used to monitor the voltage level on an external NTC resistor network. The NXQ1TXA5 stops delivering power if the input level on the NTC input pin drops below 0.8 V and starts charging again when the level rises above 1.1 V again. The NXQ1TXA5 automatically compensates for variations in the 5 V supply.

If the NXQ1TXA5 detects a voltage level below 150 mV on the NTC input pin when charging starts, the temperature sensing function via the NTC is disabled completely. A standard NTC input resistor network does not reach levels below 150 mV for normal operation. So, disabling the NTC temperature protection function can be done by connecting the NTC input pin to ground. The NTC input pin can also be connected to VDDP. As the sensing function then remains active and the input voltage level never drops below 0.8 V, the NXQ1TXA5 power delivery is not stopped. Disabling the NTC temperature sensing by connecting the NTC pin to ground is easier for a PCB layout.

The NTC input pin must always be connected to either the VDDP pin, ground, or the NTC network. It must never be left floating.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DDP}	power supply voltage	on pin VDDP1 and VDDP2	-0.3	+6.0	V
T _j	junction temperature		-	150	°C
T _{stg}	storage temperature		-55	+150	°C
T _{amb}	ambient temperature		-20	+85	°C
V _{ESD}	electrostatic discharge voltage	Human Body Model (HBM)	-2	+2	kV
		Charge Device Model (CDM)	-500	+500	V

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	2-layer application board positioned horizontally in free air; dimensions 45 mm × 45 mm × 0.8 mm; natural convection; copper coverage on each layer > 95 %; copper thickness each layer 70 μm	30	K/W

11. Characteristics

Table 7. DC characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, default settings unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{DDP}	power supply voltage	on pin VDDP1 and VDDP	3.5	-	5.25	V	
I _{DDP}	power supply current	on pins VDDP1 and VDDP2:					
		Ping mode (peak current)	[1]	-	1	-	A
		Ping mode (average current)	[1]	-	2	2.8	mA
		Standby mode (STBY HIGH)		-	2	30	μA
		Power_Transfer mode (no load)	[1]	-	15	-	mA
		Power_Transfer mode (average current with load)		-	-	2	A
		Power_Transfer mode (absolute peak current with load)	-	-	5	A	

[1] Current consumption in the NXQ1TXA5_SDS; no external load connected between terminals OUT1 and OUT2.

Table 8. AC characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, default settings unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
BTL power stage							
f _{sw}	switching frequency	Start-up and Power_Transfer modes	110	-	205	kHz	
f _{sw(step)}	switching frequency step size	Start-up and Power_Transfer modes	-	500	-	Hz	
δ	duty cycle	Start-up and Power_Transfer modes	0	-	50	%	
δ _{step}	duty cycle step size	Start-up and Power_Transfer modes	-	0.1	-	%	
STBY pin							
V _{IH}	HIGH-level input voltage	Standby mode	1.2	-	V _{DDP}	V	
V _{IL}	LOW-level input voltage	Operating mode	-	-	0.6	V	
FOD1, FOD2, FOD3, CONFIG and NTC pins							
V _I	input voltage	operating range	[1]	0	-	1.5	V
LED_G, LED_R and NFC_DIS outputs							
V _O	output voltage	set externally	400	-	V _{DDP}	mV	
I _{load}	load current	open-drain output	[2]	-	20	mA	
BUZZER output							
V _O	output voltage	set externally	400	-	V _{DDP}	mV	
I _{load}	load current	open-drain output	[2]	-	20	mA	
NFC_FD, SPR1 and SPR2 pins							
V _{IH}	HIGH-level input voltage		1	1.8	V _{DDP}	V	
V _{IL}	LOW-level input voltage		-	-	0.6	V	
I²C pins: SCL and SDA							
V _{IH}	HIGH-level input voltage		1	-	3.6	V	
V _{IL}	LOW-level input voltage		-	-	0.6	V	

Table 8. AC characteristics ...continued
 $T_{amb} = 25\text{ }^{\circ}\text{C}$, default settings unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator: pins XTAL_IN and XTAL_OUT						
V_I	input voltage		-	-	1.8	V
External crystal requirements						
f_{nom}	nominal frequency		32	32.768	33.5	kHz
D_L	drive level		-	-	1	μW
C_L	load capacitance	[3]	8	12	14	pF

- [1] The nominal operating range is from 0 V to 1.5 V. However, any level between 1.5 V and V_{DDP} has the same effect (as 1.5 V).
 [2] The output voltage at maximum load current is guaranteed not to exceed 400 mV.
 [3] The load capacitors are embedded in the NXQ1TXA5_SDS.

12. Application information

12.1 Crystal oscillator

The NXQ1TXA5 uses an external low-cost 32.768 kHz crystal, with a 1 % accuracy. The crystal should support a load capacitance of $\approx 12\text{ pF}$ (the load capacitance is embedded in the NXQ1TXA5). Do not connect the crystal to the NXQ1TXA5 using vias, but directly on the top layer of the PCB. If possible, shield the crystal by connecting the casing to ground. The crystal is connected to the oscillator input pin (XTAL_IN) via a 2.2 pF series capacitor.

12.2 Supply decoupling

Effective supply decoupling is required. The decoupling capacitors must to be chosen such that the effective capacitance is at least $10\text{ }\mu\text{F}$ at a DC bias voltage of 5.5 V and a frequency of 205 kHz for each supply pin. To improve HF behavior and reduce EMI, mount smaller (10 nF) high-quality capacitors in parallel with the larger capacitors.

12.3 Snubber network

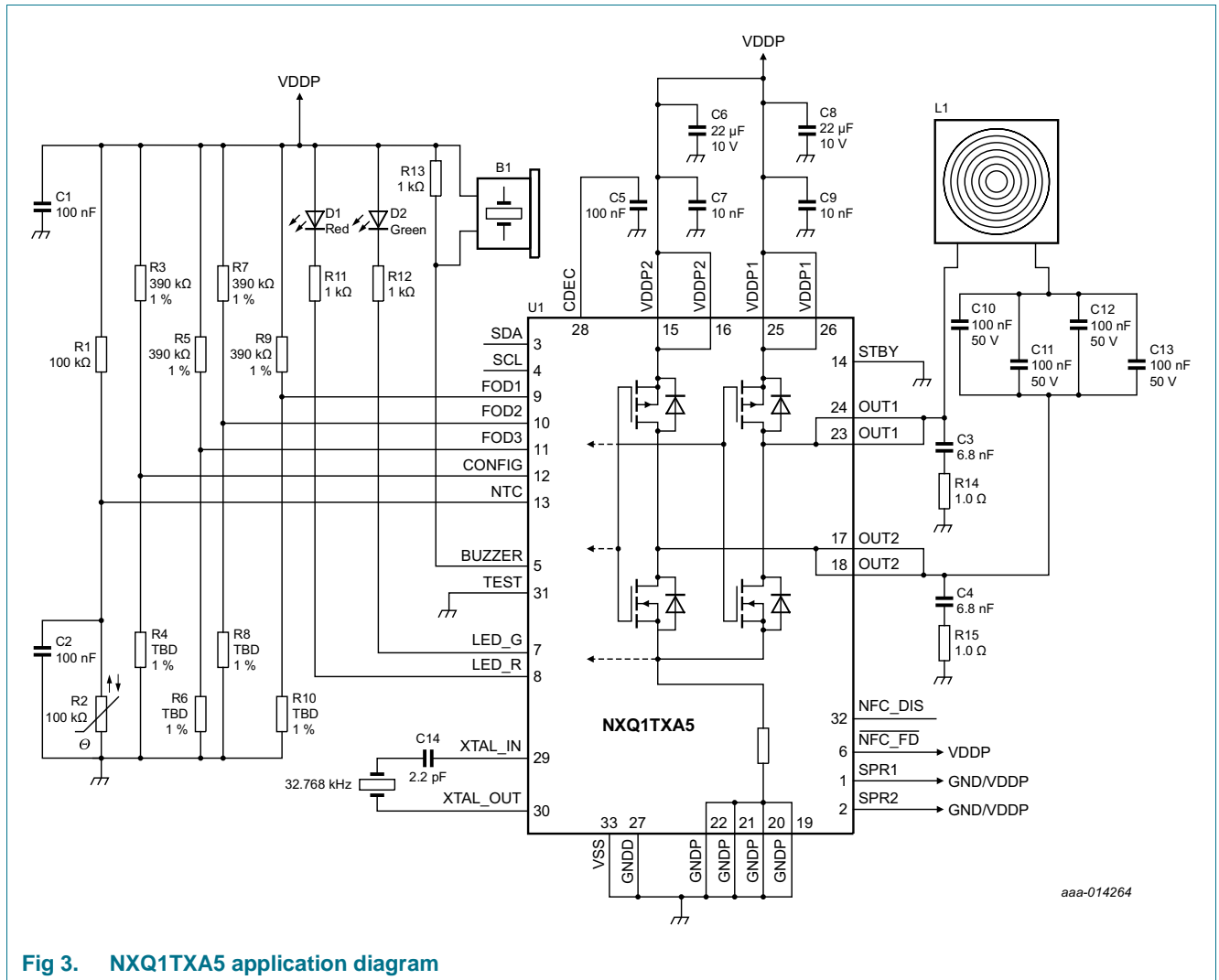
Snubber RC networks are connected to outputs OUT1 and OUT2. Each snubber network consists of a 6.8 nF capacitor in series with a $1\text{ }\Omega$ resistor to ground (see [Figure 3](#)).

12.4 Exposed die-pad ground and thermal connection

For optimal thermal and electrical performance, the device bottom exposed die-pad MUST be soldered to a PCB solder land under the exposed die-pad. To have good electrical contact and thermal flow from the device to the bottom copper layer, the PCB solder land under the device MUST be connected with plated-through vias to the copper bottom layer of the PCB. In this way, the PCB bottom copper layer can provide heat sinking for the device dissipation.

In the NXQ1TXA5 application note examples are provided for recommended layouts with good thermal and electrical performance.

12.5 Application diagram



aaa-014264

Fig 3. NXQ1TXA5 application diagram

13. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

SOT617-3

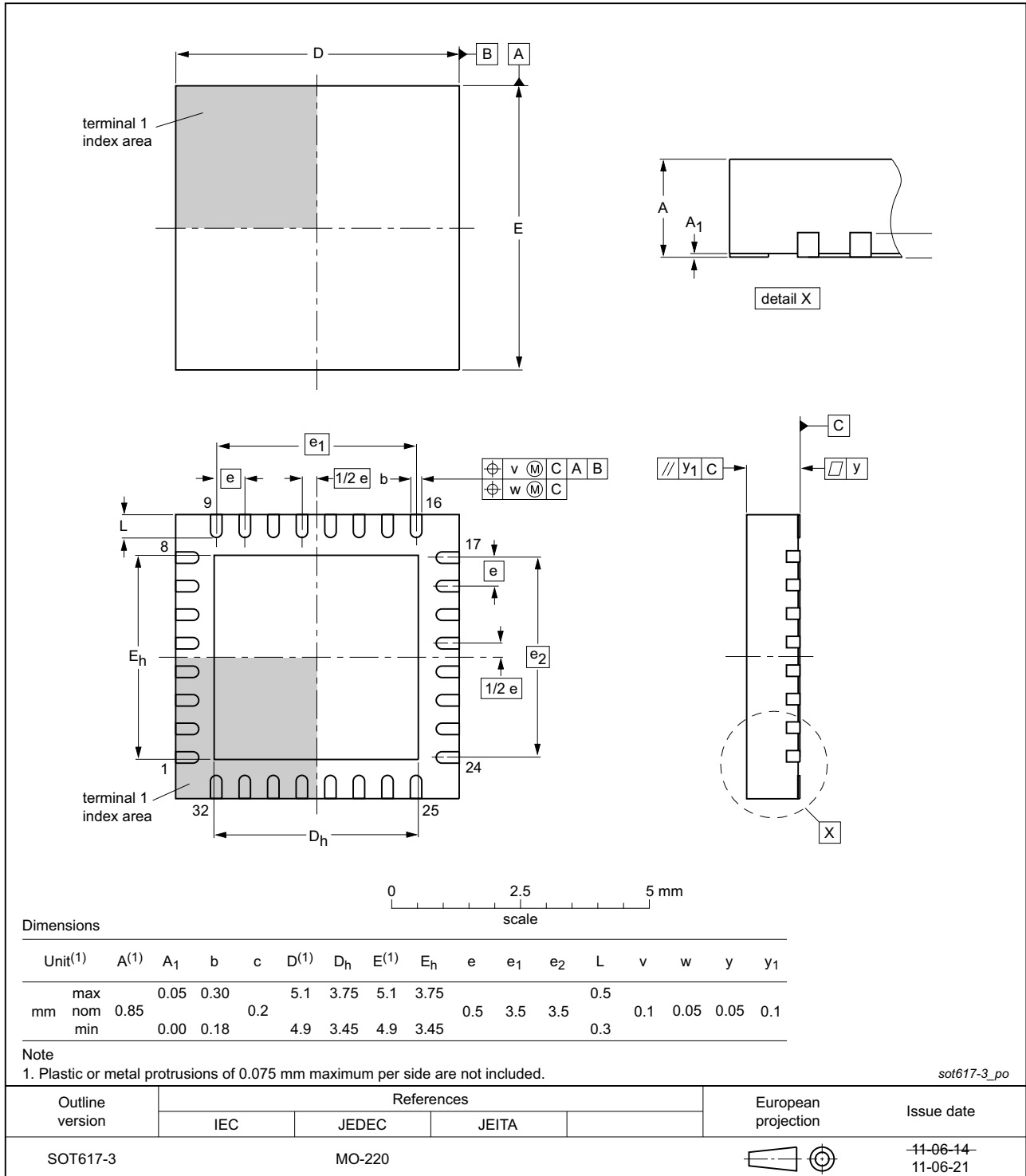


Fig 4. Package outline SOT617-3 (HVQFN32)

14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXQ1TXA5_SDS v.1.2	20150910	Product data sheet	-	NXQ1TXA5_SDS v.1.1
Modifications:	• Section 13 "Package outline" has been updated.			
NXQ1TXA5_SDS v.1.1	20150909	Product data sheet	-	NXQ1TXA5_SDS v.1
NXQ1TXA5_SDS v.1	20150730	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Quick reference data	2
5	Ordering information	2
5.1	Ordering options	2
6	Block diagram	3
7	Pinning information	4
7.1	Pinning	4
7.2	Pin description	4
8	Functional description	5
8.1	Device operation	5
8.2	Protection mechanisms	6
8.2.1	OverTemperature Protection (OTP)	6
8.2.1.1	Software OTP	6
8.2.1.2	Hardware OTP	6
8.2.2	OverCurrent Protection (OCP)	6
8.2.3	Foreign Object Detection (FOD)	6
8.2.4	Negative Temperature Coefficient (NTC)	7
9	Limiting values	7
10	Thermal characteristics	7
11	Characteristics	8
12	Application information	9
12.1	Crystal oscillator	9
12.2	Supply decoupling	9
12.3	Snubber network	9
12.4	Exposed die-pad ground and thermal connection	9
12.5	Application diagram	10
13	Package outline	11
14	Revision history	12
15	Legal information	13
15.1	Data sheet status	13
15.2	Definitions	13
15.3	Disclaimers	13
15.4	Trademarks	14
16	Contact information	14
17	Contents	15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 September 2015

Document identifier: NXQ1TXA5_SDS