MLX90363

Triaxis® Magnetometer IC
With High Speed Serial Interface

Features and Benefits

- ☐ Tria⊗is® Magnetometer (B_X, B_Y, B_Z)
- ☐ On Chip Signal Processing for Robust Position Sensin
- ☐ High Speed Serial Interface (SPI compatible – Full Duplex)
- ☐ Enhanced Self-Diagnostics Features
- ☐ 5V and 3V3 Application Compatible
- ☐ 14 bit Output Resolution
- ☐ 48 bit ID Number
- ☐ Single Die – SO8 Package RoHS Compliant
- ☐ Dual Die (Full Redundant) – TSSOP16 Package RoHS Compliant

Applications

- ☐ Absolute Contactless Position Sensor

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90363	K	DC	ABB-000	RE
MLX90363	K	DC	ABB-000	TU
MLX90363	K	GO	ABB-000	RE
MLX90363	K	GO	ABB-000	TU
MLX90363	E	DC	ABB-000	RE
MLX90363	E	DC	ABB-000	TU
MLX90363	E	GO	ABB-000	RE
MLX90363	E	GO	ABB-000	TU
MLX90363	L	DC	ABB-000	RE
MLX90363	L	DC	ABB-000	TU
MLX90363	L	GO	ABB-000	RE
MLX90363	L	GO	ABB-000	TU

Legend:

Temperature Code:	L for Temperature Range - 40℃ to 150℃, K for Temperature Range - 40℃ to 125℃, E for Temperature Range - 40℃ to 85℃.
Package Code:	DC for SOIC-8, GO for TSSOP-16.
Option Code:	xxx-000: Standard version
Packing Form:	RE for Reel TU for Tube

Ordering example: MLX90363LGO-ABB-000-TU

1. Functional Diagram

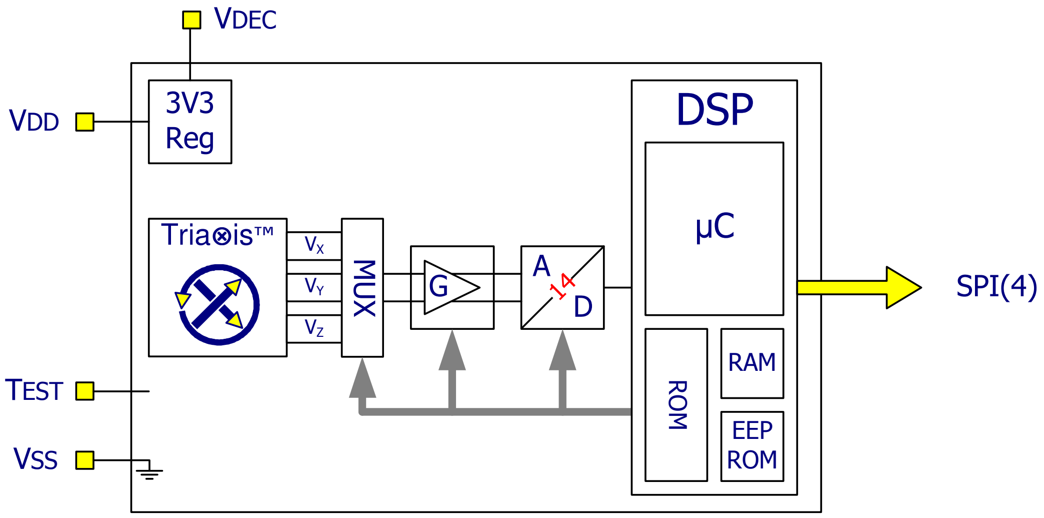

Figure 1 – Block Diagram

2. Description

The MLX90363 is a monolithic magnetic sensor IC featuring the Tria⊗is® Hall technology. Conventional planar Hall technology is only sensitive to the flux density applied orthogonally to the IC surface. The Tria⊗is® Hall sensor is also sensitive to the flux density applied parallel to the IC surface. This is obtained through an Integrated Magneto-Concentrator (IMC®) which is deposited on the CMOS die .

The MLX90363 is sensitive to the three (3) components of the flux density applied to the IC (i.e. B_X, B_Y and B_Z). This allows the MLX90363 to sense any magnet moving in its surrounding and decode its position through an appropriate signal processing.

Using its Serial Interface the MLX90363 can transmit a digital output (SP – 64 bits per frame).

The MLX90363 is intended for Embedded Position Sensor applications (vs. Stand-Alone “Remote” Sensor) for which the output is directly provided to a microcontroller (Master) close to the magnetometer IC MLX90363 (Slave). The SPI protocol confirms this intent.

The MLX90363 is using full duplex SPI protocol and requires therefore the separated SPI signal lines: MOSI, MISO, /SS and SLCK[1].

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[1] The MLX90316 multiplexes the MOSI/MISO lines. The application diagrams of the MLX90363 and MLX90316 are therefore not compatible.

TABLE of CONTENTS

FEATURES AND BENEFITS 1
APPLICATIONS 1
1. FUNCTIONAL DIAGRAM 2
2. DESCRIPTION 2
3. GLOSSARY OF TERMS – ABBREVIATIONS – ACRONYMS 5
4. PINOUT 5
5. PIN DESCRIPTION 6
6. ABSOLUTE MAXIMUM RATINGS 6
7. DETAILED DESCRIPTION 7
8. MLX90363 ELECTRICAL SPECIFICATION 8
9. MLX90363 ISOLATION SPECIFICATION 8
10. MLX90363 TIMING SPECIFICATION 9
10.1. TIMING SPECIFICATION FOR 5V APPLICATION DIAGRAM 9
10.2. TIMING SPECIFICATION FOR 3V3 APPLICATION DIAGRAM 10
11. MLX90363 ACCURACY SPECIFICATION 11
12. MLX90363 MAGNETIC SPECIFICATION 13
13. MLX90363 CPU & MEMORY SPECIFICATION 13
14. MLX90363 SERIAL INTERFACE 14
14.1. ELECTRICAL LAYER AND TIMING SPECIFICATION 14
14.2. SERIAL PROTOCOL 16
14.3. MESSAGE GENERAL STRUCTURE 16
14.4. REGULAR MESSAGES 18
14.4.1. Note for the regular message “X – Y – Z – diagnostic” (Marker = 2) *18*
14.5. TRIGGER MODE 1 19
14.6. TRIGGER MODE 2 21
14.7. TRIGGER MODE 3 22
14.8. TRIGGER MODES TIMING SPECIFICATIONS 23
14.9. OPCODE TABLE 26
14.10. TIMING SPECIFICATIONS PER OPCODE, AND NEXT ALLOWED MESSAGES 26
14.11. NOP COMMAND AND NOP ANSWER 27
14.12. OSCCOUNTERSTART AND OSCCOUNTERSTOP COMMANDS 27
14.13. PROTOCOL ERRORS HANDLING 29
14.14. READY, ERROR AND NTT MESSAGES 30
14.15. DIAGNOSTICSDETAILS COMMANDS 31
14.16. MEMORYREAD MESSAGE 32
14.17. EEPROMWRITE MESSAGE 33
14.18. REBOOT 35
14.19. STANDBY 35
14.20. START-UP SEQUENCE (SERIAL COMMUNICATION) 36
14.21. ALLOWED SEQUENCES 37
15. MLX90363 TRACEABILITY INFORMATION 38
16. MLX90363 END-USER PROGRAMMABLE ITEMS 38

17. MLX90363 DESCRIPTION OF END-USER PROGRAMMABLE ITEMS 39
17.1. USER CONFIGURATION: DEVICE ORIENTATION 39
17.2. USER CONFIGURATION: MAGNETIC ANGLE FORMULA 39
17.3. USER CONFIGURATION: 3D=0 FORMULA TRIMMING PARAMETERS SMISM AND ORTH_B1B2 39
17.3.1. Magnetic Angle ∠XY 39
17.3.2. Magnetic Angle ∠XZ and ∠YZ 40
17.4. USER CONFIGURATION: 3D=1 FORMULA TRIMMING PARAMETERS KALPHA, KBETA, KT 40
17.5. USER CONFIGURATION: FILTER 41
17.6. VIRTUAL GAIN MIN AND MAX PARAMETERS 41
17.7. HYSTERESIS FILTER 42
17.8. EMC FILTER ON SCI PINS 42
17.9. IDENTIFICATION & FREE BYTES 42
17.10. LOCK 42
18. MLX90363 SELF DIAGNOSTIC 43
19. MLX90363 FIRMWARE FLOWCHARTS 44
19.1. START-UP SEQUENCE 44
19.2. SIGNAL PROCESSING (GETX) 45
19.3. FAIL-SAFE MODE 45
19.4. AUTOMATIC GAIN CONTROL 46
20. RECOMMENDED APPLICATION DIAGRAMS 47
20.1. MLX90363 IN SOIC-8 PACKAGE AND 5V APPLICATION DIAGRAMS 47
20.2. MLX90363 IN SOIC-8 PACKAGE AND 3V3 APPLICATION DIAGRAMS 47
20.3. MLX90363 IN TSSOP-16 PACKAGE AND 5V APPLICATION DIAGRAMS 48
20.4. MLX90363 IN TSSOP-16 PACKAGE AND 3V3 APPLICATION DIAGRAMS 49
21. STANDARD INFORMATION REGARDING MANUFACTURABILITY OF MELEXIS PRODUCTS WITH DIFFERENT SOLDERING PROCESSES 50
22. ESD PRECAUTIONS 50
23. PACKAGE INFORMATION 51
23.1. SOIC8 – PACKAGE DIMENSIONS 51
23.2. SOIC8 – PINOUT AND MARKING 52
23.3. SOIC8 – IMC POSITIONNING 53
23.4. TSSOP16 – PACKAGE DIMENSIONS 54
23.5. TSSOP16 – PINOUT AND MARKING 55
23.6. TSSOP16 – IMC POSITIONNING 55
24. DISCLAIMER 57

3. Glossary of Terms – Abbreviations – Acronyms

- Gauss (G), Tesla (T): Units for the magnetic flux density – 1 mT = 10 G
- TC: **T**emperature **C**oefficient (in ppm/Deg.C.)
- NC: **N**ot **C**onnected
- Byte: 8 bits
- Word: 16 bits (= 2 bytes)
- ADC: **A**nalog-to-**D**igital **C**onverter
- LSB: **L**east **S**ignificant **B**it
- MSB: **M**ost **S**ignificant **B**it
- DNL: **D**ifferential **N**on-**L**inearity
- INL: **I**ntegral **N**on-**L**inearity
- RISC: **R**educed **I**nstruction **S**et **C**omputer
- ASP: **A**nalog **S**ignal **P**rocessing
- DSP: **D**igital **S**ignal **P**rocessing
- ATAN: trigonometric function: arctangent (or inverse tangent)
- IMC: **I**ntegrated **M**agneto-**C**oncentrator (IMC®)
- CoRDiC: **Co**ordinate **R**otation **Di**gital **C**omputer (i.e. iterative rectangular-to-polar transform)
- EMC: **E**lectro-**M**agnetic **C**ompatibility
- FE: **F**alling **E**dge
- RE: **R**ising **E**dge
- MSC: **M**essage **S**equence **C**hart
- FW: **F**irm**w**are
- HW: **H**ard**w**are

4. Pinout

Pin #	SOIC-8	TSSOP-16
1	VDD	VDEC$_1$
2	MISO	VSS$_1$ (Ground$_1$)
3	Test	VDD$_1$
4	SCLK	MISO$_1$
5	/SS	Test$_2$
6	MOSI	SCLK$_2$
7	VDEC	/SS$_2$
8	VSS (Ground)	MOSI$_2$
9		VDEC$_2$
10		VSS$_2$ (Ground$_2$)
11		VDD$_2$
12		MISO$_2$
13		Test$_1$
14		SCLK$_1$
15		/SS$_1$
16		MOSI$_1$

For optimal EMC behavior, it is recommended to connect the unused pins (Test) to the Ground (see section 19).

5. Pin Description

Name	Direction	Type	Function / Description
VDD	VDD	Analog	Supply (5V and 3V3 application diagrams)
MISO	OUT	Digital	Master In Slave Out
Test	I/O	Both	Test Pin
SCLK	IN	Digital	Clock
/SS	IN	Digital	Slave Select
MOSI	IN	Digital	Master Out Slave IN
VDEC	I/O	Analog	5V Application Diagrams Decoupling Pin 3V3 Application Diagrams Supply (Shorted to VDD)
VSS (Ground)	GND	Analog	Ground

6. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, VDD[2]	+ 18 V
Reverse VDD Voltage	– 0.3 V
Supply Voltage, VDEC	+ 3.6 V
Reverse VDEC Voltage	– 0.3 V
Positive Input Voltage	+ 11 V
Reverse Input Voltage	– 11 V
Positive Output Voltage	VDD + 0.3 V
Reverse Output Voltage	– 0.3 V
Operating Ambient Temperature Range, T_A	– 40°C … + 150°C
Storage Temperature Range, T_S	– 40°C … + 150°C
Magnetic Flux Density	± 700 mT

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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[2] Maximum rise time: 10µs. Rise time faster than 10µs might induce an extra current consumption.

7. Detailed Description

The three components of the applied flux density are measured through the Tria⊗is front end:

$$V_X \propto B_X$$
$$V_Y \propto B_Y$$
$$V_Z \propto B_Z$$

Those three (3) Hall voltages corresponding to the three (3) components of the applied flux density are provided to the ADC (Analog-to-Digital Converter). The Hall signals are processed through a fully differential analog chain featuring the classic offset cancellation technique (Hall plate 2-Phases spinning and chopper-stabilized amplifier).

The amplitude of V_Z is smaller than the two (2) components V_X and V_Y due to the fact that the magnetic gain of the IMC only affects the components parallel to the IC surface.

The conditioned analog signals are converted through a 14 bit ADC and provided to a DSP block for further processing. The DSP stage is based on a 16 bit RISC micro-controller whose primary function is the extraction of the position information (magnetic angle(s)) from the raw signals (after front-end compensation steps) through one the following operations:

$$\alpha = ATAN\left(\frac{k \cdot V_1}{V_2}\right)$$

where $V_1 = V_X$ or V_Y or V_Z , $V_2 = V_X$ or V_Y or V_Z and k (or SMISM) is a programmable factor to match the amplitude of k V_1 and V_2.

$$\alpha = ATAN\left(\frac{\sqrt{(k_\alpha V_3)^2 + (k_t V_2)^2}}{V_1}\right) \text{ and } \beta = ATAN\left(\frac{\sqrt{(k_\beta V_3)^2 + (k_t V_1)^2}}{V_2}\right)$$

where $V_1 = V_X$ or V_Y or V_Z, $V_2 = V_X$ or V_Y or V_Z, $V_3 = V_X$ or V_Y or V_Z and $k_{\alpha,}$ k_β and k_t are programmable parameters.

The DSP functionality is governed by the micro-code (firmware – FW) of the micro-controller which is stored into the ROM (mask programmable). In addition to the “ATAN” (“Arctangent”) function, the FW controls the whole analog chain, the programming/calibration and also the self-diagnostic modes.

Due to the fact that the “ATAN” operation is performed on the ratios “V_1/V_2”, “V_3/V_1” and “V_3/V_2”, the output is intrinsically self-compensated vs. flux density variations (due to airgap change, thermal or ageing effects) affecting both signals. This feature allows an improved thermal accuracy compared to a conventional linear Hall sensor.

The end-user programmable parameters are stored in EEPROM featuring a Hamming Error Correction Coding (ECC).

The programming steps do not require dedicated pins or programming tool. The operation is performed through the Master and the Serial Protocol using a dedicated and protected function(3).

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[3] For debug/demo purpose, Melexis can provide the Melexis Programming Unit PTC-04 with the SPI daughterboard (PTC-04-DB-SPI) and software library (PSF – Product Specific Functions).

8. MLX90363 Electrical Specification

DC Operating Parameters at VDD = 5V (5V Application Diagram) or VDD = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	VDD5	5V Application Diagram	4.5	5	5.5	V
Nominal Supply Voltage	VDD33	3V3 Application Diagram	3.15	3.3	3.45	V
Supply Current (4)	IDD			12.5	15.5	mA
Standby Current	ISTANDBY			3.5	4.5	mA
Supply Current at VDD MAX	IDDMAX	VDD = 18V			18	mA
POR Rising Level	POR LH	Voltage referred to VDEC	2.6	2.8	3.1	V
POR Falling Level	POR HL	Voltage referred to VDEC	2.5	2.7	2.9	V
POR Hysteresis	POR Hyst	Voltage referred to VDEC		0.1		V
MISO Switch Off Rising Level	MT8V LH	VDD level for disabling MISO(5)	7.5		9.5	V
MISO Switch Off Falling Level	MT8V HL	VDD level for disabling MISO(5)	6		7.5	V
MISO Switch Off Hysteresis	MT8V Hyst	VDD level for disabling MISO(5)	1		2	V
Input High Voltage Level	VIH		65%*VDD	-	-	V
Input Low Voltage Level	VIL		-	-	35%*VDD	V
Input Hysteresis	VHYS			20%*VDD		V
Input Capacitance	CIN	Referred to GND		20		pF
Output High Voltage Level	VOH	Current Drive IOH = 0.5 mA	VDD-0.4			V
Output Low Voltage Level	VOL	Current Drive IOH = 0.5 mA			0.4	V
Output High Short Circuit Current	I_{shortH}	VOUT forced to 0V		20	30	mA
Output Low Short Circuit Current	I_{shortL}	VOUT forced to VDD		25	30	mA

9. MLX90363 Isolation Specification

Only valid for the package code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between 2 dies	4			MΩ

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[4] For the dual version, the supply current is multiplied by 2

[5] Above the MT8V threshold, no SPI communication is possible.

10. MLX90363 Timing Specification

10.1. Timing Specification for 5V Application Diagram

DC Operating Parameters at VDD = 5V and for T_A as specified by the Temperature suffix (E, K)[6].

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck		15.2		18.8	MHz
Frame Rate	FR	Trigger Mode 1 (Trg. Mod. 1), Markers 0&2, SCI 2MHz All other modes, markers and SCI Frequencies			1000 500	s^{-1} s^{-1}
Watchdog time-out	Wd	See Section 18	15.3	18.8	20	ms
Power On to First *SCI* message (Start-up Time)	tStartUp	See Section 14.20	20			ms
SCI protocol: Slave-select rising-edge to falling-edge	tShort		120			us
SCI protocol: EEPROMWrite Time	teewrite	Trimmed oscillator	32			ms
Diagnostic Loop Time	tDiag	FR = 1000 s^{-1},Trg.Mod.1, Mark 0&2 FR = 500 s^{-1} FR = 200 s^{-1}			40 20 10	ms ms ms
Internal 1MHz signal	t1us	Ck = 19MHz		1		us
MISO Rise Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
MISO Fall Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
Magnetic Flux Density Frequency		Sinewave Flux Density(7) FR = 1000 s^{-1} FR = 500 s^{-1} FR = 100 s^{-1}			 4 8 18	 Hz Hz Hz
		FR = 1000 s^{-1}(8) FR = 500 s^{-1}(8) FR = 200 s^{-1}(8)			28 14 5.6	Hz Hz Hz

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[6] Please contact Melexis for Timing specification for "L" Temperature suffix

[7] Sensitivity monitors enable (See section 18). Beyond that frequency, the Sensitivity monitor should be disabled.

[8] Limitation linked to the Automatic Gain Control. Beyond that frequency, there is a reduced immunity to norm change (like vibration). See also Section 19.4.

10.2. Timing Specification for 3V3 Application Diagram

DC Operating Parameters at V_{DD} = 3.3V and for T_A as specified by the Temperature suffix (E, K)[9].

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck		13.1		18.8	MHz
Frame Rate	FR	Trigger Mode 1 (Trg. Mod. 1), Markers 0&2, SCI 2MHz All other modes, markers and SCI Frequencies			862 430	s^{-1} s^{-1}
Watchdog time-out	Wd	See Section 18	15.3		23.2	ms
Power On to First *SCI* message (Start-up Time)	tStartUp	See Section 14.20	23.2			ms
SCI protocol: Slave-select rising-edge to falling-edge	tShort		139			us
SCI protocol: EEPROMWrite Time	teewrite	3.3V Trimmed oscillator	37			ms
Diagnostic Loop Time	tDiag	FR = 862 s^{-1},Trg.Mod.1, Mark 0&2 FR = 430 s^{-1} FR = 215 s^{-1}			46.4 23.2 11.6	ms ms ms
Internal 1MHz signal	t1us	Ck = 19MHz		1		us
MISO Rise Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
MISO Fall Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
Magnetic Flux Density Frequency		FR = 862 s^{-1}(10) FR = 430 s^{-1}(10) FR = 215 s^{-1}(10)			24 12 4.8	Hz Hz Hz

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[9] Please contact Melexis for Timing specification for "L" Temperature suffix.

[10] Limitation linked to the Automatic Gain Control. Beyond that frequency, there is a reduced immunity to norm change (like vibration). See also Section 19.4.

11. MLX90363 Accuracy Specification

DC Operating Parameters at V_{DD} = 5V (5V Application Diagram) or V_{DD} = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals X, Y and Z	R_{ADC}			14		bit
Serial Interface Resolution	R_{SI}	On the angle value On the X,Y,Z values		14 12		bit bit
Offset on the Raw Signals X, Y and Z	X0, Y0, Z0	T_A = 25°C	-30		+30	LSB_{14}
Mismatch on the Raw Signals X, Y and Z	$SMISM_{XY}$ $SMISM_{XZ}$ $SMISM_{YZ}$	T_A = 25°C Between X and Y Between X and Z(11) Between Y and Z(11)	-1 -30 -30		1 +30 +30	% % %
Magnetic Angle Phase Error	$ORTH_{XY}$ $ORTH_{XZ}$ $ORTH_{YZ}$	T_A = 25°C Between X and Y Between X and Z(12) Between Y and Z(12)	-0.3 -10 -10		0.3 10 10	Deg Deg Deg
Intrinsic Linearity Error(13)	Le	T_A = 25°C, Magnetic Angle ∠XY Magnetic Angle ∠XZ, ∠YZ(14)	-1 -20		1 20	Deg Deg
Supply Dependency		5V Application Diagram V_{DD} = 4.5 … 5.5V	-0.1		0.1	Deg
		3V3 Application Diagram V_{DD} = 3.20 … 3.40V Temperature suffix E and K 20mT 50mT Temperature suffix L 20mT 50mT	-0.8 -0.4 -1 -0.6		0.8 0.4 1 0.6	Deg Deg Deg Deg
MLX90363 Accuracy Specification continues…						

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[11] The Mismatch between X or Y and Z can be reduced through the calibration of the SMISM (or k) factor in the end application. See section 17.3.2 for more information

[12] The Magnetic Angle Phase error X or Y and Z can be reduced through the calibration of the ORTH_B1B2 factor in the end application. See section 17.3.2 for more information

[13] The Intrinsic Linearity Error is a consolidation of the IC errors (offset, sensitivity mismatch, phase error) taking into account an ideal rotating field. Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases.

[14] The Intrisic Linearity Error for Magnetic Angle ∠XZ, ∠YZ can be reduced through the programming of the SMISM (or k) factor and ORTH_B1B2. By applying the correct compensation, a non linearity error of +/-1 deg can be reached. See section 17.3.2 for more information

… MLX90363 Accuracy Specification

Thermal Offset Drift(15)		Temperature suffix E and K Temperature suffix L	-30 -45		+30 +45	LSB_{14} LSB_{14}
Thermal Drift of Sensitivity Mismatch(16)		XY axis, XZ axis, YZ axis Temperature suffix E and K Temperature suffix L	 - 0.5 - 0.7		 + 0.5 + 0.7	 % %
Thermal Drift of Magnetic Angle Phase Error		XY axis, XZ axis, YZ axis	0.1		0.1	Deg
Magnetic Angle Noise(17)		Temperature suffix E and K 20mT, No Filter 50mT, No Filter 50mT, FILTER=1 Temperature suffix L 20mT, No Filter 50mT, No Filter 50mT, FILTER=1			 0.20 0.10 0.07 0.25 0.12 0.08	 Deg Deg Deg Deg Deg Deg
Raw signals X, Y, Z Noise(17)		Temperature suffix E and K 20mT, No Filter 50mT, No Filter 50mT, FILTER_TYPE =1 Temperature suffix L 20mT, No Filter 50mT, No Filter 50mT, FILTER=1			 12 6 4 14 7 4	 LSB_{14} LSB_{14} LSB_{14} LSB_{14} LSB_{14} LSB_{14}

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[15] For instance, Thermal Offset Drift equal ± 30LSB_{14} yields to max. ± 0.32 Deg. error. This is only valid if the Virtual Gain is not fixed (See Section 17.6).See Front End Application Note for more details.

[16] For instance, Thermal Drift of Sensitivity Mismatch equal ± 0.4% yields to max. ± 0.1 Deg. error. See Front End Application Note for more details.

[17] Noise is defined by ± 3 σ for 1000 successive acquisitions. The application diagram used is described in the recommended wiring (Section 20). For detailed information, refer to section Filter in application mode (Section 17.5).

12. MLX90363 Magnetic Specification

DC Operating Parameters at VDD = 5V (5V Application Diagram) or VDD = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density in X or Y	B_{XY}(18)		20	50	70(19)	mT
Magnetic Flux Density in Z	B_Z(18)		24	75	126	mT
Magnet Temperature Coefficient	TCm		-2400		0	ppm/°C
IMC Gain(20)	GainIMC		1.2	1.4	1.8	

13. MLX90363 CPU & Memory Specification

The digital signal processing is based on a 16 bit RISC µController featuring

- ROM & RAM
- EEPROM with hamming codes (ECC)
- Watchdog
- C Compiler

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				14		kByte
RAM				256		Byte
EEPROM				64		Byte
CPU MIPS		Ck = 15 MHz		3.5		MIPS

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[18] The condition must be fulfilled for at least one field B_X, B_Y or B_Z.

[19] Above 70 mT, the IMC starts saturating yielding an increase of the linearity error.

[20] This is the magnetic gain linked to the Integrated Magneto Concentrator structure. It applies to B_X and B_Y and not to B_Z. This is the overall variation. Within one lot, the part to part variation is typically ± 10% versus the average value of the IMC gain of that lot.

14. MLX90363 Serial Interface

The MLX90363 serial interface allows a master device to operate the position sensor. The MLX90363 interface allows multi-slave applications and synchronous start of the data acquisition among the slaves. The interface offers 2 Mbps data transfer bit rate and is full duplex. The interface accepts messages of 64 bits wide only, making the interfacing robust.
In this document, the words *message*, *frame* and *packet* refer to the same concept.

14.1. Electrical Layer and Timing Specification

Message transmissions start necessarily at a falling edge on */SS* and end necessarily at a rising edge on the */SS* signal. This defines a message. The serial interface counts the number of transmitted bits and declares the incoming message invalid when the bit count differs from 64. The master must therefore ensure the flow described below:

1. Set pin */SS* Low
2. Send and receive 8 bytes or four (4x) 16 bit words
3. Set pin */SS* High

The *MISO* and *MOSI* signals change on *SCLK* rising edge and are captured on *SCLK* falling edge. The most-significant-bit of the transmitted byte or word comes first [21].

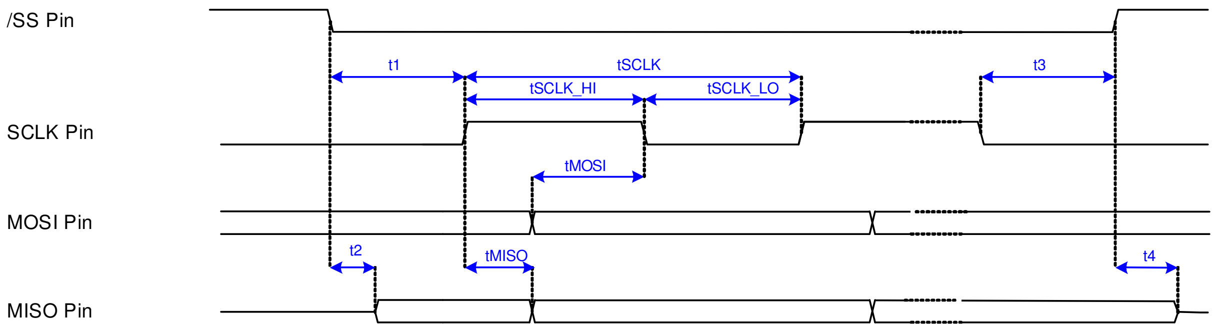

Figure 2 – Serial Interface Timing Diagram

The interface is sensitive, in Trigger mode 2 (see section 14.6), to *Sync* pulses. A *Sync* pulse is negative pulse on /*SS*, while *SCLK* is kept quiet.

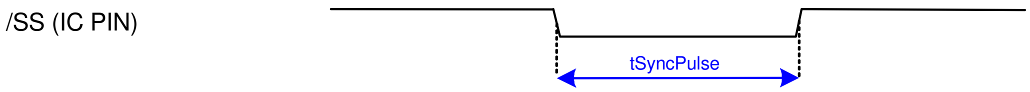

Figure 3 – Sync Pulse Timing Diagram

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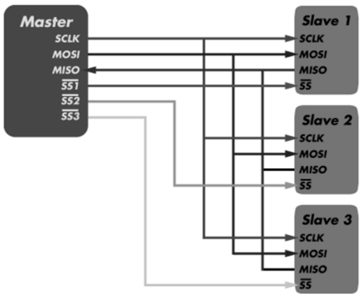
[21] For instance, for master compatible w/ the Motorola SPI protocol, the configuration bits must be *CPHA*=1, *CPOL*=0, *LSBFE*=0.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock Period	tSCLK	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3	450 900 1800	500 1000 2000		ns ns ns
Clock Low Level	tSCLK_HI	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3	225 450 900			ns ns ns
Clock High Level	tSCLK_LO	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3	225 450 900			ns ns ns
Clock to Data Delay	tMISO	EE_PINFILTER = 1 , Cload = 30pF EE_PINFILTER = 2 , Cload = 30pF EE_PINFILTER = 3 , Cload = 30pF			210 300 510	ns ns ns
Data Capture Setup Time	tMOSI		30			ns
/SS FE to SCLK RE	t1	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3	225 450 900			ns ns ns
/SS FE to MISO Low Impedance	t2	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3		90 180 370	120 210 420	ns ns ns
SCLK FE to /SS RE	t3		225			ns
/SS RE to MISO High Impedance	t4	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3		90 180 370	120 210 420	ns ns ns
Sync Pulse Duration	tSyncPulse	EE_PINFILTER = 1 EE_PINFILTER = 2 EE_PINFILTER = 3	520 610 820		10000 10000 10000	ns ns ns

Table 1 - Serial Interface Timing Specifications

Melexis recommends using the multi-slave application diagram as shown on the right.



The *SCLK*, *MISO* and *MOSI* wires interconnect the slaves with the master. A slave is selected by its dedicated */SS* input. A slave *MISO* output is in high-impedance state when the slave is not selected.

Slaves can be triggered synchronously by sending *Sync* pulses on the different */SS*. The pulses must not overlap to avoid electrical short-circuits on the *MISO* bus.

14.2. Serial Protocol

The serial protocol of MLX90363 allows the SPI master device to request the following information:

- Position (magnetic angle Alpha)
- Raw field components (X,Y and Z)
- Self-Diagnostic data

It allows customizing the calibration of the sensor, when needed, at the end-of-line, through EEPROM programming.

The serial protocol offers a transfer rate of 1000 messages/sec. A regular message holds position and diagnostic information. The data acquisition start and processing is fully under the control of the SPI master. The user configuration bits, stored in EEPROM, are programmable with this protocol.

Data integrity is guaranteed in both directions by an 8 bit CRC covering the content of the incoming and outgoing messages. In a dual sensors application, a *Sync* pulse allows a synchronous start of the raw signals acquisition.

14.3. Message General Structure

A message has a unique *Opcode*. The general structure of a message consists of 8 bytes (byte #0, transmitted first, to byte #7 transmitted last).

Byte #7 (the last byte transmitted) holds an 8 bit CRC. The byte #6 holds a *Marker* plus either an *Opcode* or a *rolling counter*.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	(4)							(3)	0	(2)							(1)
3									2								(5)
5									4								
7	CRC								6	Marker		Opcode or Roll Counter					

Table 2 – General Structure of a message and bit naming convention

(1) This bit is named Byte0[0]   (2) This bit is named Byte0[7]
(3) This bit is named Byte1[0]   (4) This bit is named Byte1[7]
(5) This bit is named Byte2[0]

A blank cell refers necessarily to a bit 0.

In a byte, the most-significant-bit is transmitted first (for instance, Byte0[7] is transmitted first, Byte0[0] transmitted last).
Parameter *CRC*[7:0] is Byte7[7:0], Parameter *Marker*[1:0] is Byte6[7:6],
Parameter *Opcode*[5:0] (or *Roll Counter*[5:0]) is Byte6[5:0]

CRCs are encoded and decoded according the following algorithm (language-C):

```
crc = 0xFF;
crc = cba_256_TAB[ Byte0 ^ crc ];
crc = cba_256_TAB[ Byte1 ^ crc ];
crc = cba_256_TAB[ Byte2 ^ crc ];
crc = cba_256_TAB[ Byte3 ^ crc ];
crc = cba_256_TAB[ Byte4 ^ crc ];
crc = cba_256_TAB[ Byte5 ^ crc ];
crc = cba_256_TAB[ Byte6 ^ crc ];
crc = ~crc;
```

The Table 3 corresponds to the CRC-8 polynomial “0xC2”.

cba_256_TAB	0	1	2	3	4	5	6	7
0	0x00	0x2f	0x5e	0x71	0xbc	0x93	0xe2	0xcd
1	0x57	0x78	0x09	0x26	0xeb	0xc4	0xb5	0x9a
2	0xae	0x81	0xf0	0xdf	0x12	0x3d	0x4c	0x63
3	0xf9	0xd6	0xa7	0x88	0x45	0x6a	0x1b	0x34
4	0x73	0x5c	0x2d	0x02	0xcf	0xe0	0x91	0xbe
5	0x24	0x0b	0x7a	0x55	0x98	0xb7	0xc6	0xe9
6	0xdd	0xf2	0x83	0xac	0x61	0x4e	0x3f	0x10
7	0x8a	0xa5	0xd4	0xfb	0x36	0x19	0x68	0x47
8	0xe6	0xc9	0xb8	0x97	0x5a	0x75	0x04	0x2b
9	0xb1	0x9e	0xef	0xc0	0x0d	0x22	0x53	0x7c
10	0x48	0x67	0x16	0x39	0xf4	0xdb	0xaa	0x85
11	0x1f	0x30	0x41	0x6e	0xa3	0x8c	0xfd	0xd2
12	0x95	0xba	0xcb	0xe4	0x29	0x06	0x77	0x58
13	0xc2	0xed	0x9c	0xb3	0x7e	0x51	0x20	0x0f
14	0x3b	0x14	0x65	0x4a	0x87	0xa8	0xd9	0xf6
15	0x6c	0x43	0x32	0x1d	0xd0	0xff	0x8e	0xa1
16	0xe3	0xcc	0xbd	0x92	0x5f	0x70	0x01	0x2e
17	0xb4	0x9b	0xea	0xc5	0x08	0x27	0x56	0x79
18	0x4d	0x62	0x13	0x3c	0xf1	0xde	0xaf	0x80
19	0x1a	0x35	0x44	0x6b	0xa6	0x89	0xf8	0xd7
20	0x90	0xbf	0xce	0xe1	0x2c	0x03	0x72	0x5d
21	0xc7	0xe8	0x99	0xb6	0x7b	0x54	0x25	0x0a
22	0x3e	0x11	0x60	0x4f	0x82	0xad	0xdc	0xf3
23	0x69	0x46	0x37	0x18	0xd5	0xfa	0x8b	0xa4
24	0x05	0x2a	0x5b	0x74	0xb9	0x96	0xe7	0xc8
25	0x52	0x7d	0x0c	0x23	0xee	0xc1	0xb0	0x9f
26	0xab	0x84	0xf5	0xda	0x17	0x38	0x49	0x66
27	0xfc	0xd3	0xa2	0x8d	0x40	0x6f	0x1e	0x31
28	0x76	0x59	0x28	0x07	0xca	0xe5	0x94	0xbb
29	0x21	0x0e	0x7f	0x50	0x9d	0xb2	0xc3	0xec
30	0xd8	0xf7	0x86	0xa9	0x64	0x4b	0x3a	0x15
31	0x8f	0xa0	0xd1	0xfe	0x33	0x1c	0x6d	0x42

Table 3 – cba_256_TAB Look-up table Polynomial “C2”

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	0xFF								0	0xC1							
3	0xFF								2	0x16							
5	0xFF								4	0xD4							
7	0x23								6	0x86							

Table 4 – Example of valid CRC

14.4. Regular Messages

The MLX90363 offers three types of regular messages:

- "α" – diagnostic
- "α – β" – diagnostic
- X – Y – Z – diagnostic

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	ALPHA [13:8]						0	ALPHA [7:0]							
3	0								2	0							
5	0								4	VG[7:0]							
7	CRC								6	0	0	ROLL					

Table 5 – "α" message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	ALPHA [13:8]						0	ALPHA [7:0]							
3			BETA [13:8]						2	BETA [7:0]							
5	0								4	VG[7:0]							
7	CRC								6	0	1	ROLL					

Table 6 – "α – β" message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	X COMPONENT [13:8]						0	X COMPONENT [7:0]							
3			Y COMPONENT [13:8]						2	Y COMPONENT [7:0]							
5			Z COMPONENT [13:8]						4	Z COMPONENT [7:0]							
7	CRC								6	1	0	ROLL					

Table 7 – "X – Y – Z" message

The bits byte6[7] and byte6[6] are markers. They allow the master to recognize the type of regular message (00b, 01b, 10b). The marker is present in all messages (incoming and outgoing). The marker of any message which is not a regular message is equal to 11b.

The bits E1 and E0 report the status of the diagnostics (4 possibilities) as described in the Table 8 – See section 18 for more details.

E1	E0	Description
0	0	First Diagnostics Sequence Not Yet Finished
0	1	Diagnostic Fail
1	0	Diagnostic Pass (Previous cycle)
1	1	Diagnostic Pass – New Cycle Completed

Table 8 - Diagnostics Status Bits

14.4.1. Note for the regular message "X – Y – Z – diagnostic" (Marker = 2)

In the case of marker = 2, the X,Y,Z components are given after offset compensation and filtering (see signal processing in section 19.2). These components are gain dependent (see also section 17.6).

The sensitivity in the X and Y direction is always higher than the Z direction by the IMC Gain factor (see parameter GainIMC in section 12). Melexis therefore recommends multiplying the Z component by the GainIMC factor inside the master in order to use the MLX90363 as a 3D magnetometer.

14.5. Trigger Mode 1

The master sends a GET1 command to initiate the magnetic field acquisition and post-processing. It waits *tSSREFE*, issues the next GET1 and receives at the same time the regular message resulting from the previous GET.

The field sensing, acquisition and post-processing is starting on */SS* rising edge events.

Although GET1 commands are preferably followed by another GET1 command or a NOP command, any other commands are accepted by the slave.

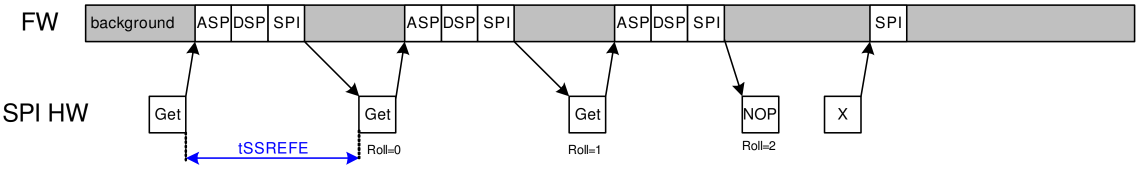

FW
background
ASP
DSP
SPI
ASP
DSP
SPI
ASP
DSP
SPI
SPI
SPI HW
Get
tSSREFE
Get
Roll=0
Get
Roll=1
NOP
Roll=2
X

Figure 4 – Trigger mode 1

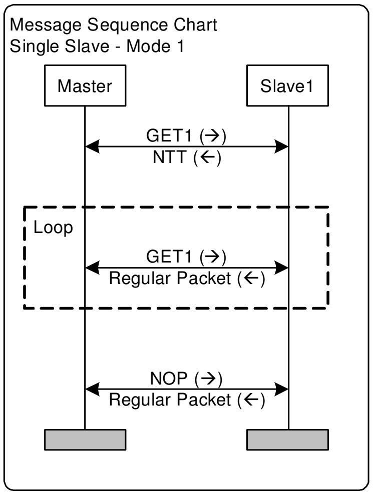

Message Sequence Chart
Single Slave - Mode 1
Master
Slave1
GET1 (→)
NTT (←)
Loop
GET1 (→)
Regular Packet (←)
NOP (→)
Regular Packet (←)

Figure 5 – Trigger Mode 1 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker		0	1	0	0	1	1

Table 9 – GET1 MOSI Message (Opcode = 19)

Note: The NOP message is described at section “14.11”

- The parameter *Marker* defines the regular data packet type expected by the master:

Marker = 0 refers to frame type “ALPHA + Diagnostic”.
Marker = 1 refers to frame type “ALPHA + BETA + Diagnostic”.
Marker = 2 refers to frame type “Components X + Y + Z +Diagnostic”.

- The parameter *Rst* (Byte1[0]) when set, resets the rolling counter attached to the regular data packets.

- The parameter *TimeOutValue* tells the maximum life time of the Regular Data Message. The time step is t1us (See table in Section 10), the maximum time-out is 65535 * t1us. The time-out timer starts when the message is ready, and stops on the SS rising edge of the next message.

  On time-out occurrence, there are two possible scenarios:

Scenario 1.	SS is high, there is no message exchange. In this case, a NTT message replaces the regular message in the SCI buffer.
Scenario 2.	SS is low, the regular packet is being sent out. In this case, the timeout violation is reported on the next message, this later being an NTT message.

14.6. Trigger Mode 2

The Trigger Mode 1 works without *Sync* pulses, as the GET1 command plays the role of a sync pulse. When a delay between the regular message readback and the start of acquisition is needed, or when two or more slaves should be triggered synchronously, the use of a sync pulse is required, and this is the meaning of the Trigger Mode 2.

Principle: The master first enables the trigger mode 2 by issuing a GET2 command.
The master then sends a *Sync* Pulse, at the appropriate time, to initiate the magnetic field acquisition and post-processing.
Finally the master reads the response message with a NOP or a GET2. The GET2 command re-initiates a sync pulse triggered acquisition, whereas the NOP command would just allow the master to receive the latest packet.

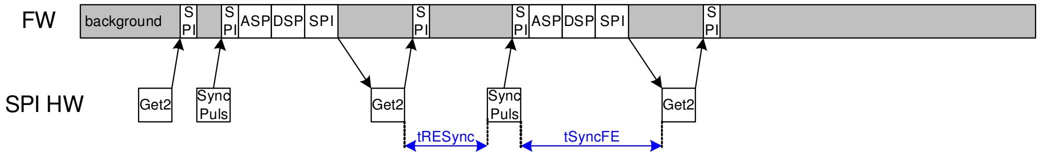

FW
background
SPI
SPI
ASP
DSP
SPI
SPI
SPI
ASP
DSP
SPI
SPI
SPI HW
Get2
Sync Puls
Get2
Sync Puls
Get2
tRESync
tSyncFE

Figure 6 – Trigger Mode 2 – Single Slave Approach

A timing constraint between GET2 and the sync pulse (*tRESync*) should be met.

When this timing is smaller than the constraint, the sync pulse might not be taken in account, causing the next GET2 to return a NTT packet.

GET1 and GET2/SyncPulse can be interlaced.

Multi-slave approach: The way of working described below fits the multi-slave applications where synchronous acquisitions are important. GET2 commands are sent one after the other to the slaves. Then the Sync Pulses are sent almost synchronously (very shortly one after the other).

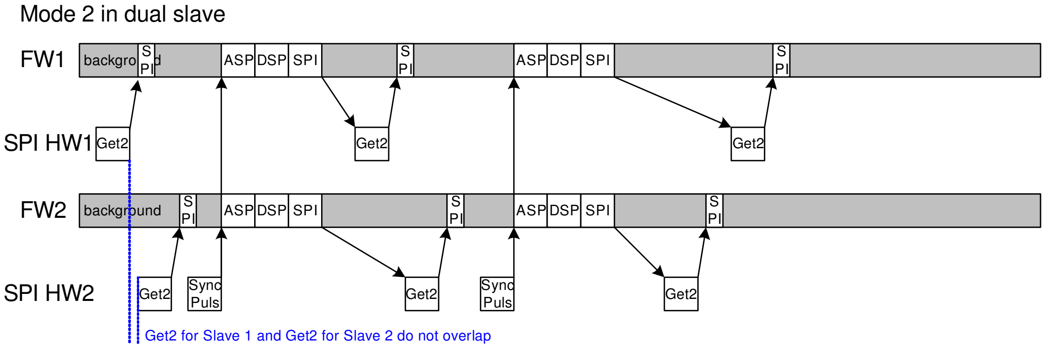

Mode 2 in dual slave
FW1
backgro
SPI
d
ASP
DSP
SPI
SPI
ASP
DSP
SPI
SPI
SPI HW1
Get2
Get2
Get2
FW2
background
SPI
ASP
DSP
SPI
SPI
ASP
DSP
SPI
SPI
SPI HW2
Get2
Sync Puls
Get2
Sync Puls
Get2
Get2 for Slave 1 and Get2 for Slave 2 do not overlap

Figure 7 – Trigger mode 2 - Multi-slave approach, example for two slaves

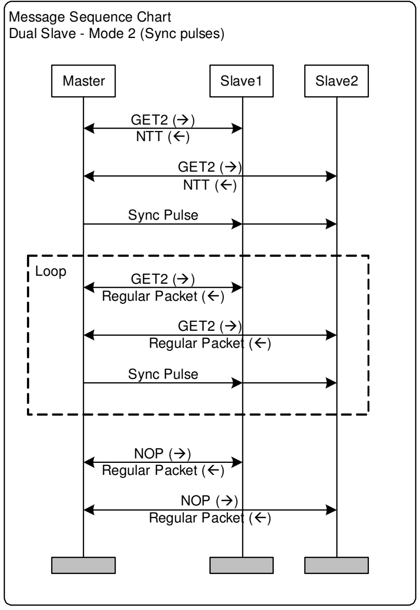

Message Sequence Chart
Dual Slave - Mode 2 (Sync pulses)
Master
Slave1
Slave2
GET2 (→)
NTT (←)
GET2 (→)
NTT (←)
Sync Pulse
Loop
GET2 (→)
Regular Packet (←)
GET2 (→)
Regular Packet (←)
Sync Pulse
NOP (→)
Regular Packet (←)
NOP (→)
Regular Packet (←)

Figure 8 – Trigger mode 2 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker		0	1	0	1	0	0

Table 10 – GET2 MOSI Message (Opcode = 20)

Parameter definition: See GET1 (Section 14.5).

14.7. Trigger Mode 3

Principle: The acquisition sequences are triggered by a GET message, but unlike the Mode 1, the resulting data (position …) is buffered. The slave-out messages contain the buffered data of the previous GET message, and not the newly computed values corresponding to the current GET slave-in request. The buffering releases constraints on the SCI clock frequency (*SCLK*). The Mode 3 offers frame rates as high as Mode 1, if not higher, with slower *SCLK* frequencies. When the clock frequency is limited (400 kbps or less), and when it matters to reach a certain frame rate, Mode 3 is preferred over Mode 1. In any other cases, for instance when the shortest response time represents the main design criteria, Mode 1 is preferred.

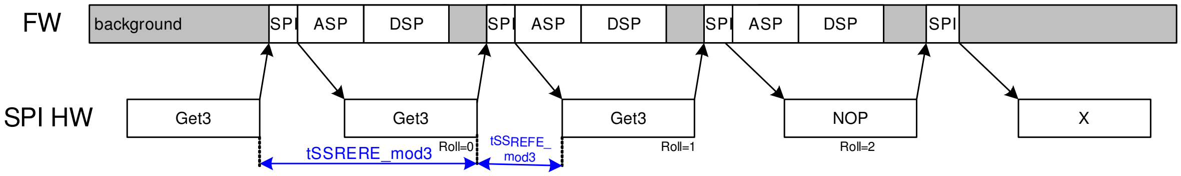

FW
background
SPI
ASP
DSP
SPI
ASP
DSP
SPI
ASP
DSP
SPI
SPI HW
Get3
Get3
Get3
NOP
X
tSSRERE_mod3
Roll=0
tSSREFE_mod3
Roll=1
Roll=2

Figure 9 – Trigger mode 3

GET3 sequences must end with a NOP.

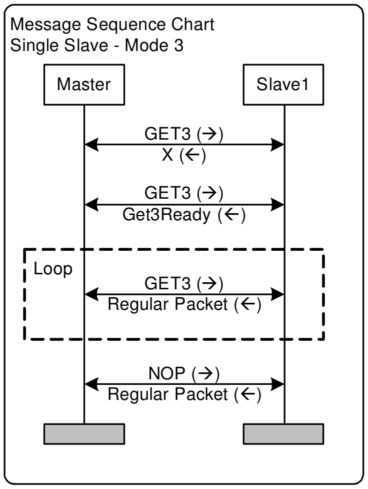

Message Sequence Chart
Single Slave - Mode 3
Master
Slave1
GET3 (→)
X (←)
GET3 (→)
Get3Ready (←)
Loop
GET3 (→)
Regular Packet (←)
NOP (→)
Regular Packet (←)

Figure 10 – Trigger mode 3 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker		0	1	0	1	0	1

Table 11 – GET3 MOSI Message (Opcode = 21)

Parameter definition: See GET1 (Section 14.5)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	1	0	1	1	0	1

Table 12 – Get3Ready Slave-Out Message (Opcode = 45)

14.8. Trigger Modes Timing Specifications

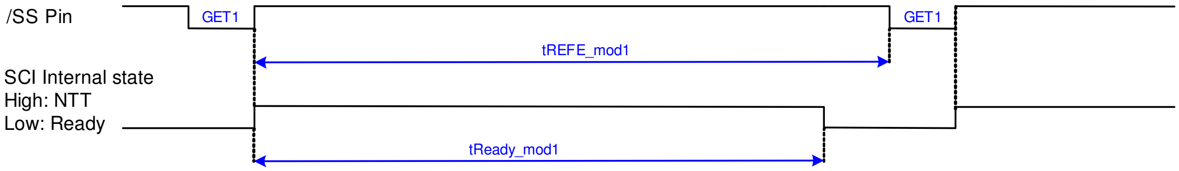

/SS Pin
GET1
GET1
tREFE_mod1
SCI Internal state
High: NTT
Low: Ready
tReady_mod1

Figure 11 – Trigger mode 1 timing diagram

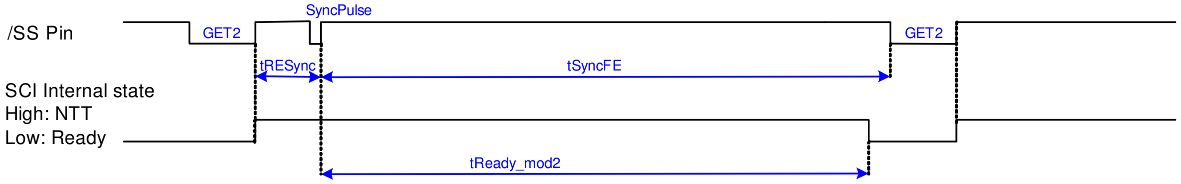

/SS Pin
GET2
SyncPulse
GET2
SCI Internal state
High: NTT
Low: Ready
tRESync
tSyncFE
tReady_mod2

Figure 12 – Trigger mode 2 timing diagram

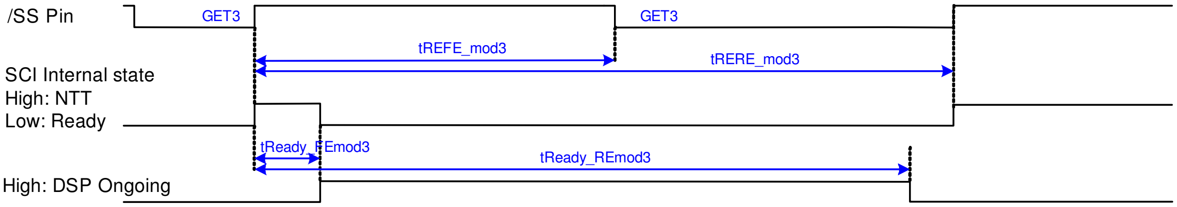

/SS Pin
GET3
GET3
tREFE_mod3
tRERE_mod3
SCI Internal state
High: NTT
Low: Ready
tReady_FEmod3
tReady_REmod3
High: DSP Ongoing

Figure 13 – Trigger mode 3 timing diagram

5V Application Diagram

Items	Definition	Marker	Min	Typ	Max	Unit
tREFE_mod1	Get1 SS Rising Edge to next Get1 SS Falling Edge	0	920			µs
		1	1050			µs
		2	920			µs
tReady_mod1	Get1 SSRE to SO Answer ReadyToTransmit	0			920	µs
		1			1050	µs
		2			920	µs

Table 13 – Trigger Modes Timing Specification (Mode 1, VDD=5V)

Items	Definition	Marker	Min	Typ	Max	Unit
tSyncFE	Sync Pulse (RE) to Get2 Falling Edge	0	874			µs
		1	1004			µs
		2	874			µs
tReady_mod2	Sync Pulse (RE) to SO Answer ReadyToTransmit	0			874	µs
		1			1004	µs
		2			874	µs
tRESync	Get2 SS Rising Edge to Sync Pulse (RE)		80			µs

Table 14 – Trigger Modes Timing Specification (Mode 2, VDD=5V)

Items	Definition	Marker	Min	Typ	Max	Unit
tRERE_mod3	Get3 SS RE to RE	0	950			µs
		1	1080			µs
		2	950			µs
tReadyRE_mod3	Get3 SS RE to DSP Completion	0			950	µs
		1			1080	µs
		2			950	µs
tREFE_mod3	Get3 SS Rising to Falling		90			µs
tReadyFE_mod3	Get3 SS RE to SO Answer ReadyToTransmit				90	µs

Table 15 – Trigger Modes Timing Specification (Mode 3, VDD=5V)

3V3 Application Diagram

Items	Definition	Marker	Min	Typ	Max	Unit
tREFE_mod1	Get1 SS Rising Edge to next Get1 SS Falling Edge	0	1067			µs
		1	1218			µs
		2	1067			µs
tReady_mod1	Get1 SSRE to SO Answer ReadyToTransmit	0			1067	µs
		1			1218	µs
		2			1067	µs

Table 16 – Trigger Modes Timing Specification (Mode 1, V_{DD} = 3.3V)

Items	Definition	Marker	Min	Typ	Max	Unit
tSyncFE	Sync Pulse (RE) to Get2 Falling Edge	0	1014			µs
		1	1165			µs
		2	1014			µs
tReady_mod2	Sync Pulse (RE) to SO Answer ReadyToTransmit	0			1014	µs
		1			1165	µs
		2			1014	µs
tRESync	Get2 SS Rising Edge to Sync Pulse (RE)		93			µs

Table 17 – Trigger Modes Timing Specification (Mode 2, V_{DD} = 3.3V)

Items	Definition	Marker	Min	Typ	Max	Unit
tRERE_mod3	Get3 SS RE to RE	0	1102			µs
		1	1253			µs
		2	1102			µs
tReadyRE_mod3	Get3 SS RE to DSP Completion	0			1102	µs
		1			1253	µs
		2			1102	µs
tREFE_mod3	Get3 SS Rising to Falling		105			µs
tReadyFE_mod3	Get3 SS RE to SO Answer ReadyToTransmit				105	µs

Table 18 – Trigger Modes Timing Specification (Mode 3, V_{DD} = 3.3V)

14.9. Opcode Table

Opcode		MOSI Message	Opcode		MISO Message
19d	0x13	GET1	n/a		Regular Data Packet
20d	0x14	GET2			
21d	0x15	GET3	45d	0x2D	Get3Ready
1d	0x01	MemoryRead	2d	0x02	MemoryRead Answer
3d	0x03	EEPROMWrite	4d	0x04	EEPROMWrite Challenge
5d	0x05	EEChallengeAns	40d	0x28	EEReadAnswer
15d	0x0F	EEReadChallenge	14d	0x0E	EEPROMWrite Status
16d	0x10	NOP / Challenge	17d	0x11	Challenge/NOP MISO Packet
22d	0x16	DiagnosticDetails	23d	0x17	Diagnostics Answer
24d	0x18	OscCounterStart	25d	0x19	OscCounterStart Acknowledge
26d	0x1A	OscCounterStop	27d	0x1B	OscCounterStopAck+CounterValue
47d	0x2F	Reboot			
49d	0x31	Standby	50d	0x32	StandbyAck
			61d	0x3D	Error frame
			62d	0x3E	NothingToTransmit (NTT)
			44d	0x2C	Ready Message (first SO after POR)

Table 19 – Opcode Table

14.10. Timing specifications per Opcode, and next allowed messages

For each slave-in message, the timing between the slave-select-rising-edge event and the slave-select-falling event, as depicted below, is specified.

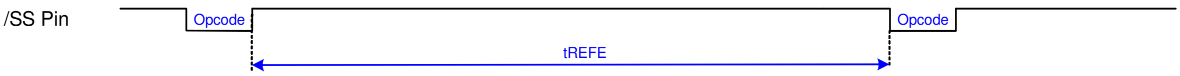


Figure 14 – Timing diagram

Op	MOSI Message	tREFE	Next allowed slave-in message
19	GET1	tREFE_mod1	GET1, MemoryRead,DiagDetails,NOP
20	GET2 followed by Sync	tSyncFE	GET2, MemoryRead,DiagDetails,NOP
21	GET3	tREFE_mod3	GET3, MemoryRead,DiagDetails,NOP
1	MemoryRead	tShort	MemoryRead, DiagDetails, NOP
3	EEPROMWrite	tShort	EEReadChallenge
5	EEChallengeAns	teewrite	NOP
15	EEReadChallenge	tShort	EEChallengeAns
16	NOP / Challenge	tShort	All commands
22	DiagnosticDetails	tShort	All commands
24	OscCounterStart	tShort	OscCounterStop
26	OscCounterStop	tShort	NOP
47	Reboot	tStartup	See Startup Sequence
49	Standby	tShort	All commands

Table 20 – Response time and Next allowed slave-in messages

14.11. NOP Command and NOP Answer

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3	KEY [15:8]								2	KEY [7:0]							
5									4								
7	CRC								6	1	1	0	1	0	0	0	0

Table 21 – NOP(Challenge) MOSI Message (Opcode = 16)

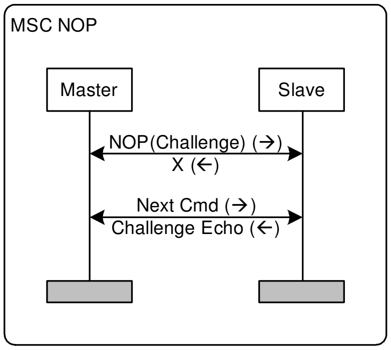


Figure 15 – NOP Message Sequence Chart

Note: the message X means “unspecified valid answer” and typically contains the answer of the previous command.

- Parameter *Key* : any 16 bit number

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3	KEY_ECHO [15:8]								2	KEY_ECHO [7:0]							
5	INVERTED KEY_ECHO [15:8]								4	INVERTED KEY_ECHO [7:0]							
7	CRC								6	1	1	0	1	0	0	0	1

Table 22 - Challenge Echo MISO Message (Opcode = 17)

- Parameter *Key_Echo* = *Key*
- Parameter *InvertedKey_Echo* = 65535 - *Key (meaning bit reversal).*

14.12. OscCounterStart and OscCounterStop Commands

The SCI Master can evaluate the slave’s internal oscillator frequency by the use of the *OscCounterStart* and *OscCounterStop* commands. This first command enables in the MLX90363 a software counter whereas the second command stops it and returns the counter value.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	0	1	1	0	0	0

Table 23 – OscCounterStart Slave-In message (opcode 24)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	0	1	1	0	0	1

Table 24 – *OscCounterStart* Acknowledge Slave-Out message (opcode 25)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	0	1	1	0	1	0

Table 25 – OscCounterStop Slave-In message (opcode 26)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3		CounterValue[14:8]							2	CounterValue[7:0]							
5									4								
7	CRC								6	1	1	0	1	1	0	1	1

Table 26 – OscCounter Slave-Out message (opcode 27)

- Parameter *CounterValue* represents the time between the two events OscCounterStart Slave Select Rising Edge and OscCounterStop Slave Select Rising Edge, in microsecond, and for an oscillator frequency equal to 19MHz exactly.

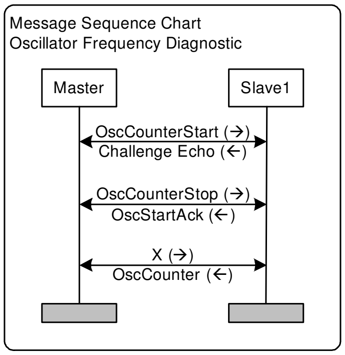

Message Sequence Chart
Oscillator Frequency Diagnostic
Master
Slave1
OscCounterStart (→)
Challenge Echo (←)
OscCounterStop (→)
OscStartAck (←)
X (→)
OscCounter (←)

Figure 16 – Oscillator Frequency Diagnostic Message Sequence Chart

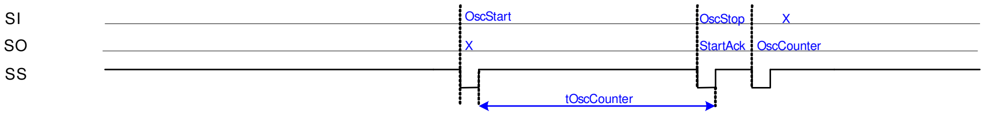

SI
SO
SS
OscStart
X
OscStop
StartAck
X
OscCounter
tOscCounter

Figure 17 – Oscillator Frequency Diagnostic Timing Diagram (SCI)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
	tOscCounter		500	1000	30000	us

14.13. Protocol Errors Handling

Error Item	Error definition	Condition	Detection	Slave Actions	MISO Message
IncorrectBitCount	Slave In Message bit count ≠ 64	all modes	FW reads the HW bit counter	Ignore Message + Re-init Protocol	Error Message (incorrect bitcount = 1)
IncorrectCRC	Slave In Message has a CRC Error	all modes	FW computes CRC	Ignore Message + Re-init Protocol	Error Message (incorrect crc = 1)
IncorrectOpcode	Invalid Slave in Message	all modes	FW	Ignore Message + Re-init Protocol	Error Message (incorrect opcode = 1)
tREFE < tReady_mod1	Regular Message Readback occurs to early	Trigger mode 1	Interrupt occurring to early + Fw reads HW bit + Protection interrupt	Ignore Frame + Re-init Protocol	NTT message
tSyncFE < tReady_mod2	Regular Message Readback occurs to early	Trigger mode 2	Interrupt occurring to early + Fw reads HW bit + Protection interrupt	Ignore Frame + Re-init Protocol	NTT message
tRESync Violation	Sync Pulse occurring to early	Trigger mode 2	none. The Sync pulse is pending internally.	none (but the sync pulse is not treated immediately)	Valid message. Note: This violation can cause a TSyncFE < TReady_mod2 violation.
tRERE_mod3 < *tReady_mod3*	Regular Message Readback occurs to early	Trigger mode 3	Protection interrupt	Re-init Protocol	NTT message
tREFE_mod3 < *tReady_FE_mod3*	Regular Message Readback occurs to early	Trigger mode 3	Protection interrupt	Re-init Protocol	NTT message
TimeOut	Regular Message Readback occurs to late	all modes	Timer Interrupt	MISO Frame = NTT + Re-init Protocol	NTT message

Table 27 – Protocol Errors Handling (Slave standpoint)

Error Items/Events	Associated Slave Event	Master recommended actions	Associated Slave Actions	Next MISO message
Receive NTT	Receive NTT	Protocol re-initialization	Protocol re-initialization	Error Message * (TimeViolation = 1)
Receive Incorrect CRC Receive Incorrect Opcode	undetected event	Protocol re-initialization	none	Normal message
Receive Error Message	Send Error Message	Protocol re-initialization	none	Normal message
Receive an unexpected *DiagDetails* message	Run in fail-safe mode	Protocol re-initialization + Slave reset	none	*DiagDetails* message

Table 28 – Protocol Errors Handling (Master standpoint)

Note 1: On NTT or Error messages, master should consider that the last command is ignored by the slave, and it should therefore, either resend the command, or more generally re-initialize the protocol.
Note 2: After protocol re-initialization, master can diagnose the communication with a NOP command.

Note 3: A slave-out error message implicitly means that the slave has re-initialized the communication and is therefore ready to receive any commands.

14.14. Ready, Error and NTT Messages

After power-on-reset, the first slave-out message is a *Ready* message.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	FWVersion[15:8]								0	HWVersion[7:0]							
3									2								
5									4								
7	CRC								6	1	1	1	0	1	1	0	0

Table 29 - *Ready* Slave-out Message (Opcode = 44)

The MLX90363 reports protocol errors using the *Error* message defined below. Diagnostics Errors (as opposed to protocol errors) are reported with the bits E1 and E0 of the regular message.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0	ERROR CODE							
3									2								
5									4								
7	CRC								6	1	1	1	1	1	1	0	1

Table 30 - *Error* Message MISO (Opcode = 61)

The description of the parameter *ErrorCode* is given in the table below.

Code	Description of Error CODE
1	Incorrect BitCount
2	Incorrect CRC
3	Answer = NTT message Two reasons: Answer Time-Out or Answer not Ready
4	OPCODE not valid

In most of the timing violations, the slave answers with a NTT message. A NTT message is stored in the slave's ROM (as opposed to the slave's RAM). NTT messages are typically seen in case of timing violation: either the firmware is still currently processing the previous SCI command, or a time-out occurred (see GET). In normal operation, NTT messages are not supposed to be observed: the Master is supposed to respect the protocol timings defined.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1			1				1		0				1				1
3		1				1			2			1	1			1	1
5		1	1			1	1		4		1		1		1		1
7	CRC								6	1	1	1	1	1	1	1	0

Table 31 – *NTT* (Nothing To Transmit) Message (Opcode = 62)

14.15. DiagnosticsDetails commands

This is the only function that can be combined with a regular message.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	0	1	0	1	1	0

Table 32 – *DiagnosticsDetails* Slave In Command (opcode =22)

Use *DiagnosticDetails* to get a detailed analysis of the diagnostics.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	D15	D14	D13	D12	D11	D10	D9	D8	0	D7	D6	D5	D4	D3	D2	D1	D0
3	FSMERC		ANADIAGCNT						2	0	0	0	D20	D19	D18	D17	D16
5									4								
7	CRC								6	1	1	0	1	0	1	1	1

Table 33 - Diagnostics *DiagnosticDetails* Master In message (Opcode = 23)

- Diagnostic bit *Dx* : see Section 18

- Parameter *ANADIAGCNT* is a sequence loop counter referring to the analog-class diagnostics (all others).

  If *FSMERC* = 3, *ANADIAGCNT* takes another meaning:
  193 protection error interruption happened
  194 invalid address error interruption happened
  195 program error interruption happened
  196 exchange error interruption happened
  197 not connected error interruption happened
  198 Stack Interrupt
  199 Flow Control Error

- Parameter *FSMERC* reports the root-cause of entry in fail-safe mode
  - *FSMERC* = 0 : the chip is not in fail safe mode
  - *FSMERC* = 1 : BIST error happened and the chip is in fail safe mode
  - *FSMERC* = 2 : digital diagnostic error happened and the chip is in fail safe mode
  - *FSMERC* = 3 : one of the 5 error interruptions listed above happened and the chip is in fail safe mode

14.16. MemoryRead message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	ADD0[15:8]								0	ADD0[7:0]							
3	ADD1[15:8]								2	ADD1[7:0]							
5									4								
7	CRC								6	1	1	0	0	0	0	0	1

Table 34 – *MemoryRead* Master-Out Slave-In Message (*Opcode* = 1)

MemoryRead returns two EEPROM or RAM words respectively pointed by the parameters *ADDR0*, *ADDR1*.

- The parameter *ADDRx* has three valid ranges: 0…254 for RAM access, 0x1000...0x103E for EEPROM access, and 0x4000…0x5FFE for ROM access

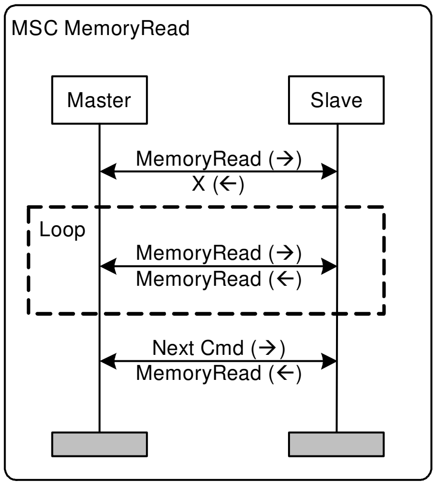


Figure 18 – MSC for RAM/ROM/EEPROM Memory Read

Note: Enter the loop for complete memory dumps.

MemoryRead Master-In Message (opcode 0x02)

The address *Addr* may be valid or not:
Case of validity: MemoryRead returns normally the data word pointed by *Addr*
Case of invalidity: MemoryRead returns *DataWord* = 0.

Note: FW makes sure that invalid addresses do not cause memory access violation

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	DATA[15:8] AT ADD0								0	DATA[7:0] AT ADD0							
3	DATA[15:8] AT ADD1								2	DATA[7:0] AT ADD1							
5									4								
7	CRC								6	1	1	0	0	0	0	1	0

Table 35 – *MemoryRead* MISO Packet (Opcode = 2)

14.17. *EepromWrite* Message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	0	0	ADDRESS[5:0][22]						0								
3	KEY[15:8]								2	KEY[7:0]							
5	DATA WORD[15:8]								4	DATA WORD[7:0]							
7	CRC								6	1	1	0	0	0	0	1	1

Table 36 – *EEPROMWrite* MOSI Message (Opcode = 3)

The EEPROM data consistency is guaranteed through two protection mechanisms: A and B.

Protection A: The parameter *ADDRESS* should match the parameter *KEY*.
The key associated to each address is public. Protection against erroneous write (in the field) is guaranteed as long as the keys are not stored in the master (ECU), but in the calibration system, which is typically a CAN or LIN Master.

Protection B: Slave challenges the Master with a randomly generated *ChallengeKey*, expects back this key exclusive-or with 0x1234

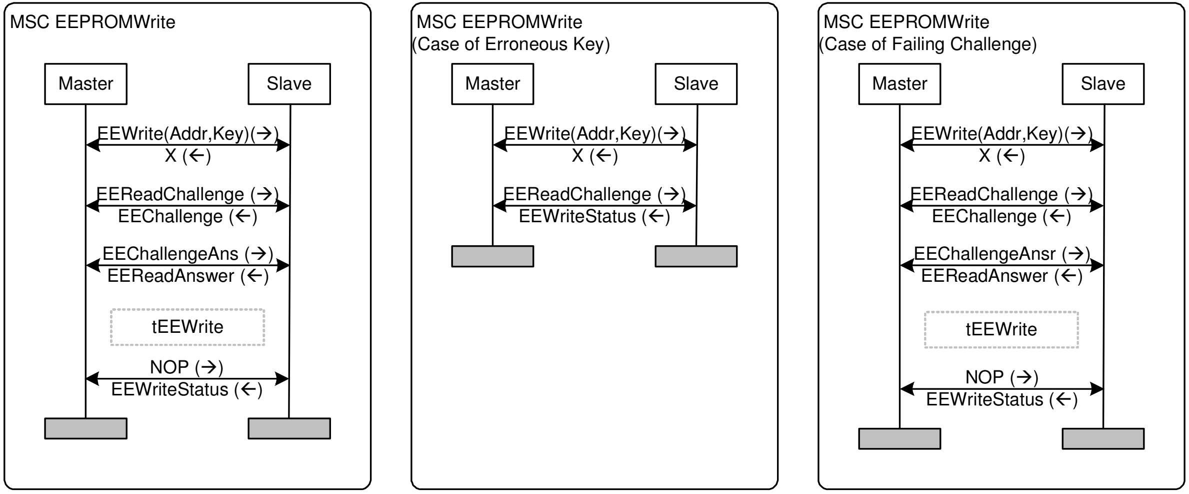

MSC EEPROMWrite
Master
Slave
EEWrite(Addr,Key)(→)
X (←)
EEReadChallenge (→)
EEChallenge (←)
EEChallengeAns (→)
EEReadAnswer (←)
tEEWrite
NOP (→)
EEWriteStatus (←)
MSC EEPROMWrite
(Case of Erroneous Key)
Master
Slave
EEWrite(Addr,Key)(→)
X (←)
EEReadChallenge (→)
EEWriteStatus (←)
MSC EEPROMWrite
(Case of Failing Challenge)
Master
Slave
EEWrite(Addr,Key)(→)
X (←)
EEReadChallenge (→)
EEChallenge (←)
EEChallengeAnsr (→)
EEReadAnswer (←)
tEEWrite
NOP (→)
EEWriteStatus (←)

Figure 19 – MSCs *EEPROMWrite*

	ADDRESS[3:1]							
ADDRESS[5:4]	0	1	2	3	4	5	6	7
0	17485	31053	57190	57724	7899	53543	26763	12528
1	38105	51302	16209	24847	13134	52339	14530	18350
2	55636	64477	40905	45498	24411	36677	4213	48843
3	6368	5907	31384	63325	3562	19816	6995	3147

Table 37 – EEPROM Write Public Keys

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	0	0	1	1	1	1

Table 38 – *EEPROMWrite* ReadChallenge Slave-In Message (Opcode = 15)

---

[22] The value of the ADDRESS[5:0] shall be even.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3	CHALLENGE KEY [15:8]								2	CHALLENGE KEY [7:0]							
5									4								
7	CRC								6	1	1	0	0	0	1	0	0

Table 39 – EEPROMWrite EEChallenge Slave-Out Message (Opcode = 4)

- The parameter *ChallengeKey* is randomly generated by the sensor, and should be echoed because of the next command

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3	KEY ECHO [15:8]								2	KEY ECHO [7:0]							
5	INVERTED KEY ECHO [15:8]								4	INVERTED KEY ECHO [7:0]							
7	CRC								6	1	1	0	0	0	1	0	1

Table 40 – *EEPROMWrite* ChallengeAns Slave-In Message (Opcode = 5)

- The parameter *KeyEcho* should match *ChallengeKey* exor'ed with 0x1234.
- The parameter *InvertedKeyEcho* should match *KeyEcho* after bit reversal.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
4									4								
7	CRC								6	1	1	1	0	1	0	0	0

Table 41 – *EEReadAnswer* Slave-Out Message (Opcode = 40)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0					CODE			
3									2								
4									4								
7	CRC								6	1	1	0	0	1	1	1	0

Table 42 – *EEPROMWriteStatus* Slave-Out Message (Opcode = 14)

- The parameter *Code* details the exact cause of EEPROM write failure

Code	Description of EEPROM Write Failure
1	Success
2	Erase/Write Fail
4	EEPROM CRC Erase/Write Fail
6	Key Invalid
7	Challenge Fail
8	Odd Address

The command *Reboot* must be sent after a series of EEPROM writes, to make sure that the new EEPROM parameters are taken into account.

14.18. Reboot

Reboot is a valid command in the following three cases.

1. After an EEPROM write
2. In fail-safe mode
3. In standby mode

In normal mode, *Reboot* reports wrong opcode.

Reboot causes a system reset identical to a true power-on reset. Start-up timings and sequences are applicable for the *reboot* message.

Reboot, after EEPROM programming
It is meant to force the FW to refresh the EEPROM cache and IO space after a series of EEPROM write commands. It forces the FW to take into account all the changes (modes enabling, disabling...) including those that are not cached.

Reboot, in fail-safe mode
ECU can issue a *reboot* message to exit the fail-safe mode before the watchdog time-out, for a fast recovery.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
4									4								
7	CRC								6	1	1	1	0	1	1	1	1

Table 43 – Reboot (Opcode = 47)

14.19. Standby

Standby sets the sensor in Standby mode: the digital clock is stopped and some analog blocks are switched off. The SCI clock remains active, allowing the sensor to be responsive to SCI messages.

The first SCI message received while in Standby wakes up the sensor. The standby mode is precisely exited on the SS rising edge. The first message following a *Standby* message is normally interpreted by the sensor. It can be NOP, a GET or anything else.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
4									4								
7	CRC								6	1	1	1	1	0	0	0	1

Table 44 – Standby (Opcode = 49)

The sensor answer to *Standby* is *StandbyAck* (opcode 50).

After resuming, the (E1, E0) error bits of the 6 following *GET* messages shall be ignored.

14.20. Start-up Sequence (Serial Communication)

The MLX90363 serial interface is enabled after the internal start-up initializations and start-up checks. Note: The start-up sequence of the MLX90363 firmware is described at chapter 19.1.
The recommended *SCI* start-up sequences (Master – Slave) are depicted in the following message sequence charts, and timing diagrams. It usually starts with a NOP SI message. *Ready* is the first SO message.

For safety critical applications, Melexis recommends performing two extra checks prior to the request of the first regular data: oscillator frequency check and a readback of the diagnostic details (ROM, RAM, ADC Monitor…)

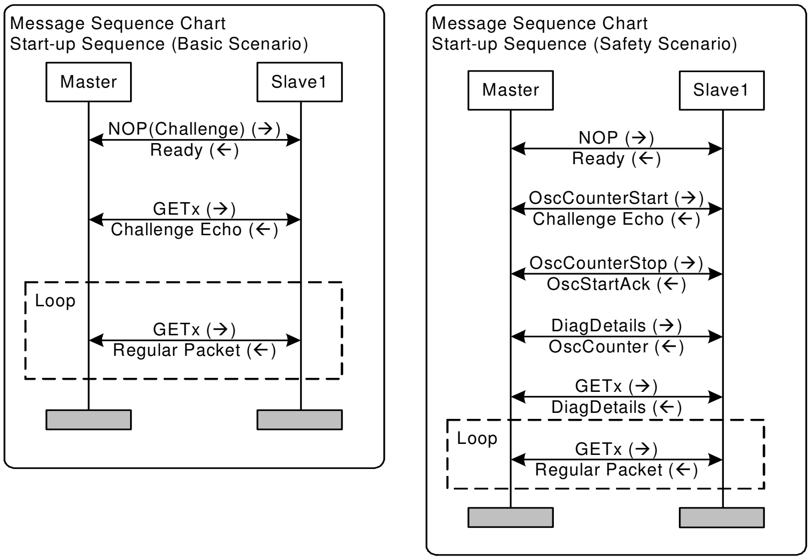

Message Sequence Chart
Start-up Sequence (Basic Scenario)
Master
Slave1
NOP(Challenge) (→)
Ready (←)
GETx (→)
Challenge Echo (←)
Loop
GETx (→)
Regular Packet (←)
Message Sequence Chart
Start-up Sequence (Safety Scenario)
Master
Slave1
NOP (→)
Ready (←)
OscCounterStart (→)
Challenge Echo (←)
OscCounterStop (→)
OscStartAck (←)
DiagDetails (→)
OscCounter (←)
GETx (→)
DiagDetails (←)
Loop
GETx (→)
Regular Packet (←)

Figure 20 – MSCs Start-up sequence examples (basic and safety critical scenario)

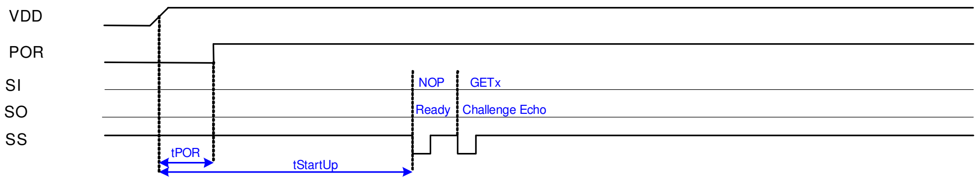

VDD
POR
SI
SO
SS
NOP
GETx
Ready
Challenge Echo
tPOR
tStartUp

Figure 21 – Start-up sequence, basic scenario, timing diagram

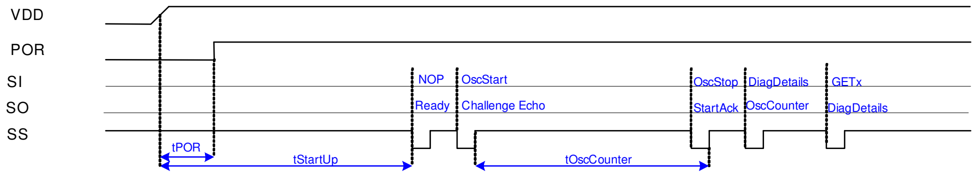

VDD
POR
SI
SO
SS
NOP
OscStart
OscStop
DiagDetails
GETx
Ready
Challenge Echo
StartAck
OscCounter
DiagDetails
tPOR
tStartUp
tOscCounter

Figure 22 – Start-up sequence, safety critical scenario, timing diagram

Notes:

- The timing tStartUp is specified at chapter Timing Specifications (Section 10)
- The slave answers with *NTT* in case the first SI message occurs prior the end of the initial checks.
- The NOP - Challenge Echo is meant to diagnose the SCI link.

14.21. Allowed sequences

Only the message sequences described in this datasheet are accepted by the sensor.

A few more are described below; they combine GET1 or GET2 with MemoryRead or DiagDetails.
The particular timings associated to these sequences do not overrule the general timing specifications.

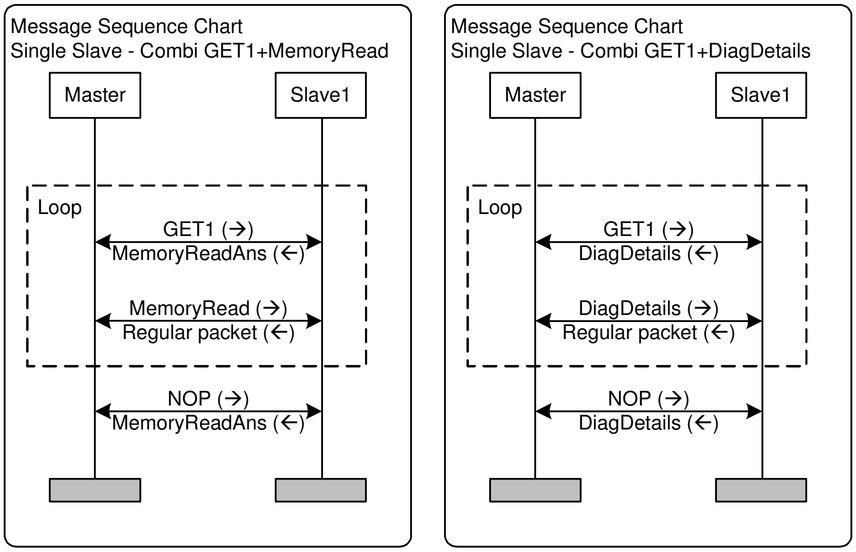

Message Sequence Chart
Single Slave - Combi GET1+MemoryRead
Master
Slave1
Loop
GET1 (→)
MemoryReadAns (←)
MemoryRead (→)
Regular packet (←)
NOP (→)
MemoryReadAns (←)
Message Sequence Chart
Single Slave - Combi GET1+DiagDetails
Master
Slave1
Loop
GET1 (→)
DiagDetails (←)
DiagDetails (→)
Regular packet (←)
NOP (→)
DiagDetails (←)

Figure 23 – MSCs Combi sequences GET1+MemoryRead and GET1+DiagDetails

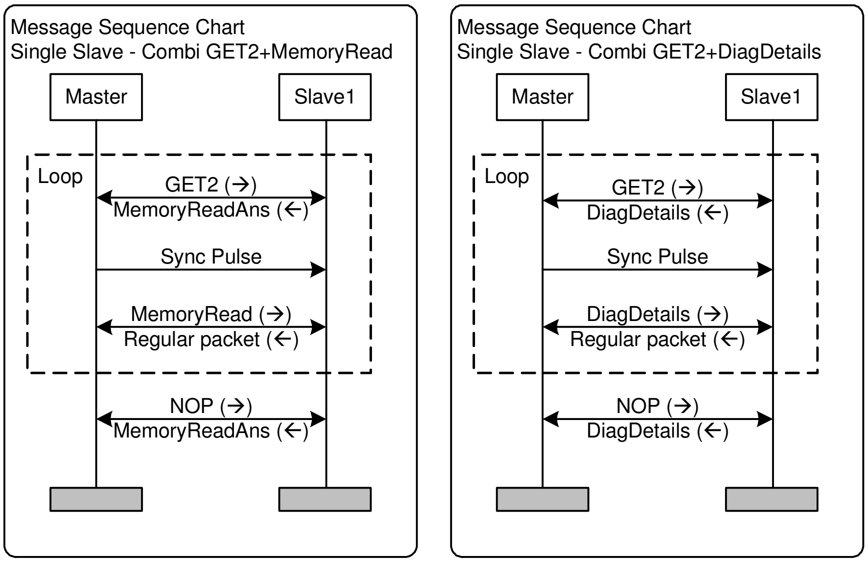

Message Sequence Chart
Single Slave - Combi GET2+MemoryRead
Master
Slave1
Loop
GET2 (→)
MemoryReadAns (←)
Sync Pulse
MemoryRead (→)
Regular packet (←)
NOP (→)
MemoryReadAns (←)
Message Sequence Chart
Single Slave - Combi GET2+DiagDetails
Master
Slave1
Loop
GET2 (→)
DiagDetails (←)
Sync Pulse
DiagDetails (→)
Regular packet (←)
NOP (→)
DiagDetails (←)

Figure 24 – MSCs Combi sequences GET2+MemoryRead and GET2+DiagDetails

15. MLX90363 Traceability Information

Every device contains a unique ID that is stored in the EEPROM. Melexis strongly recommends storing this value during the EOL (end-of-line) programming to ensure full traceability of the product.

These parameters shall never be erased during the EOL programming.

Parameter	Comments	Address	Default Values	Parameter
		(Hexa)	-	# bit
MLXID	Traceability Information	1012[15:0] 1014[15:0] 1016[15:0]	MLX	48

16. MLX90363 End-User Programmable Items

The list below describes the parameters that are available to the customer during EOL programming. The parameters will be programmed through the *EepromWrite* Message (section 14.17).
It must be noted that the data type of Eepromwrite Message is a word, and therefore it is mandatory to first readback the complete contents of the word before changing only the bits corresponding to the parameter.

Parameter	Comments	Address	Default Values	Parameter
		(Hexa)	-	# bit
MAPXYZ	XYZ Coordinates mapping	102A[2:0]	0	3
3D	Enabling of 3D formula (Joystick)	102A[3]	0	1
FILTER	Enabling of Signal Filter	102A[5:4]	0	2
VIRTUALGAINMAX	Electrical Gain Code Max	102E[15:8]	41	8
VIRTUALGAINMIN	Electrical Gain Code Min	102E[7:0]	0	8
KALPHA	Magnetic Angle Formula Parameter	1022[15:0]	0	16
KBETA	Magnetic Angle Formula Parameter	1024[15:0]	1.6	16
SMISM + SEL_SMISM	Magnetic Angle Formula Parameter	1032[15:0]	1	16
ORTH_B1B2	Magnetic Angle Formula Parameter	1026[7:0]	0	8
KT	Magnetic Angle Formula Parameter	1030[15:0]	1	16
FHYST	Hysteresis Value (Alpha + Beta)	1028[15:8]	MLX	8
PINFILTER	SCI Input Pins: EMC: Filter Bandwidth	1001[1:0]	1	2
USERID	User Identification	103A[15:0] 103C[15:0]	0001 0003	16 16
FREE	Freely usable by user	1018[15:0] 1026[15:8] 1028[7:0] 103E[7:0]	0	40

Melexis strongly recommends checking the User Identification data (Parameters USERID) during EOL calibration.

17. MLX90363 Description of End-User Programmable Items

17.1. User Configuration: Device Orientation

MAPXYZ	Assignment	Note
0	B1 = X, B2 = Y, B3 = Z	
1	B1 = X, B2 = Z, B3 = Y	
2	B1 = Y, B2 = Z, B3 = X	
3	B1 = Y, B2 = X, B3 = Z	Use mode 0 instead
4	B1 = Z, B2 = X, B3 = Y	
5	B1 = Z, B2 = Y, B3 = X	

The values B1, B2 and B3 are inputs to the 2D/3D formula (see section 17.2).

The field coordinates X, Y, Z are relative to the device (See Section 23.3 and 23.6). The parameter MAPXYZ selects the application-dependent mapping of (X, Y, Z) to (B1, B2, B3).

17.2. User Configuration: Magnetic Angle Formula

Parameter 3D	Formula	Note
0	$Alpha = \arctan\left(\frac{B2}{B1}\right)$	extended to the full circle
1	$Alpha = \arctan\left(\frac{\sqrt{(KALPHA \times B3)^2 + (KT \times B2)^2}}{B1}\right)$ $Beta = \arctan\left(\frac{\sqrt{(KBETA \times B3)^2 + (KT \times B1)^2}}{B2}\right)$	extended across B1=0 and B2=0 max 180deg

17.3. User Configuration: 3D=0 formula trimming parameters SMISM and ORTH_B1B2

17.3.1. Magnetic Angle ∠XY

Parameter	Address (hex)	Value
SMISM + SEL_MISM	1032[15:0]	Trimmed by MLX
ORTH	1038[7:0]	Trimmed by MLX
ORTH_SEL	102C[8]	0
MAPXYZ	102A[2:0]	0

This is the default condition as programmed by MLX. In such case, no front-end calibration is needed from the customer.

17.3.2. Magnetic Angle ∠XZ and ∠YZ

Parameter	Address (hex)	Range	Value
SEL_SMISM	1032[15]	0 or 1	0 or 1
SMISM	1032[14:0]	[0..2]	TYP = 1.4
ORTH_SEL	102C[8]	0 or 1	1
ORTH_B1B2	1026[7:0]	[0..2]	TYP = 0
MAPXYZ	102A[2:0]	1, 2, 4 or 5	1, 2, 4 or 5

If the magnetic angle ∠XZ or ∠YZ is read, Melexis strongly recommends calibrating the front-end parameters in order to reduce the magnetic accuracy error (see Section 11):

1) Phase Error

B2 = B1 – B2 * ORTH_B1B2 / 1024

Where ORTH_B1B2 is the phase mismatch between the B1 and B2 signals.

2) Sensitivity Mismatch between B1 and B2

The parameter SMISM is selected in such a way that:

i. Case |B1|>|B2| → SEL_SMISM = 0

B1 * SMISM[14:0] / 2^15 and B2 have the same amplitude.

ii. Case |B1|<|B2| → SEL_SMISM = 1

B1 and B2 * SMISM[14:0] / 2^15 have the same amplitude.

17.4. User Configuration: 3D=1 formula trimming parameters KALPHA, KBETA, KT

The values KAPLHA, KBETA and KT are inputs to the 3D formula (see section 17.2) and allow a targeted reduction of the linearity error through a normalization of the raw signals and a correction prior to the ATAN function.

Parameter	Value	Range	Typ.
KAPLHA	0 … 2^16-1	[0..2]	1.4
KBETA	0 … 2^16-1	[0..2]	1.4
KT	0 … 2^16-1	[0..2]	1

Note: when not trimmed by the customer, the values per default of KALPHA and KBETA must be programmed to the TYP. value of 1.4.

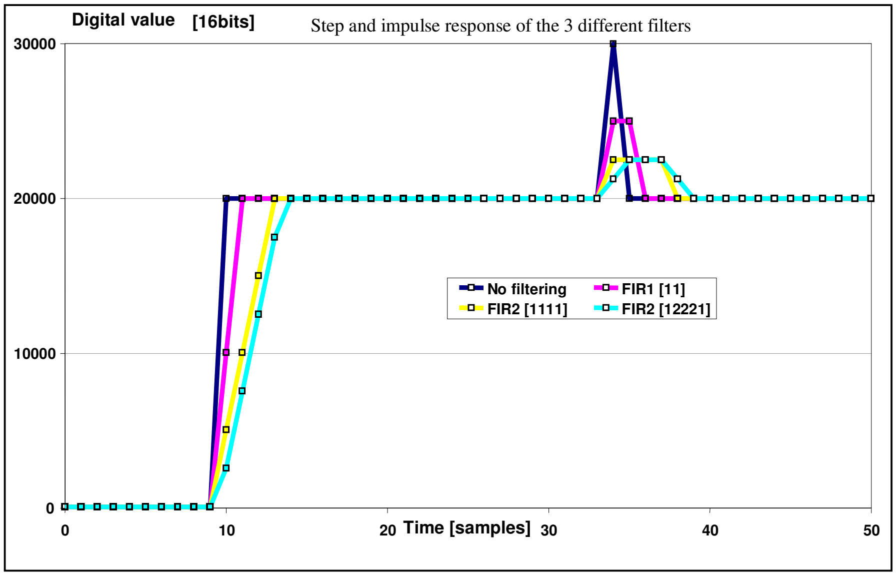
17.5. User Configuration: Filter

The MLX90363 features 3 FIR filter modes controlled with Filter = 1…3. The transfer function is described below:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

The characteristics of the filters No. 0 to 3 is given in the following table.

Filter No. (j)	0	1	2	3
Type	Disable	Finite Impulse Response		
Coefficients a_0… a_5	N/A	11	1111	12221
Title	No Filter	Extra Light	Light	Medium
99% Response Time	1	2	4	5
Efficiency RMS (dB)	0	3.0	6.0	6.6



17.6. Virtual Gain Min and Max Parameters

The MLX90363 automatic gain control (AGC) loop selects the electrical gain code within the user-defined range VIRTUALGAINMIN…VIRTUALGAINMAX. Setting VIRTUALGAINMIN=VIRTUALGAINMAX means setting a fixed gain. The min and max virtual gain codes influence directly the sensitivity of the diagnostics D17-"Field Magnitude Too High" and D18-"Field Magnitude Too Low".

]

17.7. Hysteresis FILTER

Parameter	Value	Note
FHYST	0 … 255	1 LSB = 0.044 deg

The FHYST parameter is a hysteresis filter. The output value of the IC is not updated when the digital step is smaller than the programmed FHYST parameter value. The output value is modified when the increment is bigger than the hysteresis. The hysteresis filter reduces the resolution to a level compatible with the internal noise of the IC. The hysteresis must be programmed to a value close to the noise level.

17.8. EMC Filter on SCI Pins

The EEPROM parameter PINFILTER selects the level of filtering on the serial protocol input pins.

SCI clock frequency	PINFILTER Recommended value for higher EM Immunity
2MHz	1
1MHz	2
500kHz	3

17.9. Identification & FREE bytes

Parameter	Value	Unit
USERID	0..(2^{31}-1)	
FREE	0…(2^{39}-1)	

Identification number: 32 bits freely useable by Customer for traceability purpose.
The FREE bytes can also be used for identification or any other purposes.

17.10. Lock

The calibration parameters of the MLX90363 are locked.
To unlock the write, one must follow the write procedure described in section 14.17.

18. MLX90363 Self Diagnostic

The MLX90363 provides numerous self-diagnostic features which increase the safety integrity level of the IC, by diagnosing and reporting as many as 18 internal and external failure cases.

Diagnostic Item	Action	Bit	Notes
RAM March C- 10N Test	Fail-safe mode	D0	At Startup only
Watchdog BIST	Fail-safe mode	D1	At Startup only
ROM 16 bit Checksum	Fail-safe mode	D2	
RAM Test (continuous)	Fail-safe mode	D3	
CPU Register Functional Test	Fail-safe mode	D4	
EEPROM Calibration parameters (8 bit CRC)	Fail-safe mode	D5	
EEPROM Hamming Code DED (Dual Error Detection)	Fail-safe mode	D6	
EEPROM RAM Cache Error	Report(23)	D7	
ADC Block	Report	D8	Reference Voltage Unit (VCM) + 11 Input Levels
Bz sensitivity monitor(25)	Report (Optional)	D12	See Magnetic Frequency Spec.
Bx sensitivity monitor(25)	Report	D13	See Magnetic Frequency Spec.
By sensitivity monitor(25)	Report	D14	See Magnetic Frequency Spec.
Temperature sensor monitoring (based on redundancy)	Report, temp. value set to EE_T35	D15	
Temperature > 190 deg (± 20deg) Temperature < -80 deg (± 20deg)	Report, saturate temp. value	D16	External failure
Field magnitude too high (*Norm* > 99% ADC Span)(24)	Report	D17	External failure, given that AGC keeps *Norm* below 63.5%
Field magnitude too low (*Norm* < 20% ADC Span)	Report	D18	External failure, given that AGC keeps *Norm* above 47%
ADC clipping (X, Y, Z, two phases each)	Report	D19	External failure
Supply voltage monitor (VDD) and Regulator monitor (VDEC)(25)	Report (Optional)	D20	External failure
Firmware Flow monitoring	Fail-safe mode	n/a	
Read/Write Access out of physical memory	Fail-safe mode	n/a	
Stack Overflow	Fail-safe mode	n/a	
Write Access to protected area (IO and RAM Words)	Fail-safe mode	n/a	
Unauthorized entry in “SYSTEM” Mode	Fail-safe mode	n/a	
Serial Interface Protection Error	NTT Message(26)	n/a	
Watchdog Timeout	Reset(27)	n/a	
Oscillator Frequency (Dedicated SCI Command)	n/a	n/a	Diagnostic performed by master
VDD > MT8V	MISO is HiZ	n/a	100% Hardware detection. No communication possible.

Figure 25 – Diagnostics List

---

[23] Reporting is done through the bits E0 and E1 of the regular messages or the bits Dx of the DiagnosticDetails message. See Table 8 for more details.

[24] *Norm* = max(abs(*X*),abs(*Y*),abs(*Z*))

[25] Diagnostic to be disabled in the 3V3 application diagram (VDD = VDEC).

[26] The NTT Message is followed by an Error Message.

[27] Resetting has the same effects as a POR: the next SO message is therefore *Ready*.

19. MLX90363 Firmware Flowcharts

19.1. Start-up sequence

The entry in operation mode is preceded by a startup phase or startup sequence, performing the built-in self tests (performed only once), the automatic analog gain adjustment, the temperature acquisition and a first execution of the built-in self diagnostics (also performed continuously afterwards). The start-up sequence ends with the enabling of the serial interface.

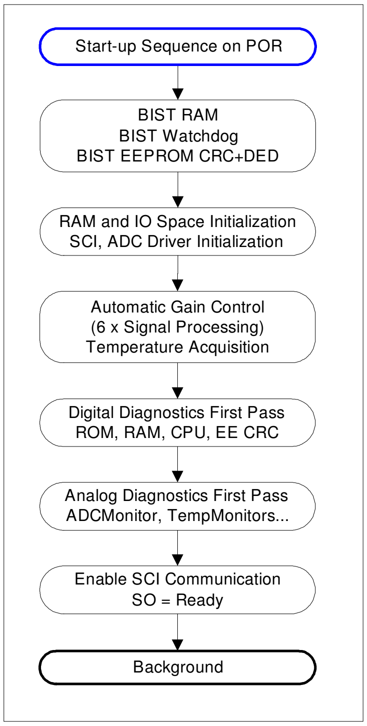

Start-up Sequence on POR
BIST RAM
BIST Watchdog
BIST EEPROM CRC+DED
RAM and IO Space Initialization
SCI, ADC Driver Initialization
Automatic Gain Control
(6 x Signal Processing)
Temperature Acquisition
Digital Diagnostics First Pass
ROM, RAM, CPU, EE CRC
Analog Diagnostics First Pass
ADCMonitor, TempMonitors...
Enable SCI Communication
SO = Ready
Background

Figure 26 – Firmware start-up sequence

19.2. Signal Processing (GETx)

The digital signal processing performed by the firmware is depicted by the following diagram.

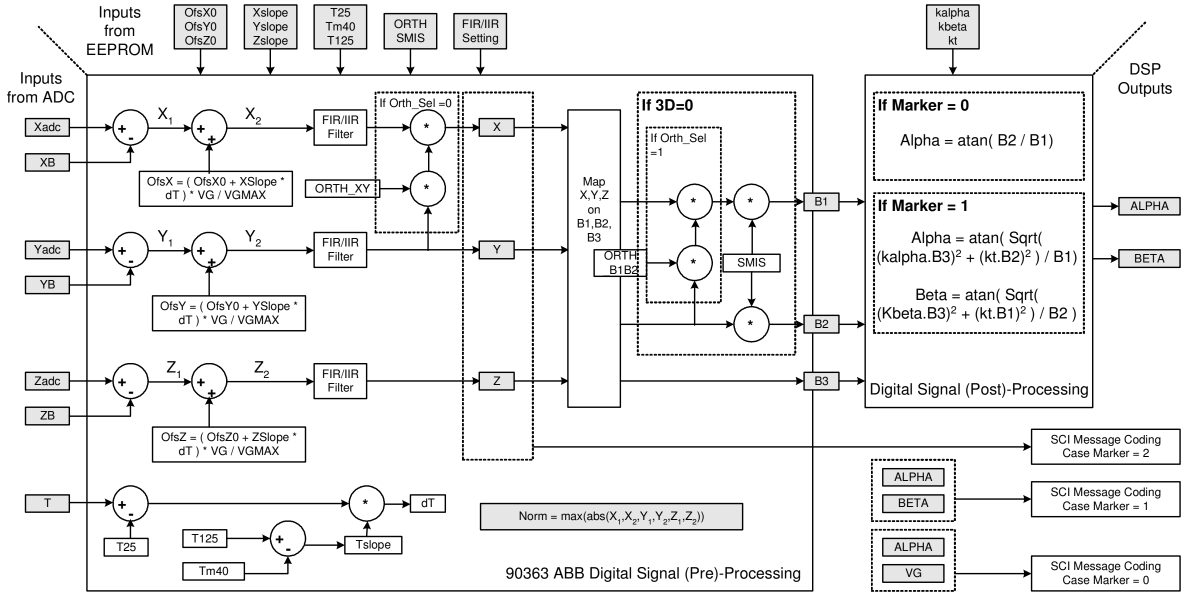

Inputs from EEPROM
OfsX0 OfsY0 OfsZ0
Xslope Yslope Zslope
T25 Tm40 T125
ORTH SMIS
FIR/IIR Setting
kalpha kbeta kt
Inputs from ADC
DSP Outputs
Xadc
XB
Yadc
YB
Zadc
ZB
T
X1
X2
Y1
Y2
Z1
Z2
OfsX = (OfsX0 + XSlope * dT) * VG / VGMAX
OfsY = (OfsY0 + YSlope * dT) * VG / VGMAX
OfsZ = (OfsZ0 + ZSlope * dT) * VG / VGMAX
FIR/IIR Filter
If Orth_Sel =0
ORTH_XY
X
Y
Z
Map X,Y,Z on B1,B2, B3
ORTH B1B2
If 3D=0
If Orth_Sel =1
SMIS
B1
B2
B3
If Marker = 0
Alpha = atan(B2 / B1)
If Marker = 1
Alpha = atan(Sqrt((kalpha.B3)² + (kt.B2)²) / B1)
Beta = atan(Sqrt((Kbeta.B3)² + (kt.B1)²) / B2)
Digital Signal (Post)-Processing
ALPHA
BETA
SCI Message Coding Case Marker = 2
ALPHA
BETA
SCI Message Coding Case Marker = 1
ALPHA
VG
SCI Message Coding Case Marker = 0
T25
T125
Tm40
dT
Tslope
Norm = max(abs(X1,X2,Y1,Y2,Z1,Z2))
90363 ABB Digital Signal (Pre)-Processing

Figure 27 – Block Diagram of Signal Processing – Function model

19.3. Fail-safe Mode

The purpose of fail-safe mode is dual:

1. To increase the safety integrity, by blocking any position calculation and position reporting whenever a critical error (WD error, ROM Checksum, Firmware flow error…) is detected
2. To report the root cause of the failure

In fail-safe mode,

- The analog is [set] inactive
- The sensor waits for the master to initiate a reset
- Autonomous reset by watchdog after 100ms, i.e. watchdog running but will not be acknowledged
- Only SPI driver and communication handler is active. The only supported MOSI commands is
    - sciREBOOT
- Upon all SPI MOSI commands, the MISO message SPI_ERROR (= DiagDetailAnswer) is sent
- Diagnostics (analog and digital) and background are not running

Fail-safe mode – entry conditions

The fail-safe mode is entered upon:

- Critical error during initialization (RAM BIST, WD BIST, ROM Checksum, EEPROM CRC)
- Critical error during background/digital diagnostics (RAM continuous test, ROM test, EEPROM CRC)
- Exception, i.e. system level interrupts (Stack-overflow, invalid address, protection error, program error)
- FW flow error

19.4. Automatic Gain Control

The Virtual Gain code is updated at every *GET* message. The new code value is based on the field strength (Norm) of every raw component (X, Y, Z).

The Automatic Gain Control (AGC) makes sure that Norm is between 47% and 63.5%, by controlling the gain code within the range (VIRTUALGAINMIN, VIRTUALGAINMAX).

The algorithm gives a limitation in term flux density frequency, see Section 10 for specification.

It is not recommended to interrupt the GET message sequence, because AGC iterations are triggered by *GET* messages. If a pause cannot be avoided, the (E1, E0) error bits of the 6 following *GET* messages shall be ignored.

20. Recommended Application Diagrams

20.1. MLX90363 in SOIC-8 Package and 5V Application Diagrams

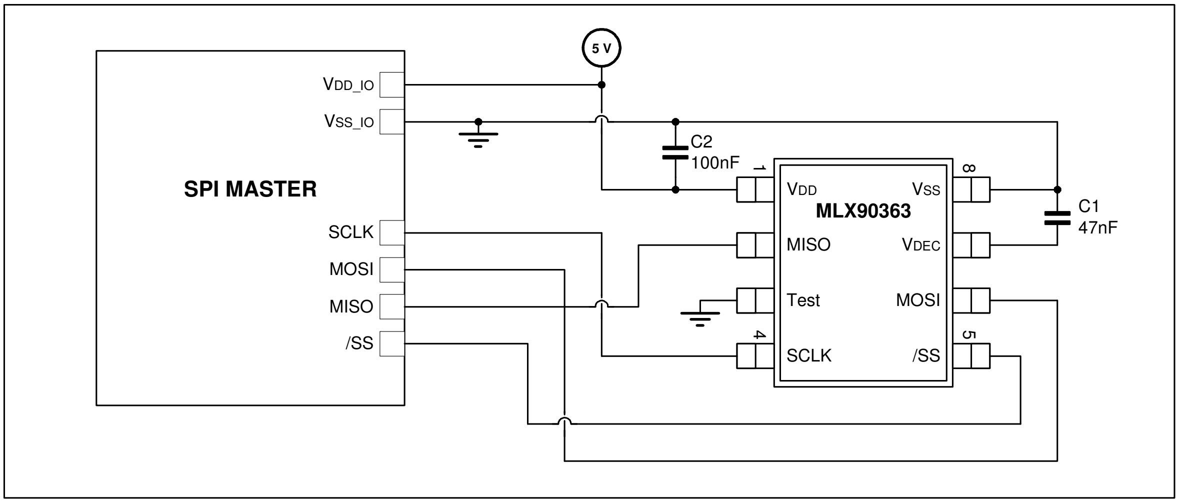

5 V
VDD_IO
VSS_IO
SPI MASTER
SCLK
MOSI
MISO
/SS
C2
100nF
1
8
4
5
VDD
VSS
MLX90363
MISO
VDEC
Test
MOSI
SCLK
/SS
C1
47nF

Figure 28 – Recommended wiring[28] for the MLX90363 in SOIC8 package and 5V Application Diagrams.

20.2. MLX90363 in SOIC-8 Package and 3V3 Application Diagrams

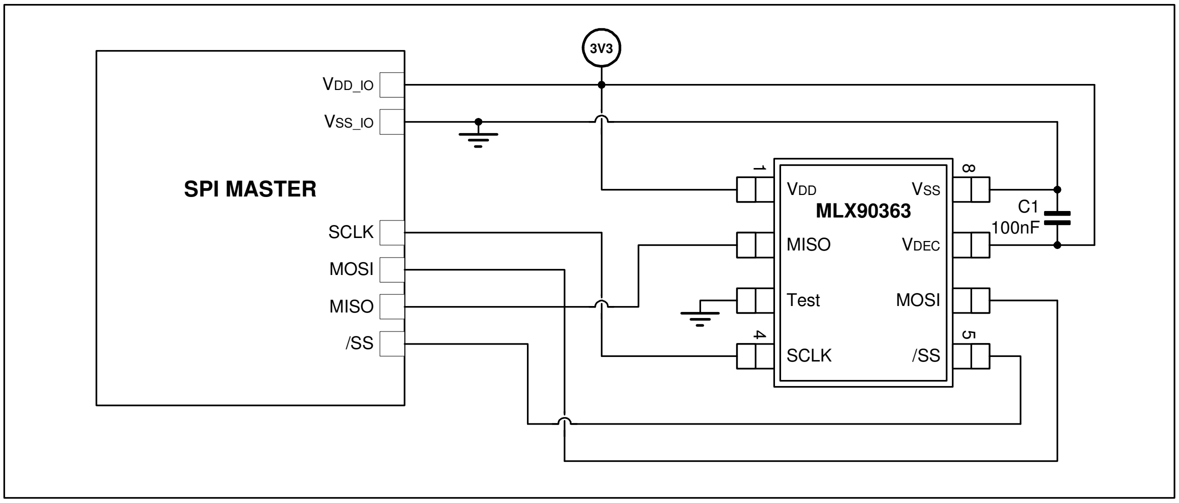

3V3
VDD_IO
VSS_IO
SPI MASTER
SCLK
MOSI
MISO
/SS
1
8
4
5
VDD
VSS
MLX90363
MISO
VDEC
Test
MOSI
SCLK
/SS
C1
100nF

Figure 29 – Recommended wiring[28] for the MLX90363 in SOIC8 package and 3V3 Application Diagrams.

---

[28] Wiring of the SCI signals must be kept short on the PCB. In other cases, Melexis advises to add 100Ω serial resistor on the SCLK, MOSI, MISO and /SS lines. Melexis also recommends doubling the C1 decoupling capacitor.

20.3. MLX90363 in TSSOP-16 Package and 5V Application Diagrams

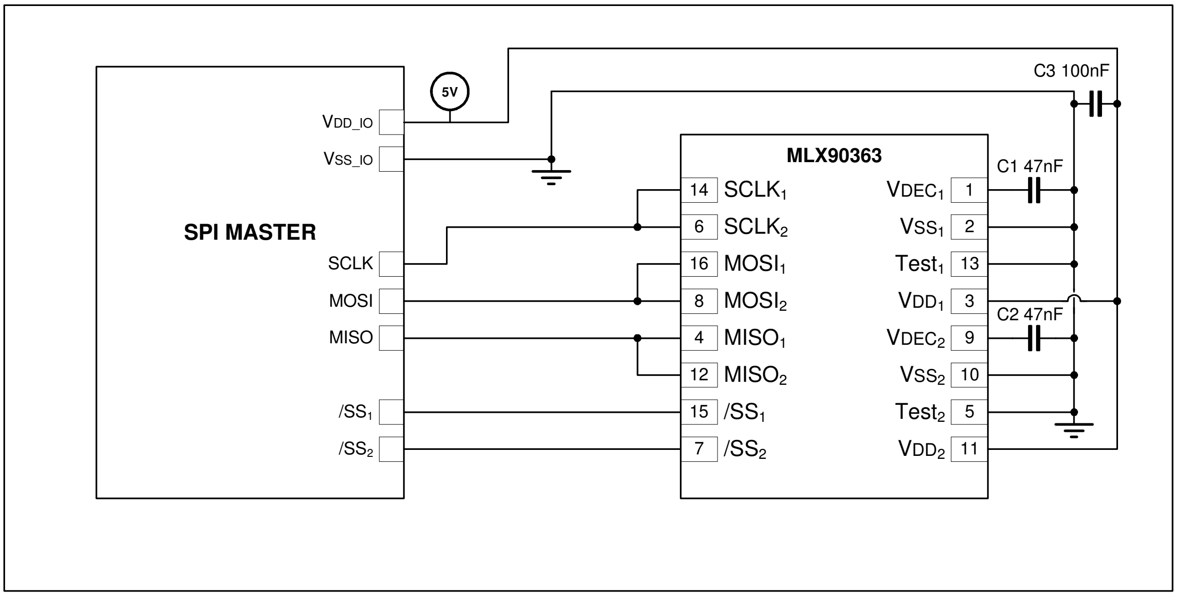

5V
VDD_IO
VSS_IO
SPI MASTER
SCLK
MOSI
MISO
/SS1
/SS2
MLX90363
14 SCLK1
6 SCLK2
16 MOSI1
8 MOSI2
4 MISO1
12 MISO2
15 /SS1
7 /SS2
VDEC1 1
VSS1 2
Test1 13
VDD1 3
VDEC2 9
VSS2 10
Test2 5
VDD2 11
C3 100nF
C1 47nF
C2 47nF

Figure 30 – Recommended(29) wiring for the MLX90363 in TSSOP16 package (dual die) and 5V Application Diagrams.

---

[29] Wiring of the SCI signals must be kept short on the PCB. In other cases, Melexis advises to add 100Ω serial resistor on the SCLK, MOSI, MISO and /SS lines. Melexis also recommends to double the C1,C2 decoupling capacitors.

20.4. MLX90363 in TSSOP-16 Package and 3V3 Application Diagrams

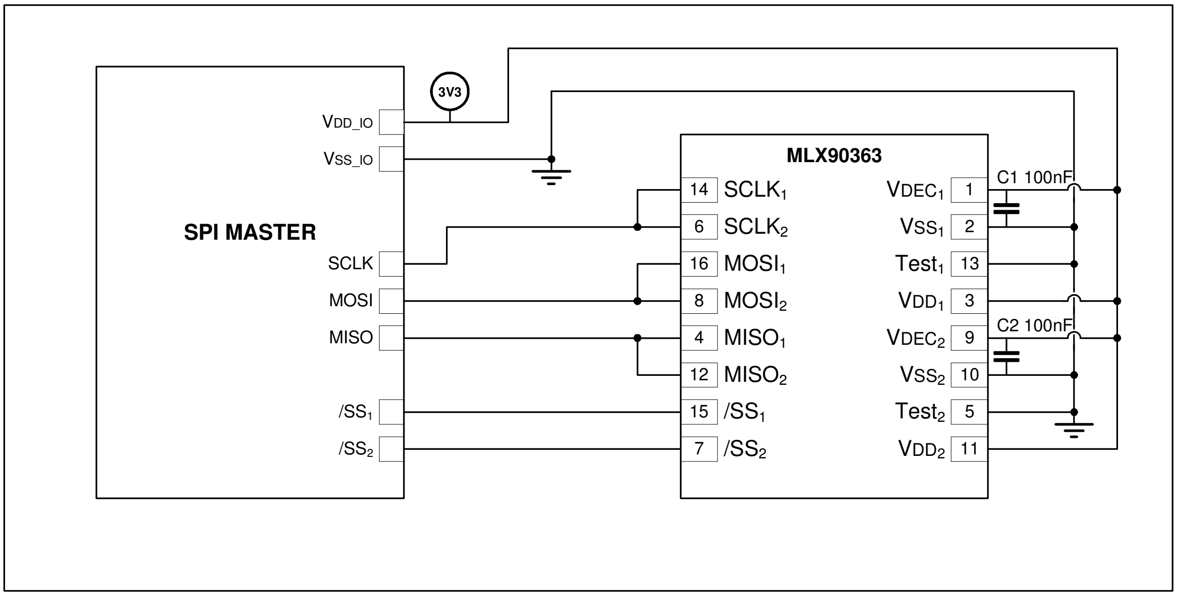

3V3
SPI MASTER
VDD_IO
VSS_IO
SCLK
MOSI
MISO
/SS1
/SS2
MLX90363
14 SCLK1
6 SCLK2
16 MOSI1
8 MOSI2
4 MISO1
12 MISO2
15 /SS1
7 /SS2
VDEC1 1
VSS1 2
Test1 13
VDD1 3
VDEC2 9
VSS2 10
Test2 5
VDD2 11
C1 100nF
C2 100nF

Figure 31 – Recommended(29) wiring for the MLX90363 in TSSOP16 package (dual die) and 3V3 Application Diagrams

21. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

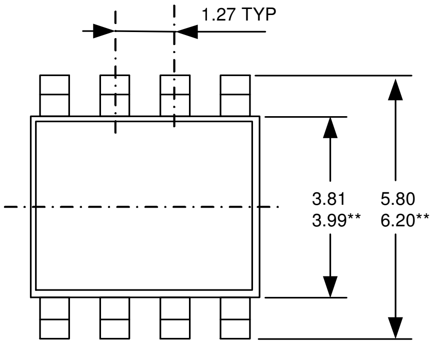
Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.aspx

22. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

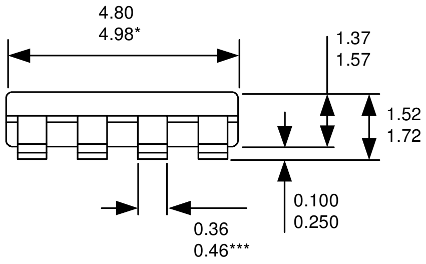
23. Package Information

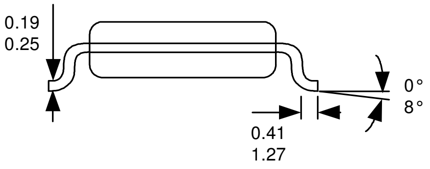
23.1. SOIC8 – Package Dimensions


1.27 TYP
3.81
3.99**
5.80
6.20**

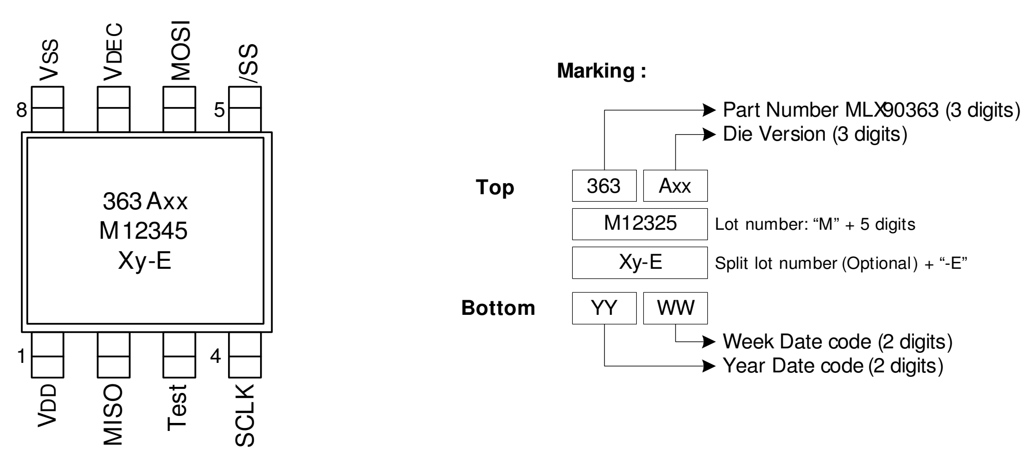
NOTES:

All dimensions are in millimeters (anlges in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

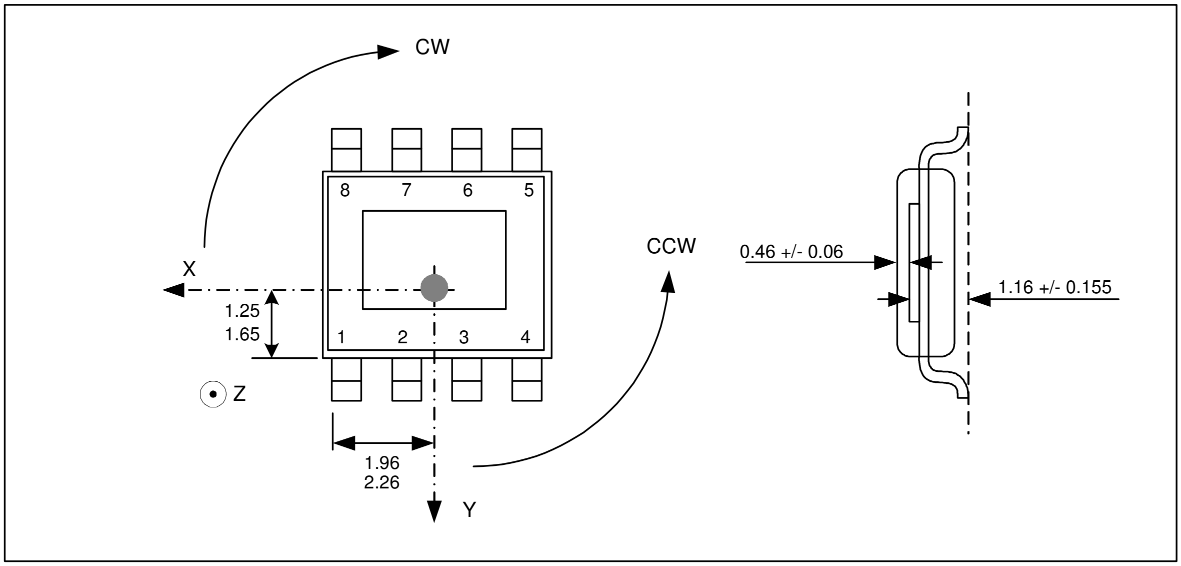

4.80
4.98*
1.37
1.57
1.52
1.72
0.100
0.250
0.36
0.46***

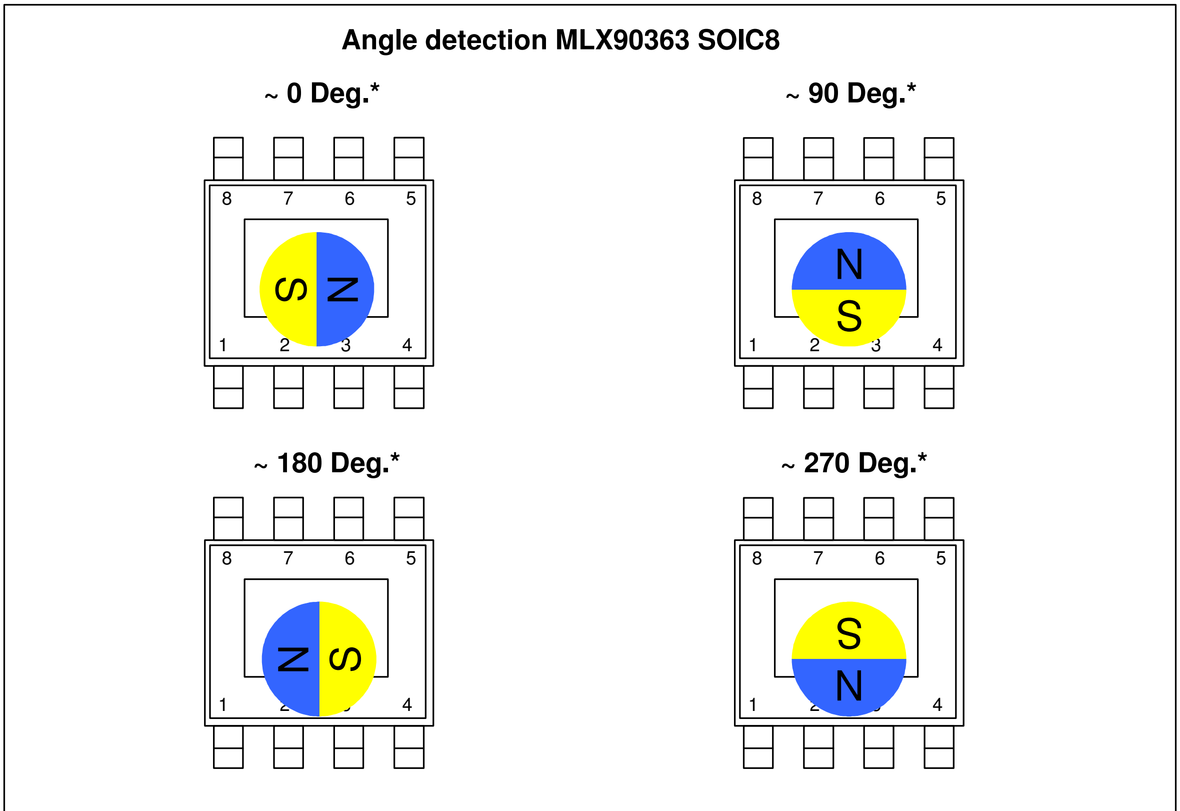

0.19
0.25
0°
8°
0.41
1.27

23.2. SOIC8 – Pinout and Marking


VSS
VDEC
MOSI
/SS
8
5
363 Axx
M12345
Xy-E
1
4
VDD
MISO
Test
SCLK
Marking :
Part Number MLX90363 (3 digits)
Die Version (3 digits)
Top
363
Axx
M12325
Lot number: “M” + 5 digits
Xy-E
Split lot number (Optional) + “-E”
Bottom
YY
WW
Week Date code (2 digits)
Year Date code (2 digits)

23.3. SOIC8 – IMC Positionning

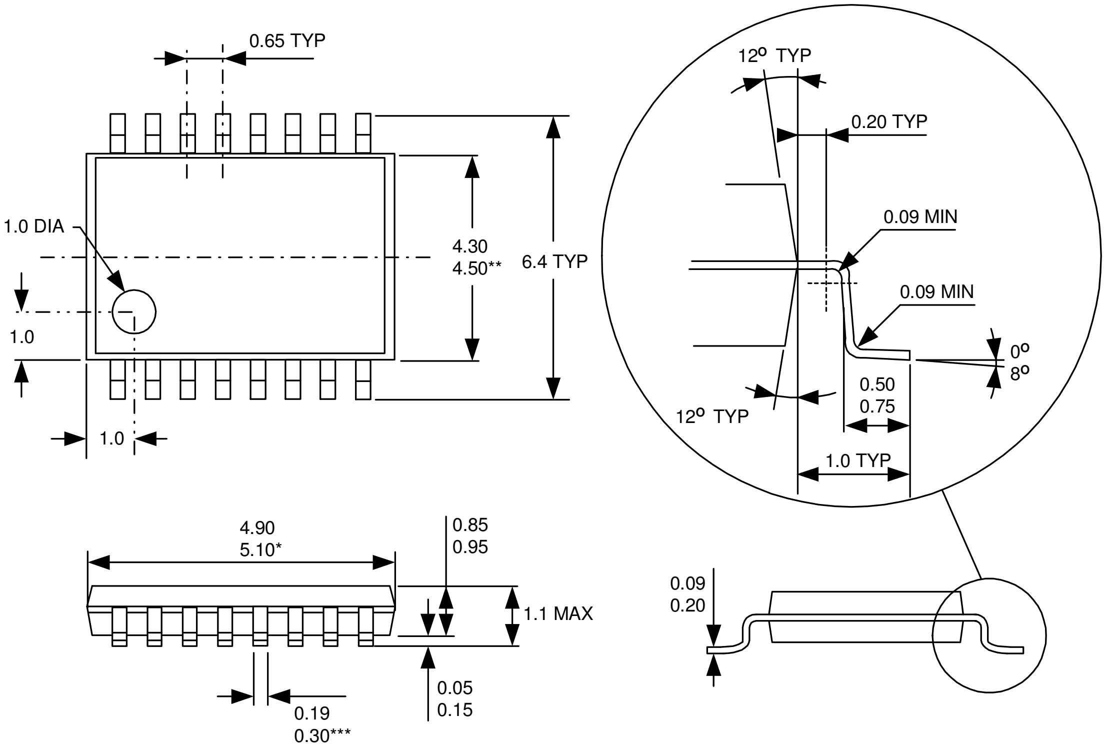

CW
8
7
6
5
CCW
0.46 +/- 0.06
X
1.25
1.65
1.16 +/- 0.155
1
2
3
4
Z
1.96
2.26
Y


Angle detection MLX90363 SOIC8
~ 0 Deg.*
~ 90 Deg.*
~ 180 Deg.*
~ 270 Deg.*
8
7
6
5
1
2
3
4
S
N

* No absolute reference for the angular information.

The MLX90363 is an absolute angular position sensor but the linearity error (Le – See Section 11) does not include the error linked to the absolute reference 0 Deg.

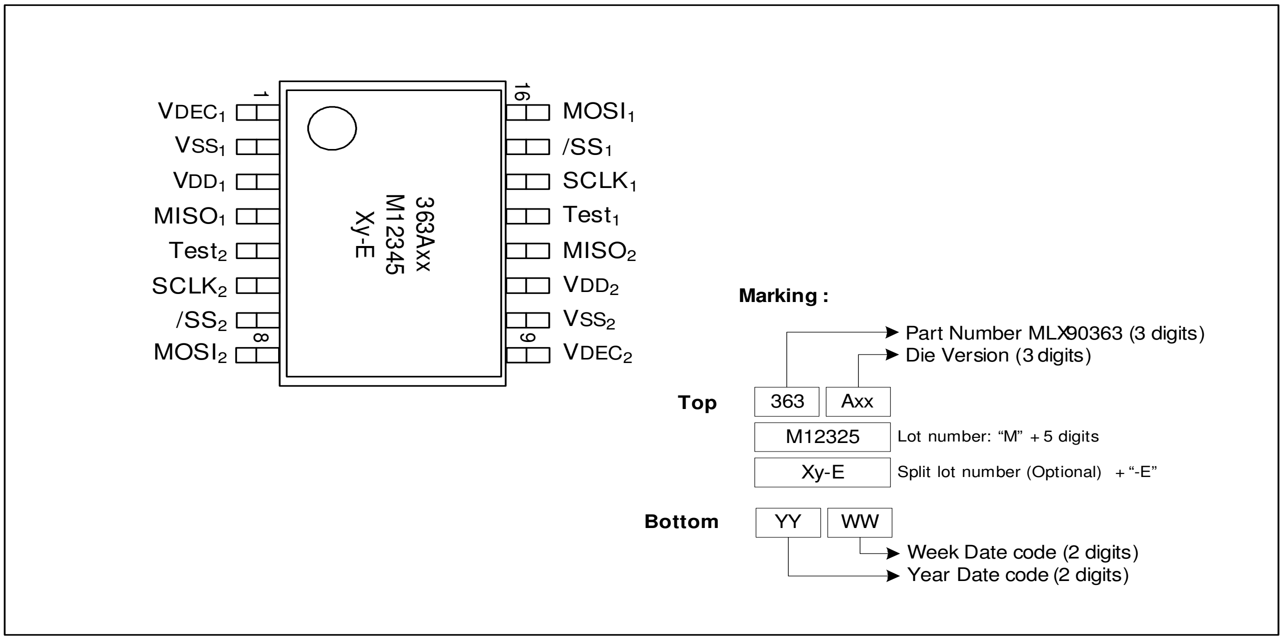
23.4. TSSOP16 – Package Dimensions


0.65 TYP
1.0 DIA
1.0
1.0
4.30
4.50**
6.4 TYP
12° TYP
0.20 TYP
0.09 MIN
0.09 MIN
0°
8°
0.50
0.75
12° TYP
1.0 TYP
4.90
5.10*
0.85
0.95
1.1 MAX
0.19
0.30***
0.05
0.15
0.09
0.20

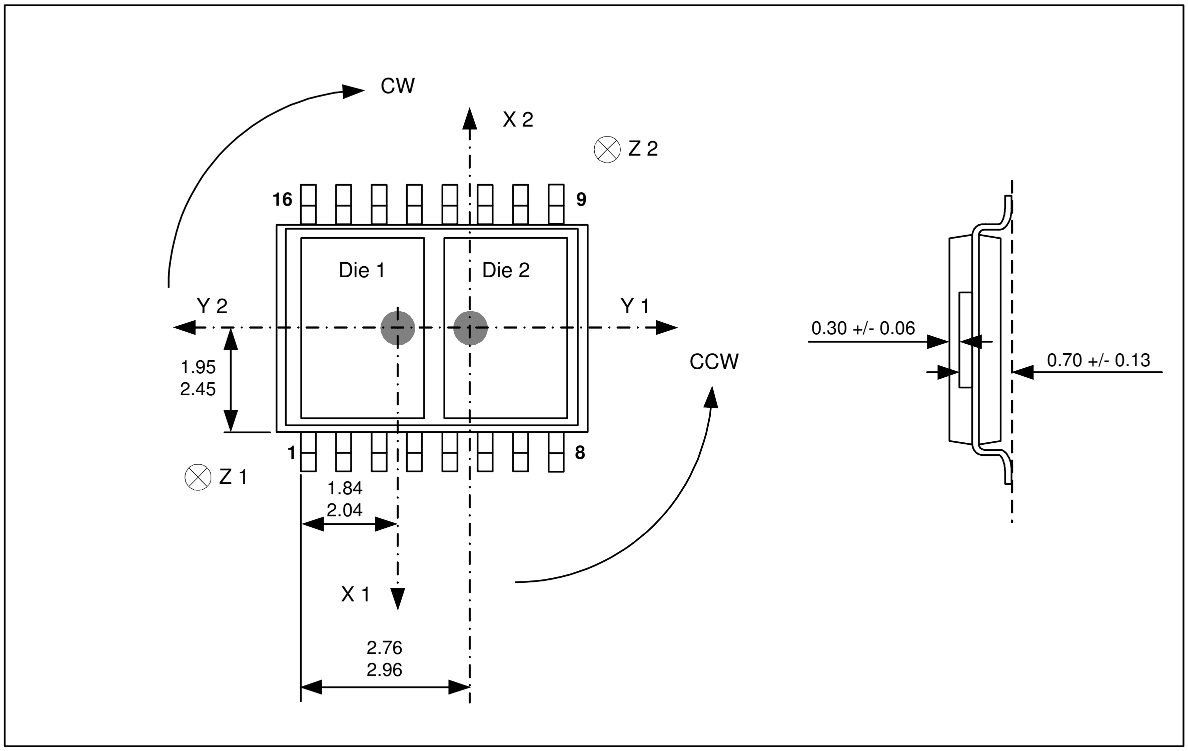
NOTES:

All dimensions are in millimeters (anlges in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

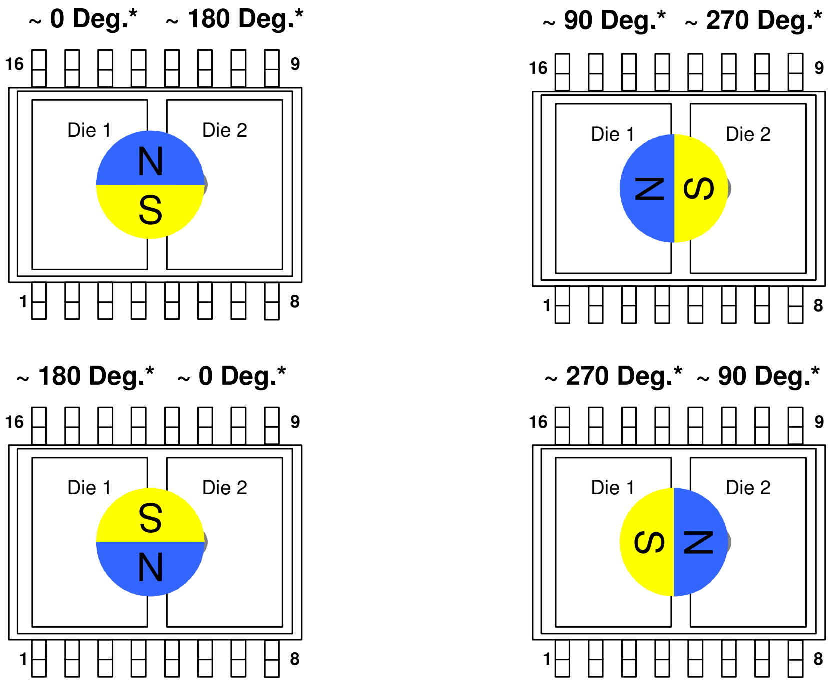
23.5. TSSOP16 – Pinout and Marking


VDEC$_1$
VSS$_1$
VDD$_1$
MISO$_1$
Test$_2$
SCLK$_2$
/SS$_2$
MOSI$_2$
1
8
16
9
MOSI$_1$
/SS$_1$
SCLK$_1$
Test$_1$
MISO$_2$
VDD$_2$
VSS$_2$
VDEC$_2$
363Axx
M12345
Xy-E
Marking :
Part Number MLX90363 (3 digits)
Die Version (3 digits)
Top
363
Axx
M12325
Lot number: "M" + 5 digits
Xy-E
Split lot number (Optional) + "-E"
Bottom
YY
WW
Week Date code (2 digits)
Year Date code (2 digits)

23.6. TSSOP16 – IMC Positionning


CW
X 2
Z 2
16
9
Die 1
Die 2
Y 2
Y 1
1.95
2.45
CCW
1
8
Z 1
1.84
2.04
X 1
2.76
2.96
0.30 +/- 0.06
0.70 +/- 0.13

Angle detection MLX90363 TSSOP16


~ 0 Deg.*
~ 180 Deg.*
~ 90 Deg.*
~ 270 Deg.*
~ 180 Deg.*
~ 0 Deg.*
~ 270 Deg.*
~ 90 Deg.*
16
9
1
8
Die 1
Die 2
N
S

* No absolute reference for the angular information.

The MLX90363 is an absolute angular position sensor but the linearity error (Le – See Section 11) does not include the error linked to the absolute reference 0 Deg.

24. Disclaimer

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