

## Hysteretic Boost-Buck (Ćuk) LED Driver IC

### Features

- Constant Current LED Driver
- Steps Input Voltage Up or Down
- Low Electromagnetic Interference (EMI)
- Variable Frequency Operation
- Internal 75V Linear Regulator
- Input and Output Current Sensing
- Input Current Limit
- Enable and Pulse-width Modulation (PWM) Dimming
- Ambient Temperature Rating of up to 125°C

### Applications

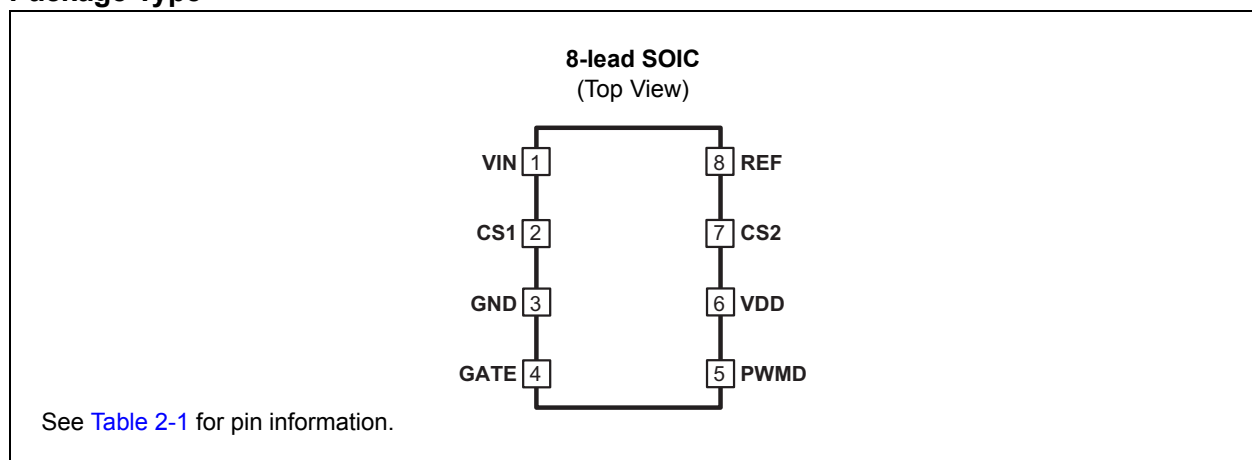
- LED Lighting Applications

### General Description

The AT9933 is a variable frequency PWM controller IC, designed to control an LED lamp driver using a low-noise boost-buck (Ćuk) topology. It uses patent-pending Hysteretic Current-mode control to regulate both the input and the output currents. This enables superior input surge immunity without the necessity for complex loop compensation. Input current control enables current limiting during Startup, Input Undervoltage and Output Overload conditions. The AT9933 provides a low-frequency PWM dimming input that can accept an external control signal with a duty cycle of 0%–100% and a high dimming ratio.

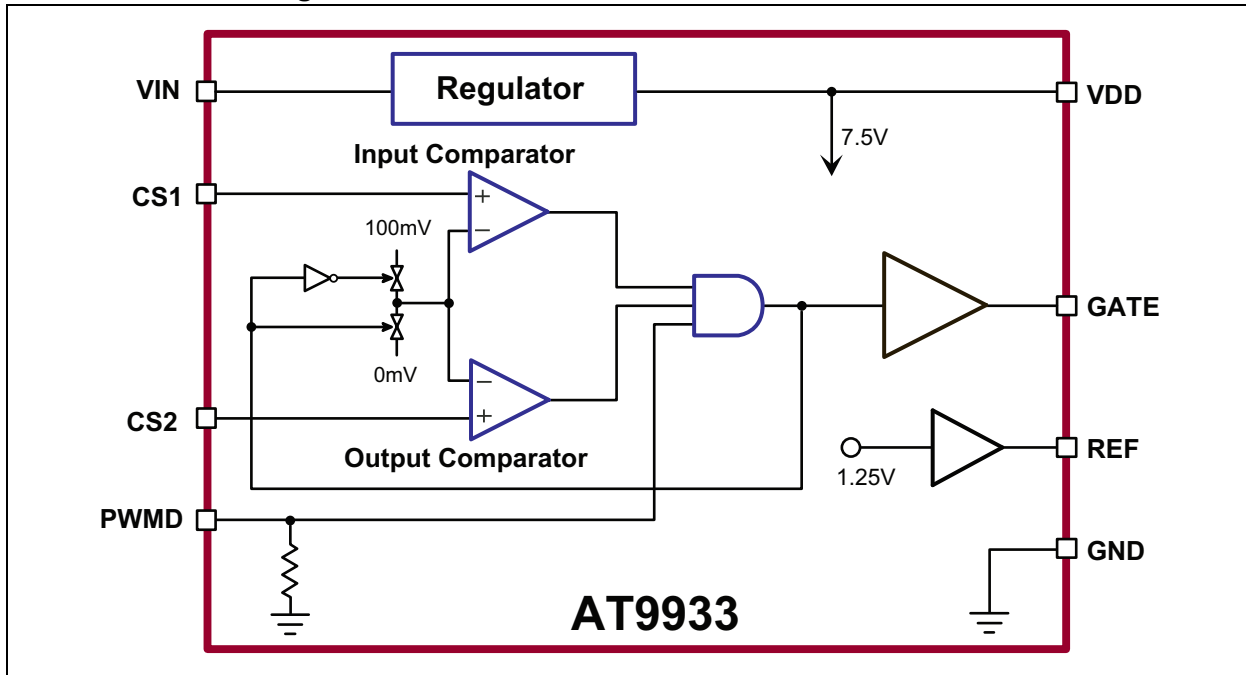
This AT9933-based LED driver is ideal for LED lamps. The part is rated for up to 125°C ambient temperatures.

### Package Type

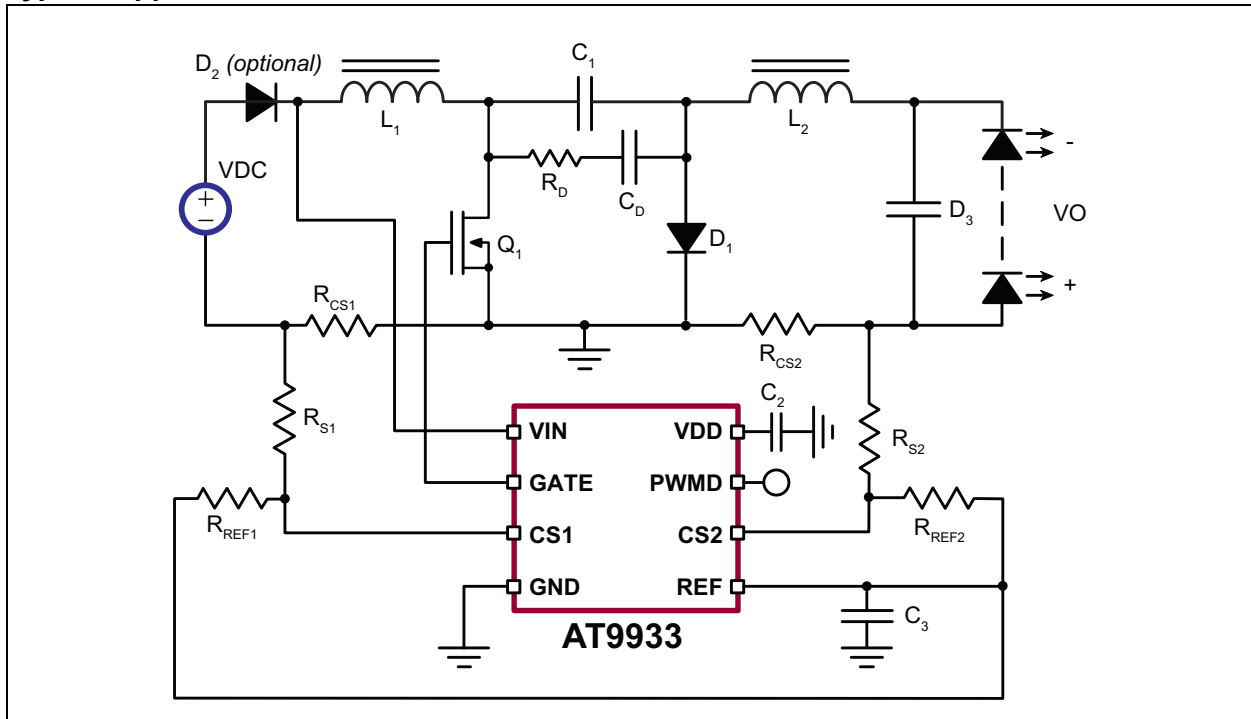


# AT9933

## Functional Block Diagram



## Typical Application Circuit



# AT9933

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

$V_{IN}$ to GND .....	-0.5V to +75V
CS1, CS2, PWMD and GATE to GND .....	-0.3V to $V_{DD}$ +0.3V
$V_{DD(MAX)}$ .....	+12V
Operating Temperature Range .....	-40°C to +125°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Continuous Power Dissipation ( $T_A = +25^\circ\text{C}$ ):	
8-lead SOIC .....	700 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = \text{Open}$  and  $V_{DD} = 7.5\text{V}$  unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>INPUT</b>						
Input DC Supply Voltage Range	$V_{INDC}$	Note 3	—	75	V	DC input voltage (Note 1 and Note 2)
Shutdown Mode Supply Current	$I_{NSD}$	—	0.5	1	mA	PWMD connected to GND, $V_{IN} = 12\text{V}$ (Note 2)
<b>INTERNAL REGULATOR</b>						
Internally Regulated Voltage	$V_{DD}$	7	7.5	9	V	$V_{IN} = 8\text{V}-75\text{V}$ , $I_{DD(EXT)} = 0$ , 500 pF capacitor at GATE, PWMD = GND (Note 1)
$V_{DD}$ Undervoltage Lockout Threshold	UVLO	6.35	6.7	7.05	V	$V_{DD}$ rising (Note 1)
$V_{DD}$ Undervoltage Lock-out Hysteresis	$\Delta\text{UVLO}$	—	500	—	mV	
<b>REFERENCE</b>						
REF Pin Voltage $0^\circ\text{C} < T_A < +85^\circ\text{C}$	$V_{REF}$	1.212	1.25	1.288	V	REF bypassed with a 0.1 $\mu\text{F}$ capacitor to GND, $I_{REF} = 0$ , PWMD = 5V
REF Pin Voltage $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.187	1.25	1.312		
Line Regulation of Reference Voltage	$V_{REFLINE}$	0	—	20	mV	REF bypassed with a 0.1 $\mu\text{F}$ capacitor to GND, $I_{REF} = 0$ , $V_{DD} = 7\text{V}-9\text{V}$ , PWMD = 5V
Reference Output Current Range	$I_{REF}$	-0.01	—	500	$\mu\text{A}$	REF bypassed with a 0.1 $\mu\text{F}$ capacitor to GND, $I_{REF} = 0$ , $V_{DD} = 7\text{V}-9\text{V}$ , PWMD = 5V
Load Regulation of Reference Voltage	$V_{REFLOAD}$	0	—	10	mV	REF bypassed with a 0.1 $\mu\text{F}$ capacitor to GND, $I_{REF} = 0 \mu\text{A}-500 \mu\text{A}$ , PWMD = 5V
<b>PWM DIMMING</b>						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	$V_{DD} = 7\text{V}-9\text{V}$ (Note 1)
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	$V_{DD} = 7\text{V}-9\text{V}$ (Note 1)

**Note 1:** Specifications apply over the full operating ambient temperature range of  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ .

**2:** Also limited by package power dissipation limit, whichever is lower

**3:** Depends on the current drawn by the part. See [Section 4.0 “Application Information”](#)

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Specifications are at $T_A = 25^\circ\text{C}$ , $V_{IN} = \text{Open}$ and $V_{DD} = 7.5\text{V}$ unless otherwise noted.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PWMD Pull-down Resistance	$R_{PWMD}$	50	100	150	k $\Omega$	$V_{PWMD} = 5\text{V}$
<b>GATE DRIVER</b>						
GATE Short Circuit Current	$I_{SOURCE}$	0.165	—	—	A	$V_{GATE} = 0\text{V}$
GATE Sinking Current	$I_{SINK}$	0.165	—	—	A	$V_{GATE} = V_{DD}$
GATE Output Rise Time	$T_{RISE}$	—	30	50	ns	$C_{GATE} = 500\text{ pF}$
GATE Output Fall Time	$T_{FALL}$	—	30	50	ns	$C_{GATE} = 500\text{ pF}$
<b>INPUT CURRENT SENSE COMPARATOR</b>						
Voltage required to turn on GATE	$V_{TURNON1}$	85	100	115	mV	$C_{S2} = 200\text{ mV}$ , $C_{S1}$ increasing, GATE goes LOW to HIGH ( <b>Note 1</b> )
Voltage required to turn off GATE	$V_{TURN-OFF1}$	-15	0	15	mV	$C_{S2} = 200\text{ mV}$ , $C_{S1}$ decreasing, GATE goes HIGH to LOW ( <b>Note 1</b> )
Delay to Output (Turn-on)	$T_{D1,ON}$	—	150	250	ns	$C_{S2} = 200\text{ mV}$ , $C_{S1} = 50\text{ mV}$ to +200 mV step
Delay to Output (Turn-off)	$T_{D1,OFF}$	—	150	250	ns	$C_{S2} = 200\text{ mV}$ , $C_{S1} = 50\text{ mV}$ to -100 mV step
<b>OUTPUT CURRENT SENSE COMPARATOR</b>						
Voltage required to turn on GATE	$V_{TURNON2}$	85	100	115	mV	$C_{S1} = 200\text{ mV}$ , $C_{S2}$ increasing, GATE goes LOW to HIGH ( <b>Note 1</b> )
Voltage required to turn off GATE	$V_{TURN-OFF2}$	-15	0	15	mV	$C_{S1} = 200\text{ mV}$ , $C_{S2}$ decreasing, GATE goes HIGH to LOW ( <b>Note 1</b> )
Delay to Output (Turn-on)	$T_{D2,ON}$	—	150	250	ns	$C_{S1} = 200\text{ mV}$ , $C_{S2} = 50\text{ mV}$ to +200 mV step
Delay to Output (Turn-off)	$T_{D2,OFF}$	—	150	250	ns	$C_{S1} = 200\text{ mV}$ , $C_{S2} = 50\text{ mV}$ to -100 mV step

**Note 1:** Specifications apply over the full operating ambient temperature range of  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ .

**Note 2:** Also limited by package power dissipation limit, whichever is lower

**Note 3:** Depends on the current drawn by the part. See [Section 4.0 "Application Information"](#)

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Temperature	$T_A$	-40	—	+125	$^\circ\text{C}$	
Junction Temperature	$T_J$	—	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-65	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
8-lead SOIC	$\theta_{JA}$	—	+101	—	$^\circ\text{C/W}$	<b>Note 1</b>

**Note 1:** Mounted on a FR-4 board, 25 mm x 25 mm x 1.57 mm

# AT9933

---

## 2.0 PIN DESCRIPTION

The details on the pins of AT9933 are listed on [Table 2-1](#). Refer to [Package Type](#) for the location of the pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	VIN	This pin is the input of an 8V–75V voltage regulator.
2	CS1	This pin is used to sense the input and output currents of the boost-buck converter. It is a non-inverting input of the internal comparator.
3	GND	This is the ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output gate driver for an external N-channel power Metal-oxide Semiconductor Field-effect Transistor (MOSFET).
5	PWMD	When this pin is left open or pulled to GND, the gate driver is disabled. Pulling the pin to a voltage greater than 2V will enable the gate driver output.
6	VDD	This is a power supply pin for all internal circuits. It must be bypassed to GND with a low-ESR capacitor greater than 0.1 $\mu$ F.
7	CS2	This pin is used to sense the input and output currents of the boost-buck converter. It is a non-inverting input of the internal comparator.
8	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 $\mu$ F–0.1 $\mu$ F capacitor to GND.

## 3.0 DETAILED DESCRIPTION

### 3.1 Power Topology

The AT9933 is optimized to drive a Continuous Conduction Mode (CCM) boost-buck DC/DC converter topology commonly referred to as Ćuk converter. (Refer to [Typical Application Circuit](#).) This power converter topology offers numerous advantages useful for driving high-brightness light-emitting diodes (HB LED). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The output load is decoupled from the input voltage with a capacitor, making the driver inherently failure-safe for the output load.

The AT9933 offers a simple and effective control technique for a boost-buck LED driver. It uses two Hysteretic mode controllers—one for the input and one for the output. The outputs of these two hysteretic comparators are ANDED and used to drive the external FET. This control scheme gives accurate current control and constant output current in the presence of input voltage transients without the need for complicated loop design.

### 3.2 Input Voltage Regulator

The AT9933 can be powered directly from its  $V_{IN}$  pin that can withstand a maximum voltage of up to 75V. When a voltage is applied to the  $V_{IN}$  pin, the AT9933 seeks to regulate a constant 7.5V (typical) at the  $V_{DD}$  pin. The regulator also has a built-in undervoltage lockout which shuts off the IC when the voltage at the  $V_{DD}$  pin falls below the UVLO threshold.

The  $V_{DD}$  pin must be bypassed by a low-ESR capacitor ( $\geq 0.1 \mu\text{F}$ ) to provide a low-impedance path for the high frequency current of the output gate driver.

The input current drawn from the  $V_{IN}$  pin is the sum of the 1 mA current drawn by the internal circuit and the current drawn by the gate driver, which in turn depends on the switching frequency and the gate charge of the external FET. Refer to [Equation 3-1](#).

#### EQUATION 3-1:

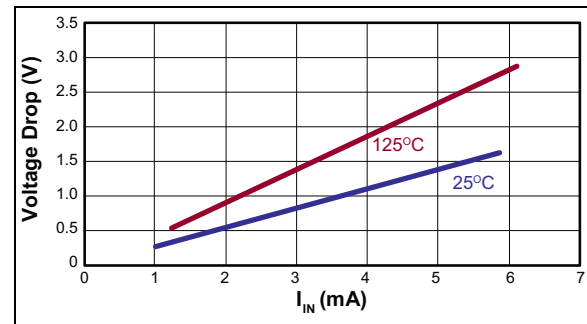
$$I_{IN} = 1\text{mA} + Q_G \times f_S$$

In the above equation,  $f_S$  is the switching frequency, and  $Q_G$  is the gate charge of the external FET which can be obtained from the data sheet of the FET.

### 3.3 Minimum Input Voltage at $V_{IN}$ Pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will control the voltage at the  $V_{DD}$  pin when  $V_{IN}$  is between 8V and 75V. However, when the  $V_{IN}$  is less than 8V, the converter will still function as long as

the  $V_{DD}$  is greater than the undervoltage lockout. Thus, under certain conditions, the converter will be able to start at  $V_{IN}$  voltages of less than 8V. The start/stop voltages at the  $V_{IN}$  pin can be determined using the maximum voltage drop across the linear regulator as a function of the current drawn. The data for ambient temperatures 25°C and 125°C are shown in [Figure 3-1](#) below:



**FIGURE 3-1:** Maximum Voltage Drop vs. Input Current.

Assume an ambient temperature of 125°C. Provided that the IC is driving a 15 nC gate charge FET at 300 kHz, the total input current is estimated to be 5.5 mA (using [Equation 3-1](#)). At this input current, the maximum voltage drop from [Figure 3-1](#) can be approximately estimated to be  $V_{DROP} = 2.7\text{V}$ . However, before the IC starts switching, the current drawn will be 1 mA. At this current level, the voltage drop is approximately  $V_{DROP1} = 0.5\text{V}$ . Thus, the start/stop  $V_{IN}$  voltages can be computed as shown in [Equation 3-2](#) and [Equation 3-3](#):

#### EQUATION 3-2:

$$\begin{aligned} V_{IN-START} &= UVLO_{MAX} + V_{DROP1} \\ &= 6.95\text{V} + 0.5\text{V} \\ &= 7.45\text{V} \end{aligned}$$

#### EQUATION 3-3:

$$\begin{aligned} V_{IN-STOP} &= UVLO_{MAX} - \Delta UVLO + V_{DROP} \\ &= 6.95\text{V} - 0.5\text{V} + 2.7\text{V} \\ &= 9.15\text{V} \end{aligned}$$

**Note:** Since the gate driver draws too much current in this situation,  $V_{IN-START}$  is less than  $V_{IN-STOP}$ . The control IC will oscillate between on and off if the input voltage is between the start and stop voltages. In these circumstances, it is recommended that the input voltage be kept higher than  $V_{IN-STOP}$ . The IC will operate normally if the input voltage is kept higher than 9.2V.

# AT9933

---

In case of input transients that reduce the input voltage below 8V (e.g. Cold Crank condition in an automotive system), the  $V_{IN}$  pin of the AT9933 can be connected to the MOSFET drain through a switching diode using a small (1 nF) capacitor between  $V_{IN}$  and GND as long as the drain voltage does not exceed 75V. Since the drain of the FET is at a voltage equal to the sum of the input and output voltages, the IC will still be operational when the input goes below 8V. Therefore, a larger capacitor is needed at the  $V_{DD}$  pin to supply power to the IC when the MOSFET is switched on.

In this case,  $V_{DD\ UVLO}$  cannot be relied upon to turn off the IC at low input voltages when input current levels can get too large. In such cases, the input current limit must be chosen to ensure that the input current is set to a safe level.

## 3.4 Reference

An internally trimmed voltage reference of 1.25V is provided at the REF pin. The reference can supply a maximum output current of 500  $\mu$ A to drive external resistor dividers.

This reference can be used to set the current thresholds of the two comparators as shown in the [Typical Application Circuit](#) section.

## 3.5 Current Comparators

The AT9933 features two identical comparators with a built-in 100 mV hysteresis. When the GATE is low, the inverting terminal is connected to 100 mV, but when the GATE is high, it is connected to GND. One comparator is used for the input current control and the other for the output current control.

The input side hysteretic controller is in operation during Start-up, Overload and Input Undervoltage conditions. This ensures that the input current never exceeds the designed value. During normal operation, the input current is less than the programmed current. Therefore, the output of the input side comparator will be high. The output of the AND gate will then be dictated by the output current controller.

The output side hysteretic comparator controls the external MOSFET during Steady state operation of the circuit. This comparator turns the MOSFET on and off based on the LED current.

## 3.6 PWM Dimming

PWM Dimming can be achieved by applying a TTL-compatible square wave signal to the PWM pin. When the PWMD pin is pulled high, the gate driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the gate driver is disabled and the external MOSFET turns off. The signal at the PWMD pin inhibits the driver only and the IC need not go through the entire start-up cycle

each time, ensuring a quick response time for the output current. The recommended PWM dimming frequency range is from 100 Hz to a few kilohertz.

The flying capacitor in the Cuk converter ( $C_1$ ) is initially charged to the input voltage VDC (through diodes  $D_1$  and  $D_2$ ). When the circuit is turned on and reaches Steady state, the voltage across  $C_1$  will be  $VDC+VO$ . In the absence of diode  $D_2$ , when the circuit is turned off, capacitor  $C_1$  will discharge through the LEDs and the input voltage source VDC. Thus, during PWM dimming, if capacitor  $C_1$  has to be charged and discharged each cycle, the transient response of the circuit will be limited. By adding diode  $D_2$ , the voltage across capacitor  $C_1$  is held at  $VDC+VO$  even when the circuit is turned off, enabling the circuit to return quickly to its Steady state (and bypassing the start-up stage) upon being enabled.



## 4.0 APPLICATION INFORMATION

### 4.1 Overvoltage Protection

Overvoltage protection can be added by splitting the output side resistor  $R_{S2}$  into two components and adding a Zener diode  $D_3$ . (Refer to [Figure 4-1](#) below.) When there is an Open LED condition, the diode  $D_3$  will clamp the output voltage and the Zener diode current will be regulated by the sum of  $R_{S2A}$  and  $R_{CS2}$ .

### 4.2 Damping Circuit

The Ćuk converter is inherently unstable when the output current is being controlled. An uncontrolled input current will lead to an undamped oscillation between  $L_1$  and  $C_1$ , causing excessively high voltages across capacitor  $C_1$ . To prevent these oscillations, a damping circuit consisting of  $R_D$  and  $C_D$  is applied across the capacitor  $C_1$ . This damping circuit will stabilize the circuit and help in the proper operation of the converter.

### 4.3 Design and Operation of the Boost-buck Converter

For details on the design for a boost-buck converter using the AT9933 and the calculation of the damping components, refer to Application Notes [AN-H51](#) and [AN-H58](#).

## 4.4 Design Example

The choice of the resistor dividers to set the input and output current levels is illustrated by means of the design example given below.

The parameters of the power circuit are:

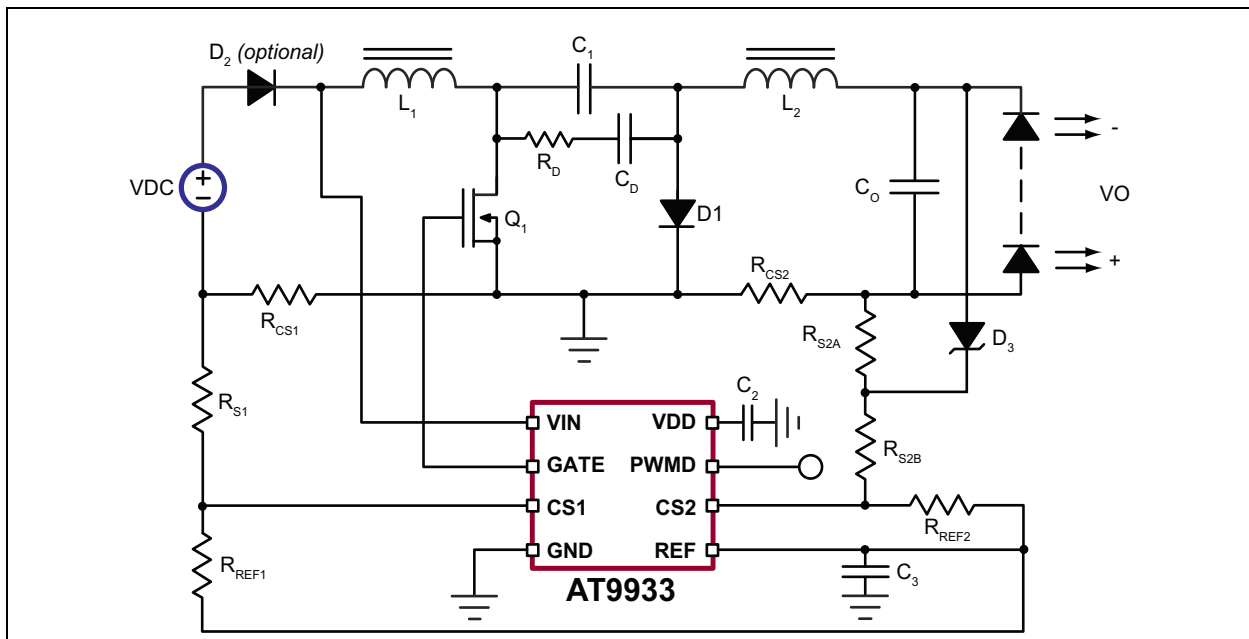
$$\begin{aligned} V_{IN,MIN} &= 9.01V \\ V_{IN,MAX} &= 16V \\ V_O &= 28V \\ I_O &= 0.35A \\ f_{S,MIN} &= 300kHz \end{aligned}$$

Using these parameters, the values of the power stage inductors and capacitor can be computed. (See figures below.) Refer to Application Note [AN-H51](#) for more details.

$$\begin{aligned} L_1 &= 82\mu H \\ L_2 &= 150\mu H \\ C_1 &= 0.22\mu F \end{aligned}$$

The input and output currents for this design are:

$$\begin{aligned} I_{IN,MAX} &= 1.6A \\ \Delta I_{IN} &= 0.21A \\ I_O &= 350mA \\ \Delta I_O &= 87.5mA \end{aligned}$$



**FIGURE 4-1:** Design Example Circuit.

## 4.5 Current Limits

The current sense resistor  $R_{CS2}$ , combined with the other resistors  $R_{S2}$  and  $R_{REF2}$ , determines the output current limits.

The resistors can be chosen using [Equation 4-1](#) and [Equation 4-2](#).

### EQUATION 4-1:

$$I \times R_{CS} = 1.2V \times \left( \frac{R_S}{R_{REF}} \right) - 0.05V$$

Where  $I$  is the current (either  $I_O$  or  $I_{IN}$ ) and  $\Delta I$  is the peak-to-peak ripple in the current (either  $\Delta I_O$  or  $\Delta I_{IN}$ ).

### EQUATION 4-2:

$$\Delta I \times R_{CS} = 0.1V \times \left( \frac{R_S}{R_{REF}} \right) + 0.1V$$

Where  $I$  is the current (either  $I_O$  or  $I_{IN}$ ) and  $\Delta I$  is the peak-to-peak ripple in the current (either  $\Delta I_O$  or  $\Delta I_{IN}$ ).

For the input side, the current level used in the equations should be larger than the maximum input current, so that it does not interfere with the normal operation of the circuit. The peak input current can be computed as shown in [Equation 4-3](#).

### EQUATION 4-3:

$$I_{IN,PK} = I_{IN,MAX} + \left( \frac{\Delta I_{IN}}{2} \right) \\ = 1.706A$$

Assuming a 30% peak-to-peak ripple when the converter is in Input Current Limit mode, the minimum value of the input current is calculated as seen in [Equation 4-4](#).

### EQUATION 4-4:

$$I_{LIM,MIN} = 0.85 \times I_{IN,LIM} \\ \text{Setting} \\ I_{LIM,MIN} = 1.05 \times I_{IN,PK}$$

The current level to limit the converter can then be computed. See equation [Equation 4-5](#).

### EQUATION 4-5:

$$I_{IN,LIM} = \left( \frac{1.05}{0.85} \right) \times I_{IN,PK} \\ = 2.1A$$

Using  $I_O = 350$  mA and  $\Delta I_O = 87.5$  mA in [Equation 4-1](#) and [Equation 4-2](#),  $R_{CS2} = 1.78\Omega$  and  $R_{S2}/R_{REF2} = 0.5625$ .

Before the design of the output side is complete, overvoltage protection has to be included in the design. For this application, choose a 33V Zener diode. This is the voltage at which the output will clamp in case of an Open LED condition. For a 350 mW diode, the maximum current rating at 33V works out to about 10 mA. Using a 2.5 mA current level during Open LED conditions, and assuming the same  $R_{S2}/R_{REF2}$  ratio, the Zener current limiting resistor can be determined as illustrated in [Equation 4-6](#).

### EQUATION 4-6:

$$R_{CS} + R_{S2A} = 120\Omega$$

Choose the following values for the resistors:

$$R_{CS2} = 1.65\Omega, 1/4W, 1\% \\ R_{REF2} = 10\text{ k}\Omega, 1/8W, 1\% \\ R_{S2A} = 100\Omega, 1/8W, 1\% \\ R_{S2B} = 5.23\text{ k}\Omega, 1/8W, 1\%$$

The current sense resistor needs to be at least a 1/4W, 1% resistor.

Similarly, using  $I_{IN} = 2.1A$  and  $\Delta I_{IN} = 0.3 \times I_{IN} = 0.63$  in [Equation 4-1](#) and [Equation 4-2](#), the following values can be determined:

$$\frac{R_{S1}}{R_{REF1}} = 0.442 \\ R_{CS1} = 0.228\Omega \\ P_{RCS1} = I_{IN,LIM}^2 \times R_{CS1} \\ = 1W$$

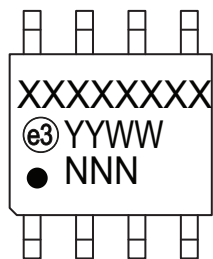
Choose the following values for the resistors:

$$R_{CS1} = \text{parallel combination of three } 0.68\Omega, 1/2W, 5\% \\ \text{resistors} \\ R_{REF1} = 10\text{ k}\Omega, 1/8W, 1\% \\ R_{S1} = 4.42\text{ k}\Omega, 1/8W, 1\%$$

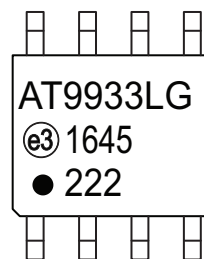
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

8-lead SOIC

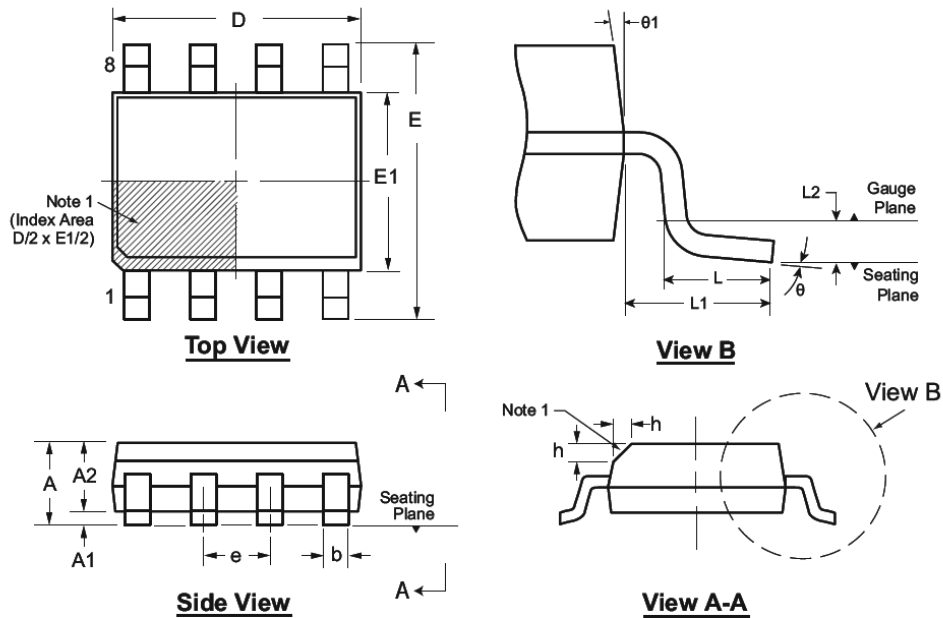


Example



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Note:**

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

## APPENDIX A: REVISION HISTORY

### Revision A (October 2016)

- Converted Supertex Doc# DSFP-AT9933 to Microchip DS20005597A
- Changed the quantity of the 8-lead SOIC package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

# AT9933

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	AT9933	=	Hysteretic Boost-Buck (Ćuk) LED Driver IC		
Package:	LG	=	8-lead SOIC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3300/Reel for an LG Package		

**Example:**  
a) AT9933LG-G: Hysteretic Boost-buck (Ćuk) LED Driver IC, 8-lead SOICPackage, 3300/Reel

---

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
= ISO/TS 16949 =**

### Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0995-3



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199

Tel: 480-792-7200

Fax: 480-792-7277

Technical Support:

[http://www.microchip.com/  
support](http://www.microchip.com/support)

Web Address:

[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA

Tel: 678-957-9614

Fax: 678-957-1455

#### Austin, TX

Tel: 512-257-3370

#### Boston

Westborough, MA

Tel: 774-760-0087

Fax: 774-760-0088

#### Chicago

Itasca, IL

Tel: 630-285-0071

Fax: 630-285-0075

#### Cleveland

Independence, OH

Tel: 216-447-0464

Fax: 216-447-0643

#### Dallas

Addison, TX

Tel: 972-818-7423

Fax: 972-818-2924

#### Detroit

Novi, MI

Tel: 248-848-4000

#### Houston, TX

Tel: 281-894-5983

#### Indianapolis

Noblesville, IN

Tel: 317-773-8323

Fax: 317-773-5453

#### Los Angeles

Mission Viejo, CA

Tel: 949-462-9523

Fax: 949-462-9608

#### New York, NY

Tel: 631-435-6000

#### San Jose, CA

Tel: 408-735-9110

#### Canada - Toronto

Tel: 905-695-1980

Fax: 905-695-2078

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon

#### Hong Kong

Tel: 852-2943-5100

Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733

Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8569-7000

Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511

Fax: 86-28-8665-7889

#### China - Chongqing

Tel: 86-23-8980-9588

Fax: 86-23-8980-9500

#### China - Dongguan

Tel: 86-769-8702-9880

#### China - Guangzhou

Tel: 86-20-8755-8029

#### China - Hangzhou

Tel: 86-571-8792-8115

Fax: 86-571-8792-8116

#### China - Hong Kong SAR

Tel: 852-2943-5100

Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460

Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355

Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533

Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829

Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8864-2200

Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300

Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7252

Fax: 86-29-8833-7256

### ASIA/PACIFIC

#### China - Xiamen

Tel: 86-592-2388138

Fax: 86-592-2388130

#### China - Zhuhai

Tel: 86-756-3210040

Fax: 86-756-3210049

#### India - Bangalore

Tel: 91-80-3090-4444

Fax: 91-80-3090-4123

#### India - New Delhi

Tel: 91-11-4160-8631

Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-3019-1500

#### Japan - Osaka

Tel: 81-6-6152-7160

Fax: 81-6-6152-9310

#### Japan - Tokyo

Tel: 81-3-6880-3770

Fax: 81-3-6880-3771

#### Korea - Daegu

Tel: 82-53-744-4301

Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200

Fax: 82-2-558-5932 or

82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857

Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870

Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065

Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870

Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-5778-366

Fax: 886-3-5770-955

#### Taiwan - Kaohsiung

Tel: 886-7-213-7828

#### Taiwan - Taipei

Tel: 886-2-2508-8600

Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351

Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39

Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828

Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20

Fax: 33-1-69-30-90-79

#### Germany - Dusseldorf

Tel: 49-2129-3766400

#### Germany - Karlsruhe

Tel: 49-721-625370

#### Germany - Munich

Tel: 49-89-627-144-0

Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611

Fax: 39-0331-466781

#### Italy - Venice

Tel: 39-049-7625286

#### Netherlands - Drunen

Tel: 31-416-690399

Fax: 31-416-690340

#### Poland - Warsaw

Tel: 48-22-3325737

#### Spain - Madrid

Tel: 34-91-708-08-90

Fax: 34-91-708-08-91

#### Sweden - Stockholm

Tel: 46-8-5090-4654

#### UK - Wokingham

Tel: 44-118-921-5800

Fax: 44-118-921-5820

06/23/16